ARM Cortex®-M0

32-bit Microcontroller

NuMicro™ M058S Series Datasheet

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www.nuvoton.com

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1 GENERAL DESCRIPTION

The NuMicro™ M058S is a 32-bit microcontroller with embedded ARM® Cortex®-M0 core for industrial control and applications which need rich communication interfaces. The Cortex®-M0 is ARM embedded processor with 32-bit performance and cost-effective microcontroller.

The NuMicro™ M058S can run up to 50 MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The NuMicro™ M058S has 32 KB flash, 4 KB data flash, 4 KB flash for the ISP, and 4 KB SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, and Brown-Out Detector, have been incorporated into the NuMicro™ M058S in order to reduce component count, board space and system cost. These useful functions make the NuMicro™ M058S powerful for a wide range of applications.

Additionally, the NuMicro™ M058S is equipped with IAP (In-Application Programming), ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex®-M0 core runs up to 50 MHz.
  - One 24-bit system timer.
  - Supports low power sleep-mode.
  - A single-cycle 32-bit hardware multiplier.
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
  - Supports Serial Wire Debug (SWD) interface and 2 watchpoints/4 breakpoints.
- Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
  - 32 KB Flash for program memory (APROM)
  - 4 KB Flash for data memory (DataFlash)
  - 4 KB Flash for loader (LDROM)
  - 4 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
  - 22.1184 MHz internal oscillator
  - 4~24 MHz external crystal input
  - 10 kHz low-power oscillator for Watchdog Timer and wake-up in Sleep mode
  - PLL allows CPU operation up to the maximum 50 MHz
- I/O Port
  - Up to 55 general-purpose I/O (GPIO) pins for LQFP-64 package
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Configurable I/O mode after POR
- Timer
  - Provides four channel 32-bit timers, one 8-bit pre-scale counter with 24-bit up-timer for each timer.
  - Independent clock source for each timer.
  - 24-bit timer value is readable through TDR (Timer Data Register)
  - Provides one-shot, periodic and toggle operation modes.
  - Provide event counter function.
  - Provide external capture/reset counter function.
  - Additional functions:
    - Two more timer clock sources from external trigger and internal 10 kHz
    - TIMER wake-up function
    - External capture input source selected from TxEX
    - Toggle mode output pins selected from TxEX or TMx
    - Inter-Timer trigger mode
- WDT (Watchdog Timer)
  - Multiple clock sources

- Supports wake-up from Power-down or Sleep mode
- Interrupt or reset selectable on watchdog time-out
- Time-out reset delay period time can be selected

- WWDT (Window Watchdog Timer)
  - 6-bit down counter with 11-bit prescale for wide range window selected
- PWM
  - Up to two built-in 16-bit PWM generators, providing four PWM outputs or two complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - 16-bit digital Capture timers (shared with PWM timers) with rising/falling capture inputs
  - Supports capture interrupt
  - Additional functions
    - Internal 10 kHz to PWM clock source
    - Polar inverse function
    - Center-aligned type function
    - Timer duty interrupt enable function
    - Two kinds of PWM interrupt period/duty type selection
    - Period/duty trigger ADC function
- UART
  - Programmable baud-rate generator
  - Buffered receiver and transmitter, each with 16 bytes FIFO
  - Optional flow control function (CTS and RTS)
  - Supports IrDA(SIR) function
  - Supports RS485 function
  - Supports LIN function
- SPI
  - Supports Master/Slave mode
  - Full-duplex synchronous serial data transfer
  - Provides 3 wire function
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Supports Byte Suspend mode in 32-bit transmission
  - Additional functions
    - PLL clock source
    - 4-level depth FIFO buffer for better performance and flexibility in SPI Burst Transfer mode
- I^2C
  - Up to two sets of I2C device
  - Supports master/slave mode
  - Bidirectional data transfer between master and slave
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

- Programmable clocks allow versatile rate control.
- Supports multiple address recognition (four slave address with mask option)

- ADC
  - 12-bit SAR ADC
  - Up to 8-ch single-ended input or 4-ch differential input
  - Supports Single mode/Burst mode/Single-cycle Scan mode/Continuous Scan mode
  - Supports 2' complement/un-signed format in differential mode conversion results
  - Each channel with an individual result register
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Conversion started either by software trigger or external pin trigger
  - Additional functions
    - A/D conversion started by PWM center-aligned trigger or edge-aligned trigger
    - PWM trigger delay function
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- IAP (In-Application Programming)
- One built-in temperature sensor with 1℃ resolution
- BOD (Brown-out Detector)
  - With 4 levels: 4.4V/3.7V/2.7V/2.2V
  - Supports Brown-Out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage levels: 2.0V
- Operating Temperature: -40℃~85℃
- Packages:
  - Green package (RoHS)
  - 64-pin LQFP, 48-pin LQFP, 33-pin QFN, 20-pin TSSOP

3 ABBREVIATIONS

3.1 List of Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro™ M058S Series Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity			PWM (16-bit)	ADC (12-bit)	WDT	WWDT	ISP/ICP/IAP	Package	Operating Temperature Range(℃)
							UART	SPI	I²C							
M058SFAN	32	4	4	4	14	4	1	1	1	1	2	√	√	√	TSSOP20	-40 to +85
M058SZAN	32	4	4	4	26	4	1	1	1	2	5	√	√	√	QFN33	-40 to +85
M058SLAN	32	4	4	4	42	4	1	1	2	4	8	√	√	√	LQFP48	-40 to +85
M058SSAN	32	4	4	4	55	4	1	1	2	4	8	√	√	√	LQFP64	-40 to +85

Table 4.1-1 NuMicro™ M058S Series Selection Guide

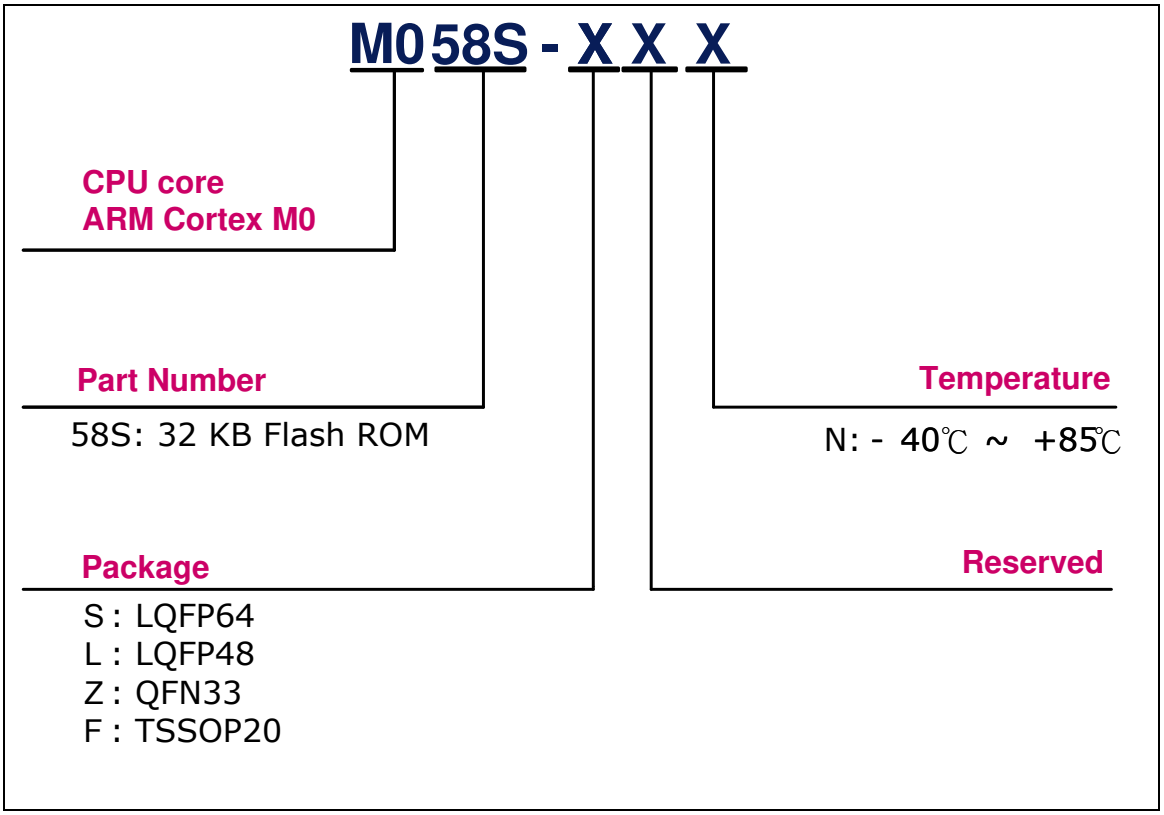


Figure 4.1-1 NuMicro™ M058S Series Selection Code

4.2 Pin Configuration

4.2.1 TSSOP20 pin

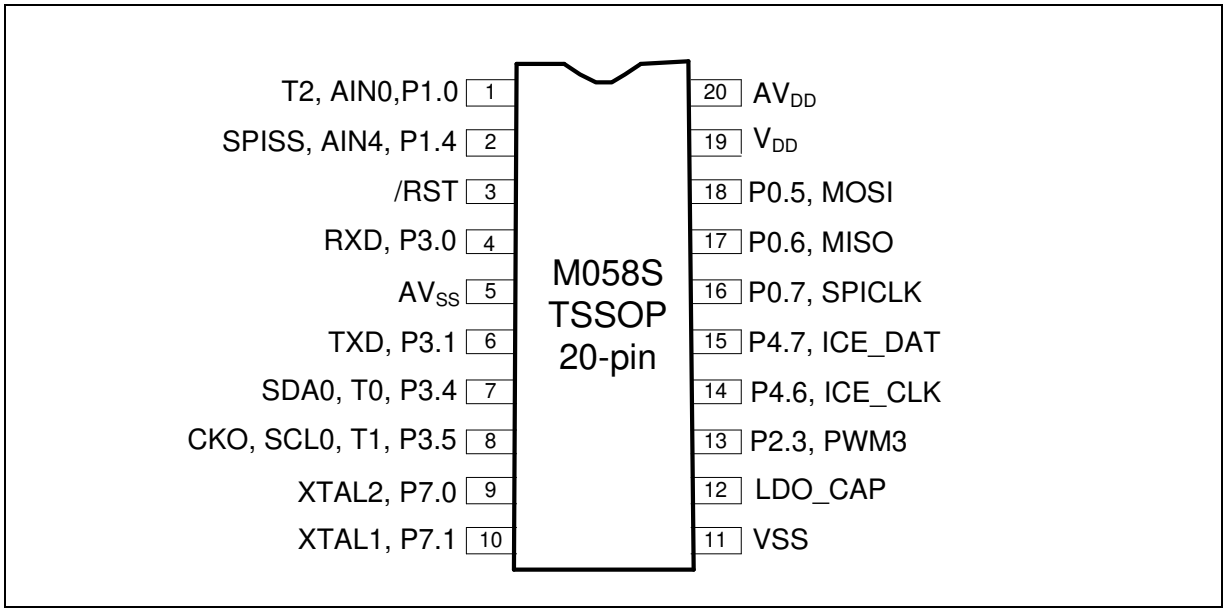


Figure 4.2-1 NuMicro™ M058S TSSOP20 Pin Diagram

4.2.2 QFN 33-pin

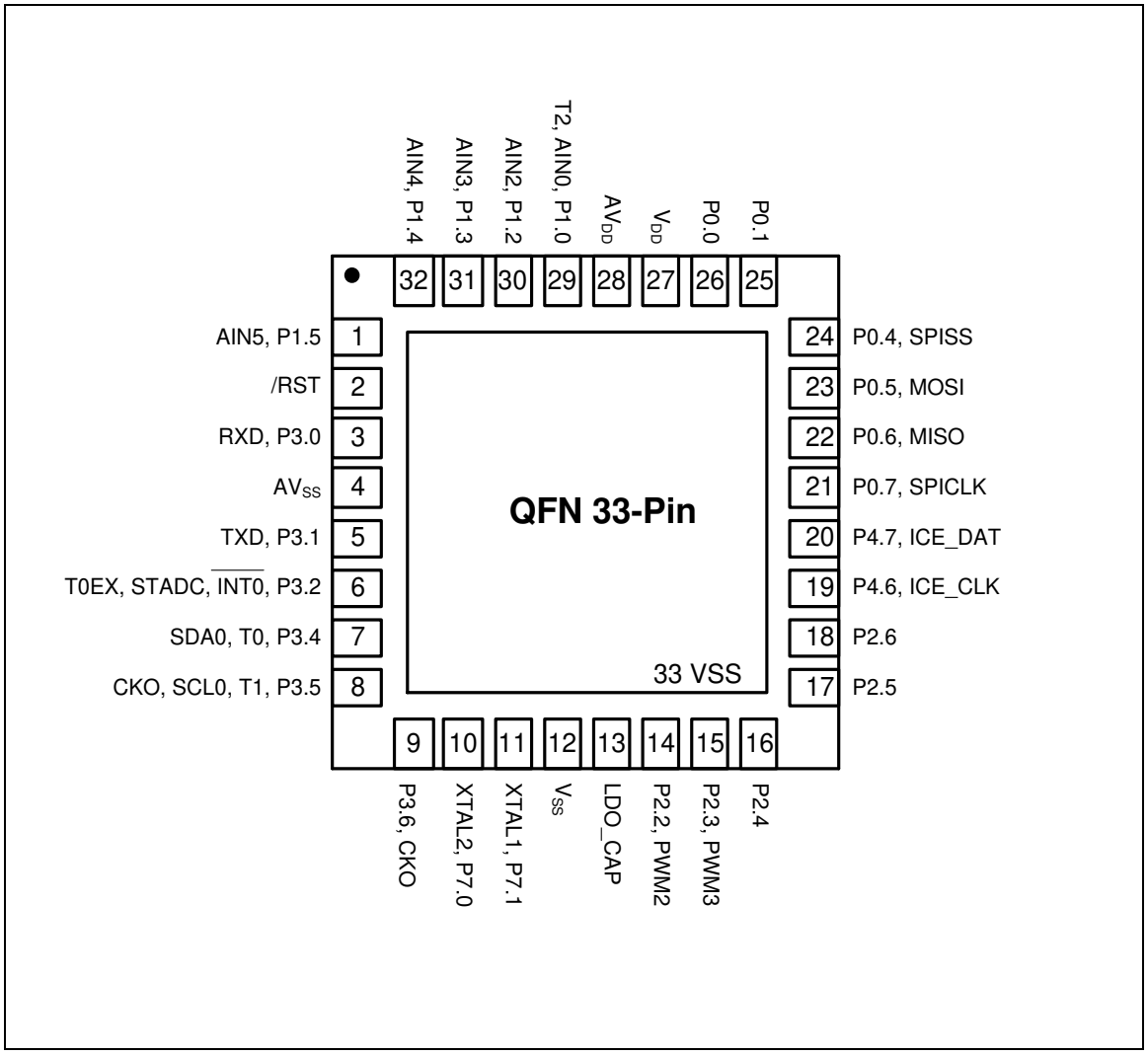


Figure 4.2-2 NuMicro™ M058S Series QFN-33 Pin Diagram

4.2.3 LQFP 48-pin

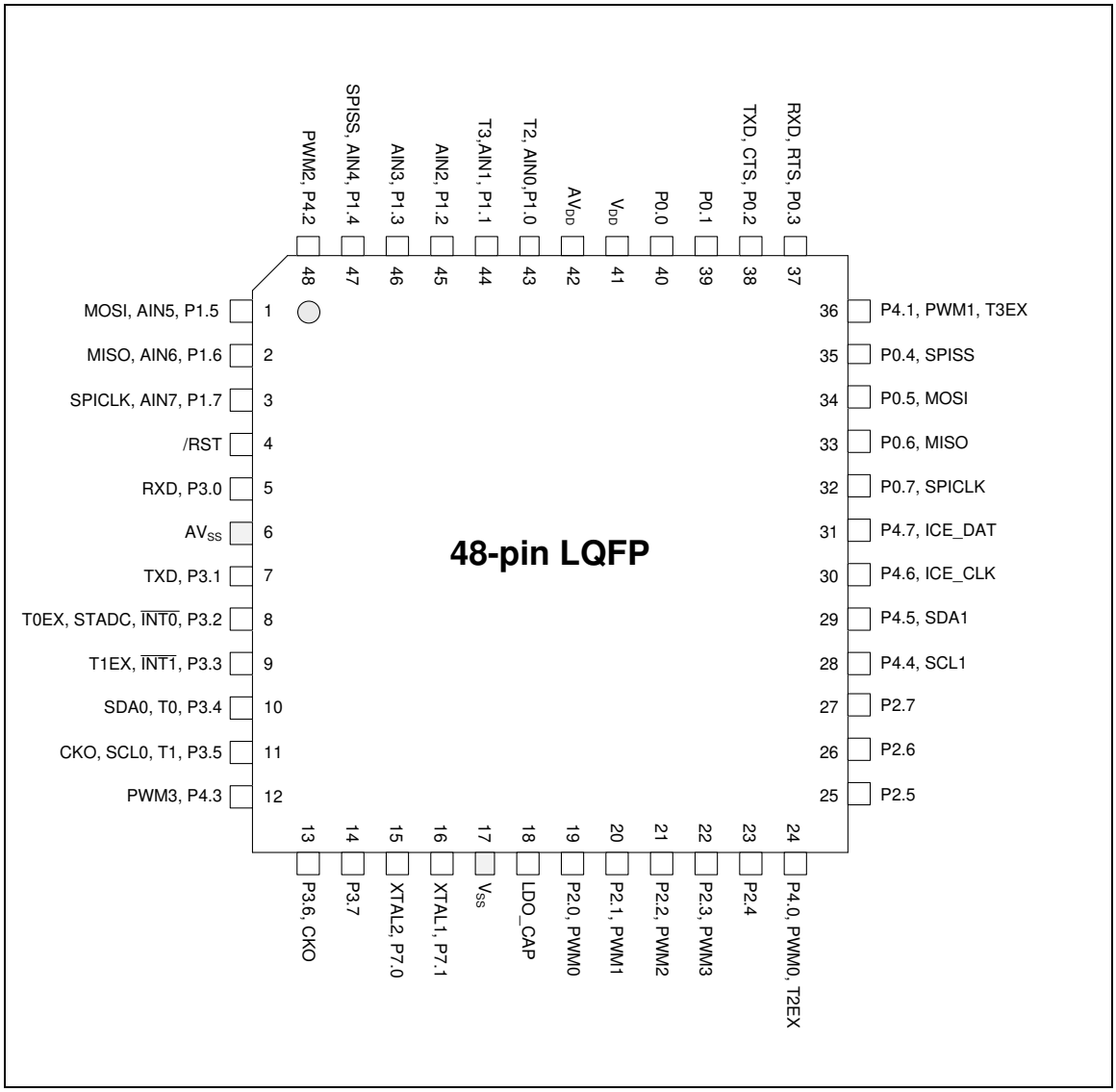


Figure 4.2-3 NuMicro™ M058S Series LQFP-48 Pin Diagram

4.2.4 LQFP 64-pin

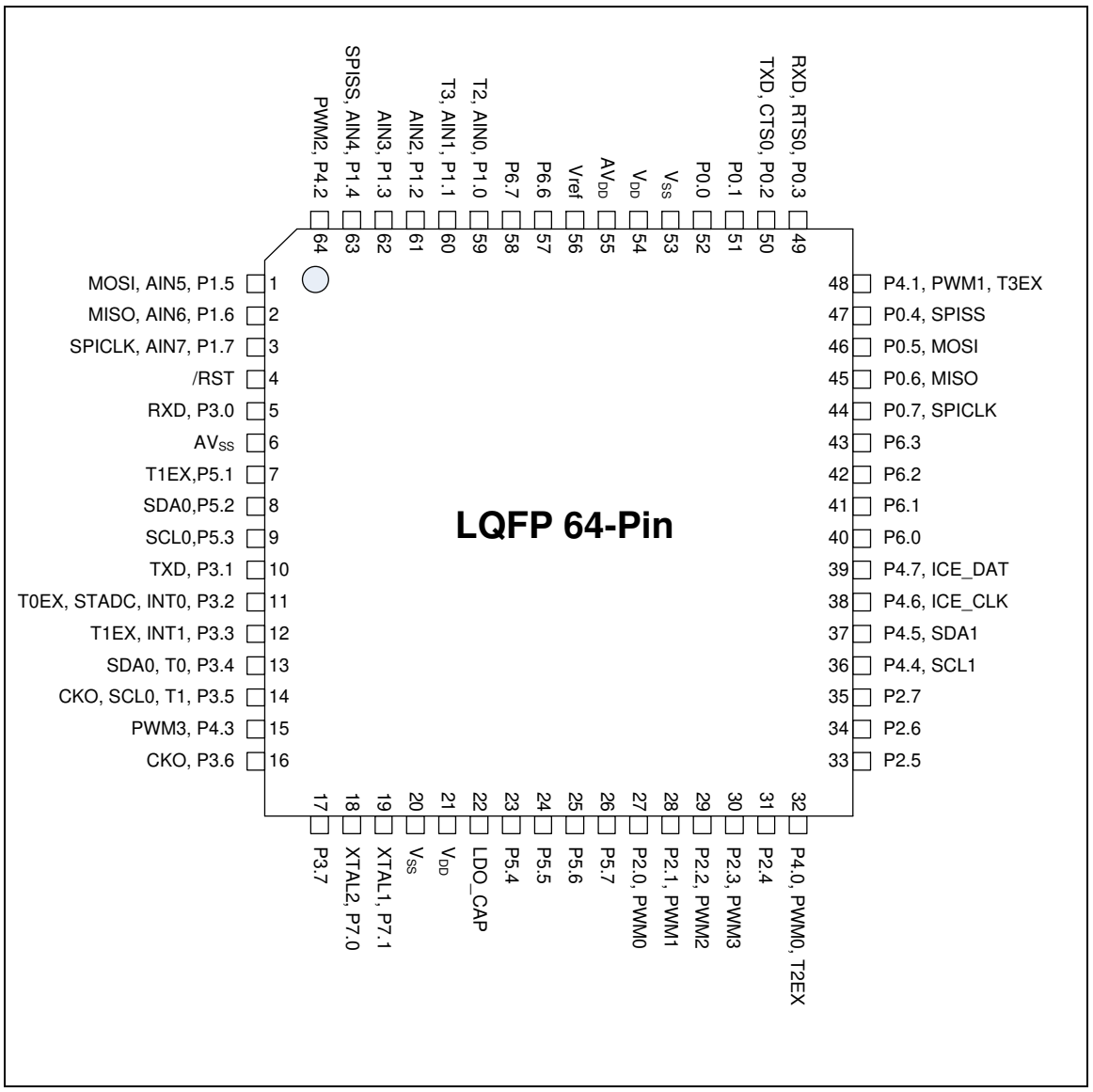


Figure 4.2-4 NuMicro™ M058S Series LQFP-64 Pin Diagram

4.3 Pin Description

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
19	27	41	21 54	V_{DD}				P	Power supply to I/O ports and LDO source for internal PLL and digital circuit.
11	12 33	17	20 53	V_{SS}				P	Ground pin for digital circuit.
20	28	42	55	AV_{DD}				P	Power supply to internal analog circuit.
5	4	6	6	AV_{SS}				P	Analog Ground pin for analog circuit.
	NC	NC	56	V_{ref}				P	Voltage reference input for ADC
12	13	18	22	LDO _CAP				P	LDO output pin **Note:** This pin needs to be connected with a 1uF capacitor.
3	2	4	4	/RST				I (ST)	/RST pin is a Schmitt trigger input pin for hardware device reset. A **"Low"** on this pin for 768 clock counter of Internal RC 22M while the system clock is running will reset the device. /RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on /RST pin.
	26	40	52	P0.0				I/O	**PORT0:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for CTS1, RTS1, CTS0, RTS0, SPISS, MOSI, MISO, and SPICLK. The pins SPISS, MOSI, MISO, and SPICLK are for the SPI function use.
	25	39	51	P0.1				I/O	
	NC	38	50	P0.2	CTS		TXD[2]	I/O	
	NC	37	49	P0.3	RTS		RXD[2]	I/O	
	24	35	47	P0.4	SPISS[2]			I/O	

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
18	23	34	46	P0.5	MOSI[2]			I/O	CTS: Clear to Send input pin for UART
17	22	33	45	P0.6	MISO[2]			I/O	RTS: Request to Send output pin for UART
16	21	32	44	P0.7	SPICLK[2]			I/O	The RXD/TXD pins are for UART function use.
1	29	43	59	P1.0	T2	AIN0		I/O	**PORT1:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for T2, T3, SPISS0, MOSI, MISO, and SPICLK. The pins SPISS0, MOSI, MISO, and SCLK are for the SPI function use. The pins AIN0~AIN7 are for the 12 bits ADC function use. The T2/T3 pins are for Timer2/3 external event counter input.
	NC	44	60	P1.1	T3	AIN1		I/O	
	30	45	61	P1.2		AIN2		I/O	
	31	46	62	P1.3		AIN3		I/O	
2	32	47	63	P1.4	SPISS[2]	AIN4		I/O	
	1	1	1	P1.5	MOSI[2]	AIN5		I/O	
	NC	2	2	P1.6	MISO[2]	AIN6		I/O	
	NC	3	3	P1.7	SPICLK[2]	AIN7		I/O	
	NC	19	27	P2.0	PWM0[2]			I/O	**PORT2:** General purpose I/O port, which can be configured by software in four modes. It has an alternative function. The pins PWM0~PWM3 are for the PWM function use.
	NC	20	28	P2.1	PWM1[2]			I/O	
	14	21	29	P2.2	PWM2[2]			I/O	
13	15	22	30	P2.3	PWM3[2]			I/O	
	16	23	31	P2.4				I/O	
	17	25	33	P2.5				I/O	
	18	26	34	P2.6				I/O	
	NC	27	35	P2.7				I/O	
4	3	5	5	P3.0	RXD[2]			I/O	**PORT3:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for RXD, TXD, /INT0, /INT1, T0 and T1. The RXD/TXD pins are for
6	5	7	10	P3.1	TXD[2]			I/O	
	6	8	11	P3.2	/INT0	STADC	T0EX	I/O	
	NC	9	12	P3.3	/INT1		T1EX	I/O	

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
7	7	10	13	P3.4	T0	SDA0		I/O	UART function use. The SDA0/SCL0 pins are for I²C0 function use. CKO: HCLK clock output The STADC pin is for ADC external trigger input. The T0/T1 pins are for Timer0/1 external event counter input. The T0EX/T1EX pins are for external capture/reset trigger input of Timer0/1.
8	8	11	14	P3.5	T1	SCL0	CKO[2]	I/O	
	9	13	16	P3.6		CKO		I/O	
	NC	14	17	P3.7				I/O	
	NC	24	32	P4.0	PWM0[2]		T2EX	I/O	**PORT4:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for PWM0-3, SCL1, SDA1, ICE_CLK and ICE_DAT. The ICE_CLK/ICE_DAT pins are for JTAG-ICE function use. PWM0-3 can be used from P2.0-P2.3 or P4.0-P4.3. The T2EX/T3EX pins are for external capture/reset trigger input of Timer2/3. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK and ICE_DAT pins.
	NC	36	48	P4.1	PWM1[2]		T3EX	I/O	
	NC	48	64	P4.2	PWM2[2]			I/O	
	NC	12	15	P4.3	PWM3[2]			I/O	
	NC	28	36	P4.4		SCL1		I/O	
	NC	29	37	P4.5		SDA1		I/O	
14	19	30	38	P4.6	ICE_CLK			I/O	
15	20	31	39	P4.7	ICE_DAT			I/O	
	NC	NC	7	P5.1	T1EX			I/O	**PORT5:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for T0EX, T1EX, SDA0 and SCL0. The T0EX/T1EX pins are for external capture/reset trigger input of Timer0/1. The SDA0/SCL0 pins are for I²C0 function use.
	NC	NC	8	P5.2	SDA0			I/O	
	NC	NC	9	P5.3	SCL0			I/O	
	NC	NC	23	P5.4				I/O	
	NC	NC	24	P5.5				I/O	
	NC	NC	25	P5.6				I/O	
	NC	NC	26	P5.7				I/O	
	NC	NC	40	P6.0				I/O	**PORT6:** General purpose I/O

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
	NC	NC	41	P6.1				I/O	port, which can be configured by software in four modes.
	NC	NC	42	P6.2				I/O	
	NC	NC	43	P6.3				I/O	
	NC	NC	57	P6.6				I/O	
	NC	NC	58	P6.7				I/O	
9	10	15	18	P7.0	XTAL2			I/O, O	PORT7: General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for XTAL
10	11	16	19	P7.1	XTAL1			I/O, I(ST)	XTAL: External 4~24 MHz (high speed) crystal pin.

Note 1: I/O type description. I: Input, O: Output, I/O: Quasi-bidirectional, D: Open-drain, P: Power pins, ST: Schmitt trigger.

Note 2: The PWM0 ~ PWM3, RXD, TXD, RXD1, TXD1, SCL1, SDA1 and CKO can be assigned to different pins. However, a pin function can only be assigned to a pin at the same time, i.e. software cannot assign RXD to P0.3 and P3.0 at the same time.

5 BLOCK DIAGRAM

5.1 NuMicro™ M058S Block Diagram

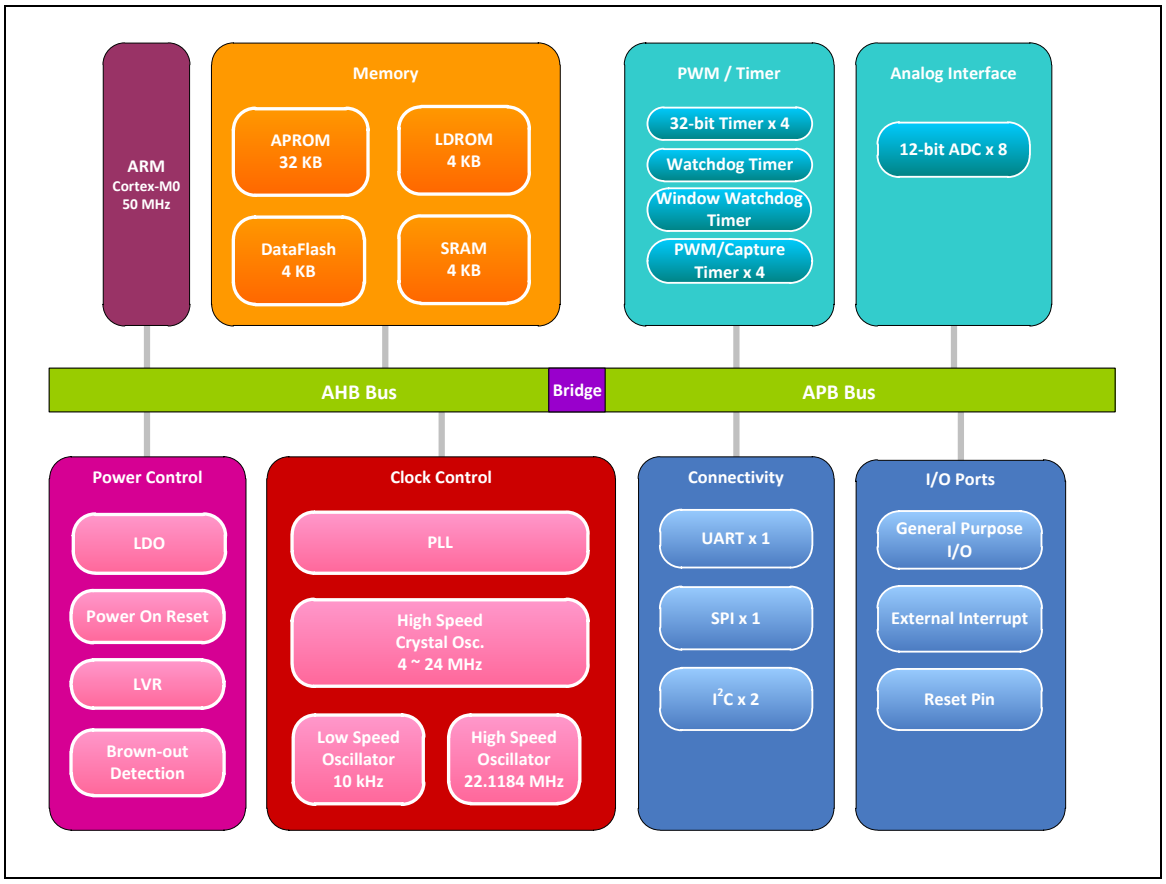


Figure 5.1-1 NuMicro™ M058S Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes -Thread and Handler modes. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of processor.

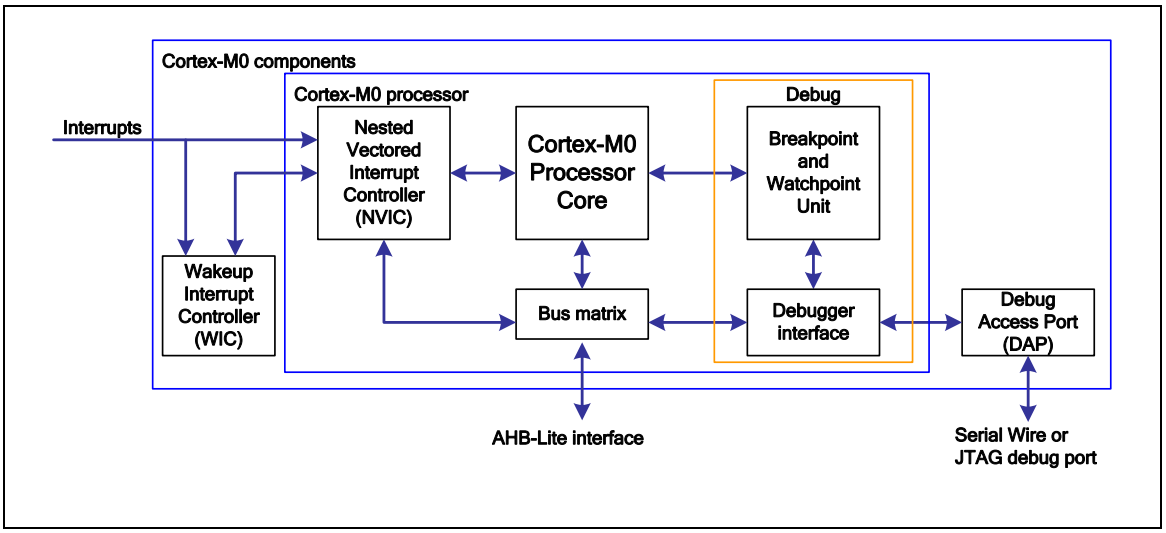


Figure 6.1-1 Functional Block Diagram

The implemented device provides:

- **A low gate count processor the features:**
  - The ARMv6-M Thumb® instruction set.
  - Thumb-2 technology.
  - ARMv6-M compliant 24-bit SysTick timer.
  - A 32-bit hardware multiplier.
  - The system interface supports little-endian data accesses.
  - The ability to have deterministic, fixed-latency, interrupt handling.
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling.
  - C Application Binary Interface compliant exception model.
    This is the ARMv6-M, C Application Binary Interface(C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers.

- Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event(WFE) instructions, or the return from interrupt sleep-on-exit feature.

- **NVIC features:**
  - 32 external interrupt inputs, each with four levels of priority.
  - Dedicated non-Maskable Interrupt (NMI) input.
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and provides Ultra-low Power Sleep mode
- **Debug support:**
  - Four hardware breakpoints.
  - Two watchpoints.
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
  - Single step and vector catch capabilities.
- **Bus interfaces:**
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the Reset Pin (nRST)
  - Watchdog Timer Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD)
- Software Reset
  - MCU Reset - SYSRESETREQ(AIRCR[2])
  - Cortex-M0 Core One-shot Reset - CPU_RST(IPRSTC1[1])
  - Chip One-shot Reset - CHIP_RST(IPRSTC1[0])

Note: ISPCON.BS keeps the original value after MCU Reset and CPU Reset.

6.2.3 System Power Architecture

In this device, the power architecture is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. AV_{DD} must be equal to V_{DD} to avoid leakage current.
- Digital power from V_{DD} and V_{SS} supplies the power to the I/O pins and internal regulator which provides a fixed 1.8 V power for digital operation.

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level as the digital power (V_{DD}). The following figure shows the power distribution of the M058S series.

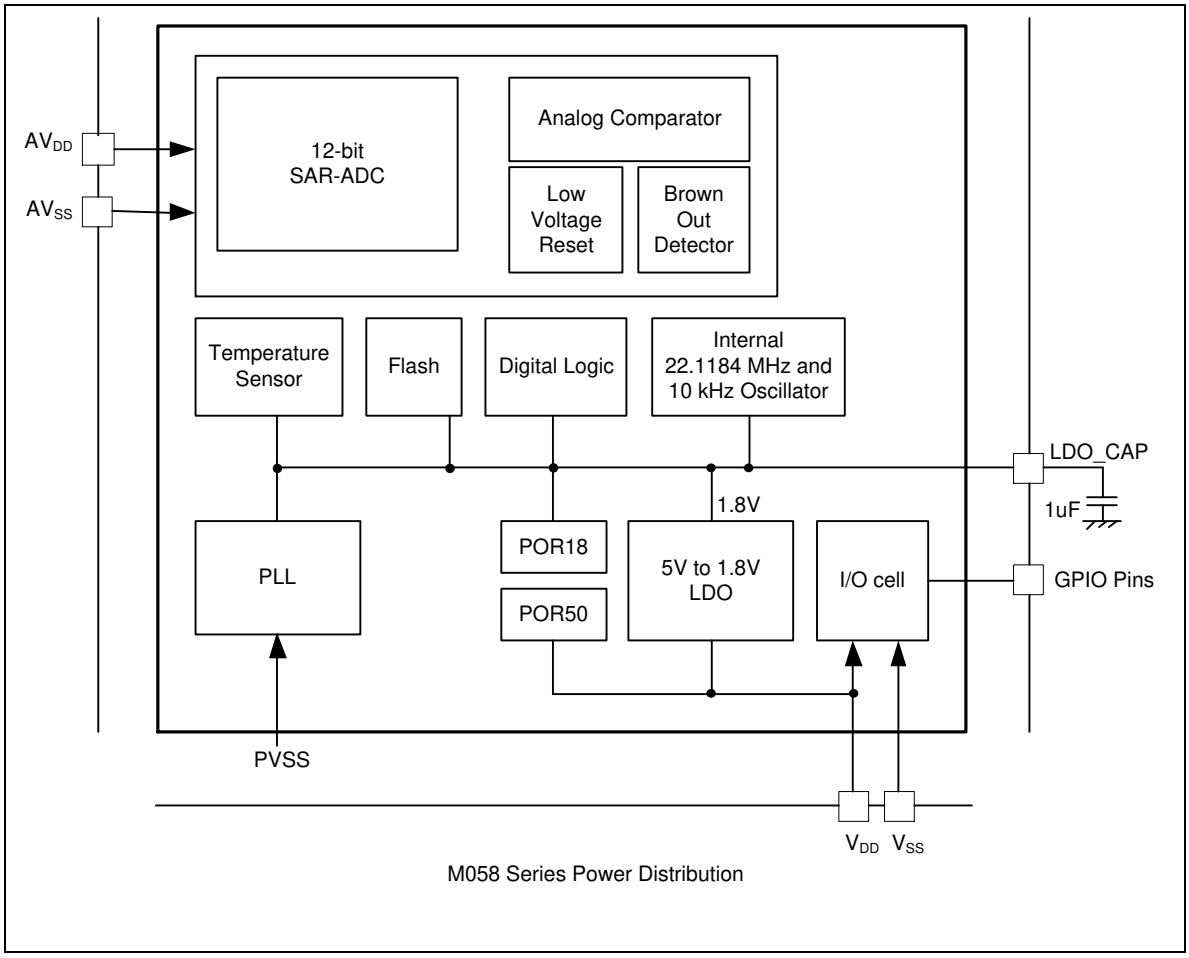


Figure 6.2-1 NuMicro™ M058S Power Architecture Diagram

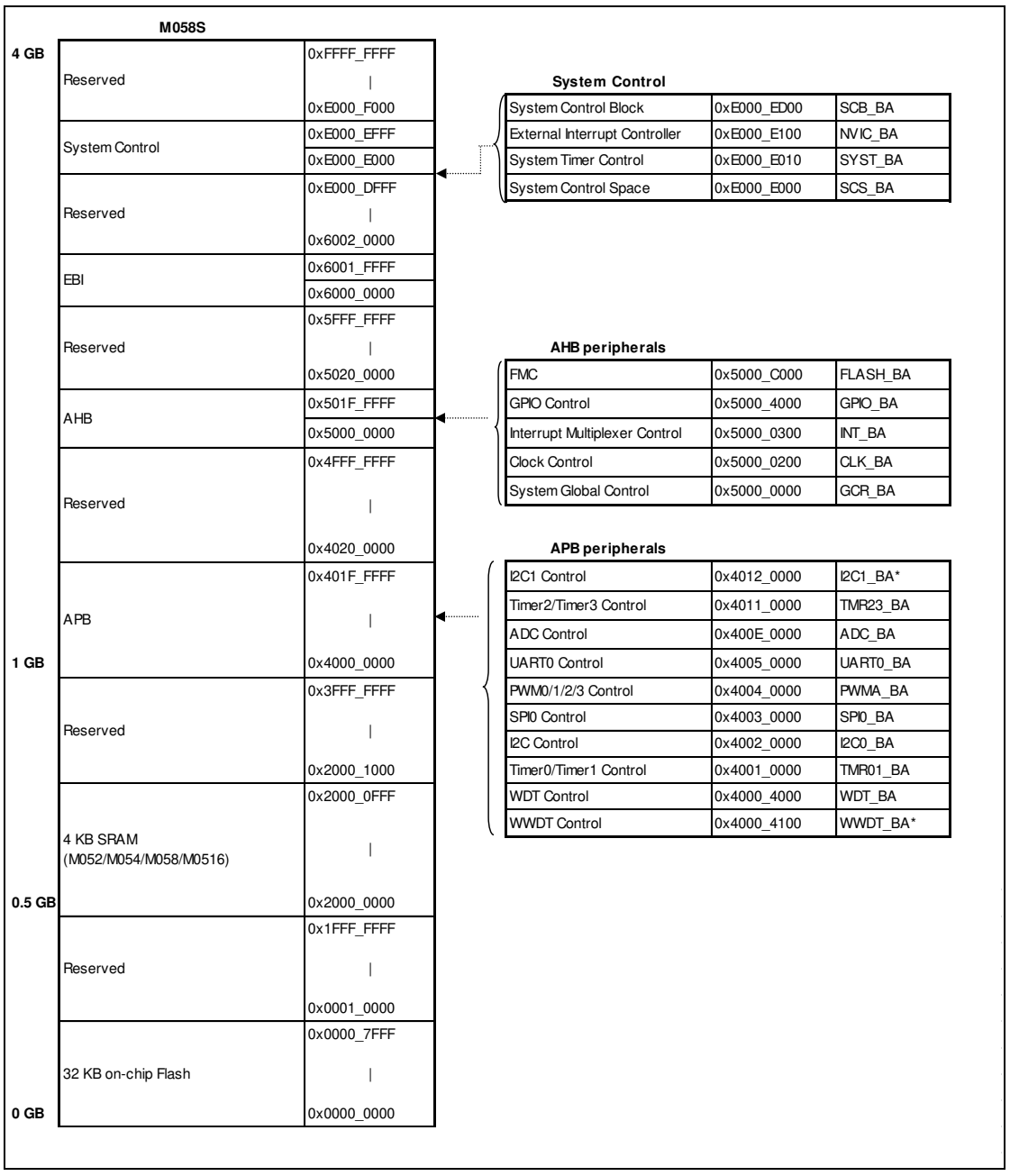
6.2.4 System Memory Map

The NuMicro™ M058S series provides 4 GB addressing space. The addressing space assigned to each on-chip controllers are shown in the following table. The detailed register definition, addressing space, and programming details will be described in the following sections for each on-chip peripheral. The NuMicro™ M058S series only supports little-endian data format.

Addressing Space	Token	Modules
Flash & SRAM Memory Space		
0x0000_0000 – 0x0000_7FFF	FLASH_BA	FLASH Memory Space (32 KB)
0x2000_0000 – 0x2000_0FFF	SRAM_BA	SRAM Memory Space (4 KB)
AHB Modules Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO (P0~P7) Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB Modules Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_00FF	WDT_BA	Watchdog Timer Control Registers
0x4000_4100 – 0x4000_7FFF	WWDT_BA	Window Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
System Control Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SYST_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	NVIC_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Block Registers

Table 6.2-1 Address Space Assignments for On-Chip Modules

6.2.5 Whole System Memory Mapping



6.2.6 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.7 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.7.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro™ M058S series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-2 Exception Model

Exception Number	Vector Address	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source Module	Interrupt description	Power-down Wakeup
1-15					System exceptions	
16	0x40	0	BOD_INT	Brown-out	Brown-out low voltage detected interrupt	Yes
17	0x44	1	WDT_INT	WDT	Watchdog Timer interrupt	Yes
18	0x48	2	EINT0	GPIO	External signal interrupt from P3.2 pin	Yes
19	0x4C	3	EINT1	GPIO	External signal interrupt from P3.3 pin	Yes
20	0x50	4	GP01_INT	GPIO	External signal interrupt from P0[7:0] / P1[7:0]	Yes
21	0x54	5	GP234_INT	GPIO	External interrupt from P2[7:0]/P3[7:0]/P4[7:0], except P32 and P33	Yes
22	0x58	6	PWMA_INT	PWM0~3	PWM0, PWM1, PWM2 and PWM3	No

					interrupt	
23	0x5C	7	Reserved	-	-	-
24	0x60	8	TMR0_INT	TMR0	Timer 0 interrupt	No
25	0x64	9	TMR1_INT	TMR1	Timer 1 interrupt	No
26	0x68	10	TMR2_INT	TMR2	Timer 2 interrupt	No
27	0x6C	11	TMR3_INT	TMR3	Timer 3 interrupt	No
28	0x70	12	UART0_INT	UART0	UART0 interrupt	Yes
29	0x74	13	Reserved	-	-	-
30	0x78	14	SPI0_INT	SPI0	SPI0 interrupt	No
31	0x7C	15	Reserved	-	-	-
32	0x80	16	GP5_INT	GPIO	External signal interrupt from P5[7:0]	Yes
33	0x84	17	GP67_INT	GPIO	External signal interrupt from P6[7:0] / P7[1:0]	Yes
34	0x88	18	I2C0_INT	I^2C0	I^2C0 interrupt	Yes
35	0x8C	19	I2C1_INT	I^2C1	I^2C1 interrupt	Yes
36	0x90	20	CAP0_INT	PWM	PWM0 capture in interrupt	No
37	0x94	21	CAP1_INT	PWM	PWM1 capture in interrupt	No
38	0x98	22	CAP2_INT	PWM	PWM2 capture in interrupt	No
39	0x9C	23	CAP3_INT	PWM	PWM3 capture in interrupt	No
40-43	0x90-0xAC	20-27	Reserved	-	-	-
44	0xB0	28	PWRWU_INT	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	0xB4	29	ADC_INT	ADC	ADC interrupt	No
46-47	0xB8-0xBC	30-31	Reserved	-	-	

Table 6.2-3 System Interrupt Map Vector Table

6.2.7.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6.2-4 Vector Figure Format

6.2.7.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

6.3.2 Clock Generator Block Diagram

The clock generator consists of 4 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 22.1184 MHz internal high speed oscillator (HIRC)) (PLL FOUT)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

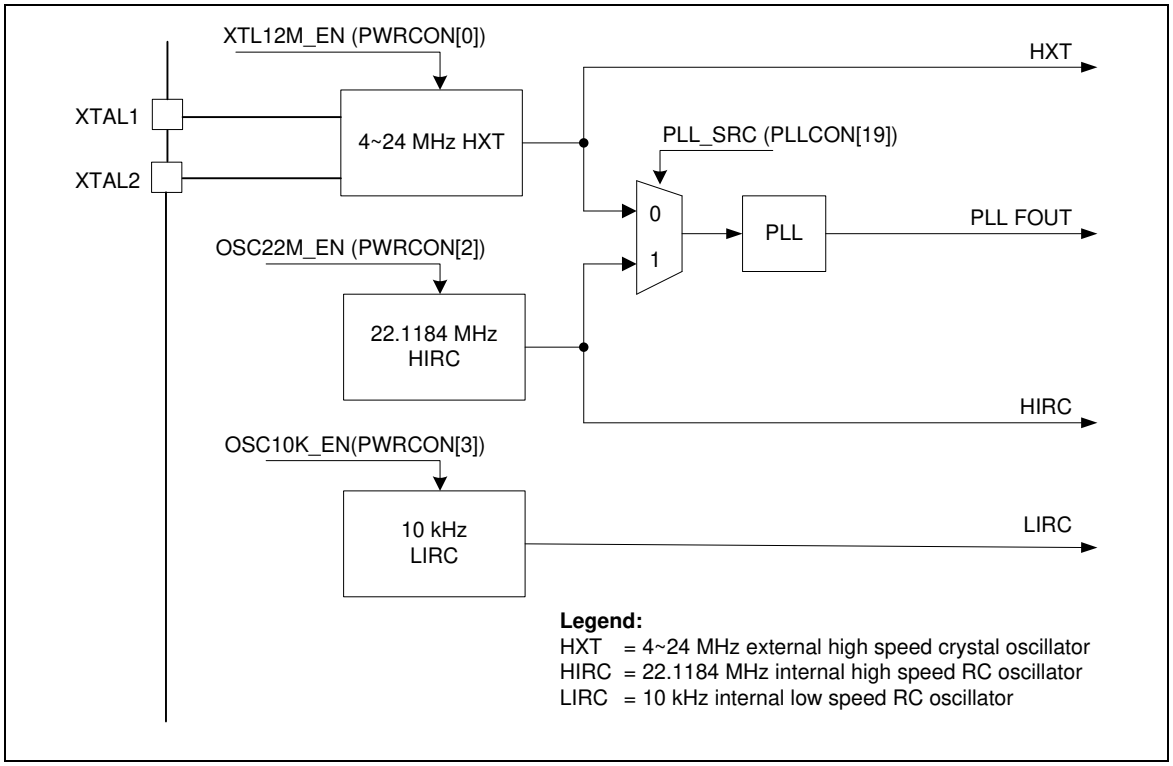


Figure 6.3-1 Clock Generator Block Diagram

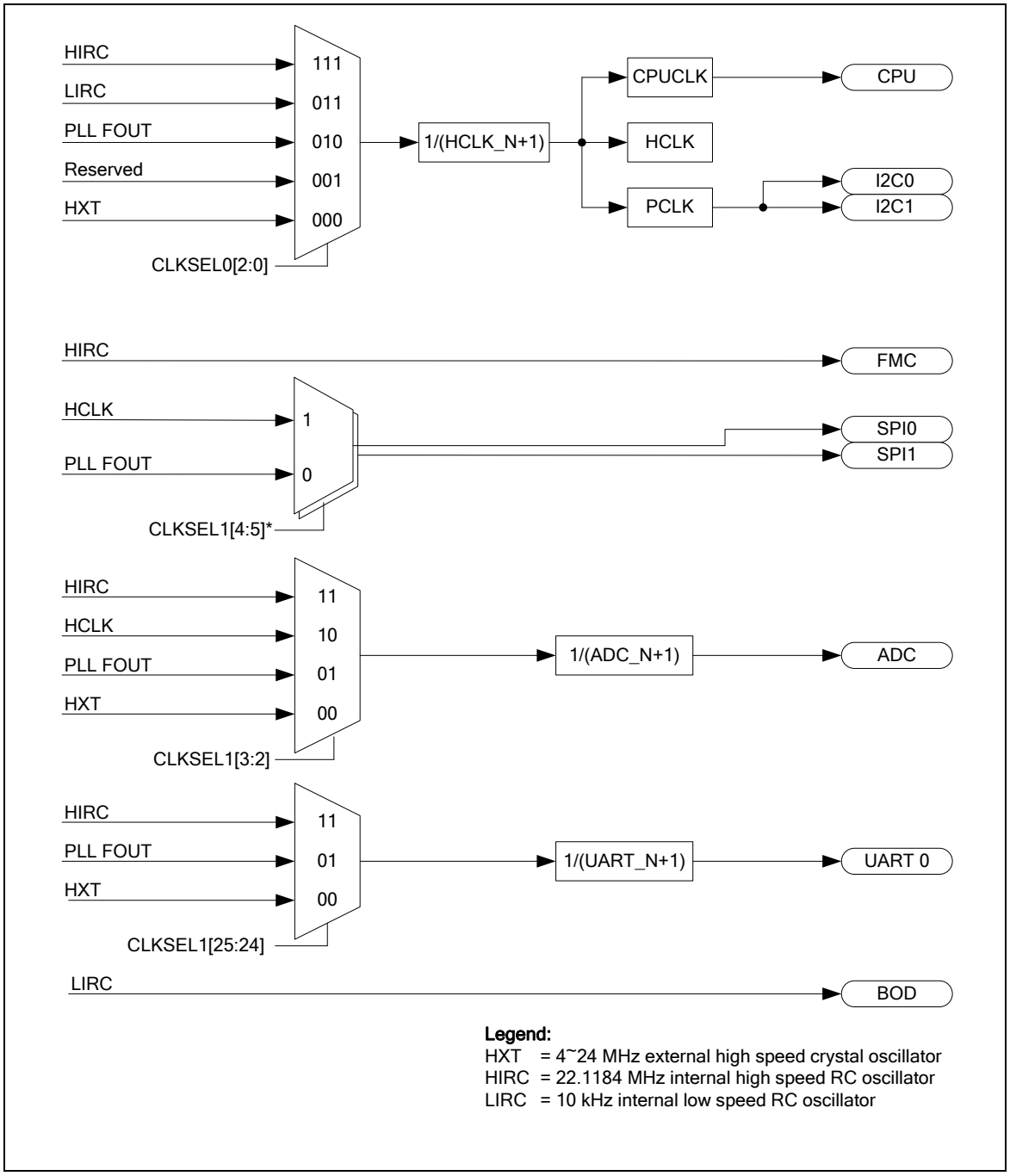
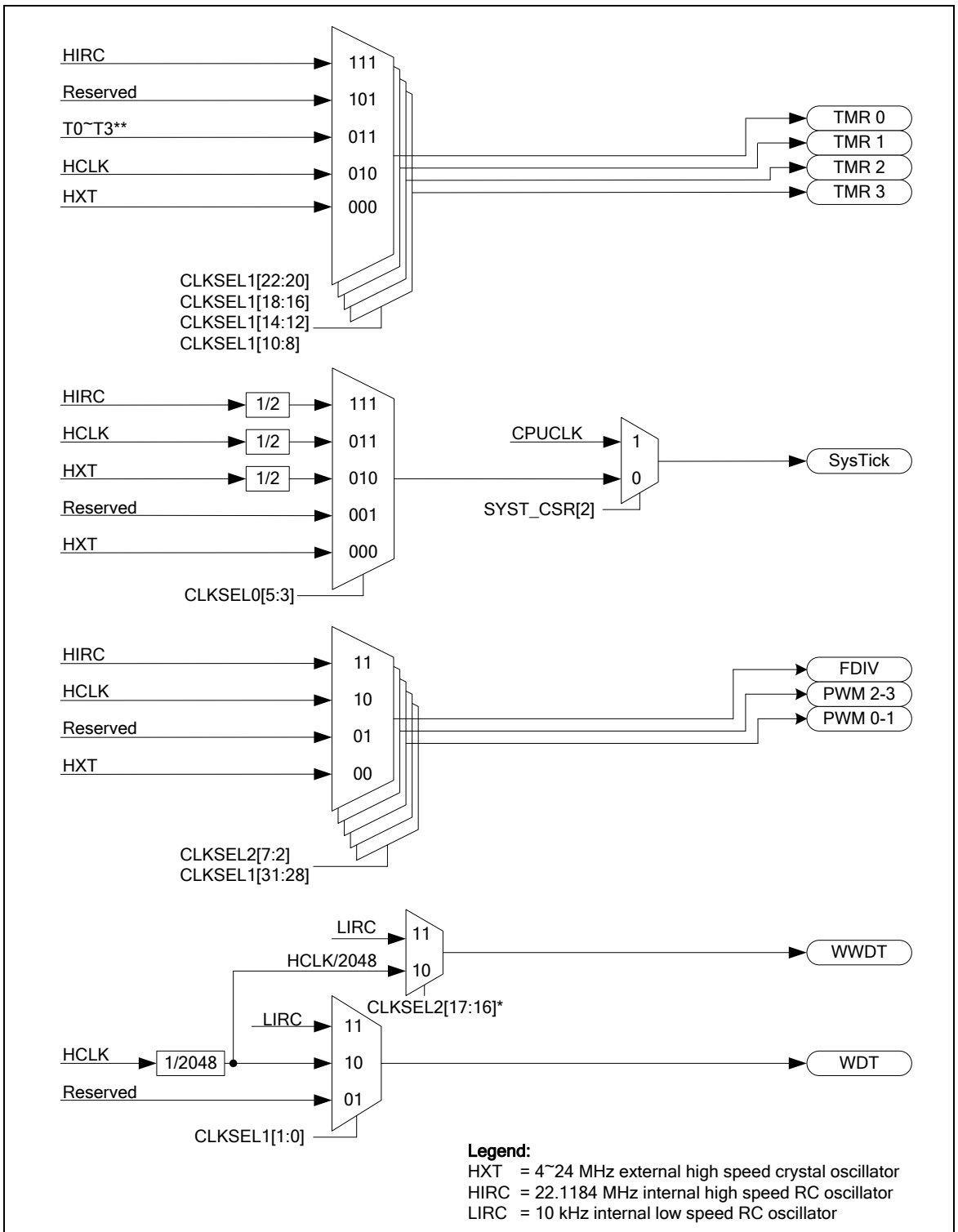


Figure 6.3-2 Clock Source Controller Overview (1/2)



Note1: T0 is for TMR0, T1 is for TMR1, T2 is for TMR2 and T3 is for TMR3.

Figure 6.3-3 Clock Source Controller Overview (2/2)

6.3.3 System Clock & SysTick Clock

The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown below.

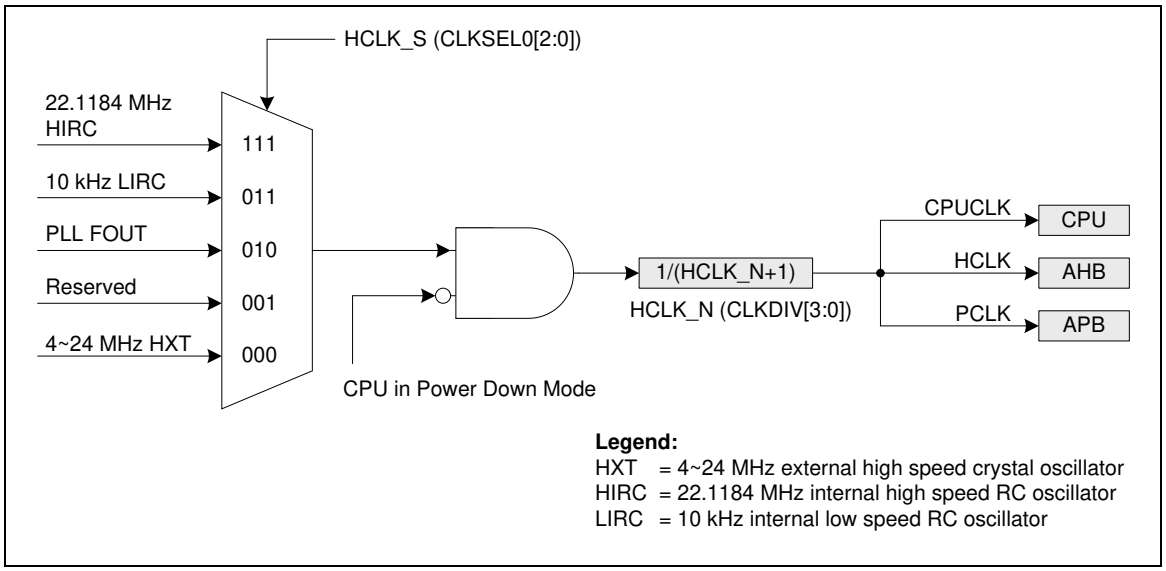


Figure 6.3-4 System Clock Block Diagram

The clock source of SysTick in Cortex-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]. The block diagram is shown below.

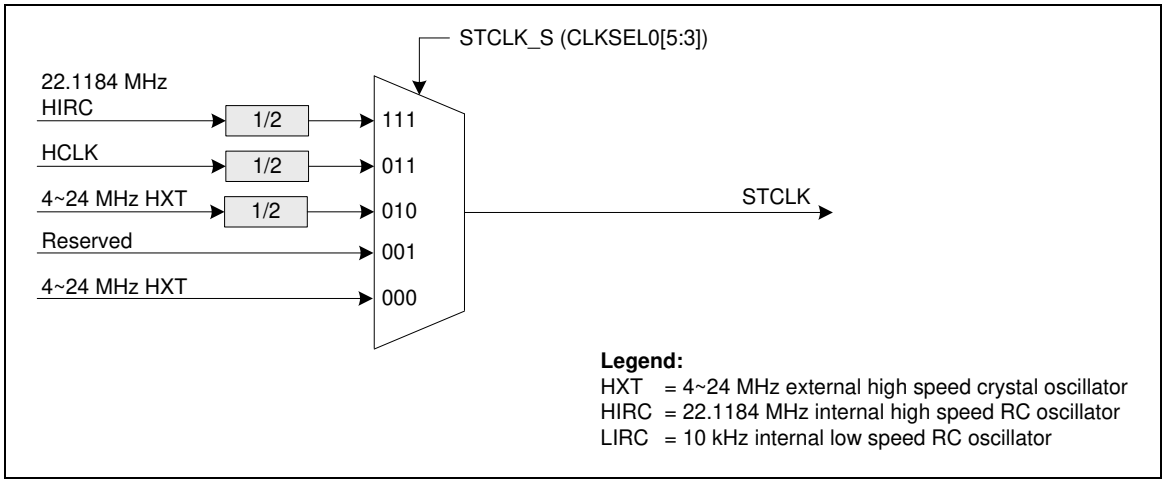


Figure 6.3-5 SysTick clock Control Block Diagram

6.3.4 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator clock
- Peripherals Clock (when 10 kHz low speed oscillator is adopted as clock source)

6.3.5 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\boldsymbol{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQDIV.FSEL[3:0].

When write 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When write 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1(FRQDIV[5]) set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CKO pin directly.

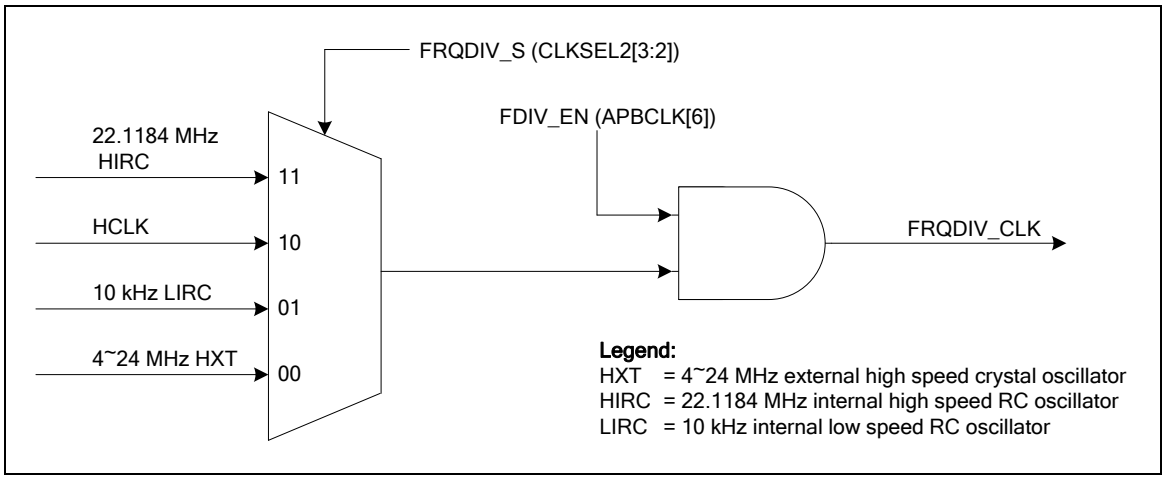


Figure 6.3-6 Clock Source of Frequency Divider

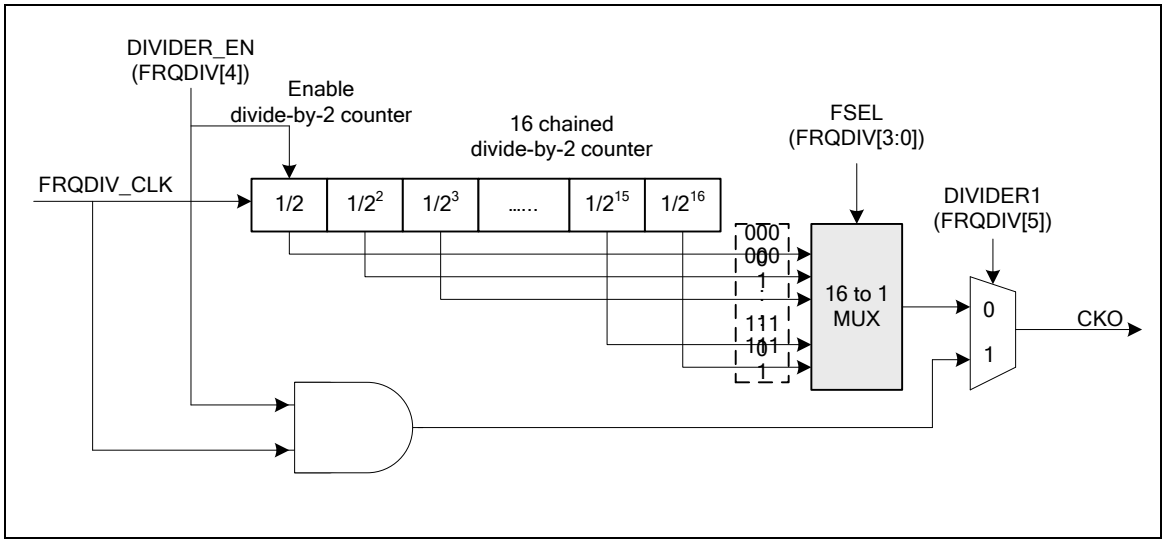


Figure 6.3-7 Block Diagram of Frequency Divider

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The M058S Series are equipped with 64/32/16/8 KB on chip embedded Flash memory for application program (APROM) that can be updated through ISP registers. In-System-Programming (ISP) and In-Application-Programming (IAP) enable user to update program memory when chip is soldered on PCB. After chip power on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, it also provides additional 4 KB DATA Flash for user to store some application depended data before chip power off in 64/32/16/8 KB APROM model.

It provides more settings in CONFIG0 to support more advanced functions, including power-on with tri-state I/O, default to enable WDT after booting, enable WDT in Power-down mode, and IAP functions. The following table shows the added functions of M058S Series.

	M058S Series
CONFIG[6]	To support IAP function and Multi-Boot function
CONFIG[10]	Select I/O state after booting
CONFIG[30]	To support WDT in Power-Down mode when WDT is default on after booting
CONFIG[31]	To support WDT default on after booting

Table 6.4-1 M058S Series Function Difference List (FMC)

6.4.2 Features

- Runs up to 50 MHz with zero wait state for continuous address read access
- 32 KB application program memory (APROM)
- 4 KB in system programming (ISP) loader program memory (LDROM)
- Fixed 4 KB Data Flash
- All embedded flash memory supports 512 bytes page erase

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

There are 58 General Purpose I/O pins shared with special feature functions in this MCU. The 58 pins are arranged in 9 ports named with P0, P1… to P7. Each port equips maximum 8 pins except P7[1:0]. Each one of the 58 pins is independent and has the corresponding register bits to control the pin mode function and data

The I/O type of each of I/O pins can be software configured individually as input, output, open-drain or quasi-bidirectional mode. The all pins of I/O type stay in quasi-bidirectional mode and port data register Px_DOUT[7:0] resets to 0x000_00FF. Each I/O pin equips a very weakly individual pull-up resistor which is about 110KΩ~300KΩ for V_{DD} which is from 5.0V to 2.5V.

6.5.2 Features

- Four I/O modes:
  - Input only with high impedance
  - Push-pull output
  - Open-drain output
- Quasi-bidirectional TTL/Schmitt trigger input mode selected by Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function
- Configurable default I/O mode of all pins after reset by CIOINI(CONFIG[10]) setting
  - CIOINI = 0, all GPIO pins in Input tri-state mode after chip reset
  - CIOINI = 1, all GPIO pins in Quasi-bidirectional mode after chip reset

6.6 Timer Controller (TMR)

6.6.1 Overview

The Timer Controller includes four 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features:

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (Period time of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period time of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the input event from external counter pin (T0~T3)
- 24-bit capture value is readable through TCAP (Timer Capture Data Register)
- Supports external capture pin (T0EX~T3EX) for interval measurement
- Supports external capture pin (T0EX~T3EX) to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Inter-Timer trigger mode

6.7 PWM Generator and Capture Timer (PWM)

6.7.1 Overview

The NuMicro™ M058S has one sets of PWM groups supporting a total of two sets of PWM generators, which can be configured as four independent PWM outputs, PWM0~PWM3, or as two complementary PWM pairs, (PWM0, PWM1) and (PWM2, PWM3) with 2 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 2 sets of PWM generators provide four independent PWM period interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM period interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When DZEN01 (PCR[4]) is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-zone are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3) are controlled by PWM2 timers and Dead-zone generator 2. Refer to figures below for the architecture of PWM Timers.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be loaded into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-Timer is set as Auto-reload mode when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically and then starts decreasing repeatedly. If the PWM-Timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-Timer is digital input Capture function. If Capture function is enabled, the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must set the PWM-Timer before enabling the Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CRL_IE0 (CCR0[1]) (Rising latch Interrupt enable) and CFL_IE0 (CCR0[2]) (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CRL_IE1 (CCR0[17]) and CFL_IE1 (CCR0[18]). The capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read PIIR to get interrupt source, read CRLRx/CFLRx (x = 0~3) to get capture value and finally write 1 to clear PIIR to 0. If interrupt latency will take time T0 to finish, the capture signal mustn't

transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0.

6.7.2 Features

PWM function:

PWM group has two PWM generators. Each PWM generator supports one 8-bit prescaler, one clock divider, two PWM-Timers (down counter), one dead-zone generator and two PWM outputs.

- PWMA (PWM group A) is a group of PWM which support 4 PWM channels or 2 complementary PWM paired channels
- PWM group has two PWM generators with each PWM generator supporting one 8-bit prescaler, two clock dividers, two PWM-Timers, one Dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- One-shot or Auto-reload mode
- Edge-aligned type or Center-aligned type option
- PWM trigger ADC start-to-conversion

Capture function:

- Timing control logic shared with PWM generators
- Supports 4 Capture input channels shared with 4 PWM output channels
- Each channel supports one rising latch register (CRLRx), one falling latch register (CFLRx) and Capture interrupt flag (CAPIFx)

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.8.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer reset delay period
  - ◆ Selectable reset delay period 3/18/130/1026 * WDT_CLK
- Supports to force Watchdog Timer enabled after chip powered on or reset while CWDTEN (CONFIG[31] Watchdog Enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The purpose of Window Watchdog Timer is to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.9.2 Features

- 6-bit down counter value (WWDTCVAL) and 6-bit compare window value (WINCMP) to make the WWDT time-out window period flexible
- Supports 4-bit value to programmable maximum 11-bit prescale counter period of WWDT counter

6.10 UART Interface Controller (UART)

6.10.1 Overview

The NuMicro™ M058S provides two channels of Universal Asynchronous Receiver/Transmitters (UART). UART Controller performs Normal Speed UART, and support flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, LIN master/slave function and RS-485 function mode. Each UART Controller channel supports seven types of interrupts.

6.10.2 Features

- Full duplex, asynchronous communications
- Separate receive / transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake up function
- Supports 8 bit receiver buffer time out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5, 6, 7, 8 bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- Supports RS-485 function mode.
  - Supports RS-485 9bit mode
  - Supports hardware or software enable to program RTS pin to control RS-485 transmission direction directly

6.11 I²C Serial Interface Controller (I²C)

6.11.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. There are two sets of I²C which supports Power-down wake up function.

6.11.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between master and slave
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down Wake-up function

6.12 Serial Peripheral Interface (SPI)

6.12.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full-duplex transfer. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. The NuMicro™ M058S contains one set of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. SPI controller can be configured as a master or a slave device.

6.12.2 Features

- One set of SPI controllers
- Supports Master or Slave mode operation
- Configurable transfer bit length
- Provides transmit/receive can be transferred up to two times word transaction in one transfer
  - Provides FIFO buffers
- Supports MSB or LSB first transfer
- Supports byte reorder function
- Supports byte or word suspend mode
- Supports Slave 3-wire mode
- SPI bus clock rate can be configured to equal the system clock rate

6.13 Analog-to-Digital Converter (ADC)

6.13.1 Overview

The NuMicro™ M058S series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with eight input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (STADC/P3.2) or PWM trigger.

6.13.2 Features

- Analog input voltage range: 0 ~ AV_{DD}.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to eight single-end analog input channels or 4 differential analog input channels
- Maximum ADC peripheral clock frequency is 16 MHz
- Up to 760 kSPS sample rate
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - PWM trigger with optional start delay period
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- Channel 7 supports 3 input sources: external analog voltage, internal band-gap voltage and
- Internal temperature sensor output.

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD} –V_{SS}	-0.3	+7.0	V
Input Voltage	VIN	V_{SS}-0.3	V_{DD} +0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

7.2 DC Electrical Characteristics

(V_{DD} -V_{SS}=2.5~5.5V, TA = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
LDO Output Voltage	V_{LDO}	1.7	1.8	1.9	V	V_{DD} ≥ 2.5V
Band Gap Analog Input	V_{BG}	-5%	1.20	+5%	V	V_{DD} =2.5V ~ 5.5V
Analog Operating Voltage	AV_{DD}	V_{DD}		V_{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	IDD1		20.6		mA	V_{DD} = 5.5V@ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
	IDD2		14.4		mA	V_{DD} =5.5V@ 50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
	IDD3		18.9		mA	V_{DD} = 3.3V@ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
	IDD4		12.8		mA	V_{DD} = 3.3V@ 50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 22 MHz	IDD5		6.2		mA	V_{DD} = 5.5V@ 22 MHz, enable all peripherals and IRC 22 MHz, disable PLL
	IDD6		3.4		mA	V_{DD} =5.5V@ 22 MHz, disable all peripherals and enable IRC 22 MHz, disable PLL
	IDD7		6.1		mA	V_{DD} = 3.3V@ 22 MHz, enable all peripherals and IRC 22 MHz, disable PLL
	IDD8		3.4		mA	V_{DD} = 3.3V@ 22 MHz, disable all peripherals and enable IRC 22 MHz, disable PLL
Operating Current Normal Run Mode @ 12 MHz	IDD9		5.3		mA	V_{DD} = 5.5V@ 12 MHz, enable all peripherals and disable PLL, XTAL=12 MHz
	IDD10		3.7		mA	V_{DD} = 5.5V@ 12 MHz, disable all peripherals and disable PLL, XTAL=12 MHz
	IDD11		4.0		mA	V_{DD} = 3.3V@ 12 MHz, enable all peripherals and disable PLL, XTAL=12 MHz
	IDD12		2.3		mA	V_{DD} = 3.3V@ 12 MHz, disable all peripherals and disable PLL, XTAL=12 MHz

Operating Current Normal Run Mode @ 4 MHz	IDD13		3.4		mA	V_{DD} = 5.5V@ 4 MHz, enable all peripherals and disable PLL, XTAL=4 MHz
	IDD14		2.6		mA	V_{DD} = 5.5V@ 4 MHz, disable all peripherals and disable PLL, XTAL=4 MHz
	IDD15		2.0		mA	V_{DD} = 3.3V@ 4 MHz, enable all peripherals and disable PLL, XTAL=4 MHz
	IDD16		1.3		mA	V_{DD} = 3.3V@ 4 MHz, disable all peripherals and disable PLL, XTAL=4 MHz
Operating Current Normal Run Mode @10 KHz	IDD17		98.7		uA	V_{DD} = 5.5V@ 10 KHz, enable all peripherals and IRC10 KHz, disable PLL
	IDD18		97.4		uA	V_{DD} = 5.5V@ 10 KHz, disable all peripherals and enable IRC 10KHz, disable PLL
	IDD19		86.4		uA	V_{DD} = 3.3V@ 10 KHz, enable all peripherals and IRC 10 KHz, disable PLL
	IDD20		85.2		uA	V_{DD} = 3.3V@ 10 KHz, disable all peripherals and enable IRC 10 KHz, disable PLL
Operating Current Idle Mode @ 50 MHz	IIDLE1		16.2		mA	V_{DD} = 5.5V@ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
	IIDLE2		10.0		mA	V_{DD} =5.5V@ 50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
	IIDLE3		14.6		mA	V_{DD} = 3V@ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
	IIDLE4		8.5		mA	V_{DD} = 3V@50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
Operating Current Idle Mode @ 22 MHz	IIDLE5		4.3		mA	V_{DD} = 5.5V@ 22MHz, enable all peripherals and IRC 22MHz, disable PLL
	IIDLE6		1.5		mA	V_{DD} =5.5V@ 22MHz, disable all peripherals and enable IRC 22 MHz, disable PLL
	IIDLE7		4.2		mA	V_{DD} = 3.3V@ 22 MHz, enable all peripherals-and IRC 22 MHz, disable PLL
	IIDLE8		1.4		mA	V_{DD} = 3.3V@ 22 MHz, disable all peripherals and enable IRC 22MHz, disable PLL
Operating Current Idle Mode @ 12 MHz	IIDLE9		4.3		mA	V_{DD} = 5.5V@ 12 MHz, enable all peripherals and disable PLL, XTAL=12MHz
	IIDLE10		2.6		mA	V_{DD} = 5.5V@ 12 MHz, disable all peripherals and disable PLL, XTAL=12MHz

	IIDLE11		2.9		mA	V_{DD} = 3.3V@ 12 MHz, enable all peripherals and disable PLL, XTAL=12MHz
	IIDLE12		1.3		mA	V_{DD} = 3.3V@ 12 MHz, disable all peripherals and disable PLL, XTAL=12MHz
Operating Current Idle Mode @ 4 MHz	IIDLE13		3.0		mA	V_{DD} = 5.5V@ 4 MHz, enable all peripherals and disable PLL, XTAL=4MHz
	IIDLE14		2.3		mA	V_{DD} = 5.5V@ 4 MHz, disable all peripherals and disable PLL, XTAL=4MHz
	IIDLE15		1.7		mA	V_{DD} = 3.3V@ 4 MHz, enable all peripherals and disable PLL, XTAL=4MHz
	IIDLE16		1.0		mA	V_{DD} = 3.3V@ 4 MHz, disable all peripherals and disable PLL, XTAL=4MHz
Operating Current Idle Mode @10 KHz	IIDLE17		97.8		uA	V_{DD} = 5.5V@ 10 KHz, enable all peripherals and IRC 10 KHz, disable PLL
	IIDLE18		96.5		uA	V_{DD} = 5.5V@ 10 KHz, disable all peripherals and enable IRC 10 KHz, disable PLL
	IIDLE19		85.5		uA	V_{DD} = 3.3V@ 10 KHz, enable all peripherals and IRC 10 KHz, disable PLL
	IIDLE20		84.4		uA	V_{DD} = 3.3V@ 10 KHz, disable all peripherals and enable IRC 10 KHz, disable PLL
Standby Current Power-down Mode (Deep Sleep Mode)	IPWD1		10		μA	V_{DD} = 5.5V, No load @ Disable BOV function
	IPWD2		10		μA	V_{DD} = 3.0V, No load @ Disable BOV function
Input Current P0/1/2/3/4 (Quasi-bidirectional mode)	IIN1	-75	-	+15	μA	V_{DD} = 5.5V, VIN = 0V or VIN= V_{DD}
Input Leakage Current P0/1/2/3/4	ILK	-1	-	+1	μA	V_{DD} = 5.5V, 0<VIN< V_{DD}
Input Low Voltage P0/1/2/3/4 (TTL input)	VIL1	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage P0/1/2/3/4 (TTL input)	VIH1	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V
Input Low Voltage XT1[*2]	VIL3	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 2.5V
Input High Voltage XT1[*2]	VIH3	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input), /RST	VILS	-0.5	-	0.2 V_{DD}	V	
Positive going threshold (Schmitt input), /RST	VIHS	0.7 V_{DD}	-	V_{DD} +0.5	V	

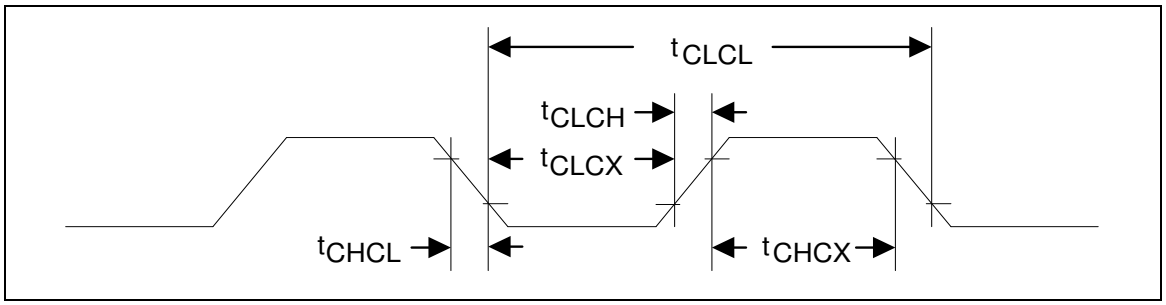
Internal /RST pin pull up resistor	RRST	40		150	KΩ	
Negative going threshold (Schmitt input), P0/1/2/3/4	VILS	-0.5	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), P0/1/2/3/4	VIHS	0.7 V_{DD}	-	V_{DD} +0.5	V	
Source Current P0/1/2/3/4 (Quasi-bidirectional Mode)	ISR11	-300	-370	-450	μA	V_{DD} = 4.5V, VS = 2.4V
	ISR12	-50	-70	-90	μA	V_{DD} = 2.7V, VS = 2.2V
	ISR13	-40	-60	-80	μA	V_{DD} = 2.5V, VS = 2.0V
Source Current P0/1/2/3/4 (Push-pull Mode)	ISR21	-20	-24	-28	mA	V_{DD} = 4.5V, VS = 2.4V
	ISR22	-4	-6	-8	mA	V_{DD} = 2.7V, VS = 2.2V
	ISR23	-3	-5	-7	mA	V_{DD} = 2.5V, VS = 2.0V
Sink Current P0/1/2/3/4 (Quasi-bidirectional and Push-pull Mode)	ISK11	10	16	20	mA	V_{DD} = 4.5V, VS = 0.45V
	ISK12	7	10	13	mA	V_{DD} = 2.7V, VS = 0.45V
	ISK13	6	9	12	mA	V_{DD} = 2.5V, VS = 0.45V
Brown-Out voltage with BOV_VL [1:0] =00b	VBO2.2	2.0	2.2	2.4	V	V_{DD} =5.5V
Brown-Out voltage with BOV_VL [1:0] =01b	VBO2.7	2.5	2.7	2.9	V	V_{DD} =5.5V
Brown-Out voltage with BOV_VL [1:0] =10b	VBO3.7	3.5	3.7	3.9	V	V_{DD} =5.5V
Brown-Out voltage with BOV_VL [1:0] =11b	VBO4.4	4.2	4.4	4.6	V	V_{DD} =5.5V
Hysteresis range of BOD voltage	VBH	30	-	150	mV	V_{DD} = 2.5V~5.5V

Notes:

1. /RST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0 - P7 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when Vin approximates to 2V.

7.3 AC Electrical Characteristics

7.3.1 External Crystal



Note: Duty cycle is 50%.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	t_{CHCX}	20	-	-	nS	
Clock Low Time	t_{CLCX}	20	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

7.3.2 External Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	°C
V_{DD}	-	2.5	5	5.5	V
Operating current	12 MHz@ V_{DD} = 5V	-	1	-	mA

7.3.3 Typical Crystal Application Circuits

CRYSTAL	C1	C2
4 MHz ~ 24 MHz	Optional (Depend on crystal specification)	

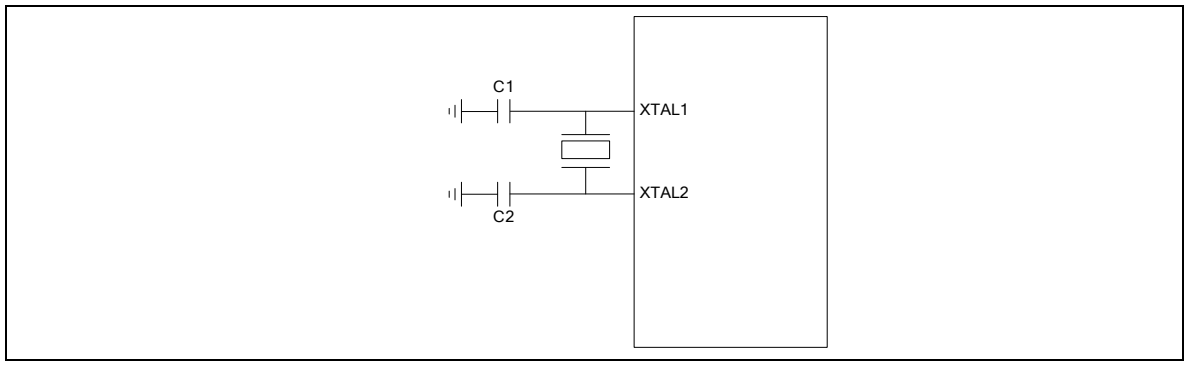


Figure 7.3-1 Typical Crystal Application Circuit

7.3.4 Internal 22.1184 MHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Center Frequency	-	-	22.1184		MHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-3	-	+3	%
	-40°C~+85°C; V_{DD}=2.5V~5.5V	-5	-	+5	%
Operating current	V_{DD} =5V	-	500	-	uA

7.3.5 Internal 10 kHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-30	-	+30	%
	-40°C~+85°C; V_{DD}=2.5V~5.5V	-50	-	+50	%
Operating current	V_{DD} =5V	-	5	-	uA

Notes:

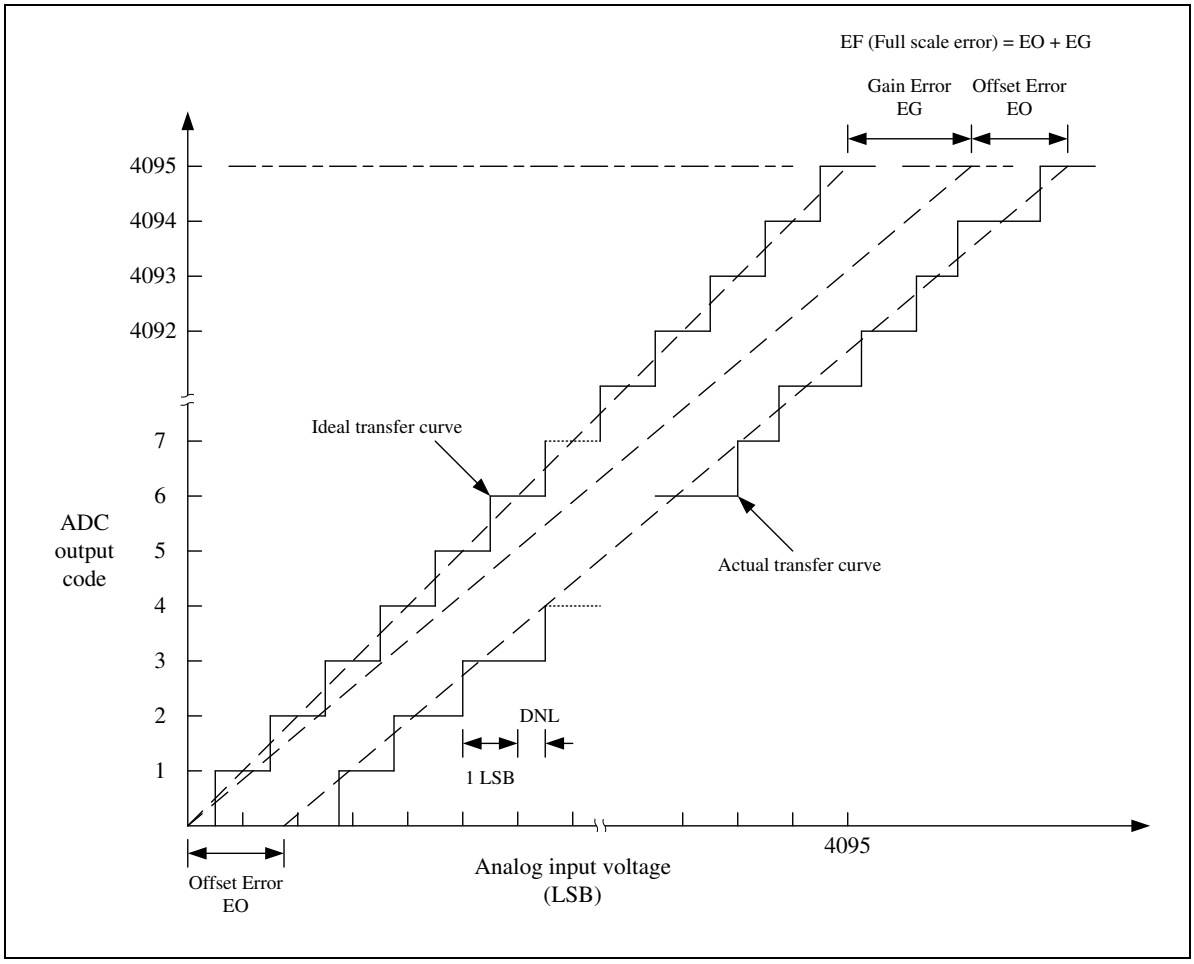
1. Internal operation voltage comes from LDO.

7.4 Analog Characteristics

7.4.1 12-bit SARADC Specification

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
-	Resolution		-	-	12	Bit
DNL	Differential nonlinearity error		-	-1~2.0	-1~4.0	LSB
INL	Integral nonlinearity error		-	±2	±4	LSB
E_O	Offset error		-	3	-	LSB
E_G	Gain error (Transfer gain)		-	1	1.005	-
E_F	Full scale error			±2		LSB
E_A	Absolute error	AV_{DD} =5V		5		LSB
		AV_{DD} =3V		4		
-	Monotonic		Guaranteed			
F_{ADC}	ADC clock frequency	AV_{DD} =5V	-	-	16	MHz
		AV_{DD} =3V			8	
F_S	Sample rate		-	-	760	K SPS
T_S	Sampling time		7			ADC clock
V_{DDA}	Supply voltage		3	-	5.5	V
I_{DD}	Supply current (Avg.)		-	0.5	-	mA
I_{DDA}	Supply current (Avg.) @ AV_{DD} =3.0V		-	2.5	-	mA
V_{IN}	Analog Input voltage		0	-	V_{ref}[1]	V

Note[1]: V_{ref} is connected to AV_{DD} for LQFP48/QFN33 package.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

7.4.2 LDO Specification

RAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5		5.5	V	V_{DD} input voltage
Output Voltage	-10%	1.8	+10%	V	LDO output voltage
Temperature	-40	25	85	℃	
C	-	1	-	uF	Resr=1ohm

Note:

1. It is recommended a 100nF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

7.4.3 Low Voltage Reset Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	5	5.5	V
Temperature	-	-40	25	85	℃
Quiescent current	V_{DD} =5.5V	-	-	5	uA
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.3	-	V
	Temperature=85°	-	1.8	-	V
Hysteresis	-	0	0	0	V

7.4.4 Brown-Out Detector Specification

Parameter	Condition	Min.	Typ.	Max.	Unit
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV_{DD} =5.5V	-	-	140	μA
Temperature	-	-40	25	85	℃
Brown-Out voltage	BOV_VL[1:0]=11	4.2	4.4	4.6	V
	BOV_VL [1:0]=10	3.5	3.7	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30m	-	150m	V

7.4.5 Power-On Reset Specification (5V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

7.4.6 Temperature Sensor Specification

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]		1.62	1.8	1.98	V
Temperature		-40	-	85	℃
Gain		-1.72	-1.76	-1.80	mV/℃
Offset	Temp=0 ℃	717	725	733	mV

Note[1]: Internal operation voltage comes from LDO.

7.4.7 Comparator Specification

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
V_{DD}	-	2.4	3	5.5	V
V_{DD} current	-	-	40	80	uA
Input offset voltage	-		10	20	mV
Output swing	-	0.1	-	V_{DD} -0.1	V
Input common mode range	-	0.1	-	V_{DD} -0.1	V
DC gain	-	-	70	-	dB
Propagation delay	@VCM=1.2 V and VDIFF=0.1 V	-	200	-	ns
Hysteresis	@VCM=0.2 V ~ V_{DD} -0.2V	-	±10	-	mV
Stable time	@CINP=1.3 V CINN=1.2 V	-	-	2	us

7.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{RET}	Retention time	Temp=85 ℃	10			year
T_{ERASE}	Page erase time		19	20	21	ms
T_{MESS}	Mess erase time		30	40	50	ms
T_{PROG}	Program time		38	40	42	us
V_{DD}	Supply voltage		1.62	1.8	1.98	V[2]
I_{DD1}	Read current				0.25	mA
I_{DD2}	Program/Erase current				7	mA
I_{PD}	Power down current			1	20	uA

1. Number of program/erase cycles.
2. V_{DD} is source from chip LDO output voltage.
3. Guaranteed by design, not test in production.

7.6 SPI Dynamic Characteristics

7.6.1 Dynamic Characteristics of Data Input and Output Pin

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI Master Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	3	-	-	ns
t_V	Data output valid time	-	3.5	4.5	ns
SPI Master Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time				ns
t_{DH}	Data hold time				ns
t_V	Data output valid time				ns
SPI Slave Mode (VDD = 4.5 V ~ 5.5 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	3	-	-	ns
t_V	Data output valid time	-	20	27.5	ns
SPI Slave Mode (VDD = 3.0 V ~ 3.6 V, 30 pF loading Capacitor)					
t_{DS}	Data setup time				ns
t_{DH}	Data hold time				ns
t_V	Data output valid time				ns

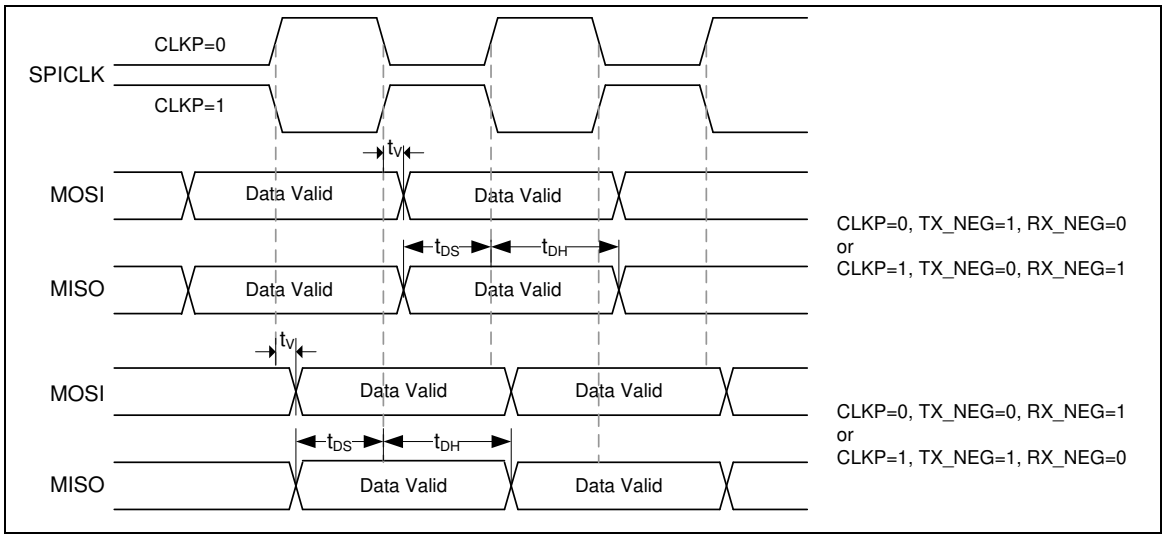


Figure 7.6-1 SPI Master Mode Timing

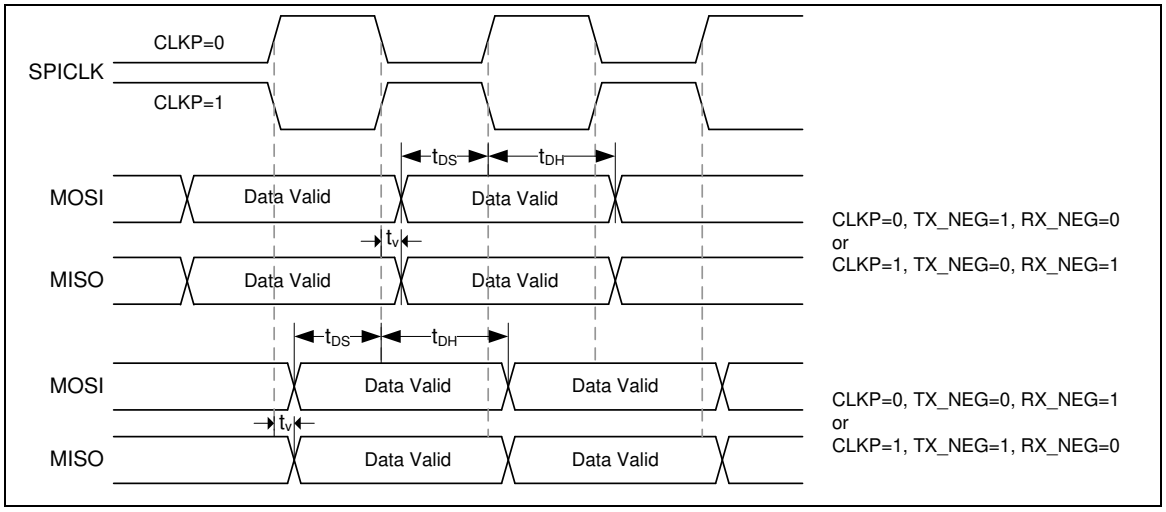


Figure 7.6-2 SPI Slave Mode Timing

7.7 I2C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I^2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I^2C frequency.
3. I^2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

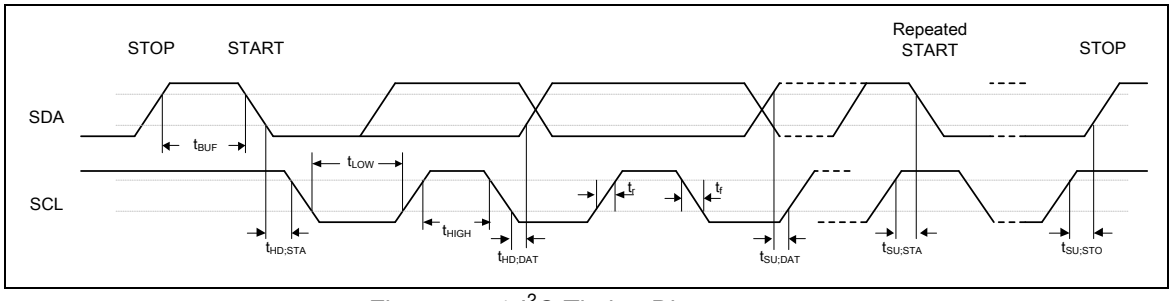
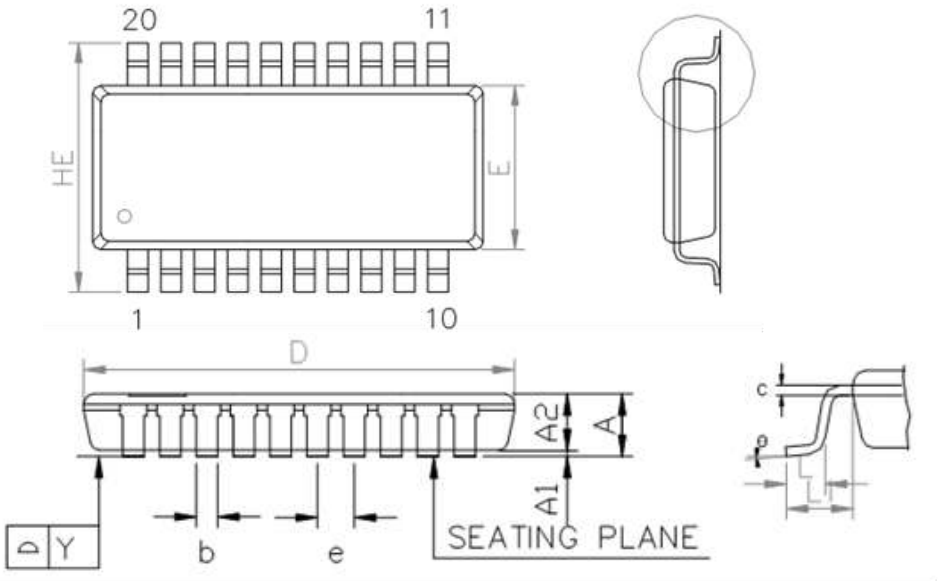


Figure 7.7-1 I^2C Timing Diagram

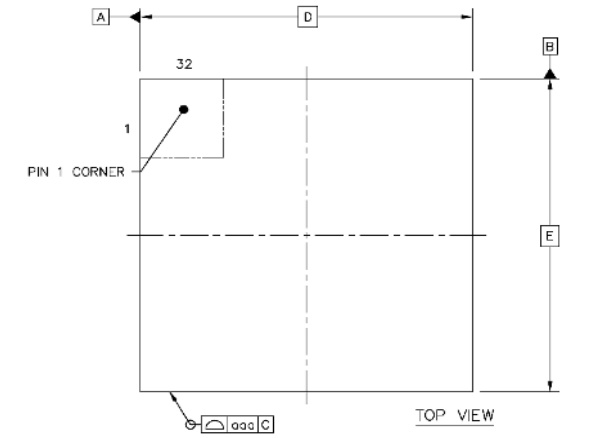
8 PACKAGE DIMENSIONS

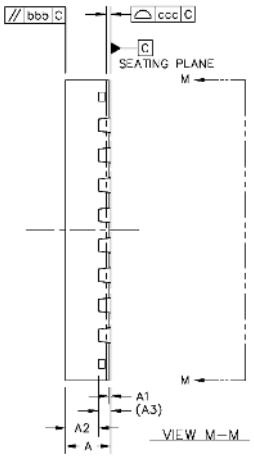
8.1 TSSOP-20 (4.4x6.5 mm)

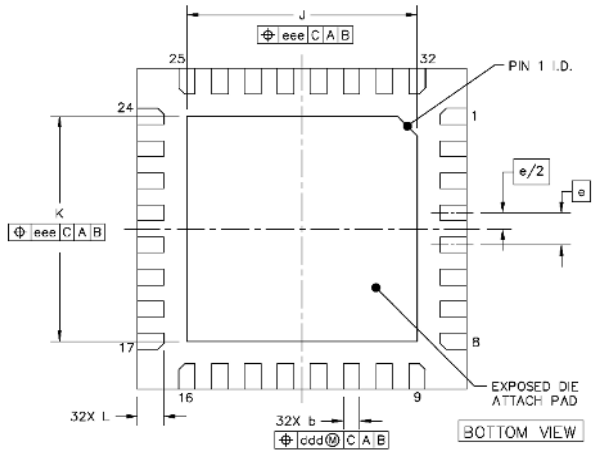


SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		

8.2 QFN-33 (5X5 mm^2, Thickness 0.8mm, Pitch 0.5 mm)

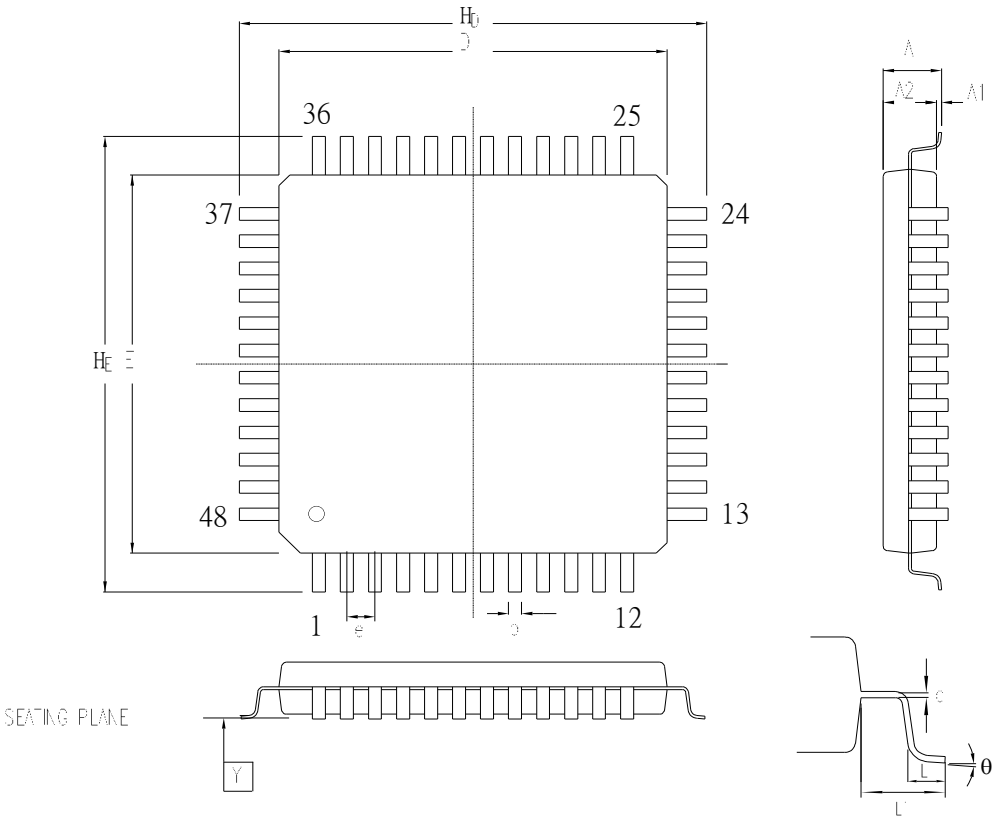






		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

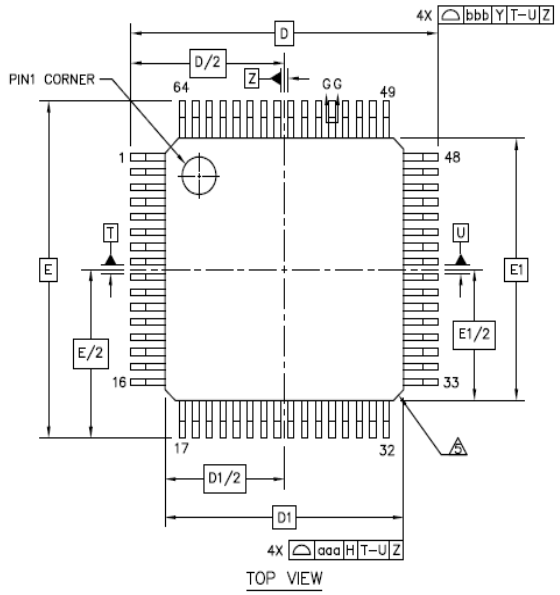
8.3 LQFP-48 (7x7x1.4mm² Footprint 2.0mm)

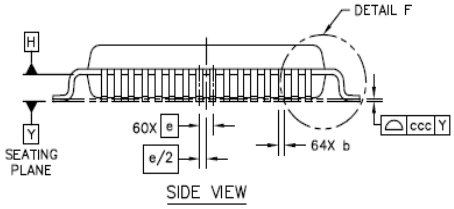


Controlling dimension : Millimeters

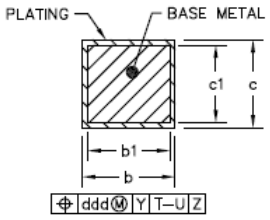
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

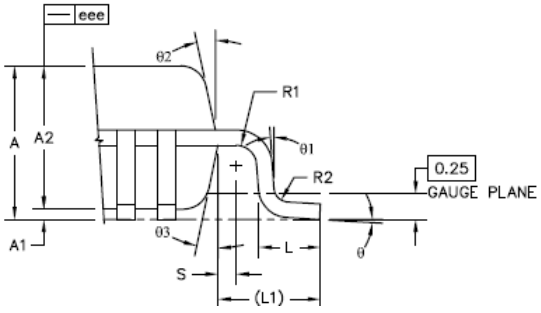
8.4 LQFP-64 (7x7x1.4mm² Footprint 2.0mm)





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		





9 REVISION HISTORY

Revision	Date	Description
1.00	Jun. 12, 2014	First version
1.01	Jul. 24, 2014	Corrected 7.5 Flash DC Electrical Characteristics.
1.02	Sep. 12, 2014	1. Adjusted the format of Table 4.1-1 NuMicro™ M058S Series Selection Guide. 2. Updated Figure 4.1-1 NuMicro™ M058S Series Selection Code. 3. Added Chapter 3 ABBREVIATIONS. 4. Added 7.6 SPI Dynamic Characteristics. 5. Changed the order of Chapter 5 BLOCK DIAGRAM and Chapter 6 FUNCTIONAL DESCRIPTION. 6. Fixed typos and obscure descriptions.
1.03	Nov. 27, 2014	1. Fixed typos of Table 4.1-1 NuMicro™ M058S Series Selection Guide
1.04	Jun. 26, 2018	1. Added 7.7 SPI Dynamic Characteristics.
1.05	Apr. 30, 2020	1. Added notes about the hardware reference design for ICE_DAT, ICE_CLK and /RST pins in section 4.3

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