Serial FIR Filter

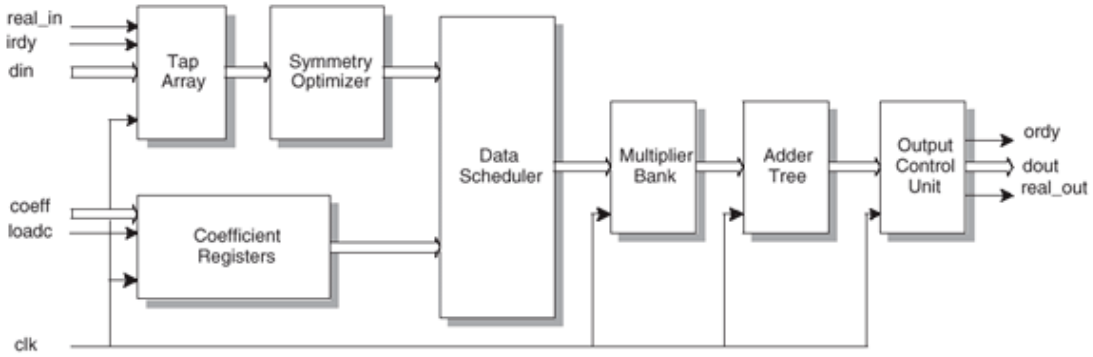
Overview

Many digital systems use filters to remove noise, provide spectral shaping, or perform signal detection. Two types of common filters that provide these functions are Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) filters. IIR filters are used in systems that can tolerate phase distortion. FIR filters have an inherently stable structure, and are used in systems that require linear phase. This benefit makes FIR filters attractive enough that they are designed into a large number of systems. However, for a given frequency response specification, FIR filters are of higher order than IIR, making them computationally expensive.

The Lattice Serial FIR filter uses serial arithmetic elements to achieve a compact size. Due to the serial nature of the arithmetic, the data rate is slower than the clock rate and dependant on the data width. The effective throughput is defined as:

Data rate = (f/(ofw + 1)

where ofw is the Output Full Width and f is the clock frequency.



Features

- Serial Arithmetic for Reduced Resource Utilization
- Variable Number of Taps up to 64
- Data and Coefficients up to 32 Bits
- Output Size Consistent with Data Size
- Signed or Unsigned Data and Coefficients
- Full Arithmetic Precision
- Fixed or Loadable Coefficients
- Decimation and Interpolation
- Real or Complex Data
- Selectable Rounding
- Scaleable Outputs
- Multi-cycle Modes for Area/Time Tradeoffs
- Supports Symmetric or Anti-Symmetric Filters
- Optimization Based on Symmetry of Filter
- Fully Synchronous Design

Evaluation Configurations

Performance and Resource Utilization

Parameter	LUT4s[2]	PFUs[3]	Registers	External Pins	System EBRs	f_{MAX}[1]
fir_ser_xp_1_002.lpc [4]	260	115	382	41	None	185

[1] Performance and utilization characteristics using LFX1200B-04FE680C in Lattice's ispLEVER™ v.3.0 design tool. Synthesized using Synplicity's Synplify Pro v.7.2.1. When using this IP core in a different density, package, speed, or grade within the ispXPGA family, performance may vary slightly.

[2] Look-Up Table (LUT) is a standard logic block of Lattice devices. LUT4 is a 4-input LUT. For more information check the data sheet of the device.

[3] Programmable Function Unit (PFU) is a standard logic block of some Lattice devices. For more information, check the data sheet of the device.

[4] Configuration fir_ser_xp_1_002.lpc has the following settings: Number of Taps (n) = 16, Data Width(w) = 8, Coeff Width = 8, Output Width = 20, Signed, Single-Cycle, Real, Symmetric Coeff, Loadable Coeff (8 Coeffs).

Parameter Values for Evaluation Configuration(s)

Parameter File Name	Input Data Width (Bits)	Number of Taps	FIR Type	Symmetry	Arithmetic type	Data Type	Output Data Width (Full Data Width)[2]
fir_ser_xp_1_002.lpc [1]	8	16	Single cycle	Symmetric	Signed	Real	Full (20)

[1] The latency for the fir_ser_xp_1_002 configuration is (6 + Output_Full_Width + 1) or 27.

[2] The Output Data Width is the same as the Full Data Width.

Ordering Information

Part Numbers: For XPGA: FIR-SER-XP-N1

To find out how to purchase the Serial FIR Filter IP Core, please contact your local Lattice Sales Office.