2.5V PROGRAMMABLE SKEW DUAL PLL CLOCK DRIVER TURBOCLOCK™ W

IDT5T9955

FEATURES:

- Ref input is 3.3V tolerant
- 8 pairs of programmable skew outputs
- Low skew: 185ps same pair, 250ps same bank, 350ps both banks
- Selectable positive or negative edge synchronization on each bank: excellent for DSP applications
- Synchronous output enable on each bank
- Input frequency: 2MHz to 160MHz
- Output frequency: 6MHz to 160MHz
- 3-level inputs for skew and PLL range control
- 3-level inputs for feedback divide selection multiply / divide ratios of (1-6, 8, 10, 12) / (2, 4)
- PLL bypass for DC testing
- External feedback, internal loop filter
- 12mA balanced drive outputs
- Low Jitter: <100ps cycle-to-cycle
- Power-down mode on each bank
- Lock indicator on each bank
- Available in BGA package

DESCRIPTION:

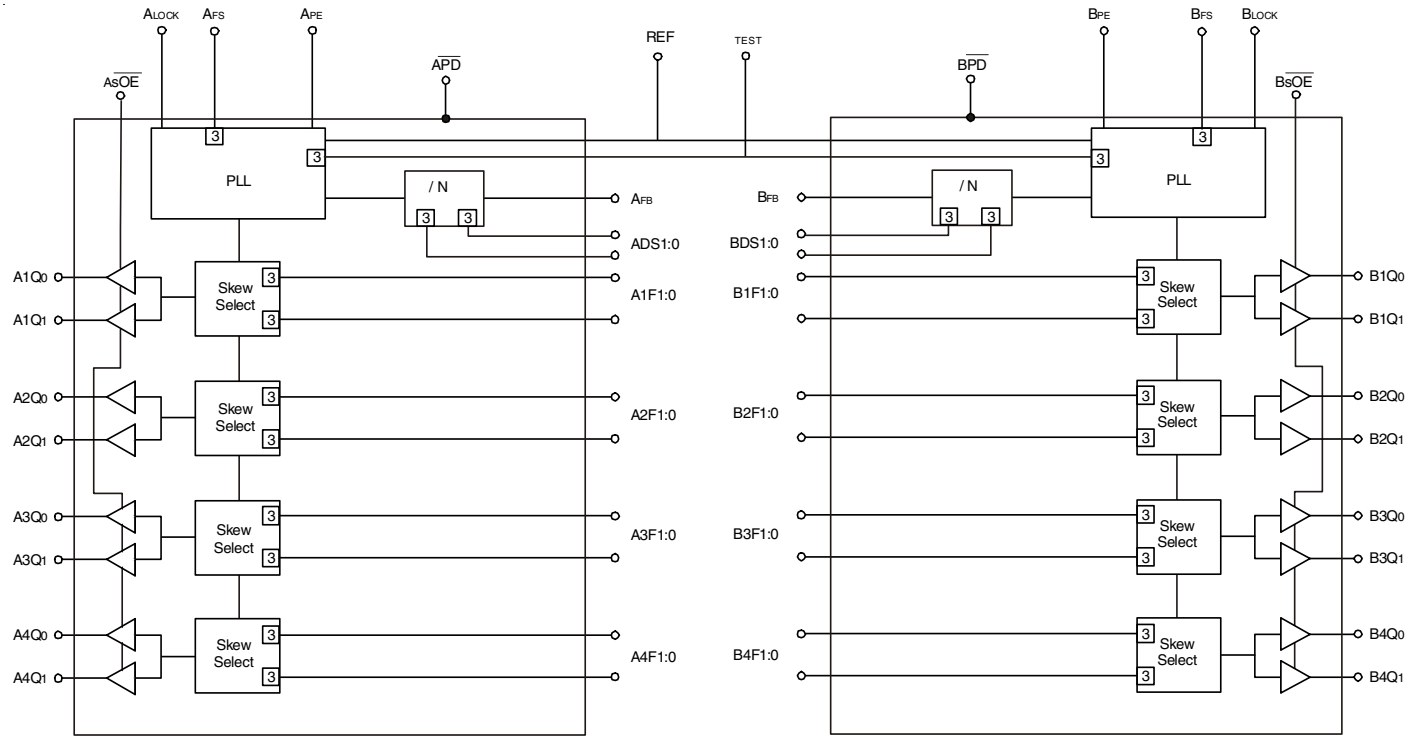
The IDT5T9955 is a high fanout 2.5V PLL based clock driver intended for high performance computing and data-communications applications. A key feature of the programmable skew is the ability of outputs to lead or lag the REF input signal. The IDT5T9955 has sixteen programmable skew outputs in eight banks of 2. The two separate PLLs allow the user to independently control A and B banks. Skew is controlled by 3-level input signals that may be hard-wired to appropriate high-mid-low levels.

The feedback input allows divide-by-functionality from 1 to 12 through the use of the xDS[1:0] inputs. This provides the user with frequency multiplication from 1 to 12 without using divided outputs for feedback.

When the $x\overline{sOE}$ pin is held low, all the xbank outputs are synchronously enabled. However, if $x\overline{sOE}$ is held high, all the xbank outputs except x2Q0 and x2Q1 are synchronously disabled. The xLOCK output is high when the xbank PLL has achieved phase lock.

Furthermore, when xPE is held high, all the outputs are synchronized with the positive edge of the REF clock input. When xPE is held low, all the outputs are synchronized with the negative edge of REF. The IDT5T9955 has LVTTL outputs with 12mA balanced drive outputs.

FUNCTIONAL BLOCK DIAGRAM

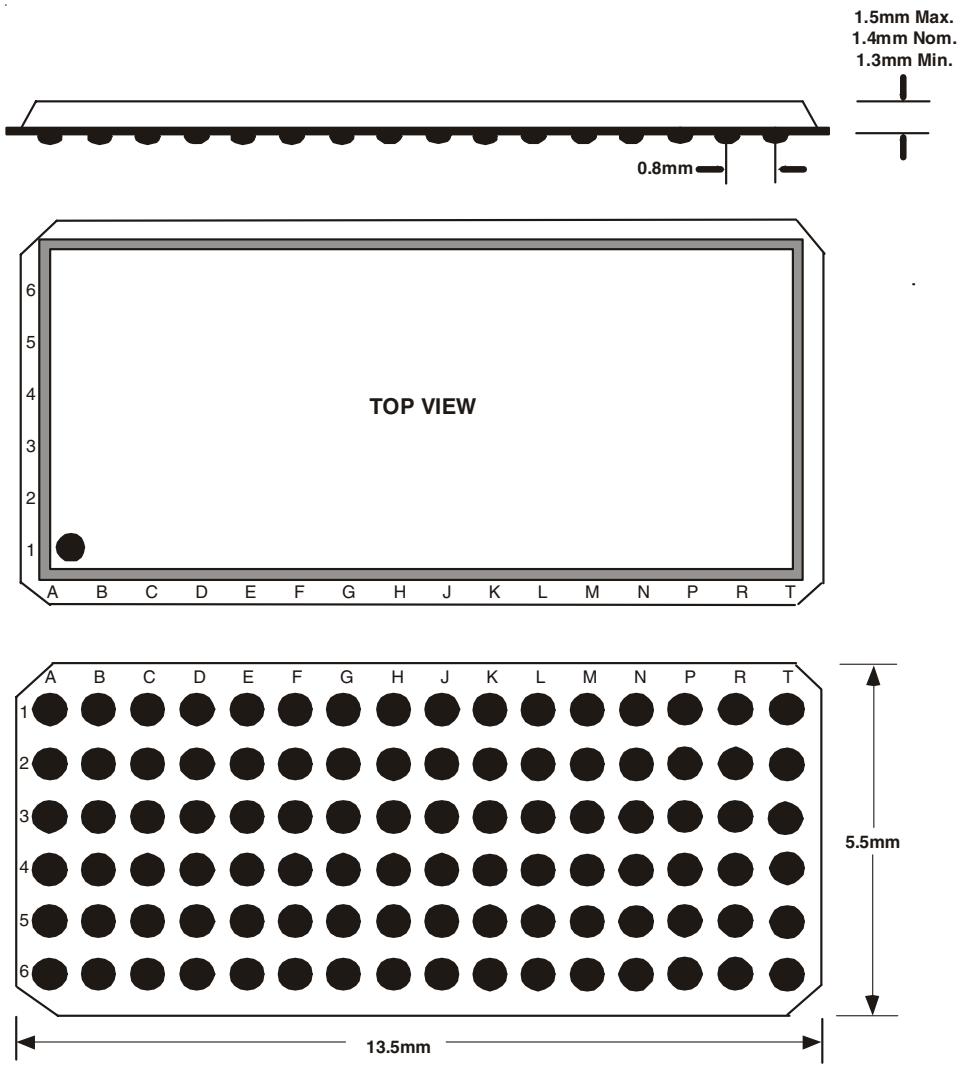


PIN CONFIGURATION

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
6	A3Q1	A4Q0	A4Q1	APE	$\overline{APD}$	A4F1	A3F1	AFS	B2F1	B1F1	BDS1	BLOCK	BVDDQ	B1Q0	B1Q1	B2Q0
5	A3Q0	AGND	AGND	AGND	AS$\overline{OE}$	A4F0	A3F0	AVDD	BGND	B2F0	B1F0	BDS0	BVDDQ	BGND	BGND	B2Q1
4	AGND	AGND	AGND	AVDDQ	AVDDQ	AVDDQ	AVDDQ	AVDDQ	TEST	BVDDQ	BVDDQ	BVDDQ	BVDDQ	BGND	BGND	BFB
3	AFB	AGND	AGND	AVDDQ	AVDDQ	AVDDQ	AVDDQ	REF	BVDDQ	BVDDQ	BVDDQ	BVDDQ	BVDDQ	BGND	BGND	BGND
2	A2Q1	AGND	AGND	AVDDQ	ADS0	A1F0	A2F0	AGND	BVDD	B3F0	B4F0	BS$\overline{OE}$	BGND	BGND	BGND	B3Q0
1	A2Q0	A1Q1	A1Q0	AVDDQ	ALOCK	ADS1	A1F1	A2F1	BFS	B3F1	B4F1	B$\overline{PD}$	BPE	B4Q1	B4Q0	B3Q1

FPBGA
TOP VIEW

96 BALL FPBGA PACKAGE ATTRIBUTES



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description		Max	Unit
V_{DDQ}, V_{DD}	Supply Voltage to Ground		–0.5 to +4.6	V
V_I	DC Input Voltage		–0.5 to V_{DD}+0.5	V
	REF Input Voltage		–0.5 to +4.6	V
	Maximum Power Dissipation	T_A = 85°C	1.1	W
		T_A = 55°C	1.9	
T_{STG}	Storage Temperature Range		–65 to +150	°C

NOTE:
1. Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Parameter	Description		Typ.	Max.	Unit
C_{IN}	Input Capacitance	REF	8	10	pF
		Others	5	7	

NOTE:
1. Capacitance applies to all inputs except TEST, xFS, xnF[1:0], and xDS[1:0].

PIN DESCRIPTION

Pin Name	Type	Description
REF	IN	Reference Clock Input
xFB	IN	Individual Feedback Inputs for A and B banks
TEST(1)	IN	When MID or HIGH, disables PLL for A and B banks (except for conditions of Note 1). REF goes to all outputs. Skew Selections (See Control Summary Table) remain in effect. Set LOW for normal operation.
$xs\overline{OE}$(1)	IN	Individual Synchronous Output Enable for A and B banks. When HIGH, it stops clock outputs (except x2Q_0 and x2Q_1) in a LOW state (for xPE = H) - x2Q_0 and x2Q_1 may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and $xs\overline{OE}$ is HIGH, the nF[1:0] pins act as output disable controls for individual banks when xnF[1:0] = LL. Set $xs\overline{OE}$ LOW for normal operation (has internal pull-down).
xPE	IN	Individual Selectable positive or negative edge control for A and B banks. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock (has internal pull-up).
xnF[1:0]	IN	3-level inputs for selecting 1 of 9 skew taps or frequency functions
xFS	IN	Selects appropriate oscillator circuit based on anticipated frequency range. (See Programmable Skew Range.) Individual control on A and B banks.
xnQ[1:0]	OUT	Eight banks of two outputs with programmable skew
xDS[1:0]	IN	3-level inputs for feedback divider selection for A and B banks
$x\overline{PD}$	IN	Power down control. Shuts off either A or B bank of the chip when LOW (has internal pull-up).
xLOCK	OUT	PLL lock indication signal for A and B banks. HIGH indicates lock. LOW indicates that the PLL is not locked and outputs may not be synchronized to the inputs. (For more information on application specific use of the LOCK pin, please see AN237.)
V_{DDQ}	PWR	Power supply for output buffers
V_{DD}	PWR	Power supply for phase locked loop, lock output, and other internal circuitry
GND	PWR	Ground

NOTE:
1. When TEST = MID and $xs\overline{OE}$ = HIGH, PLL remains active with xnF[1:0] = LL functioning as an output disable control for individual output banks. Skew selections remain in effect unless xnF[1:0] = LL.

PROGRAMMABLE SKEW

Output skew with respect to the REF input is adjustable to compensate for PCB trace delays, backplane propagation delays or to accommodate requirements for special timing relationships between clocked components. Skew is selectable as a multiple of a time unit (t_U) which ranges from 782ps to 1.5625ns (see Programmable Skew Range and Resolution Table). There are nine skew configurations available for each output pair. These configurations are chosen by the $xnF_{1:0}$ control pins. In order to minimize the number of control pins, 3-level inputs (HIGH-MID-LOW) are used, they are intended for but not restricted to hard-wiring. Undriven 3-level inputs default to the MID level. Where programmable skew is not a requirement, the control pins can be left open for the zero skew default setting. The Control Summary Table shows how to select specific skew taps by using the $xnF_{1:0}$ control pins.

EXTERNAL FEEDBACK

By providing two separate external feedbacks, the IDT5T9955 gives users flexibility with regard to skew adjustment. The xFB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

PROGRAMMABLE SKEW RANGE AND RESOLUTION TABLE

	xFS = LOW	xFS = MID	xFS = HIGH	Comments
Timing Unit Calculation (t_U)	1/(32 x F_{NOM})	1/(16 x F_{NOM})	1/(8 x F_{NOM})	
VCO Frequency Range (F_{NOM})(1,2)	24 to 40MHz	40 to 80MHz	80 to 160MHz	
Skew Adjustment Range(3) Max Adjustment:	±7.8125ns	±9.375ns	±9.375ns	ns
	±67.5°	±135°	±270°	Phase Degrees
	±18.75%	±37.5%	±75%	% of Cycle Time
Example 1, F_{NOM} = 25MHz	t_U = 1.25ns	—	—	
Example 2, F_{NOM} = 37.5MHz	t_U = 0.833ns	—	—	
Example 3, F_{NOM} = 50MHz	—	t_U = 1.25ns	—	
Example 4, F_{NOM} = 75MHz	—	t_U = 0.833ns	—	
Example 5, F_{NOM} = 100MHz	—	—	t_U = 1.25ns	
Example 6, F_{NOM} = 150MHz	—	—	t_U = 0.833ns	

NOTES:
1. The device may be operated outside recommended frequency ranges without damage, but functional operation is not guaranteed.
2. The level to be set on xFS is determined by the nominal operating frequency of the VCO and Time Unit Generator. The VCO frequency always appears at $x1Q_{1:0}$, $x2Q_{1:0}$, and the higher outputs when they are operated in their undivided modes. The frequency appearing at the REF and xFB inputs will be F_{NOM} when the output connected to xFB is undivided and $xDS[_{1:0}]$ = MM. The frequency of the REF and xFB inputs will be F_{NOM} /2 or F_{NOM} /4 when the part is configured for frequency multiplication by using a divided output as the xFB input and setting $xDS[_{1:0}]$ = MM. Using the $xDS[_{1:0}]$ inputs allows a different method for frequency multiplication (see Divide Selection Table).
3. Skew adjustment range assumes that a zero skew output is used for feedback. If a skewed xQ output is used for feedback, then adjustment range will be greater. For example if a $4t_U$ skewed output is used for feedback, all other outputs will be skewed $-4t_U$ in addition to whatever skew value is programmed for those outputs. 'Max adjustment' range applies to output pairs 3 and 4 where $\pm 6t_U$ skew adjustment is possible and at the lowest F_{NOM} value.

DIVIDE SELECTION TABLE

xDS[1:0]	xFB Divide-by-n	Permitted Output Divide-by-n connected to xFBIN(1)
LL	2	1 or 2
LM	3	1
LH	4	1, 2, or 4
ML	5	1 or 2
MM	1	1, 2, or 4
MH	6	1 or 2
HL	8	1 or 2
HM	10	1
HH	12	1

NOTE:
1. Permissible output division ratios connected to xFB. The frequency of the REF input will be FNOM/N when the part is configured for frequency multiplication by using an undivided output for xFB and setting xDS[1:0] to N (N = 1-6, 8, 10, 12).

CONTROL SUMMARY TABLE FOR FEEDBACK SIGNALS

xnF1:0	Skew (Pair #1, #2)	Skew (Pair #3)	Skew (Pair #4)
LL(1)	–4tU	Divide by 2	Divide by 2
LM	–3tU	–6tU	–6tU
LH	–2tU	–4tU	–4tU
ML	–1tU	–2tU	–2tU
MM	Zero Skew	Zero Skew	Zero Skew
MH	1tU	2tU	2tU
HL	2tU	4tU	4tU
HM	3tU	6tU	6tU
HH	4tU	Divide by 4	Inverted(2)

NOTES:
1. LL disables outputs if TEST = MID and $\overline{xsOE}$ = HIGH.
2. When pair #4 is set to HH (inverted), $\overline{xsOE}$ disables pair #4 HIGH when xPE = HIGH, $\overline{xsOE}$ disables pair #4 LOW when xPE = LOW.

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
VDD/VDDQ	Power Supply Voltage	2.3	2.5	2.7	V
TA	Ambient Operating Temperature	-40	+25	+85	°C

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]		Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH (REF, xFB Inputs Only)		2	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW (REF, xFB Inputs Only)		—	0.7	V
V_{IHH}	Input HIGH Voltage[2]	3-Level Inputs Only		V_{DD}—0.4	—	V
V_{IMM}	Input MID Voltage[2]	3-Level Inputs Only		V_{DD}/2—0.2	V_{DD}/2+0.2	V
V_{ILL}	Input LOW Voltage[2]	3-Level Inputs Only		—	0.4	V
I_{IN}	Input Leakage Current (REF, xFB Inputs Only)	V_{IN} = V_{DD} or GND V_{DD} = Max.		—5	+5	µA
I_3	3-Level Input DC Current (TEST, xFS, xnF[1:0], xDS[1:0])	V_{IN} = V_{DD}	HIGH Level	—	+400	µA
		V_{IN} = V_{DD}/2	MID Level	—100	+100	
		V_{IN} = GND	LOW Level	—400	—	
I_{PU}	Input Pull-Up Current (xPE, x$\overline{PD}$)	V_{DD} = Max., V_{IN} = GND		—25	—	µA
I_{PD}	Input Pull-Down Current (x$\overline{sOE}$)	V_{DD} = Max., V_{IN} = V_{DD}		—	+100	µA
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = —2mA (xLOCK Output)		2	—	V
		V_{DDQ} = Min., I_{OH} = —12mA (xnQ[1:0] Outputs)		2	—	
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 2mA (xLOCK Output)		—	0.4	V
		V_{DDQ} = Min., I_{OL} = 12mA (xnQ[1:0] Outputs)		—	0.4	

NOTES:
1. All conditions apply to A and B banks.
2. These inputs are normally wired to V_{DD}, GND, or unconnected. Internal termination resistors bias unconnected inputs to V_{DD}/2. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Typ.[2]	Max.	Unit
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max., TEST = MID, REF = LOW, xPE = LOW, x$\overline{sOE}$ = LOW, x$\overline{PD}$ = HIGH FS = MID, All outputs unloaded		40	60	mA
I_{DDPD}	Power Down Current	V_{DD} = Max., x$\overline{PD}$ = LOW, x$\overline{sOE}$ = LOW xPE = HIGH, TEST = HIGH, xFS = HIGH xnF[1:0] = HH, xDS[1:0] = HH		—	50	µA
ΔI_{DD}	Power Supply Current per Input HIGH (REF and xFB inputs only)	V_{IN} = 2.3V, V_{DD} = Max., x$\overline{PD}$ = LOW TEST = HIGH		1	60	µA
I_{DDD}	Dynamic Power Supply Current per Output	xFS = L		190	290	µA/MHz
		xFS = M		150	230	
		xFS = H		130	200	
I_{TOT}	Total Power Supply Current	xFS = L	F_{VCO} = 40MHz, C_L = 0pF	98	—	mA
		xFS = M	F_{VCO} = 80MHz, C_L = 0pF	132	—	
		xFS = H	F_{VCO} = 160MHz, C_L = 0pF	206	—	

NOTES:
1. Measurements are for divide-by-1 outputs, xnF[1:0] = MM, and xDS[1:0] = MM. All conditions apply to A and B banks.
2. For nominal voltage and temperature.

INPUT TIMING REQUIREMENTS

Symbol	Description[1]		Min.	Max.	Unit
t_R, t_F	Maximum input rise and fall times, 0.7V to 1.7V		—	10	ns/V
t_{PWC}	Input clock pulse, HIGH or LOW		2	—	ns
D_H	Input duty cycle		10	90	%
F_{REF}	Reference clock input frequency	xFS = LOW	2	40	MHz
		xFS = MID	3.33	80	
		xFS = HIGH	6.67	160	

NOTE:

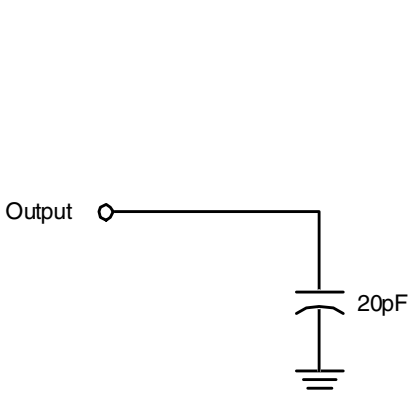
1. Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

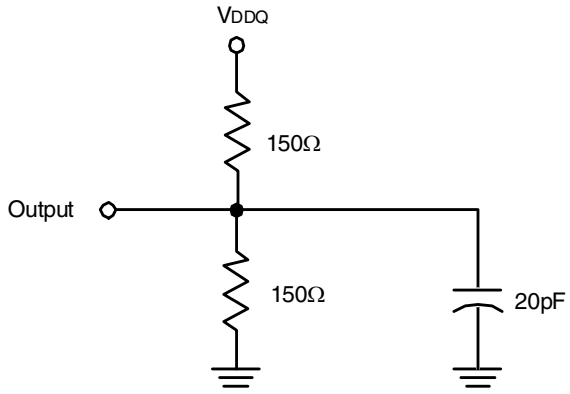
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{NOM}	VCO Frequency Range	See Programmable Skew Range and Resolution Table			
t_{RPWH}	REF Pulse Width HIGH[1]	2	—	—	ns
t_{RPWL}	REF Pulse Width LOW[1]	2	—	—	ns
t_U	Programmable Skew Time Unit	See Control Summary Table			
t_{SKEWPR}	Zero Output Matched-Pair Skew (xnQ_0, xnQ_1)[2,3]	—	50	185	ps
t_{SKEW0}	Zero Output Skew (All Outputs)[4]	—	0.1	0.25	ns
t_{SKEWB}	Bank Skew[5]	—	0.1	0.35	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs)[6]	—	0.1	0.25	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[6]	—	0.2	0.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[6]	—	0.15	0.5	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted)[2]	—	0.3	0.9	ns
t_{DEV}	Device-to-Device Skew[2,7]	—	—	0.75	ns
$t_{(\phi)1\text{-}3}$	Static Phase Offset (xFS = L, M, H) (FB Divide-by-n = 1, 2, 3)[8]	—0.3	—	0.3	ns
$t_{(\phi)H}$	Static Phase Offset (xFS = H)[7]	—0.5	—	0.5	ns
$t_{(\phi)M}$	Static Phase Offset (xFS = M)[7]	—0.7	—	0.7	ns
$t_{(\phi)L1\text{-}6}$	Static Phase Offset (xFS = L) (xFB Divide-by-n = 1, 2, 3, 4, 5, 6)[8]	—0.7	—	0.7	ns
$t_{(\phi)L8\text{-}12}$	Static Phase Offset (xFS = L) (xFB Divide-by-n = 8, 10, 12)[8]	—1	—	1	ns
t_{ODCV}	Output Duty Cycle Variation from 50%	—1	—	1	ns
t_{PWH}	Output HIGH Time Deviation from 50%[9]	—	—	1.5	ns
t_{PWL}	Output LOW Time Deviation from 50%[10]	—	—	2	ns
t_{ORISE}	Output Rise Time	0.15	0.7	1.5	ns
t_{OFALL}	Output Fall Time	0.15	0.7	1.5	ns
t_{LOCK}	PLL Lock Time[11,12]	—	—	0.5	ms
t_{CCJH}	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, xFS = H, xFB divide-by-n=1,2)	—	—	100	ps
t_{CCJHA}	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, xFS = H, xFB divide-by-n=any)	—	—	150	
t_{CCJM}	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, xFS = M)	—	—	200	
t_{CCJL}	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, xFS = L, F_{REF} > 3MHz)	—	—	200	
t_{CCJLA}	Cycle-to-Cycle Output Jitter (peak-to-peak) (divide by 1 output frequency, xFS = L, F_{REF} < 3MHz)	—	—	300	

NOTES:
1. Refer to Input Timing Requirements table for more detail.
2. Skew is the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with the specified load.
3. t_{SKEWPR} is the skew between a pair of outputs (xnQ0 and xnQ1) when all sixteen outputs are selected for $0t_U$.
4. $t_{SK(0)}$ is the skew between outputs when they are selected for $0t_U$.
5. t_{SKEWB} is the skew between outputs (xnQ0 and xnQ1) from A and B banks when they are selected for $0t_U$.
6. There are 3 classes of outputs: Nominal (multiple of t_U delay), Inverted (x4Q0 and x4Q1 only with x4F0 = x4F1 = HIGH), and Divided (x3Q1:0 and x4Q1:0 only in Divide-by-2 or Divide-by-4 mode). Test condition: xnF0:1=MM is set on unused outputs.
7. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{DDQ}, V_{DD}, ambient temperature, air flow, etc.)
8. $t\phi$ is measured with REF input rise and fall times (from 0.7V to 1.7V) of 0.5ns. Measured from 1.25V on REF to 1.25V on xFB.
9. Measured at 1.7V.
10. Measured at 0.7V.
11. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{DD}/V_{DDQ} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or xFB until t_{PD} is within specified limits.
12. Lock detector may be unreliable for input frequencies less than approximately 4MHz, or for input signals which contain significant jitter.

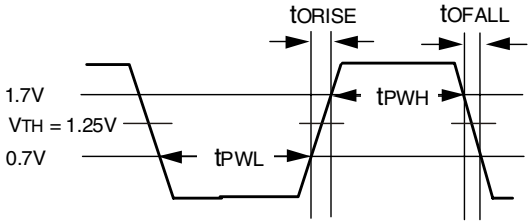
AC TEST LOADS AND WAVEFORMS



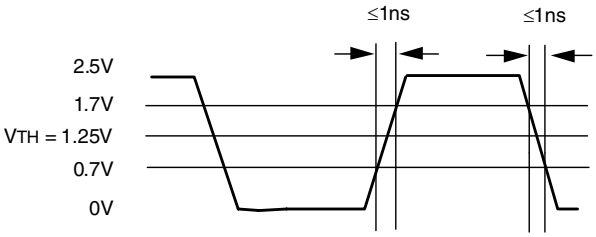
For LOCK output



For all other outputs

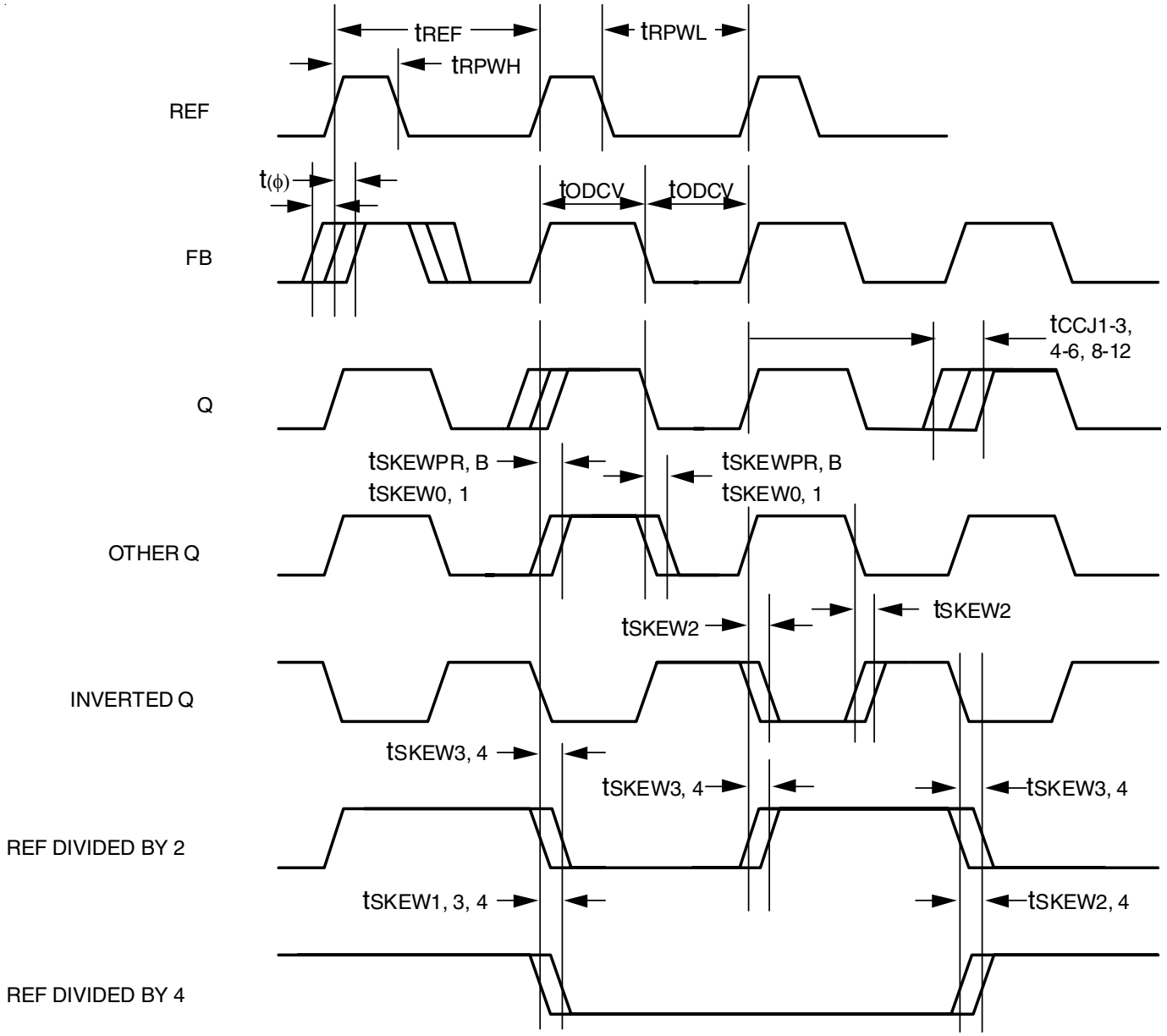


2.5V Output Waveform



LVTTL Input Test Waveform

AC TIMING DIAGRAM



NOTES:

PE: The AC Timing Diagram applies to PE=V_{DD}. For PE=GND, the negative edge of FB aligns with the negative edge of REF, divided outputs change on the negative edge of REF, and the positive edges of the divide-by-2 and the divide-by-4 signals align.

Skew: The time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 20pF and terminated with 75Ω to $V_{DDQ}/2$.

t_{SKEWPR}: The skew between a pair of outputs (xnQ_0 and xnQ_1) when all eight outputs are selected for $0t_U$.

t_{SKEWB}: The skew between outputs (xnQ_0 and xnQ_1) from A and B banks when they are selected for $0t_U$.

t_{SKEW0}: The skew between outputs when they are selected for $0t_U$.

t_{DEV}: The output-to-output skew between any two devices operating under the same conditions (V_{DDQ}, V_{DD}, ambient temperature, air flow, etc.)

t_{ODCV}: The deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.

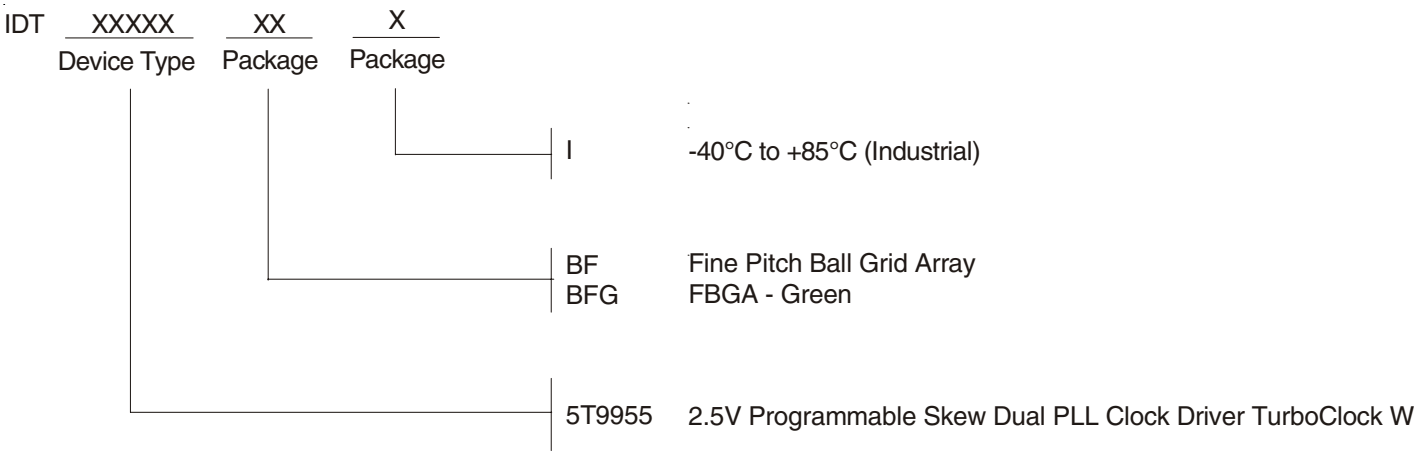
t_{PWH} is measured at 1.7V.

t_{PWL} is measured at 0.7V.

t_{ORISE} and t_{OFALL} are measured between 0.7V and 1.7V.

t_{LOCK}: The time that is required before synchronization is achieved. This specification is valid only after V_{DD}/V_{DDQ} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

ORDERING INFORMATION



CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
clockhelp@idt.com