19-3884; Rev 2; 2/07

±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

General Description

The MAX3394E/MAX3395E/MAX3396E bidirectional level translators provide level shifting required for data transfer in a multivoltage system. Internal slew-rate enhancement circuitry features 10mA current-sink and 15mA current-source drivers to isolate capacitive loads from lower current drivers. In open-drain systems, slew-rate enhancement enables fast data rates with larger pullup resistors and increased bus load capacitance. Externally applied voltages, V_{CC} and V_L, set the logic-high levels for the device. A logic-low signal on one I/O side of the device appears as a logic-low signal on the opposite I/O side, and vice-versa. Each I/O line is pulled up to V_{CC} or V_L by an internal pullup resistor, allowing the devices to be driven by either push-pull or open-drain drivers.

The MAX3394E/MAX3395E/MAX3396E feature a tri-state output mode, thermal-shutdown protection, and ±15kV Human Body Model (HBM) ESD protection on the V_{CC} side for greater protection in applications that route signals externally.

The MAX3394E/MAX3395E/MAX3396E accept V_{CC} voltages from +1.65V to +5.5V, and V_L voltages from +1.2V to V_{CC}, making them ideal for data transfer between low voltage ASIC/PLDs and higher voltage systems. The MAX3394E/MAX3395E/MAX3396E operate at a guaranteed data rate of 6Mbps with push-pull drivers and 1Mbps with open-drain drivers.

The MAX3394E is a dual-level translator available in 9-bump UCSP™ and 8-pin 3mm x 3mm TDFN packages. The MAX3395E is a quad-level translator available in 12-bump UCSP, and 12-pin 4mm x 4mm TQFN packages. The MAX3396E is an octal-level translator available in 20-bump UCSP and 20-pin 5mm x 5mm TQFN packages. The MAX3394E/MAX3395E/MAX3396E operate over the extended -40°C to +85°C temperature range.

Applications

Multivoltage Bidirectional Level Translation

SPI™, MICROWIRE™, and I²C Level Translation

Open-Drain Rise-Time Speed-Up

High-Speed Bus Fan-Out Expansion

Cell Phones

Telecom, Networking, Servers, RAID/SAN

MICROWIRE is a trademark of National Semiconductor Corp.

SPI is a trademark of Motorola, Inc.

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- ♦ **±15kV ESD Protection on I/O $V_{CC\_}$ Lines**
- ♦ **Bidirectional Level Translation Without Direction Pin**
- ♦ **I/O $V_{L\_}$ and I/O $V_{CC\_}$ 10mA Sink-/15mA Source-Current Capability**
- ♦ **Slew-Rate Enhancement Circuitry Supports Larger Capacitive Loads or Larger External Pullup Resistors**
- ♦ **6Mbps Push-Pull/1Mbps Open-Drain Guaranteed Data Rate**
- ♦ **Wide Supply-Voltage Range: Operation Down to +1.2V on V_L and +1.65V on V_{CC}**
- ♦ **Low Supply Current in Tri-State Output Mode (3µA typ)**
- ♦ **Low Quiescent Current**
- ♦ **Thermal-Shutdown Protection**
- ♦ **UCSP, TDFN, and TQFN Packages**

Ordering Information

PART	PIN-PACKAGE	PKG CODE
MAX3394EETA+T	8 TDFN-EP**	T833-1
MAX3394EEBL+T	9 UCSP	B9-5
MAX3395EETC+	12 TQFN-EP**	T1244-4
MAX3395EEBC+T	12 UCSP	B12-1
MAX3396EEBP+T*	20 UCSP	B20-1
MAX3396EETP+*	20 TQFN-EP**	T2055-4

Note: *All devices specified over the -40°C to +85°C operating range.*

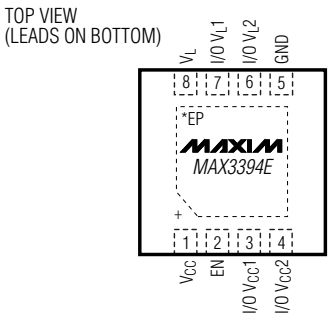
+Denotes lead(Pb)-free/RoHS-compliant package.

**Future product—contact factory for availability.*

***EP = Exposed paddle.*

Selector Guide appears at end of data sheet.

Pin Configurations



TDFN

*CONNECT EXPOSED PAD TO GROUND

Pin Configurations continued at end of data sheet.

±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC} ..... -0.3V to +6V
V_L ..... -0.3V to +6V
I/O $V_{CC\_}$ ..... -0.3V to V_{CC} + 0.3V
I/O $V_{L\_}$ ..... -0.3V to V_L + 0.3V
EN ..... -0.3V to +6V
Short-Circuit Duration I/O $V_{L\_}$, I/O $V_{CC\_}$ to GND ..... Continuous
Maximum Continuous Current ..... ±50mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 18.2mW/°C above +70°C) 1455mW
9-Bump UCSP (derate 4.7mW/°C above +70°C) 379mW
12-Pin TQFN (derate 16.9mW/°C above +70°C) 1349mW
12-Bump UCSP (derate 6.5mW/°C above +70°C) 519mW
20-Pin TQFN (derate 20.8mW/°C above +70°C) 1667mW
20-Bump UCSP (derate 10.0mW/°C above +70°C) 800mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature .....+150°C
Bump Temperature (soldering) ..... +235°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}; C_{IOVL} ≤ 15pF, C_{IOVCC} ≤ 15pF; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
V_L Supply Range	V_L			1.2		V_{CC}	V
V_{CC} Supply Range	V_{CC}			1.65		5.50	V
Supply Current from V_{CC}	I_{CC}	I/O lines internally pulled up	MAX3394E			150	µA
			MAX3395E			300	
			MAX3396E			600	
Supply Current from V_L	I_L	I/O lines internally pulled up	MAX3394E			30	µA
			MAX3395E			30	
			MAX3396E			30	
V_{CC} Tri-State Supply Current	I_{CC-3}	EN = GND, T_A = +25°C			3	6	µA
V_L Tri-State Supply Current	I_{L-3}	EN = GND, T_A = +25°C			0.7	2	µA
LOGIC I/O							
I/O $V_{L\_}$ Input-Voltage High Threshold	V_{IHL}					0.7 x V_L	V
I/O $V_{L\_}$ Input-Voltage Low Threshold	V_{ILL}			0.3 x V_L			V
I/O $V_{L\_}$ Internal Pullup DC Resistance	R_L	EN = V_{CC} or V_L		5	10	20	kΩ
I/O $V_{L\_}$ Source Current During Low-to-High Transition	I_{IHL}	V_L = +1.2V			15		mA
I/O $V_{L\_}$ Sink Current During High-to-Low Transition	I_{ILL}	V_{CC} = +1.65V			10		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}; C_{IOVL} ≤ 15pF, C_{IOVCC} ≤ 15pF; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{L\_}$ Low-to-High Transition Threshold	V_{L-TH}	V_{CC} = +3.3V, V_L = +1.8V	0.3 x V_L	0.5 x V_L		V
I/O $V_{L\_}$ Output-Voltage Low	V_{OLL}	I/O $V_{L\_}$ sink current = 5mA, V_{ILC} = 0V			0.25	V
		I/O $V_{L\_}$ sink current = 10mA, V_{ILC} ≤ 0.4V or 0.2 x V_L			V_{ILC} + 0.4V	
I/O $V_{L\_}$ Tri-State Output Leakage Current		EN = GND, T_A = +25°C	-1		+1	µA
I/O $V_{CC\_}$ Input-Voltage High Threshold	V_{IHC}	(Note 2)			0.7 x V_{CC}	V
I/O $V_{CC\_}$ Input-Voltage Low Threshold	V_{ILC}	(Note 2)	0.3 x V_{CC}			V
I/O $V_{CC\_}$ Internal Pullup DC Resistance	R_{CC}	EN = V_{CC} or V_L	5	10	20	kΩ
I/O $V_{CC\_}$ Source Current During Low-to-High Transition	I_{IHCC}	V_{CC} = +1.65V		15		mA
I/O $V_{CC\_}$ Sink Current During High-to-Low Transition	I_{ILCC}	V_{CC} = +1.65V		10		mA
I/O $V_{CC\_}$ Low-to-High Transition Threshold	V_{CC-TH}	V_{CC} = +3.3V, V_L = +1.8V	0.3 x V_{CC}	0.5 x V_{CC}		V
I/O $V_{CC\_}$ Output-Voltage Low	V_{OLC}	I/O $V_{CC\_}$ sink current = 5mA, V_{ILL} = 0V			0.25	V
		I/O $V_{CC\_}$ sink current = 10mA, V_{ILL} ≤ 0.4V or 0.2 x V_L			V_{ILL} + 0.4V	
I/O $V_{CC\_}$ Tri-State Output Leakage Current		EN = GND, T_A = +25°C	-1		+1	µA
EN Input-Voltage High Threshold	V_{IHE}				0.7 x V_L	V
EN Input-Voltage Low Threshold	V_{ILE}		0.3 x V_L			V
EN Pin Input Leakage Current		T_A = +25°C	-1		+1	µA
ESD PROTECTION						
I/O $V_{CC\_}$ ESD Protection		C_{VCC} = 1µF, Human Body Model		±15		kV

TIMING CHARACTERISTICS

(V_{CC} = +1.65V to +5.5V, V_L = +1.2V to V_{CC}; $C_{IOVL} \le 15pF$, $C_{IOVCC} \le 15pF$; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$ Rise Time	t_{RVCC}	Push-pull driver, Figure 1			50	ns
		Open-drain driver, internal pullup, Figure 2			500	
I/O $V_{CC\_}$ Fall Time	t_{FVCC}	Push-pull driver, Figure 1			50	ns
		Open-drain driver, internal pullup, Figure 2			50	
I/O $V_{L\_}$ Rise Time	t_{RVL}	Push-pull driver, Figure 3			50	ns
		Open-drain driver, internal pullup, Figure 4			500	
I/O $V_{L\_}$ Fall Time	t_{FVL}	Push-pull driver, Figure 3			50	ns
		Open-drain driver, internal pullup, Figure 4			50	
Propagation Delay	$t_{I/OVL-VCC}$	Push-pull driver, Figure 1			50	ns
		Open-drain driver, internal pullup, Figure 2			600	
	$t_{I/OVCC-VL}$	Push-pull driver, Figure 3			50	
		Open-drain driver, internal pullup, Figure 4			600	
Propagation Delay After EN	t_{EN}	Push-pull or open-drain driver, Figure 5			5	µs
Channel-to-Channel Skew	t_{SKEW}	Push-pull driver			5	ns
		Open-drain driver, internal pullup			100	
Maximum Data Rate		Push-pull driver, Figures 1, 3			6	Mbps
		Open-drain driver, internal pullup, Figures 2, 4			1	

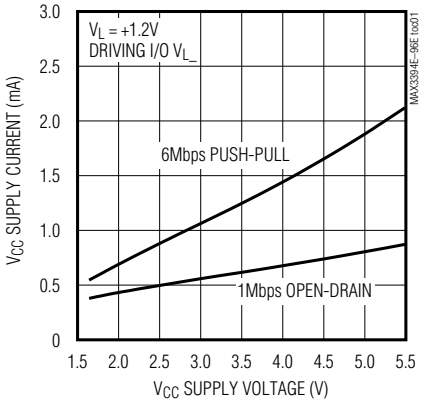
Note 1: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 2: During a low-to-high transition, the threshold at which the I/O changes state is the lower of V_{ILL} and V_{ILC} since the two sides are internally connected by an internal switch while the device is in the logic-low state.

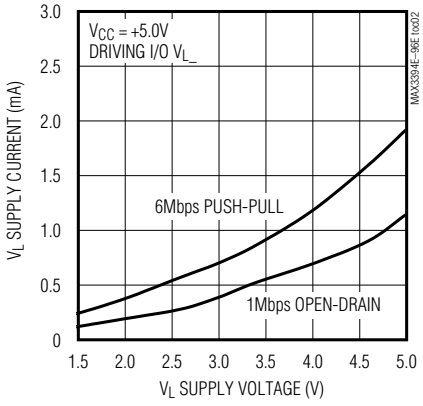
Typical Operating Characteristics

(V_{CC} = +2.5V, V_L = +1.8V, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

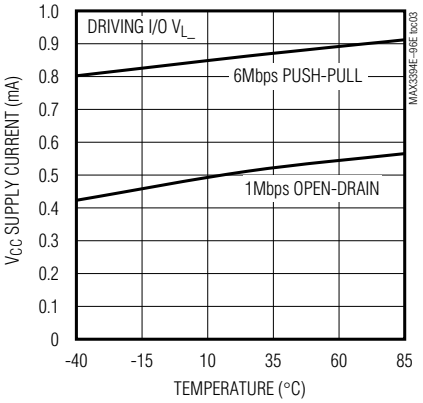
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE



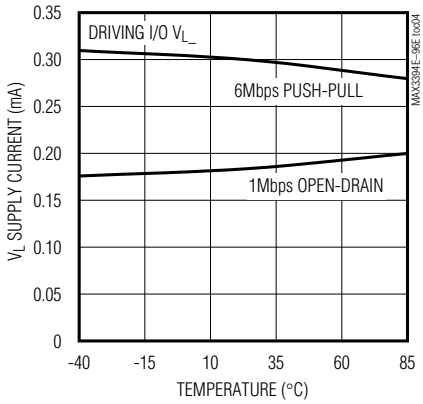
V_L SUPPLY CURRENT vs. SUPPLY VOLTAGE



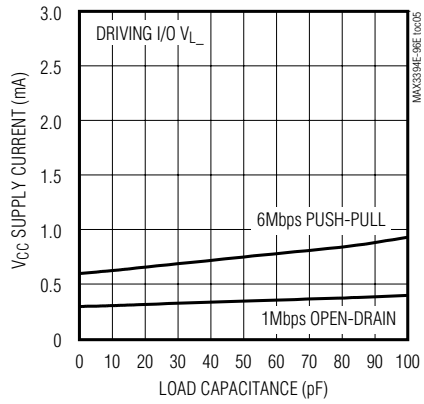
V_{CC} SUPPLY CURRENT vs. TEMPERATURE



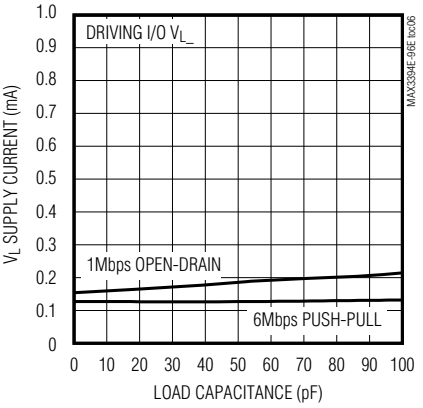
V_L SUPPLY CURRENT vs. TEMPERATURE



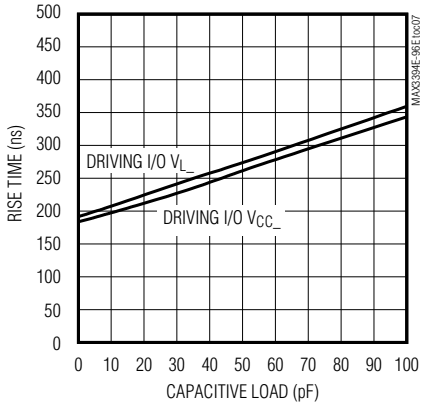
V_{CC} SUPPLY CURRENT vs. LOAD CAPACITANCE



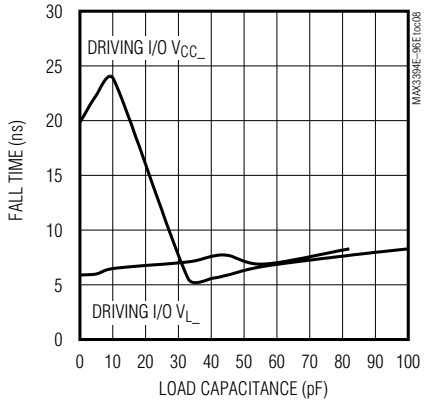
V_L SUPPLY CURRENT vs. LOAD CAPACITANCE



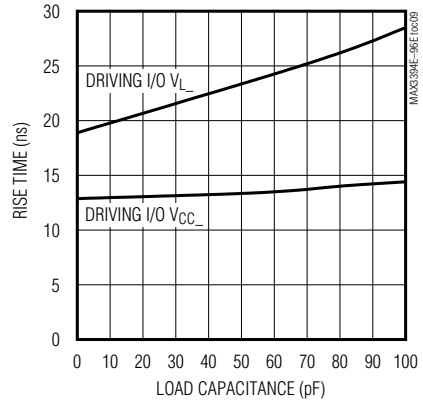
OPEN-DRAIN RISE TIME vs. LOAD CAPACITANCE



OPEN-DRAIN FALL TIME vs. LOAD CAPACITANCE



PUSH-PULL RISE TIME vs. LOAD CAPACITANCE

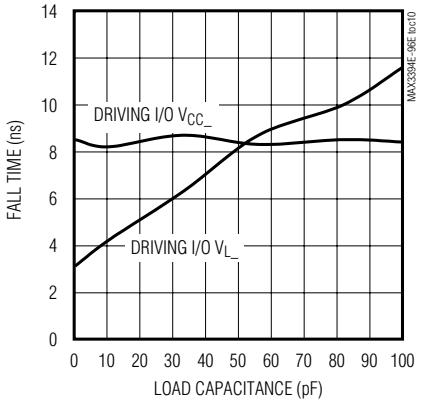


±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/ Octal-Level Translators with Speed-Up Circuitry

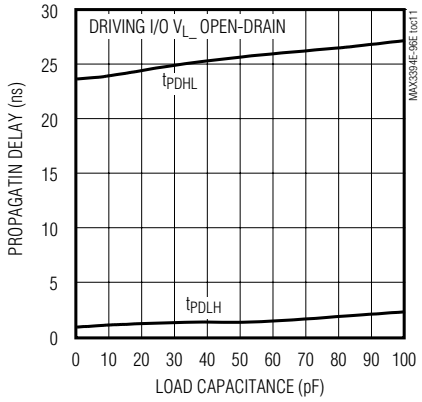
Typical Operating Characteristics (continued)

(V_{CC} = +2.5V, V_L = +1.8V, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

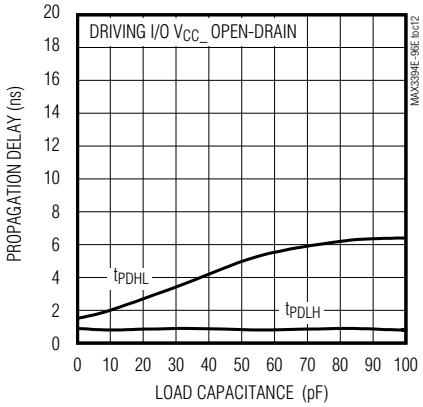
PUSH-PULL FALL TIME vs. LOAD CAPACITANCE



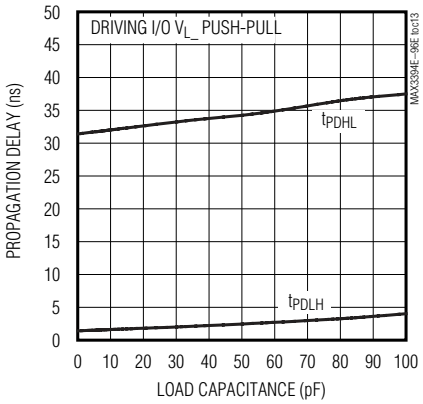
PROPAGATION DELAY vs. LOAD CAPACITANCE



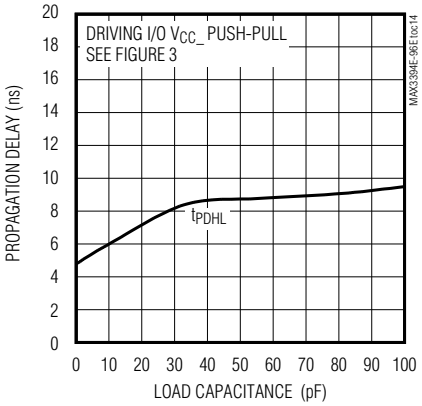
PROPAGATION DELAY vs. LOAD CAPACITANCE



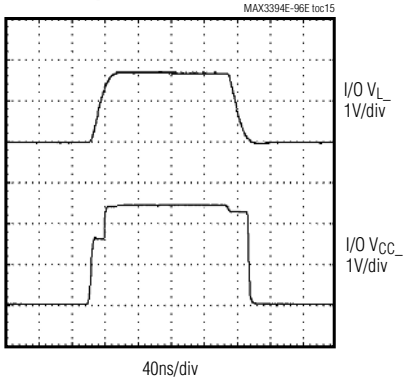
PROPAGATION DELAY vs. LOAD CAPACITANCE



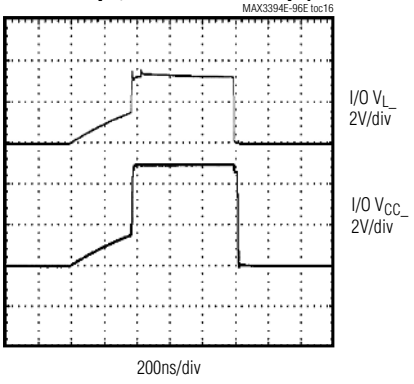
PROPAGATION DELAY vs. LOAD CAPACITANCE



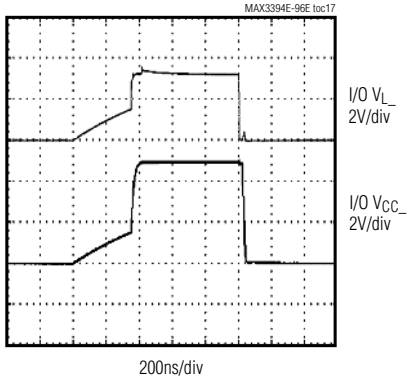
(DRIVING I/O $V_{L\_}$, V_{CC} = +2.5V, V_L = +1.8V, C_L = 15pF, DATA RATE = 6Mbps)



(DRIVING I/O $V_{L\_}$, V_{CC} = +5.0V, V_L = +3.3V, C_L = 100pF, DATA RATE = 1Mbps)



(DRIVING I/O $V_{L\_}$, V_{CC} = +5.0V, V_L = +3.3V, C_L = 400pF, EXTERNAL 4.7kΩ PULLUPS, DATA RATE = 1Mbps)



Pin Description

PIN						NAME	FUNCTION
MAX3394E		MAX3395E		MAX3396E			
TDFN	UCSP	TQFN	UCSP	TQFN	UCSP		
1	A1	11	B1	14	D3	V_{CC}	V_{CC} Supply Voltage +1.65V ≤ V_{CC} ≤ +5.5V. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor and a 1µF or greater ceramic capacitor as close to the device as possible.
2	B1	6	B3	4	A4	EN	Enable Input. Drive EN logic high for normal operation. Drive EN logic low to force all I/O lines to a high-impedance state and disconnect internal pullup resistors.
3	A2	10	C1	18	C1	I/O V_{CC}1	I/O 1 Referred to V_{CC}
4	A3	9	C2	16	D1	I/O V_{CC}2	I/O 2 Referred to V_{CC}
5	B3	5	B4	13	D4	GND	Ground
6	C3	2	A2	20	A1	I/O V_L2	I/O 2 Referred to V_L
7	C2	1	A1	19	B1	I/O V_L1	I/O 1 Referred to V_L
8	C1	12	B2	3	A3	V_L	Logic Supply Voltage +1.2V ≤ V_L ≤ V_{CC}. Bypass V_L to GND with a 0.1µF or greater ceramic capacitor as close to the device as possible.
—	—	3	A3	1	B2	I/O V_L3	I/O 3 Referred to V_L
—	—	4	A4	2	A2	I/O V_L4	I/O 4 Referred to V_L
—	—	7	C4	15	D2	I/O V_{CC}4	I/O 4 Referred to V_{CC}
—	—	8	C3	17	C2	I/O V_{CC}3	I/O 3 Referred to V_{CC}
—	—	—	—	12	C3	I/O V_{CC}5	I/O 5 Referred to V_{CC}
—	—	—	—	11	D5	I/O V_{CC}6	I/O 6 Referred to V_{CC}
—	—	—	—	10	C4	I/O V_{CC}7	I/O 7 Referred to V_{CC}
—	—	—	—	9	C5	I/O V_{CC}8	I/O 8 Referred to V_{CC}
—	—	—	—	5	B3	I/O V_L5	I/O 5 Referred to V_L
—	—	—	—	6	A5	I/O V_L6	I/O 6 Referred to V_L
—	—	—	—	7	B4	I/O V_L7	I/O 7 Referred to V_L
—	—	—	—	8	B5	I/O V_L8	I/O 8 Referred to V_L
EP	—	EP	—	EP	—	EP	Exposed Pad. Connect exposed pad to GND.

Detailed Description

The MAX3394E/MAX3395E/MAX3396E bidirectional level translators provide level shifting required for data transfer in a multivoltage system. Internal slew-rate enhancement circuitry features 10mA current-sink and 15mA current-source drivers to isolate capacitive loads from lower current drivers. In open-drain systems, slew-rate enhancement enables fast data rates with larger pullup resistors and increased bus load capacitance. Externally applied voltages, V_{CC} and V_L, set the logic-high levels for the device. A logic-low signal on one I/O side of the device appears as a logic-low signal on the opposite I/O side and vice-versa. Each I/O line is pulled up to V_{CC} or V_L by an internal pullup resistor, allowing the devices to be driven by either push-pull or open-drain drivers.

±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

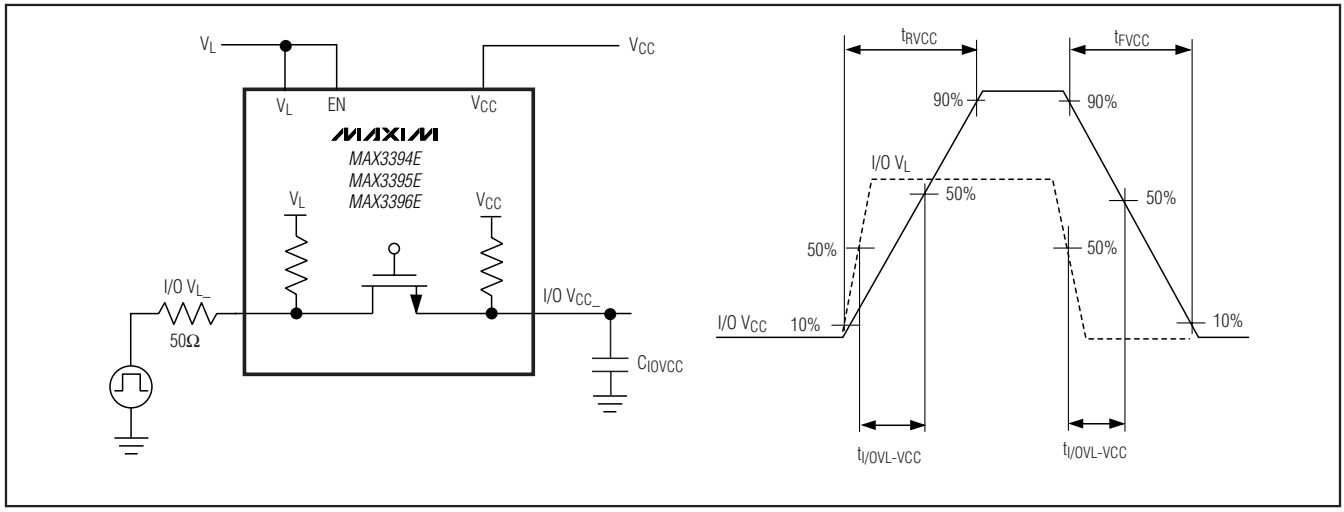


Figure 1. Push-Pull Driving I/O $V_{L\_}$ Test Circuit and Timing

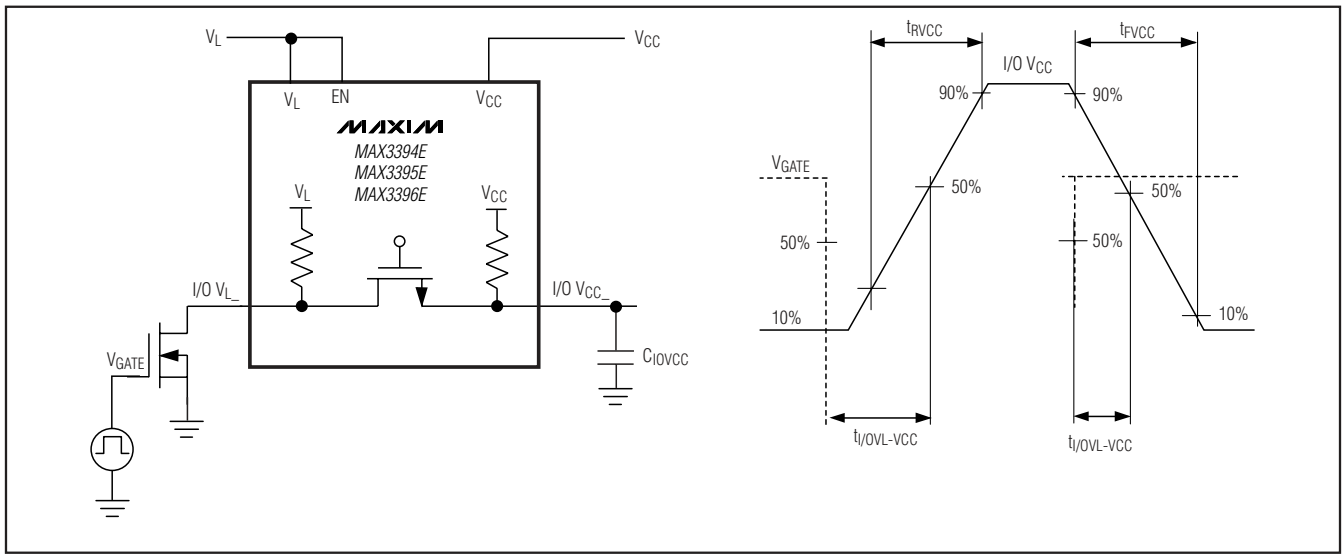


Figure 2. Open-Drain Driving I/O $V_{L\_}$ Test Circuit and Timing

The MAX3394E/MAX3395E/MAX3396E feature a tri-state output mode, thermal-shutdown protection, and ±15kV Human Body Model (HBM) ESD protection on the V_{CC} side for greater protection in applications that route signals externally.

The MAX3394E/MAX3395E/MAX3396E accept V_{CC} voltages from +1.65V to +5.5V, and V_L voltages from +1.2V to V_{CC}, making them ideal for data transfer between low-voltage ASIC/PLDs and higher voltage systems. The MAX3394E/MAX3395E/MAX3396E operate at a guaranteed data rate of 6Mbps with push-pull drivers and 1Mbps with open-drain drivers.

Level Translation

The MAX3394E/MAX3395E/MAX3396E utilize a transmission gate architecture to provide bidirectional level translation between I/O $V_{L\_}$ and I/O $V_{CC\_}$. The transmission gate architecture is comprised of a pass-FET, gate-control logic, and slew-rate enhancement circuitry. When both I/O $V_{L\_}$ and I/O $V_{CC\_}$ are logic high, the gate-control logic disables the pass-FET, providing

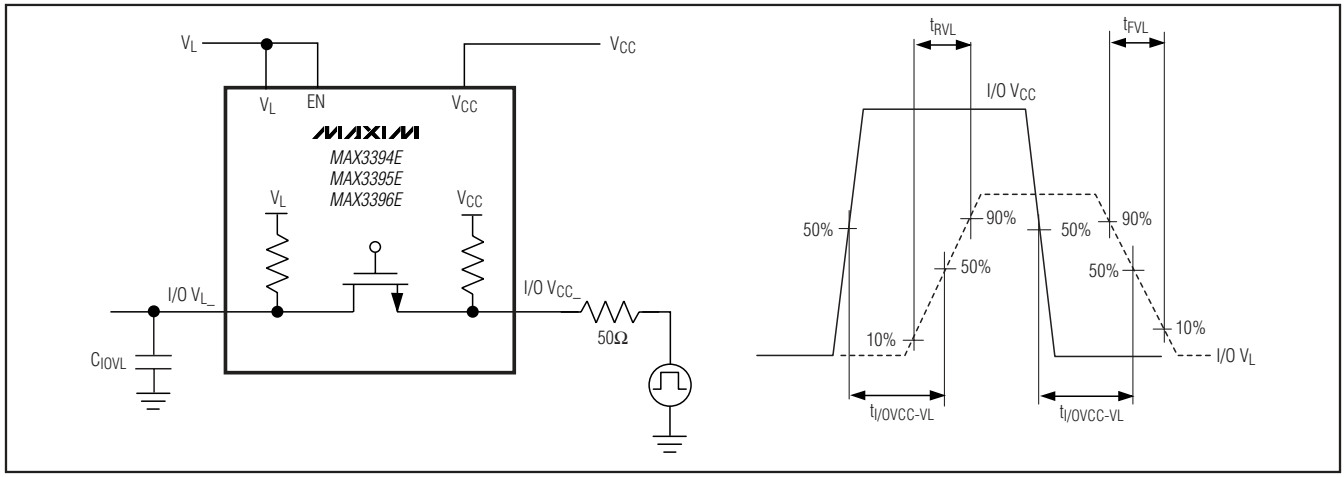


Figure 3. Push-Pull Driving I/O $V_{CC\_}$ Test Circuit and Timing

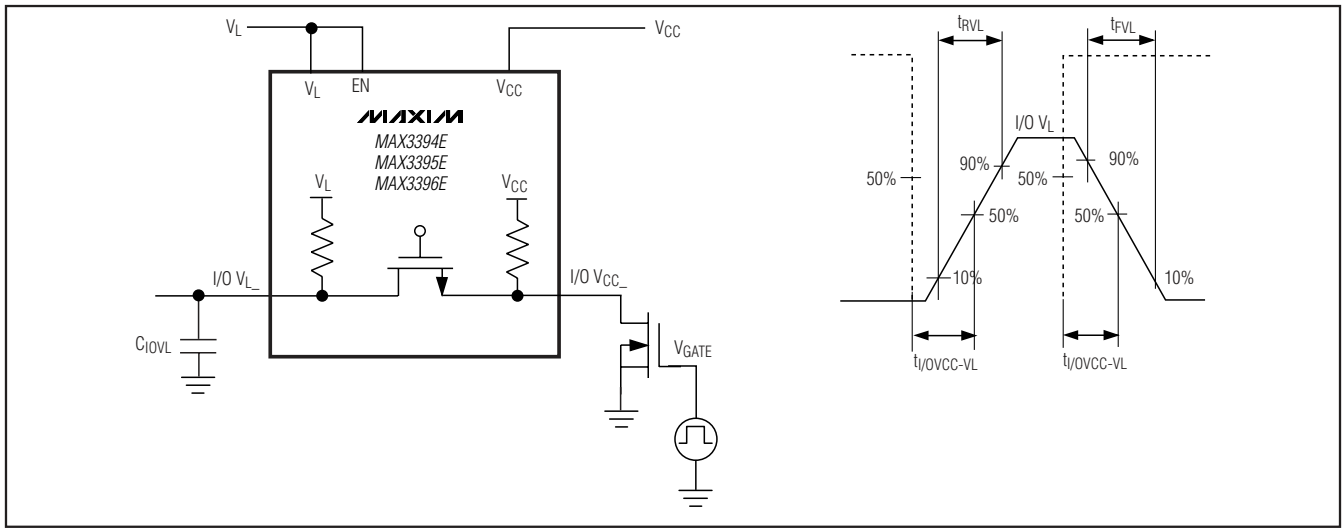


Figure 4. Open-Drain Driving I/O $V_{CC\_}$ Test Circuit and Timing

capacitive isolation between I/O lines. When one or both I/O lines are at a logic-low level, the gate-control logic turns the pass-FET on. When the pass-FET is active, I/O $V_{L\_}$ and I/O $V_{CC\_}$ are connected, allowing the logic-low signal to be expressed simultaneously on both I/O lines.

The MAX3394E/MAX3395E/MAX3396E have internal 10kΩ (typ) pullup resistors from I/O $V_{L\_}$ and I/O $V_{CC\_}$ to the respective supply voltages, allowing operation with open-drain drivers. Internal slew-rate enhancement circuitry accelerates logic-state transitions, maintaining a fast data rate with a higher bus load capacitance. Additionally, the 10mA current sink drivers permit the use of smaller external pullup resistors.

Internal Slew-Rate Enhancement

Internal slew-rate enhancement circuitry accelerates logic-state changes by turning on MOSFETs M_{P1} and M_{P2} during low-to-high logic transitions, and MOSFETs M_{N3} and M_{N4} during high-to-low logic transitions (see the *Functional Diagram*). During logic-state changes, speed-up MOSFETS are triggered by I/O line voltage thresholds. MOSFETS M_{N3} and M_{N4} sink 10mA during high-to-low logic transitions. M_{P1} and M_{P2} source 15mA during low-to-high logic transitions. Slew-rate enhancement allows a fast data rate despite large capacitive bus loads, and permits larger external pullup resistors.

±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

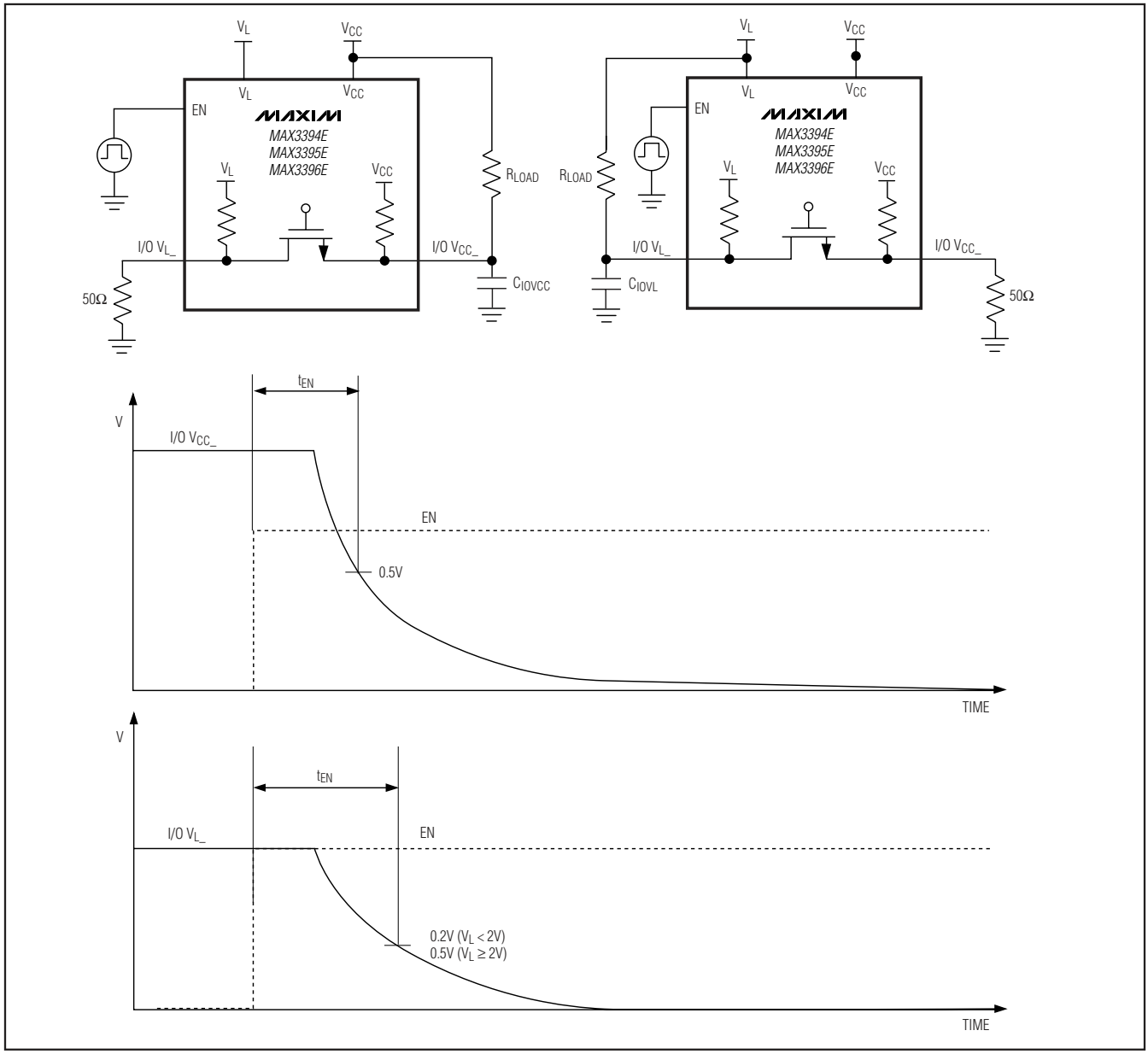


Figure 5. Enable Test Circuit and Timing

Power-Supply Sequencing

The MAX3394E/MAX3395E/MAX3396E require two supply voltages. For proper operation, ensure that +1.65V ≤ V_{CC} ≤ +5.5V, and +1.2V ≤ V_L ≤ V_{CC}. There are no restrictions on power-supply sequencing. During power-up or power-down, the MAX3394E/MAX3395E/MAX3396E can withstand either the V_L or the V_{CC} supply floating while the other supply is applied. The device will not latch up in this state.

Tri-State Output Mode

Connect EN to V_L or V_{CC} for normal operation. Drive EN low to force the MAX3394E/MAX3395E/MAX3396E to a tri-state output mode. In tri-state output mode, all I/O lines are driven to a high-impedance state, and the pass-FET is disabled to prevent current flow between I/O lines. Tri-state output mode disables the internal pullup resistors on I/O V_L_ and I/O V_{CC}_, and reduces supply current to 3µA typ (V_{CC}) and 0.7µA typ (V_L).

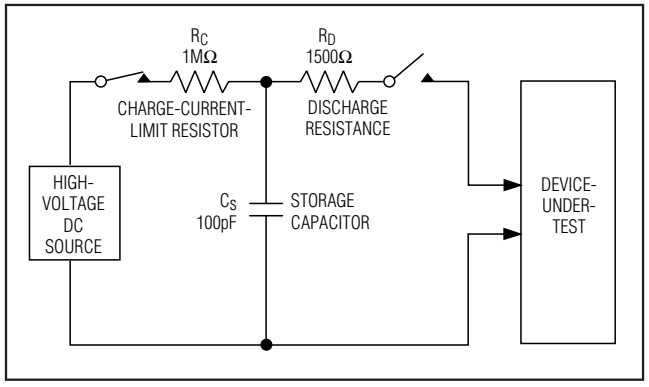


Figure 6a. Human Body ESD Test Model

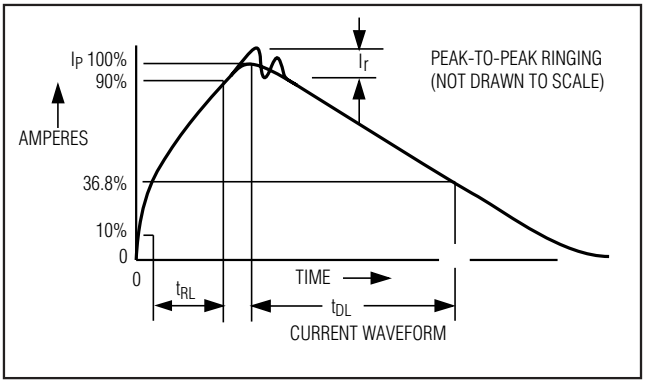


Figure 6b. HBM Discharge Current Waveform

The high-impedance state of the I/O lines during tri-state output mode facilitates use in multidrop networks. In tri-state output mode, do not exceed (V_L + 0.3V) on I/O $V_{L\_}$ or (V_{CC} + 0.3V) on I/O $V_{CC\_}$.

Thermal-Shutdown Protection

The MAX3394E/MAX3395E/MAX3396E are protected from thermal damage resulting from short-circuit faults. In the event of a short-circuit fault, when the junction temperature (T_J) reaches +125°C, a thermal sensor forces the device into the tri-state output mode. When T_J drops below +115°C, normal operation resumes.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against ESD encountered during handling and assembly. The I/O $V_{CC\_}$ lines are further protected by advanced ESD structures to guard these pins from damage caused by ESD of up to ±15kV. Protection structures prevent damage caused by ESD events in normal operation, tri-state output mode, and when the device is unpowered. After arresting an ESD event, MAX3394E/MAX3395E/MAX3396E continue to function without latching up, whereas competing devices can enter a latched-up state and must be power cycled to restore functionality.

Several ESD testing standards exist for gauging the robustness of ESD structures. The ESD protection of the MAX3394E/MAX3395E/MAX3396E is characterized for the human body model (HBM). Figure 6a shows the model used to simulate an ESD event resulting from contact with the human body. The model consists of a 100pF storage capacitor that is charged to a high voltage then discharged through a 1.5kΩ resistor. Figure 6b shows the current waveform when the storage capacitor is discharged into a low impedance.

To ensure full ±15kV ESD protection, bypass V_{CC} to ground with a 0.1µF ceramic capacitor and an additional 1µF ceramic capacitor as close to the device as possible.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report documenting test setup, methodology, and results.

Applications Information

Power-Supply Decoupling

Bypass V_L and V_{CC} to ground with 0.1µF ceramic capacitors. To ensure full ±15kV ESD protection, bypass V_{CC} to ground with an additional 1µF or greater ceramic capacitor. Place all capacitors as close to the device as possible.

Open-Drain Mode vs. Push-Pull Mode

The MAX3394E/MAX3395E/MAX3396E are compatible with push-pull (active) and open-drain drivers. For push-pull operation, maximum data rate is guaranteed to 6Mbps. For open-drain applications, the MAX3394E/MAX3395E/MAX3396E include internal pullup resistors and slew-rate enhancement circuitry, providing a maximum data rate of 1Mbps. External pullup resistors can be added to increase data rate when the bus is loaded by high capacitance. (See the *Use of External Pullup Resistors* section.)

Serial-Interface Level Translation

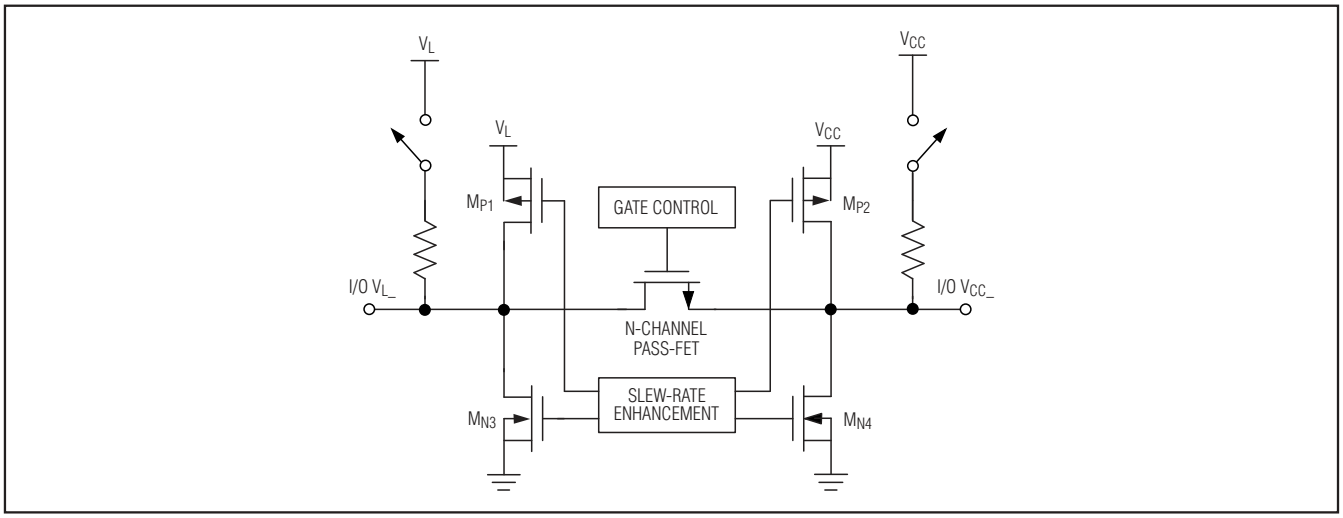
The MAX3395E provides level translation on four I/O lines, making it an ideal device for multivoltage I²C, MICROWIRE, and SPI serial interfaces.

Use of External Pullup Resistors

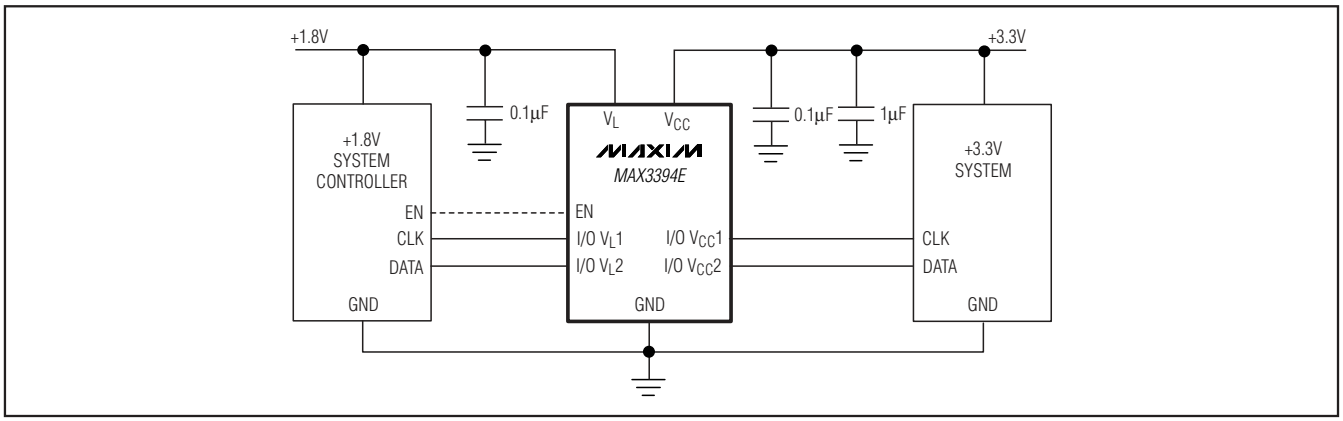
The MAX3394E/MAX3395E/MAX3396E include internal 10kΩ pullup resistors. During a low-to-high logic transition, the internal pullup resistors charge the bus capac-

±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

Functional Diagram



Typical Operating Circuit



itance with a characteristic RC charging waveform. When the low-to-high transition threshold ($V_{CC\text{-}TH}$ or $V_{L\text{-}TH}$) is reached, the rise time accelerators switch on, sourcing 15mA to fully charge the bus capacitance. External pullup resistors reduce the time needed to reach the low-to-high transition threshold, thereby increasing the data rate. In the logic-low state however, external pullup resistors increase the DC current through the internal pass-FET, increasing the output voltage of the device.

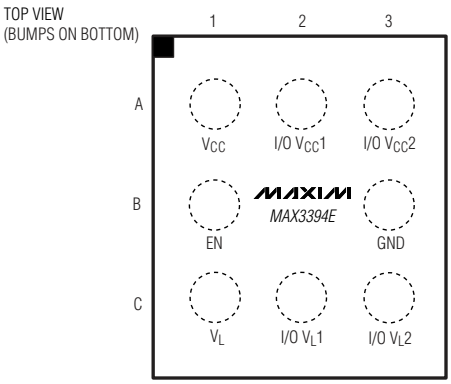
Smart-Card Interface

The MAX3395E provides level translation for Class A, B, and C smart cards. When supply voltage V_{CC} is interrupted due to the disconnection of a smart card, the device does not latch up. Normal operation resumes upon restoration of the V_{CC} supply voltage. The MAX3395E provides bidirectional level translation on four I/O lines, making it well suited for buffering and translating 4-wire serial interfaces.

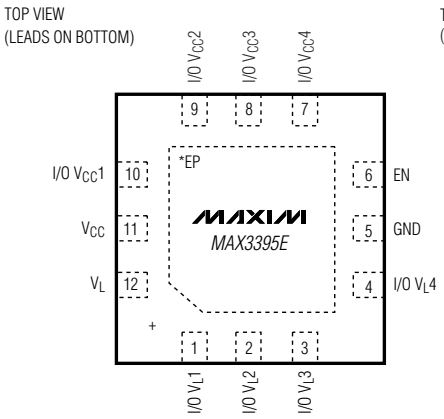
UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profiles, as well as the latest information on reliability testing results, go to Maxim's web site at **www.maxim-ic.com/ucsp** to find the Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications*.

Pin Configurations (continued)

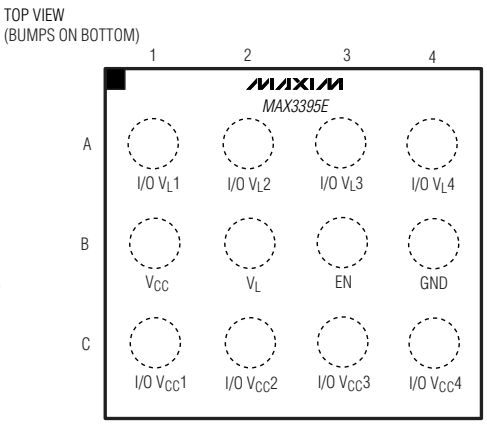


UCSP

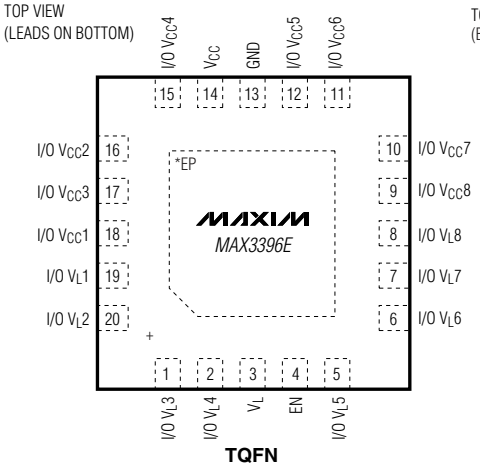


TQFN

*CONNECT EXPOSED PAD TO GROUND

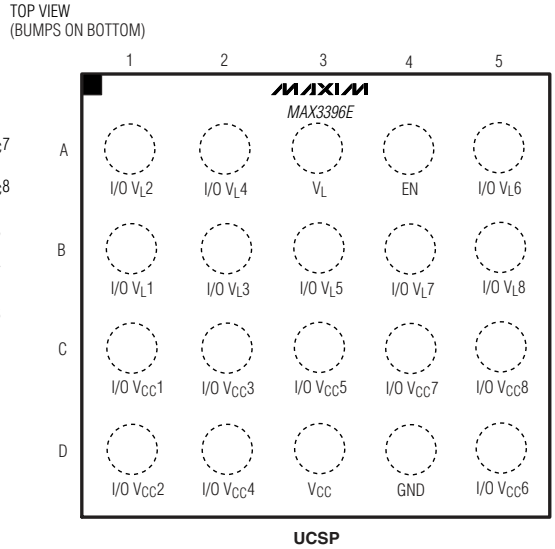


UCSP



TQFN

*CONNECT EXPOSED PAD TO GROUND



UCSP

±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

Selector Guide

PART	NUMBER OF TRANSLATORS	TOP MARK
MAX3394EETA+T	2	APE
MAX3394EEBL+T	2	AEZ
MAX3395EETC+	4	AAFZ
MAX3395EEBC+T	4	ACO
MAX3396EEBP+T	8	—
MAX3396EETP+	8	—

Note: *All devices specified over the -40°C to +85°C operating range.*

+Denotes lead(Pb)-free/RoHS-compliant package.

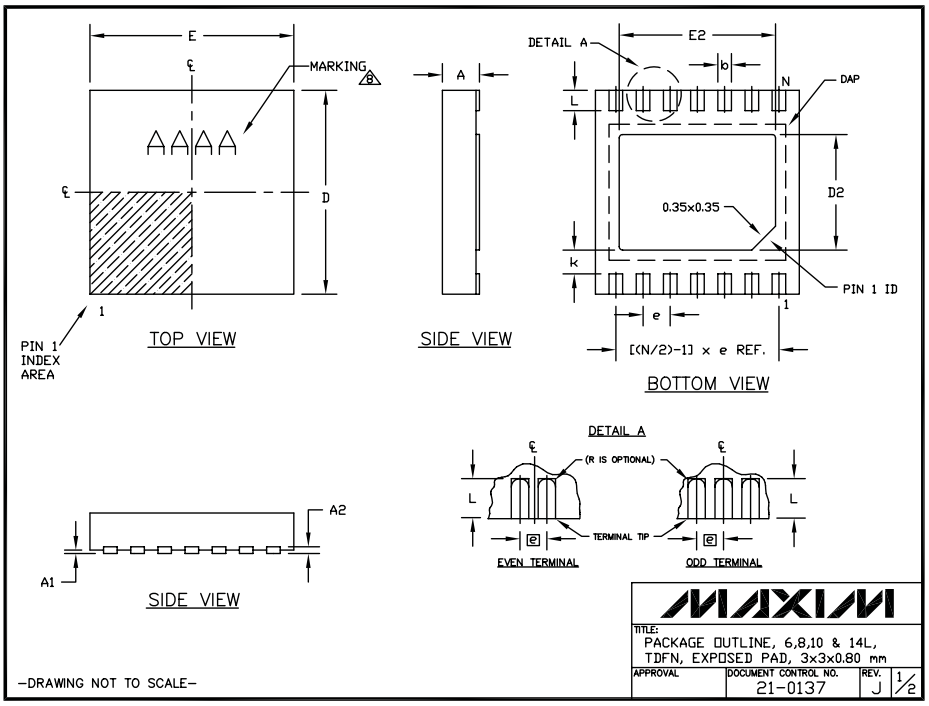
Chip Information

PROCESS: BiCMOS

CONNECT EXPOSED PAD TO GND.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033MK-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF
T1433-3F	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

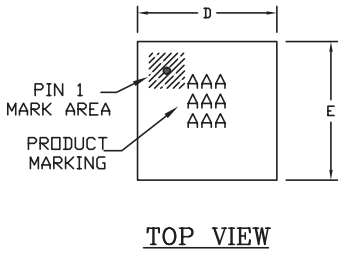
MAXIM
TITLE:
PACKAGE OUTLINE, 6,8,10 & 14L,
TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0137
REV.
J
2/2
–DRAWING NOT TO SCALE–

±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

9LUCSP, 3x3.EPS

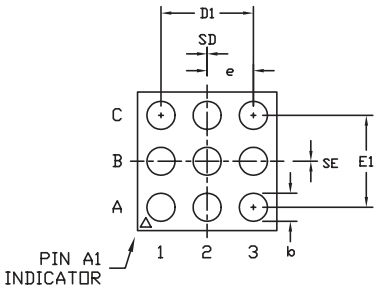


TOP VIEW

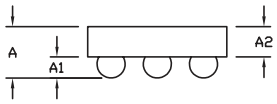
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.52±0.05	1.52±0.05	A2, B1, B2, B3, C2
B9-8	1.98±0.05	1.75±0.05	B1, B2, B3

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

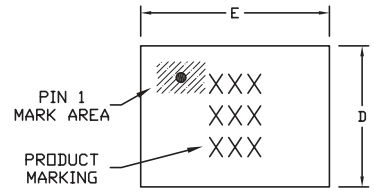
TITLE: PACKAGE OUTLINE, 3x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0093	L	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

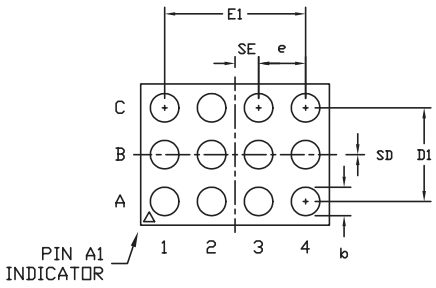
12L, UCSP 4x3.EPS



TOP VIEW

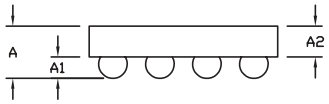
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 4x3 UCSP

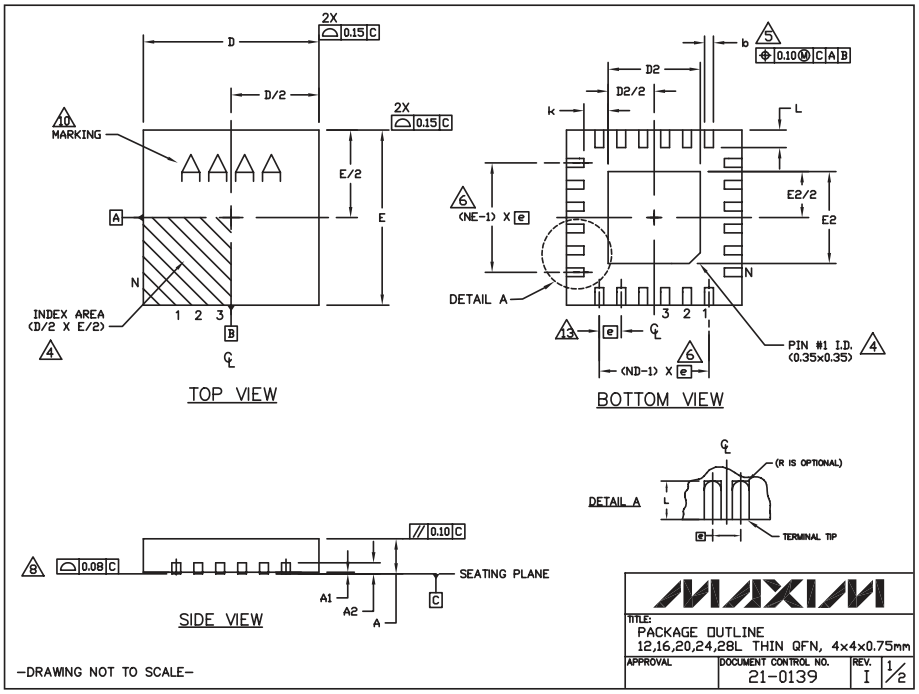
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0104	F	1/1

±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



–DRAWING NOT TO SCALE–

TITLE: PACKAGE OUTLINE 12,16,20,24,28L THIN QFN, 4x4x0.75mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0139	REV. I	1/2

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

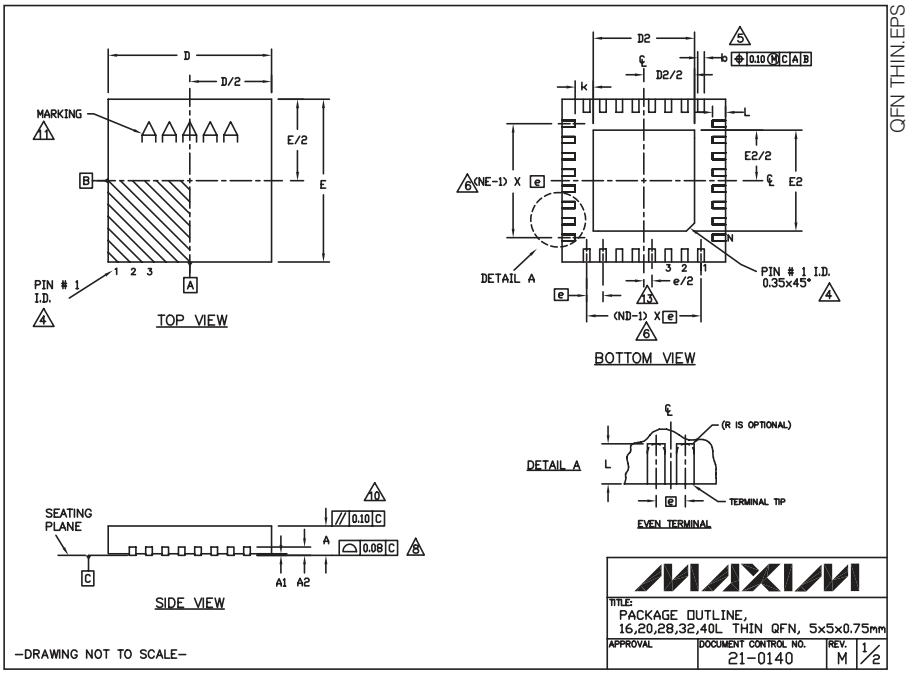
–DRAWING NOT TO SCALE–

TITLE: PACKAGE OUTLINE 12,16,20,24,28L THIN QFN, 4x4x0.75mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0139	REV. I	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



–DRAWING NOT TO SCALE–

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.75mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0140	REV. M	1/2

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655-4	2.19	2.29	2.39	2.19	2.29	2.39
T165N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055N-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

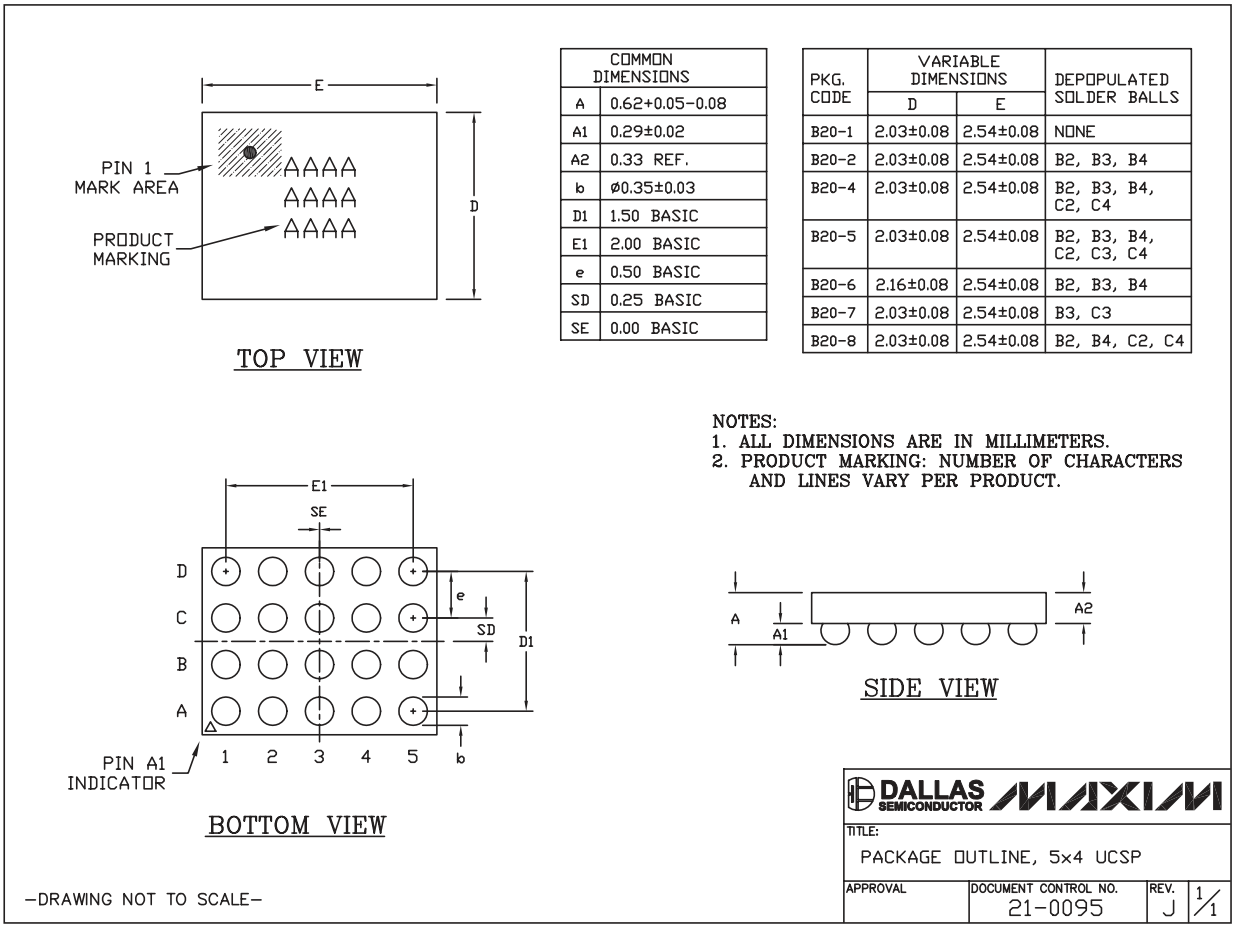
–DRAWING NOT TO SCALE–

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.75mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0140	REV. M	2/2

±15kV ESD-Protected, High-Drive Current, Dual-/Quad-/Octal-Level Translators with Speed-Up Circuitry

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.50 BASIC
E1	2.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B20-1	2.03±0.08	2.54±0.08	NONE
B20-2	2.03±0.08	2.54±0.08	B2, B3, B4
B20-4	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C4
B20-5	2.03±0.08	2.54±0.08	B2, B3, B4, C2, C3, C4
B20-6	2.16±0.08	2.54±0.08	B2, B3, B4
B20-7	2.03±0.08	2.54±0.08	B3, C3
B20-8	2.03±0.08	2.54±0.08	B2, B4, C2, C4

Revision History

Pages changed at Rev 2: 1–4, 9, 11, 12, 14, 20