

# FAN6210

## Primary-Side Synchronous Rectifier (SR) Trigger Controller for Dual Forward Converter

### Features

- Primary-Side Trigger Controller for Dual Forward Converters with Synchronous Rectifier (SR)
- Specialized SR Controller for Dual Forward Converter
- Programmable Turn-on Delay Time for the Powering SR (RDLY Pin)
- Winding Voltage Detection for Precision Control at Light-Load Condition (DET Pin)
- Green-Mode Operation to Improve Light-Load Efficiency
- Differential Mode Control Signal with Better Noise Immunity
- V<sub>DD</sub> Over-Voltage Protection (OVP)

### Applications


- Personal Computer (PC) Power Supply
- Entry-Level Server Power Supply

### Description

FAN6210 is a primary-side SR trigger Integrated Circuit (IC) specially designed for the synchronous rectifier (SR) in dual forward converters employing FAN6206. FAN6210 provides drive signal for the primary-side power switches by using an output signal from PWM controller. FAN6210 can be combined with any PWM controller that can drive a dual-forward converter. To obtain optimal timing for the SR drive signals, transformer winding voltage is also monitored. To improve light-load efficiency, green mode operation is employed, which disables the SR turn-on trigger signal, minimizing gate drive power consumption at light load.

FAN6210 is available in 8-pin SOP package.

### Ordering Information

Part Number	Operating Temperature Range	 Eco Status	Package	Packing Method
FAN6210MY	-40°C to +105°C	Green	8-Pin Small Outline Package (SOP)	Tape & Reel

 For Fairchild's definition of Eco Status, please visit: [http://www.fairchildsemi.com/company/green/rohs\\_green.html](http://www.fairchildsemi.com/company/green/rohs_green.html).

## Application Diagram

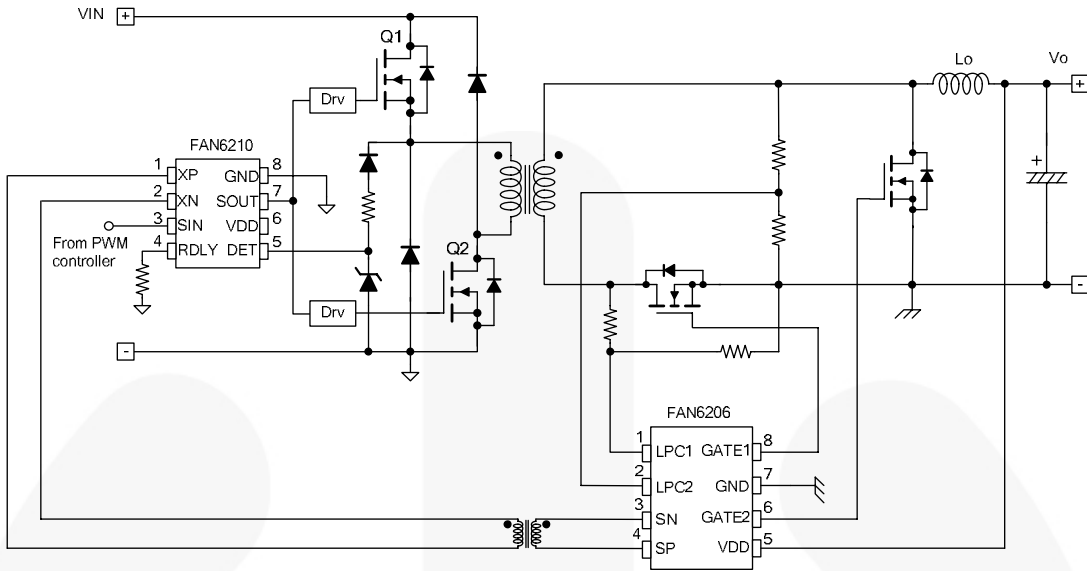


Figure 1. Typical Application

## Internal Block Diagram

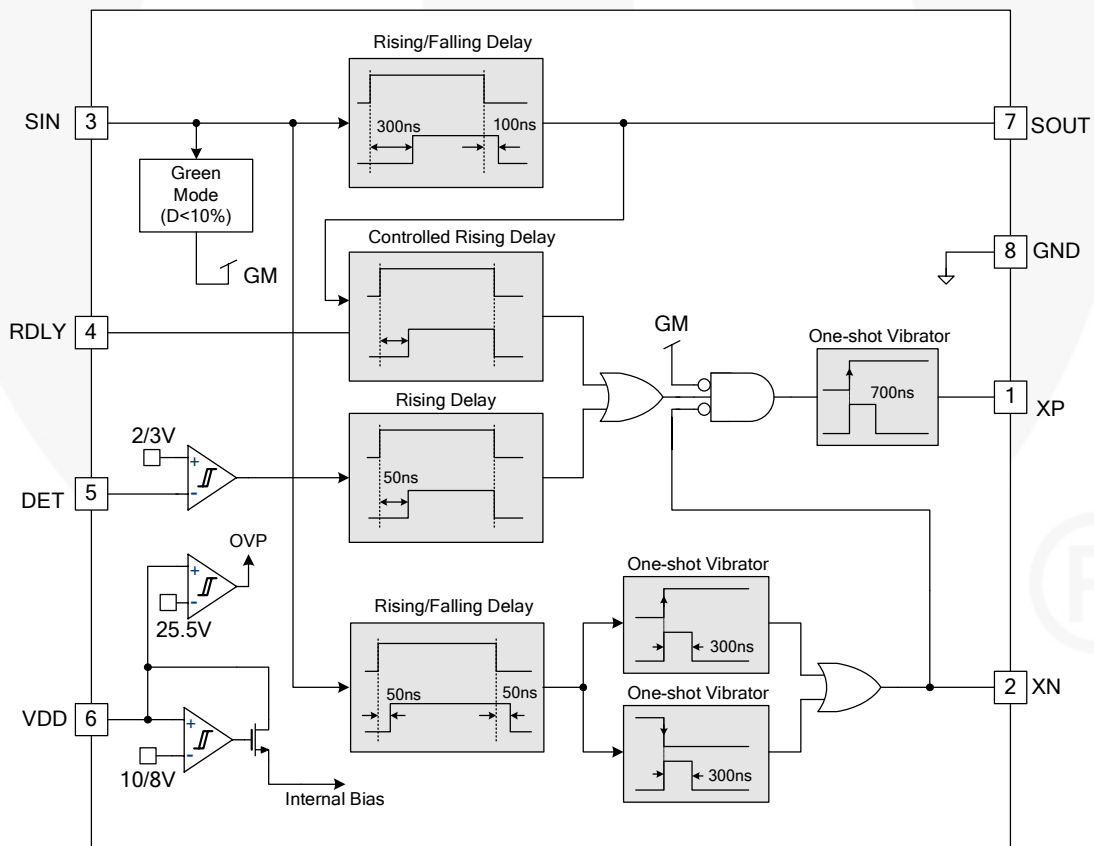
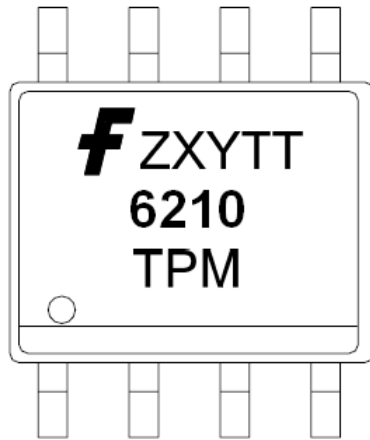


Figure 2. Functional Block Diagram

## Marking Information



**F:** Fairchild Logo  
**Z:** Plant Code  
**X:** Year Code  
**Y:** Week Code  
**TT:** Package Type  
**T:** M=SOP  
**P:** Y: Green Package  
**M:** Manufacture Flow Code

Figure 3. Top Mark

## Pin Configuration

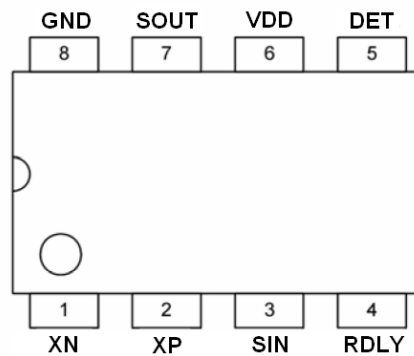


Figure 4. Pin Configuration

## Pin Definitions

Pin #	Name	Description
1	XN	Pulse signal output terminal for SR off control signal.
2	XP	Pulse signal output terminal for SR on control signal.
3	SIN	Input signal for high- and low-side gate driver outputs.
4	RDLY	Delay time setting. This delay time is SOUT rising to trigger XP pulse delay time.
5	DET	Sensing freewheel diode voltage.
6	VDD	The power supply pin.
7	SOUT	Gate driving to high- and low-side gate driver.
8	GND	Ground.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V <sub>DD</sub>	DC Supply Voltage		30	V
V <sub>SIN</sub>	Logic Input Voltage		30	V
V <sub>SOUT</sub>	Low Side Output Voltage		18	V
V <sub>H</sub>	XP, XN		30	V
V <sub>L</sub>	DET, RDLY		7	V
P <sub>D</sub>	Power Dissipation T <sub>A</sub> < 50°C		400	mW
θ <sub>JA</sub>	Thermal Dissipation (Junction-to-Air)		150	°C/W
T <sub>J</sub>	Operating Junction Temperature	-40	+125	°C
T <sub>STG</sub>	Storage Temperature Range	-55	+150	°C
T <sub>L</sub>	Lead Temperature (Soldering) 10 Seconds		260	°C
ESD	Human Body Model, JEDEC:JESD22-A114		4.0	KV
	Charged Device Model, JEDEC:JESD22-C101		1.5	KV

### Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to GND pin.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T <sub>A</sub>	Operating Ambient Temperature	-40	+105	°C

## Electrical Characteristics

$V_{DD}=20V$ ,  $T_A=25^{\circ}C$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>VDD Section</b>						
$V_{DD}$	DC Supply Voltage		7		24	V
$V_{DD-ON}$	Turn-On Threshold Voltage		9	10	11	V
$V_{TH-OFF}$	Turn-Off Threshold Voltage		7	8	9	V
$V_{DD-OVP}$	$V_{DD}$ Over-Voltage Protection (OVP)		23.0	25.5	28.0	V
$V_{DD-OVP-HYS}$	Hysteresis voltage for $V_{DD}$ OVP		0.3	0.8	1.3	V
$t_{OVP}$	$V_{DD}$ OVP Debounce Time			250		$\mu s$
<b>SIN Section</b>						
$V_{SIN}$	Logic Input Voltage		10.5		24.5	V
$t_{DLY\_OUTH}$	Delay Time Between SIN-HIGH and SOUT-HIGH		240	300	350	ns
$t_{DLY\_OUTL}$	Delay Time Between SIN-LOW and SOUT-LOW		75	100	150	ns
$t_{ON\_MAX}$	SOUT Maximum On Time and Stop XP Pulse		8.5	10.0	12.0	$\mu s$
<b>DET Section</b>						
$V_{DET\_H}$	Detect Input Voltage to Send XP After SOUT Falling		2.5	3.0	3.5	V
$V_{DET\_L}$	Voltage to Drive XP Signal After SOUT Falling		1.5	2.0	2.5	V
$t_{PD\_DET}$	Delay Time to Send XP		30	50	100	ns
<b>XP XN Section</b>						
$t_{PLS\_XN}$	High-Level Pulsewidth of XN Signal		250	300	350	ns
$t_{PLS\_XP}$	High-Level Pulsewidth of XP Signal		600	700	800	ns
$t_{PD\_XN}$	Delay Time to Trigger XN by SIN Rising or Falling Edge		25	50	75	ns
$D_{PLS\_OFF}$	SIN Duty Ratio Shorter than $D_{PLS\_OFF}$ Stop XP Pulse			10		%
$V_{XN}$	XN Signal Output Voltage Level		5.5		8.0	V
$V_{XP}$	XP Signal Output Voltage Level		5.5		8.0	V
$t_{R\_XP}$	XP Rising Time	$V_{DD} = 15V$ ; $C_L = 100pF$ ; SOUT= 1V to 6V			30	ns
$t_{F\_XP}$	XP Falling Time	$V_{DD} = 15V$ ; $C_L = 100pF$ ; SOUT= 7V to 2V			30	ns
<b>RDLY Section</b>						
$V_{RDLY}$	RDLY Voltage	$R_{RDLY}=24k\Omega$	1.08	1.20	1.32	V
$t_{DLY\_XP}$	Delay Time to Trigger XP by SOUT Rising Edge	$R_{RDLY}=24k\Omega$	280	340	400	ns
$V_Z$	Output Voltage Maximum (Clamp)	$V_{DD}=25V$			18.5	V
$V_{OL}$	Output Voltage LOW	$V_{DD}=15V$ ; $I_O = 50mA$			1.5	V
$V_{OH}$	Output Voltage HIGH	$V_{DD}=15V$ ; $I_O = 50mA$	10			V
$t_R$	SOUT Rising Time	$V_{DD} = 15V$ ; $C_L = 5nF$ ; SOUT= 2V to 9V	30	70	120	ns
$t_F$	SOUT Falling Time	$V_{DD} = 15V$ ; $C_L = 5nF$ ; SOUT= 9V to 2V	30	50	100	ns

## Typical Performance Characteristics

These characteristic graphs are normalized at  $T_A = 25^\circ\text{C}$ .

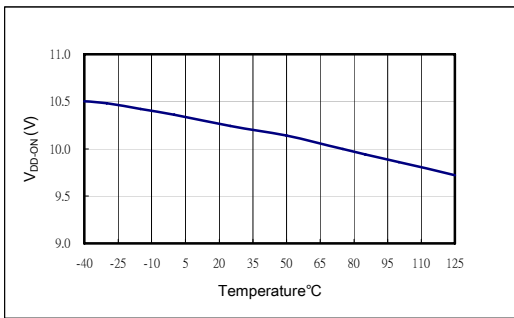


Figure 5. Turn-On Threshold Voltage

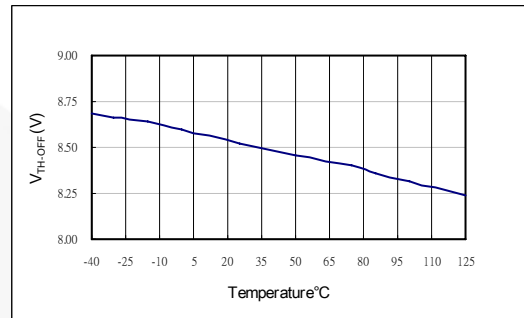


Figure 6. Turn-Off Threshold Voltage

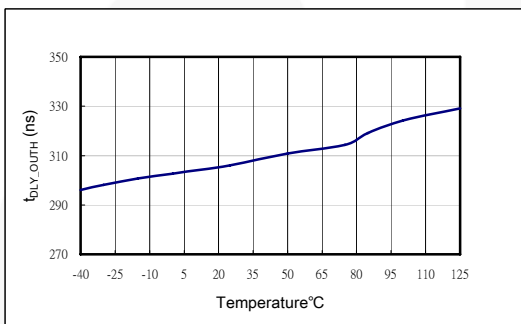


Figure 7. Delay Time Between SIN-HIGH and SOUT-HIGH

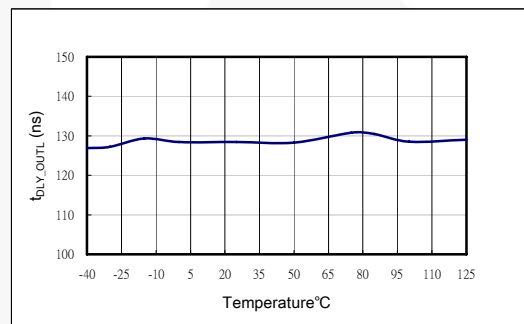


Figure 8. Delay Time Between SIN-LOW and SOUT-LOW

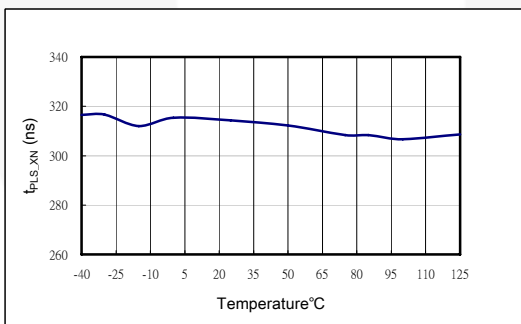


Figure 9. High-Level Pulswidth of XN Signal

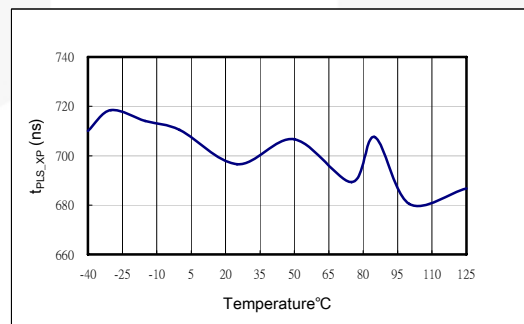


Figure 10. High-Level Pulswidth of XP Signal

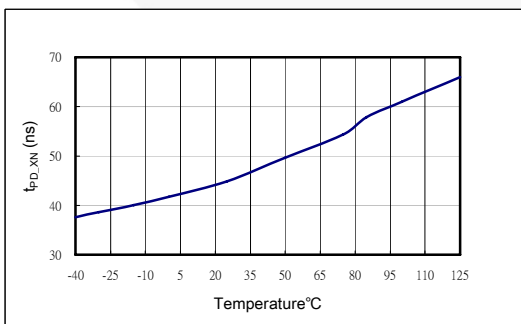


Figure 11. Delay Time to Trigger XN by SIN Rising or Falling Edge

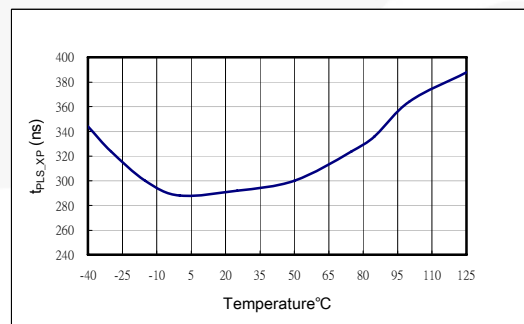
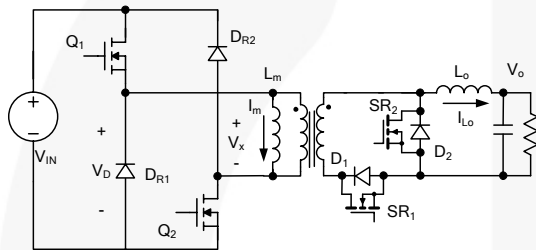


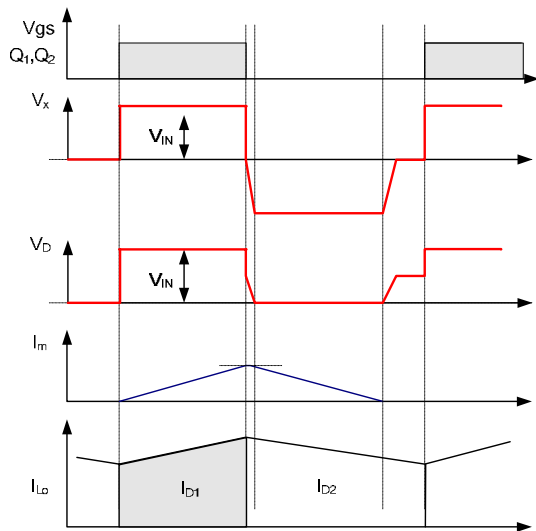
Figure 12. Delay Time to Trigger XP by SOUT Rising Edge

## Function Description

Figure 13 and Figure 14 show the simplified circuit diagram of dual-forward converter and its key waveforms. Switches  $Q_1$  and  $Q_2$  are turned on and off together. Once  $Q_1$  and  $Q_2$  are turned on, input voltage is applied across the transformer primary side and power is delivered to the secondary side through the transformer, powering diode  $D_1$ . During this time, the magnetizing current linearly increases. When  $Q_1$  and  $Q_2$  are turned off, the magnetizing current of the transformer forces the reset diodes ( $D_{R1}$  and  $D_{R2}$ ) and negative input voltage is applied across the transformer primary side. During this time, magnetizing current linearly decreases to zero and the secondary-side inductor current freewheels through diode  $D_2$ . When synchronous rectifiers  $SR_1$  and  $SR_2$  are used instead of diodes  $D_1$  and  $D_2$ , it is important to have proper timing between drive signals for  $SR_1$  and  $SR_2$ .



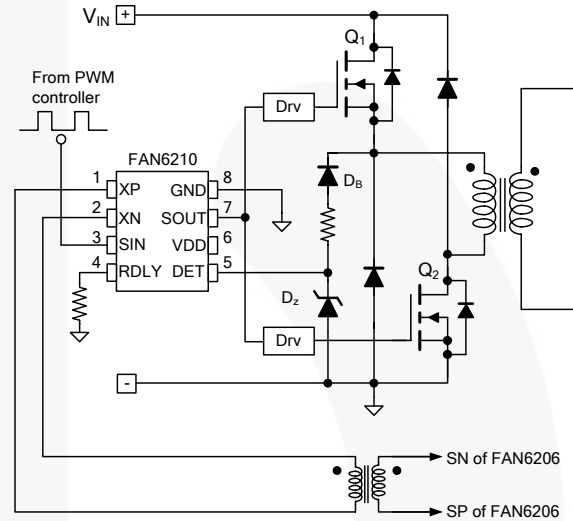
**Figure 13. Simplified Circuit Diagram of Dual-Forward Converter**



**Figure 14. Key Waveforms of Dual-Forward Converter**

Figure 15 shows the typical application circuit of FAN6210. SIN is the gate drive output of the PWM controller. SOUT is obtained from SIN by adding a delay, which is used to drive two switches  $Q_1$  and  $Q_2$ .

The value of the DET resistor is recommended as 10k $\Omega$  and  $D_B$  is used to block high voltage on winding. The breakdown voltage of Zener diode  $D_z$  is typically 5~6V to protect the DET pin from over voltage.



**Figure 15. Typical Application Circuit**

Figure 16 shows the timing diagrams for heavy-load and light-load conditions.

The switching operation of the secondary SR MOSFETs is determined by the SN and SP signals. FAN6206 turns on SR MOSFETs at the rising edge of the XP signal, while it turns off SR MOSFETs at the rising edge of XN. Within one switching cycle, XP and XN are obtained two times, respectively.

The XN signal has a 300ns pulse-width and is triggered by the rising edge and falling edge of the SIN signal after a short time delay ( $t_{PD\_XN}$ ).

XP signal has a 700ns pulse-width and is triggered by the rising edge of the SOUT signal after an adjustable time delay ( $t_{DLY\_XP}$ ) and by the falling edge of the DET signal. The relation between the delay resistor ( $R_{DELAY}$ ) and the delay time is shown in Figure 17. The triggering of the XP signal by DET is prohibited while the XN signal is HIGH. Therefore, the XP signal is not triggered at the falling edge of the DET signal and is delayed until the XN signal drops to zero at heavy-load condition. At light-load condition, the DET falling edge comes after the XN signal drops to zero and the XP signal is triggered at the falling edge of the DET signal after a short time delay ( $t_{PD\_DET}$ ).

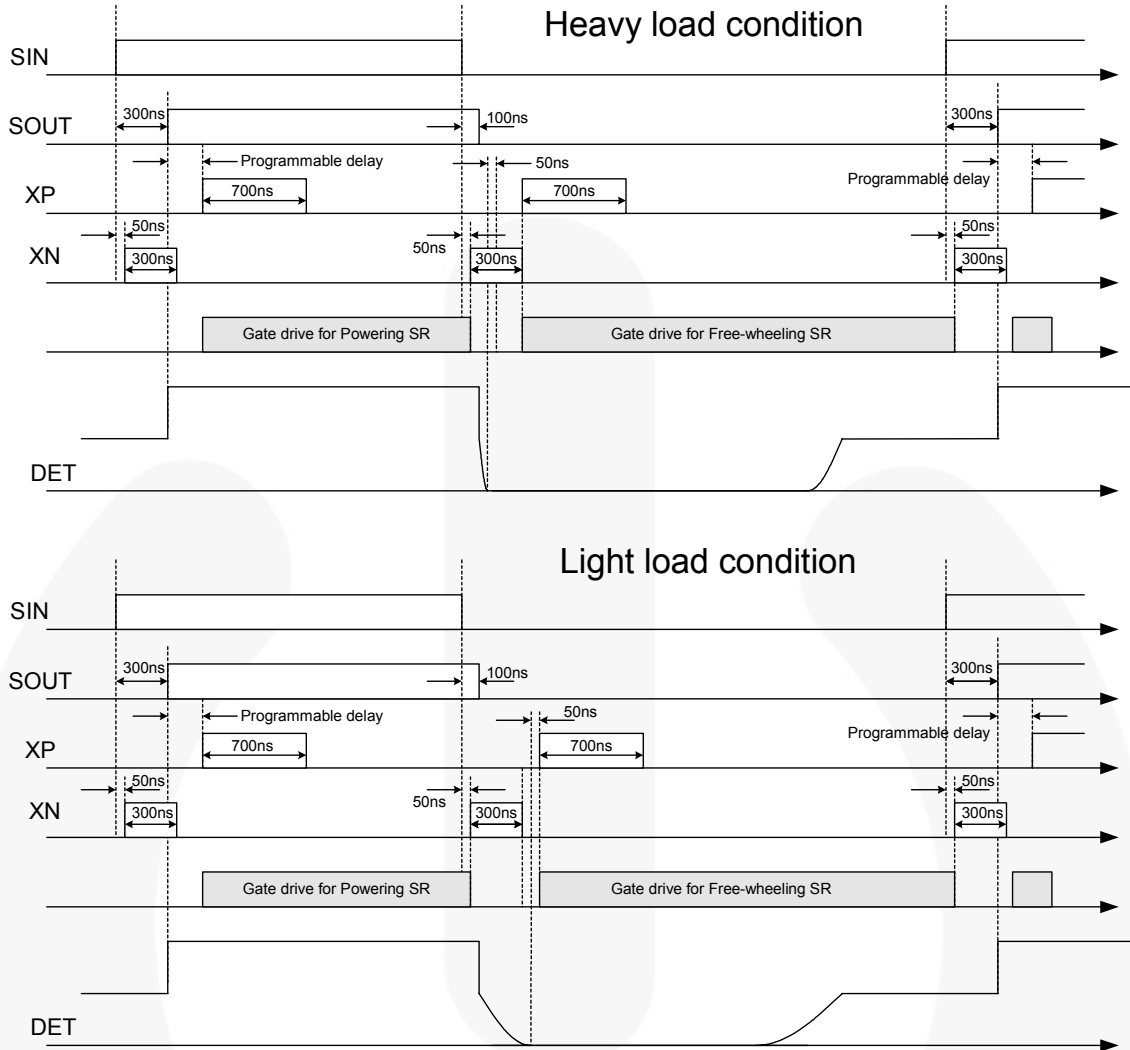


Figure 16. Timing Diagram

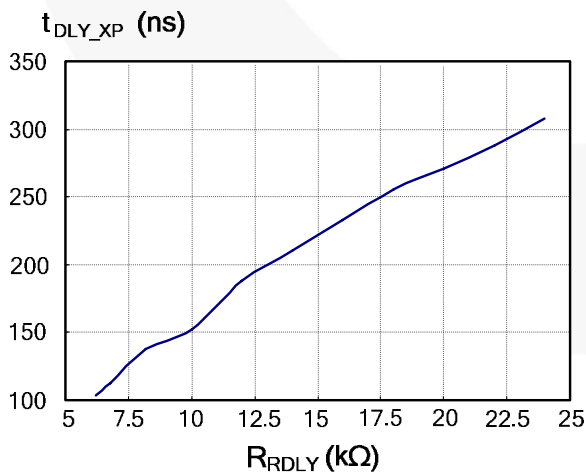


Figure 17. Programmable Delay with Resistor

#### Under-Voltage Lockout (UVLO)

The power-on and -off threshold of FAN6210 are fixed at 10V and 8V, respectively. The V<sub>DD</sub> pin can be connected with the power source of the PWM controller.

#### V<sub>DD</sub> Pin Over-Voltage Protection

V<sub>DD</sub> over-voltage protection prevents damage due to abnormal conditions. Once the V<sub>DD</sub> voltage exceeds the V<sub>DD</sub> over-voltage protection voltage (V<sub>DD-OVP</sub>) and lasts for t<sub>OVP</sub>, FAN6210 stops operation.

#### Green-Mode Operation

To improve light-load efficiency, green-mode operation is employed, which disables the SR turn-on trigger signal, minimizing gate drive power consumption at light-load condition. Green mode is enabled when the duty cycle of SIN is smaller than 10%.









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