TPS51716 Complete DDR2, DDR3, DDR3L, LPDDR3, and DDR4 Memory Power Solution Synchronous Buck Controller, 2-A LDO, With Buffered Reference

1 Features

- Synchronous Buck Controller (VDDQ)
  - Conversion Voltage Range: 3 to 28 V
  - Output Voltage Range: 0.7 to 1.8 V
  - 0.8% V_{REF} Accuracy
  - D-CAP2™ Mode for Ceramic Output Capacitors
  - Selectable 500-kHz/670-kHz Switching Frequencies
  - Optimized Efficiency at Light and Heavy Loads With Auto-Skip Function
  - Supports Soft-Off in S4/S5 States
  - OCL/OVP/UVP/UVLO Protections
  - Powergood Output
- 2-A LDO (VTT), Buffered Reference (VTTREF)
  - 2-A (Peak) Sink and Source Current
  - Requires Only 10-µF of Ceramic Output Capacitance
  - Buffered, Low Noise, 10-mA VTTREF Output
  - 0.8% VTTREF, 20-mV VTT Accuracy
  - Support High-Z in S3 and Soft-Off in S4/S5
- Thermal Shutdown
- 20-Pin, 3 mm × 3 mm, WQFN Package

2 Applications

- DDR2, DDR3, DDR3L, LPDDR3, and DDR4 Memory Power Supplies
- SSTL_18, SSTL_15, SSTL_135, and HSTL Termination

3 Description

The TPS51716 provides a complete power supply for DDR2, DDR3, DDR3L, LPDDR3, and DDR4 memory systems in the lowest total cost and minimum space. It integrates a synchronous buck regulator controller (VDDQ) with a 2-A sink/source tracking LDO (VTT) and buffered low noise reference (VTTREF). The TPS51716 employs D-CAP2 mode coupled with 500 kHz or 670 kHz operating frequencies that supports ceramic output capacitors without an external compensation circuit. The VTTREF tracks VDDQ/2 with excellent 0.8% accuracy. The VTT, which provides 2-A sink/source peak current capabilities, requires only 10 µF of ceramic capacitance. In addition, the device features a dedicated LDO supply input.

The TPS51716 provides rich, useful functions as well as excellent power supply performance. It supports flexible power state control, placing VTT at high-Z in S3 and discharging VDDQ, VTT and VTTREF (soft-off) in S4/S5 state. It includes programmable OCL with low-side MOSFET $R_{DS(on)}$ sensing, OVP/UVP/UVLO and thermal shutdown protections.

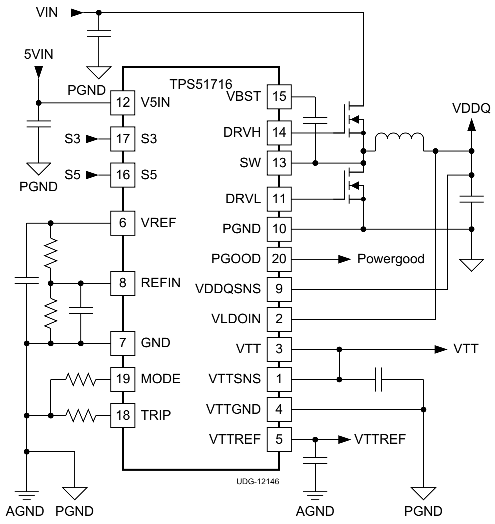
TI offers the TPS51716 in a 20-pin, 3 mm × 3 mm, WQFN package and specifies it for an ambient temperature range between –40°C and 85°C.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS51716	WQFN (20)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

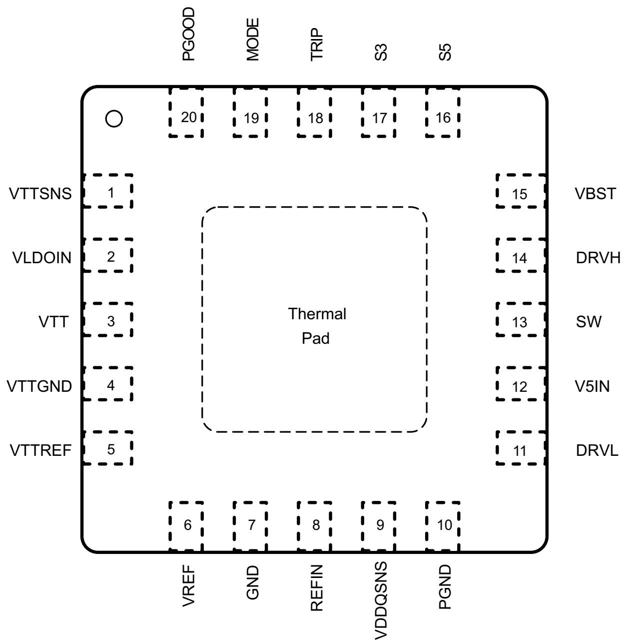
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2012) to Revision A **Page**

- Added *ESD Ratings* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Updated the Title From: Complete DDR2, DDR3, DDR3L, and LPDDR3 Memory Power Solution To: Complete DDR2, DDR3, DDR3L, LPDDR3, and DDR4 Memory Power 1
- Changed *Applications* list From: DDR2/DDR3/DDR3L/LPDDR3 Memory Power Supplies To: DDR2, DDR3, DDR3L, LPDDR3, and DDR4 Memory Power Supplies 1

5 Pin Configuration and Functions

RUK Package
20-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DRVH	14	O	High-side MOSFET gate driver output.
DRVL	11	O	Low-side MOSFET gate driver output.
GND	7	—	Signal ground.
MODE	19	I	Connect resistor to GND to configure switching frequency, control mode and discharge mode. (See Table 2)
PGND	10	—	Gate driver power ground. $R_{DS(on)}$ current sensing input(+).
PGOOD	20	O	Powergood signal open drain output. PGOOD goes high when VDDQ output voltage is within the target range.
REFIN	8	I	Reference input for VDDQ. Connect to the midpoint of a resistor divider from VREF to GND. Add a capacitor for stable operation.
SW	13	I/O	High-side MOSFET gate driver return. $R_{DS(on)}$ current sensing input(–).
S3	17	I	S3 signal input. (See Table 1)
S5	16	I	S5 signal input. (See Table 1)
TRIP	18	I	Connect resistor to GND to set OCL at $V_{TRIP}/8$. Output 10-μA current at room temperature, T_C = 4700 ppm/°C.
VBST	15	I	High-side MOSFET gate driver bootstrap voltage input. Connect a capacitor from the VBST pin to the SW pin.
VDDQSNS	9	I	VDDQ output voltage feedback. Reference input for VTTREF. Also serves as power supply for VTTREF.
VLDOIN	2	I	Power supply input for VTT LDO. Connect VDDQ in typical application.
VREF	6	O	1.8-V reference output
VTT	3	O	VTT 2-A LDO output. Need to connect 10 μF or larger capacitance for stability.
VTTGND	4	—	Power ground for VTT LDO
VTTREF	5	O	Buffered VTT reference output. Need to connect 0.22 μF or larger capacitance for stability.
VTTSNS	1	I	VTT output voltage feedback.
V5IN	12	I	5-V power supply input for internal circuits and MOSFET gate drivers.
Thermal pad	—	—	Thermal pad. Connect directly to system GND plane with multiple vias.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage(2)	VBST	–0.3	36	V
	VBST(3)	–0.3	6	
	SW	–5	30	
	VLDOIN, VDDQSNS, REFIN	–0.3	3.6	
	VTTSNS	–0.3	3.6	
	PGND, VTTGND	–0.3	0.3	
	V5IN, S3, S5, TRIP, MODE	–0.3	6	
Output voltage(2)	DRVH	–5	36	V
	DRVH(3)	–0.3	6	
	VTTREF, VREF	–0.3	3.6	
	VTT	–0.3	3.6	
	DRVL	–0.3	6	
	PGOOD	–0.3	6	
Junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V5IN	4.5		5.5	V
Input voltage range	VBST	–0.1		33.5	V
	VBST(1)	–0.1		5.5	
	SW	–3		28	
	SW(2)	–4.5		28	
	VLDOIN, VDDQSNS, REFIN	–0.1		3.5	
	VTTSNS	–0.1		3.5	
	PGND, VTTGND	–0.1		0.1	
	S3, S5, TRIP, MODE	–0.1		5.5	
Output voltage range	DRVH	–3		33.5	V
	DRVH(1)	–0.1		5.5	
	DRVH(2)	–4.5		33.5	
	VTTREF, VREF	–0.1		3.5	
	VTT	–0.1		3.5	
	DRVL	–0.1		5.5	
	PGOOD	–0.1		5.5	
T_A	Operating free-air temperature	–40		85	°C

(1) Voltage values are with respect to the SW terminal.
(2) This voltage should be applied for less than 30% of the repetitive period.

6.4 Thermal Information

THERMAL METRIC(1)		TPS51716 RUK (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range, V_{V5IN} = 5 V, VLDOIN is connected to VDDQ output, V_{MODE}= 0 V, V_{S3}= V_{S5}= 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{V5IN(S0)}$	V5IN supply current, in S0	T_A = 25°C, No load, V_{S3} = V_{S5} = 5 V		590		µA
$I_{V5IN(S3)}$	V5IN supply current, in S3	T_A = 25°C, No load, V_{S3} = 0 V, V_{S5} = 5 V		500		µA
$I_{V5INSDN}$	V5IN shutdown current	T_A = 25°C, No load, V_{S3} = V_{S5} = 0 V			1	µA
$I_{VLDOIN(S0)}$	VLDOIN supply current, in S0	T_A = 25°C, No load, V_{S3} = V_{S5} = 5 V			5	µA
$I_{VLDOIN(S3)}$	VLDOIN supply current, in S3	T_A = 25°C, No load, V_{S3} = 0 V, V_{S5} = 5 V			5	µA
$I_{VLDOINSDN}$	VLDOIN shutdown current	T_A = 25°C, No load, V_{S3} = V_{S5} = 0 V			5	µA
VREF OUTPUT						
V_{VREF}	Output voltage	I_{VREF} = 30 µA, T_A = 25°C		1.8000		V
		0 µA ≤ I_{VREF} <300 µA, T_A = –10°C to 85°C	1.7856		1.8144	
		0 µA ≤ I_{VREF} <300 µA, T_A = –40°C to 85°C	1.7820		1.8180	
$I_{VREFOCL}$	Current limit	V_{VREF} = 1.7 V	0.4	0.8		mA
VTTREF OUTPUT						
V_{VTTREF}	Output voltage			$V_{VDDQSNS}$ / 2		V
V_{VTTREF}	Output voltage tolerance to V_{VDDQ}	|I_{VTTREF}| <100 µA, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V	49.2%		50.8%	
		|I_{VTTREF}| <10 mA, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V	49%		51%	
$I_{VTTREFOCLSRC}$	Source current limit	$V_{VDDQSNS}$ = 1.8 V, V_{VTTREF}= 0 V	10	18		mA
$I_{VTTREFOCLSNK}$	Sink current limit	$V_{VDDQSNS}$ = 1.8 V, V_{VTTREF} = 1.8 V	10	17		mA
$I_{VTTREFDIS}$	VTTREF discharge current	T_A = 25°C, V_{S3} = V_{S5} = 0 V, V_{VTTREF} = 0.5 V	0.8	1.3		mA
VTT OUTPUT						
V_{VTT}	Output voltage			V_{VTTREF}		V
V_{VTTTOL}	Output voltage tolerance to VTTREF	|I_{VTT}| ≤ 10 mA, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V, I_{VTTREF}= 0 A	–20		20	mV
		|I_{VTT}| ≤ 1 A, 1.2 ≤ $V_{VDDQSNS}$ ≤ 1.8 V, I_{VTTREF}= 0 A	–30		30	
		|I_{VTT}| ≤ 2 A, 1.4 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V, I_{VTTREF}= 0 A	–40		40	
		|I_{VTT}| ≤ 1.5 A, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.4 V, I_{VTTREF}= 0 A	–40		40	
$I_{VTTOCLSRC}$	Source current limit	$V_{VDDQSNS}$ = 1.8 V, V_{VTT} = V_{VTTSNS} = 0.7 V, I_{VTTREF}= 0 A	2	3		A
$I_{VTTOCLSNK}$	Sink current limit	$V_{VDDQSNS}$ = 1.8V, V_{VTT} = V_{VTTSNS} = 1.1 V, I_{VTTREF}= 0 A	2	3		A
I_{VTTLK}	Leakage current	T_A = 25°C , V_{S3} = 0 V, V_{S5} = 5 V, V_{VTT} = V_{VTTREF}			5	µA
$I_{VTTSNSBIAS}$	VTTSNS input bias current	V_{S3} = 5 V, V_{S5} = 5 V, V_{VTTSNS} = V_{VTTREF}	–0.5	0.0	0.5	µA
$I_{VTTSNSLK}$	VTTSNS leakage current	V_{S3} = 0 V, V_{S5} = 5 V, V_{VTTSNS} = V_{VTTREF}	–1	0	1	µA
I_{VTTDIS}	VTT Discharge current	T_A = 25°C, V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 1.8 V, V_{VTT} = 0.5 V, I_{VTTREF}= 0 A		7.8		mA
VDDQ OUTPUT						
$V_{VDDQSNS}$	VDDQ sense voltage			V_{REFIN}		
$I_{VDDQSNS}$	VDDQSNS input current	$V_{VDDQSNS}$ = 1.8 V		39		µA
I_{REFIN}	REFIN input current	V_{REFIN} = 1.8 V	–0.1	0.0	0.1	µA
$I_{VDDQDIS}$	VDDQ discharge current	V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 0.5 V, non-tracking discharge mode		12		mA
$I_{VLDOINDIS}$	VLDOIN discharge current	V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 0.5 V, tracking discharge mode		1.2		A
SWITCH MODE POWER SUPPLY (SMPS) FREQUENCY						
f_{SW}	VDDQ switching frequency	V_{IN} = 12 V, $V_{VDDQSNS}$ = 1.8 V, R_{MODE} = 1 kΩ		500		kHz
		V_{IN} = 12 V, $V_{VDDQSNS}$ = 1.8 V, R_{MODE} = 12 kΩ		670		
$t_{ON(min)}$	Minimum on time	DRVH rising to falling(1)		60		ns
$t_{OFF(min)}$	Minimum off time	DRVH falling to rising	200	320	450	ns
VDDQ MOSFET DRIVER						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = –50 mA		1.6	3	Ω
		Sink, I_{DRVH} = 50 mA		0.6	1.5	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = –50 mA		0.9	2	Ω
		Sink, I_{DRVL} = 50 mA		0.5	1.2	

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(1) Specified by design. Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range, V_{V5IN} = 5 V, VLDOIN is connected to VDDQ output, V_{MODE}= 0 V, V_{S3}= V_{S5}= 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DEAD}	Dead time	DRVH-off to DRVL-on		10		ns
		DRVL-off to DRVH-on		20		
INTERNAL BOOT STRAP SW						
V_{FBST}	Forward voltage	$V_{V5IN\text{-}VBST}$, T_A = 25°C, I_F = 10 mA		0.1	0.2	V
I_{VBSTLK}	VBST leakage current	T_A = 25°C, V_{VBST} = 33 V, V_{SW} = 28 V		0.01	1.5	µA
LOGIC THRESHOLD						
I_{MODE}	MODE source current		14	15	16	µA
V_{THMODE}	MODE threshold voltage	MODE 0-1	109	129	149	mV
		MODE 1-2	235	255	275	
		MODE 2-3	392	412	432	
V_{IL}	S3/S5 low-level voltage				0.5	V
V_{IH}	S3/S5 high-level voltage		1.8			V
V_{IHYST}	S3/S5 hysteresis voltage			0.25		V
I_{ILK}	S3/S5 input leak current		–1	0	1	µA
SOFT START						
t_{SS}	VDDQ soft-start time	Internal soft-start time, C_{VREF} = 0.1 µF, S5 rising to $V_{VDDQSNS}$ > 0.99 × V_{REFIN}		1.1		ms
PGOOD COMPARATOR						
V_{THPG}	VDDQ PGOOD threshold	PGOOD in from higher	106%	108%	110%	
		PGOOD in from lower	90%	92%	94%	
		PGOOD out to higher	114%	116%	118%	
		PGOOD out to lower	82%	84%	86%	
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.5 V	3	5.9		mA
t_{PGDLY}	PGOOD delay time	Delay for PGOOD in	0.8	1	1.2	ms
		Delay for PGOOD out, with 100 mV over drive		330		ns
$t_{PGSSDLY}$	PGOOD start-up delay	C_{VREF} = 0.1 µF, S5 rising to PGOOD rising		2.5		ms
PROTECTIONS						
I_{TRIP}	TRIP source current	T_A = 25°C, V_{TRIP} = 0.4 V	9	10	11	µA
TC_{ITRIP}	TRIP source current temperature coefficient(1)			4700		ppm/°C
V_{TRIP}	V_{TRIP} voltage range		0.2		3	V
V_{OCL}	Current limit threshold	V_{TRIP} = 3.0 V	360	375	390	mV
		V_{TRIP} = 1.6 V	190	200	210	
		V_{TRIP} = 0.2 V	20	25	30	
V_{OCLN}	Negative current limit threshold	V_{TRIP} = 3.0 V	–390	–375	–360	mV
		V_{TRIP} = 1.6 V	–210	–200	–190	
		V_{TRIP} = 0.2 V	–30	–25	–20	
V_{ZC}	Zero cross detection offset			0		mV
V_{UVLO}	V5IN UVLO threshold voltage	Wake-up	4.2	4.4	4.5	V
		Shutdown	3.7	3.9	4.1	
V_{OVP}	VDDQ OVP threshold voltage	OVP detect voltage	118%	120%	122%	
t_{OVPDLY}	VDDQ OVP propagation delay	With 100 mV over drive		430		ns
V_{UVP}	VDDQ UVP threshold voltage	UVP detect voltage	66%	68%	70%	
t_{UVPDLY}	VDDQ UVP delay			1		ms
$t_{UVPENDLY}$	VDDQ UVP enable delay			1.2		ms
V_{OOB}	OOB Threshold voltage			108%		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(1)		140		°C
		Hysteresis(1)		10		

6.6 Typical Characteristics

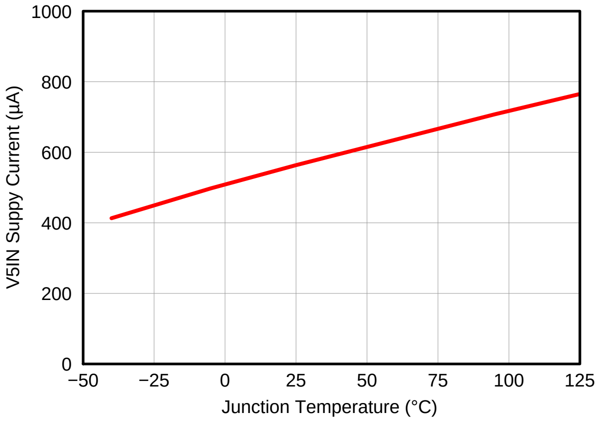


Figure 1. V5IN Supply Current vs Junction Temperature

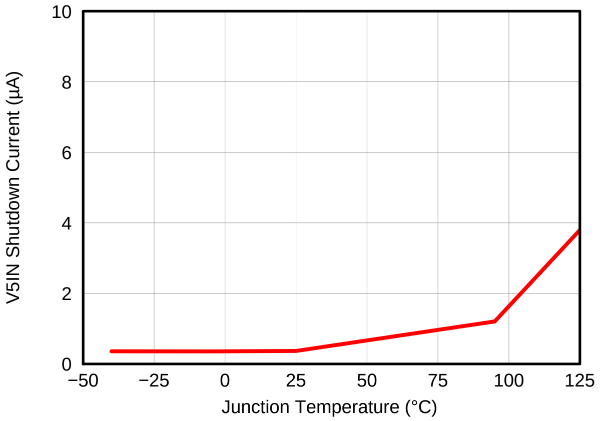


Figure 2. V5IN Shutdown Current vs Junction Temperature

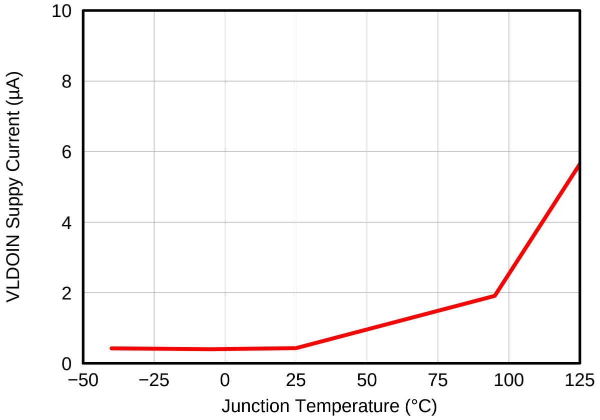


Figure 3. VLDOIN Supply Current vs Junction Temperature

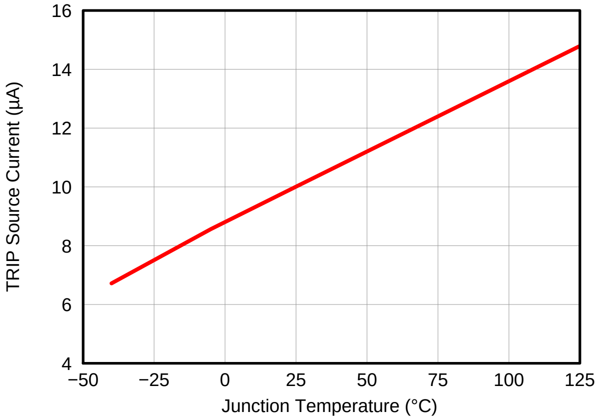


Figure 4. Current Sense Current vs Junction Temperature

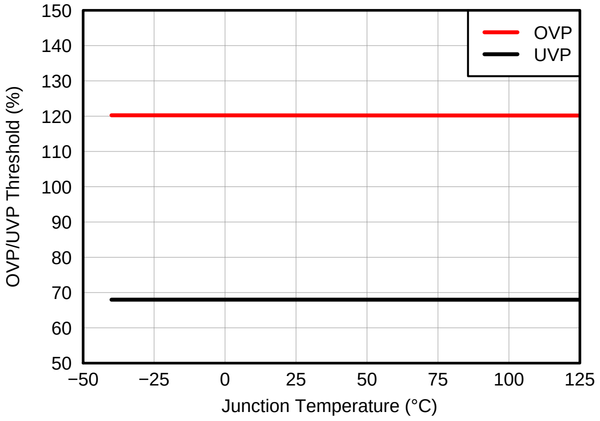


Figure 5. OVP/UVP Threshold vs Junction Temperature

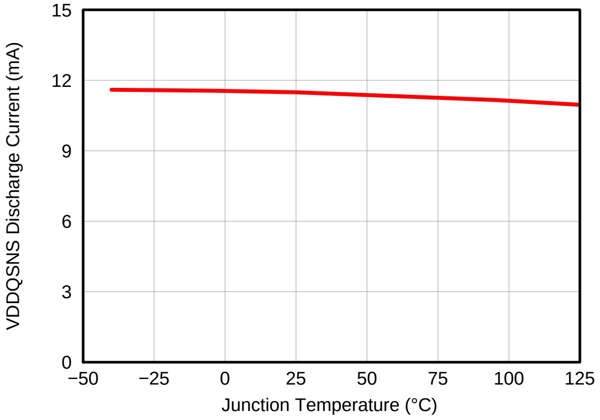


Figure 6. VDDQSNS Discharge Current vs Junction Temperature

Typical Characteristics (continued)

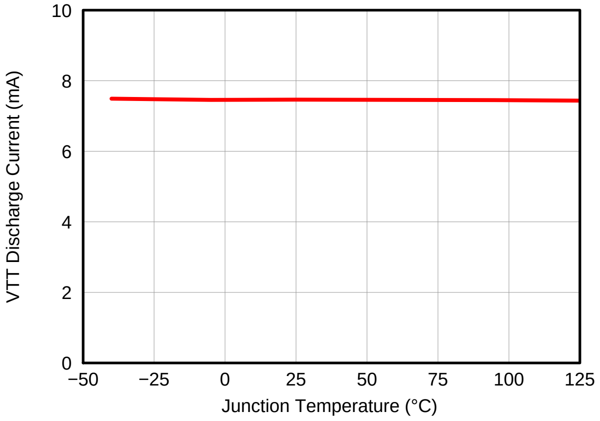


Figure 7. VTT Discharge Current vs Junction Temperature

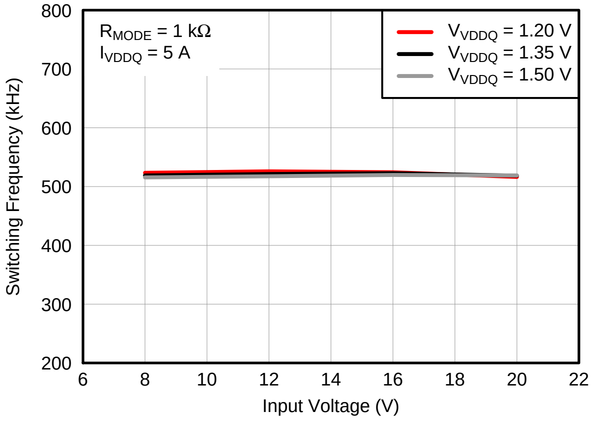


Figure 8. Switching Frequency vs Input Voltage

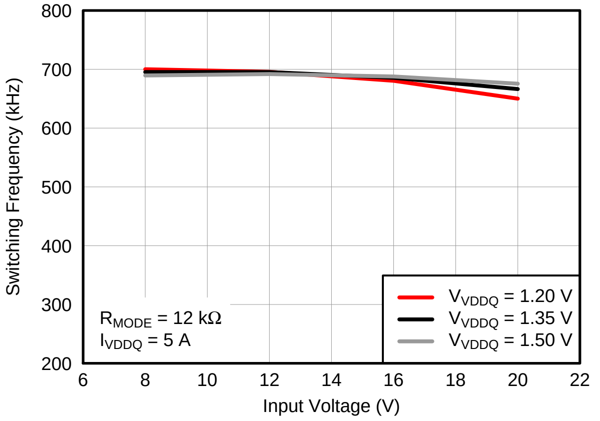


Figure 9. Switching Frequency vs Input Voltage

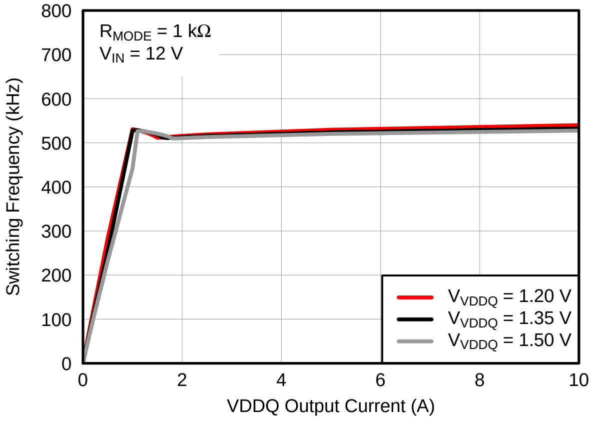


Figure 10. Switching Frequency vs Load Current

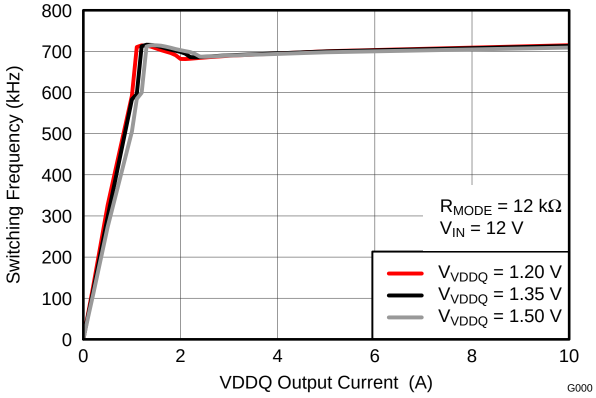


Figure 11. Switching Frequency vs Load Current

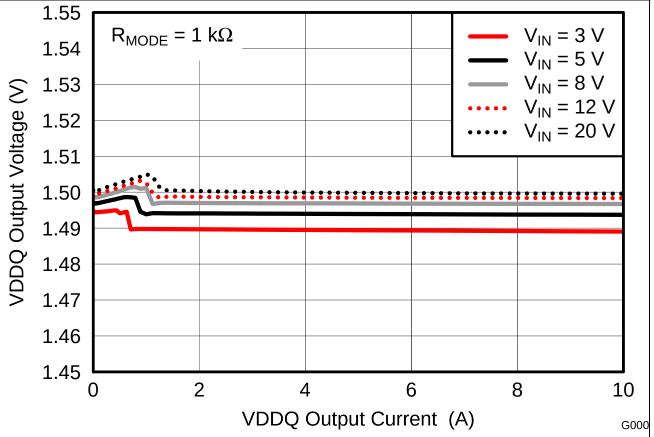


Figure 12. Load Regulation

Typical Characteristics (continued)

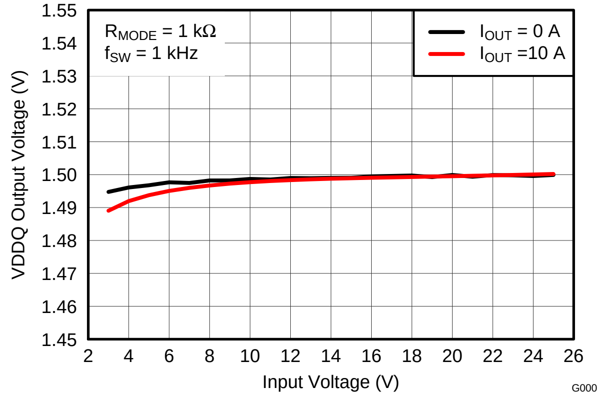


Figure 13. Line Regulation

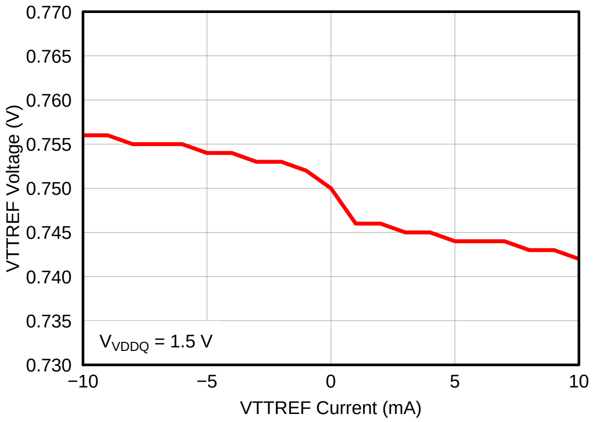


Figure 14. VTTREF Load Regulation

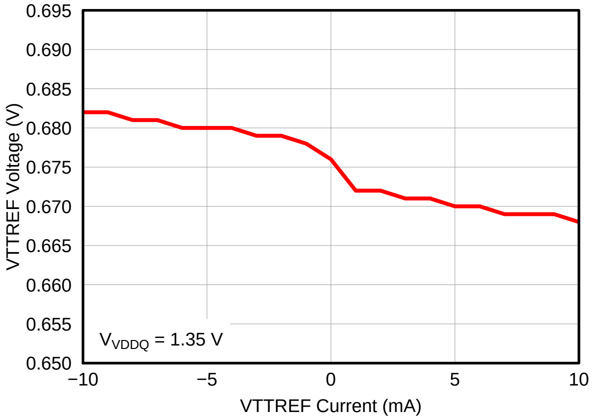


Figure 15. VTTREF Load Regulation

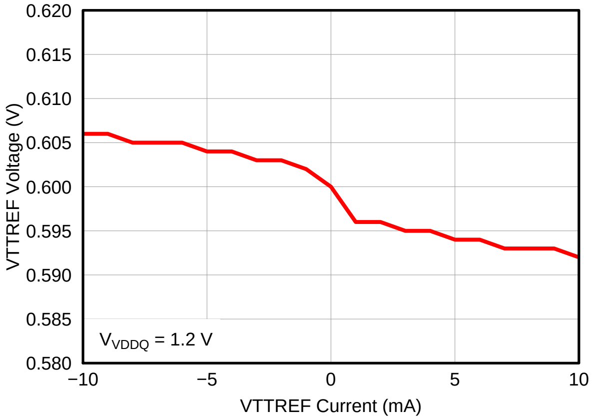


Figure 16. VTTREF Load Regulation

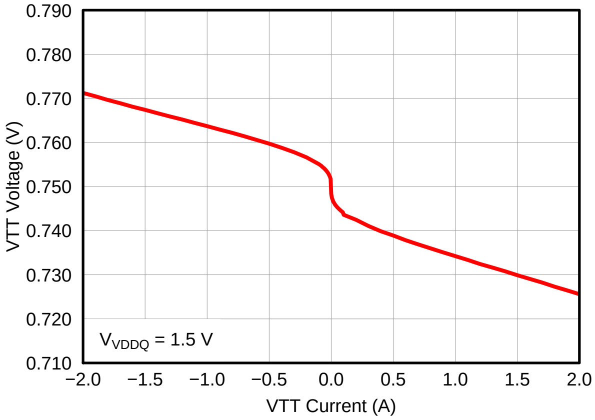


Figure 17. VTT Load Regulation

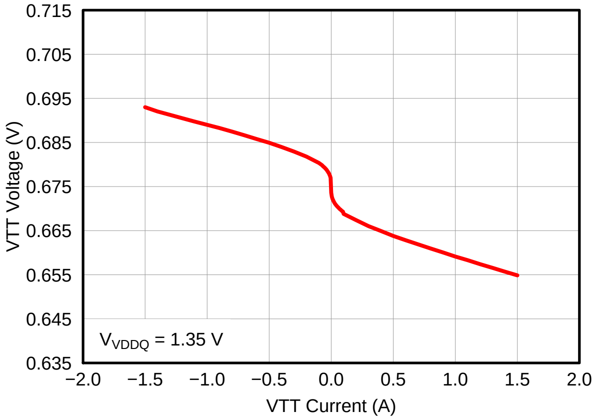


Figure 18. VTT Load Regulation

Typical Characteristics (continued)

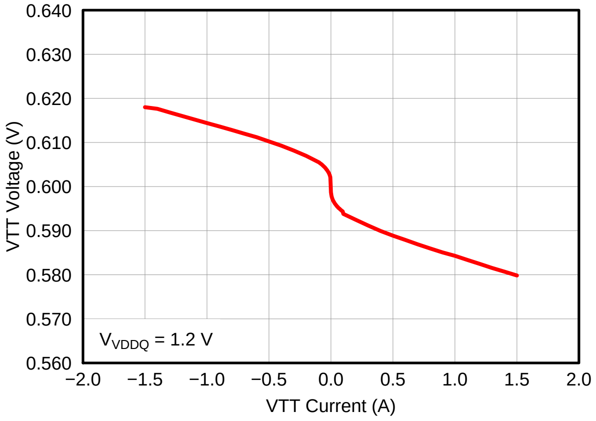


Figure 19. VTT Load Regulation

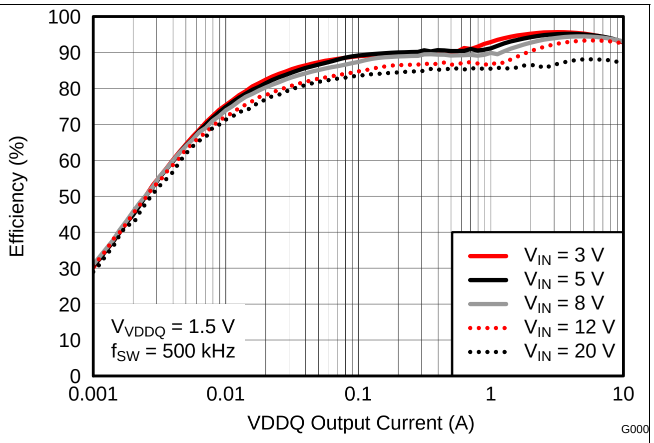


Figure 20. Efficiency

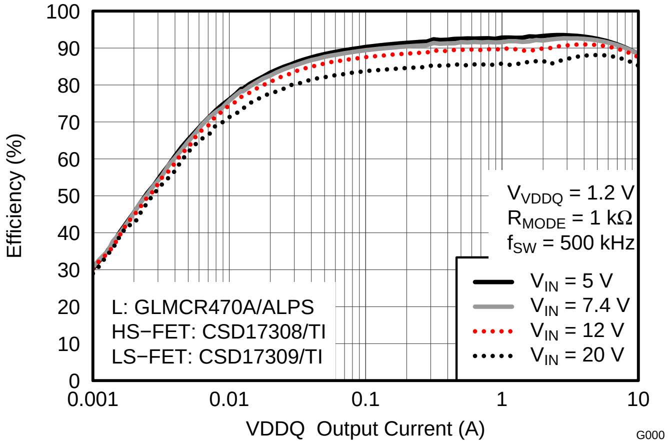


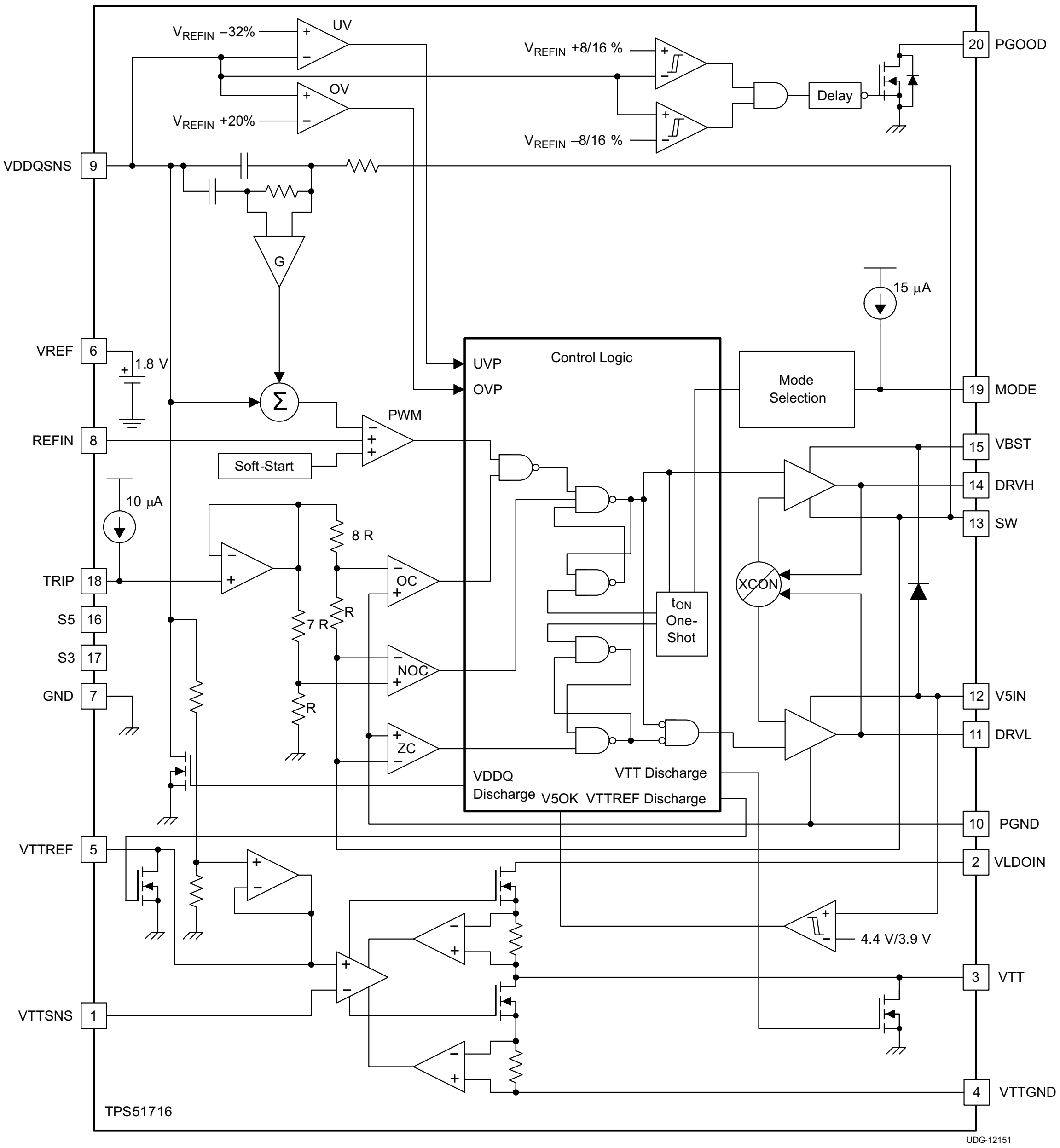
Figure 21. Efficiency

7 Detailed Description

7.1 Overview

The TPS51716 provides a complete power supply for DDR2, DDR3, DDR3L, LPDDR3, and DDR4 memory systems in the lowest total cost and minimum space. It integrates a synchronous buck regulator controller (VDDQ) with a 2-A sink/source tracking LDO (VTT) and buffered low noise reference (VTTREF). The TPS51716 employs D-CAP2 mode coupled with 500 kHz or 670 kHz operating frequencies that supports ceramic output capacitors without an external compensation circuit. The VTTREF tracks VDDQ/2 with excellent 0.8% accuracy. The VTT, which provides 2-A sink/source peak current capabilities, requires only 10-µF of ceramic capacitance. In addition, the device features a dedicated LDO supply input.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 VDDQ Switch Mode Power Supply Control

The TPS51716 supports D-CAP2 mode, which does not require complex external compensation networks and are suitable for designs with small external components counts. The D-CAP2 mode is dedicated for a configuration with very low ESR output capacitors such as multi-layer ceramic capacitors (MLCC). An adaptive on-time control scheme is used to achieve pseudo-constant frequency. The TPS51716 adjusts the on-time (t_{ON}) to be inversely proportional to the input voltage (V_{IN}) and proportional to the output voltage (V_{VDDQ}). This produces a switching frequency that is approximately constant over the variation of input voltage at the steady state condition.

7.3.2 VREF and REFIN, VDDQ Output Voltage

The part provides a 1.8-V, ±0.8% accurate, voltage reference from VREF. This output has a 300-µA (max) current capability to drive the REFIN input voltage through a voltage divider circuit. A capacitor with a value of 0.1-µF or larger should be attached close to the VREF terminal.

The VDDQ switch-mode power supply (SMPS) output voltage is defined by REFIN voltage, within the range between 0.7 V and 1.8 V, programmed by the resister-divider connected between VREF and GND. (See *External Components Selection* section.) A few nano farads of capacitance from REFIN to GND is recommended for stable operation.

7.3.3 Soft-Start and Powergood

Provide a voltage supply to VIN and V5IN before asserting S5 to high. TPS51716 provides integrated VDDQ soft-start functions to suppress in-rush current at start-up. The soft-start is achieved by controlling internal reference voltage ramping up. Figure 22 shows the start-up waveforms. The switching regulator waits for 400µs after S5 assertion. The MODE pin voltage is read in this period. A typical VDDQ ramp up duration is 700µs.

TPS51716 has a powergood open-drain output that indicates the VDDQ voltage is within the target range. The target voltage window and transition delay times of the PGOOD comparator are ±8% (typ) and 1-ms delay for assertion (low to high), and ±16% (typ) and 330-ns delay for de-assertion (high to low) during running. The PGOOD start-up delay is 2.5 ms after S5 is asserted to high. Note that the time constant which is composed of the REFIN capacitor and a resistor divider needs to be short enough to reach the target value before PGOOD comparator enabled.

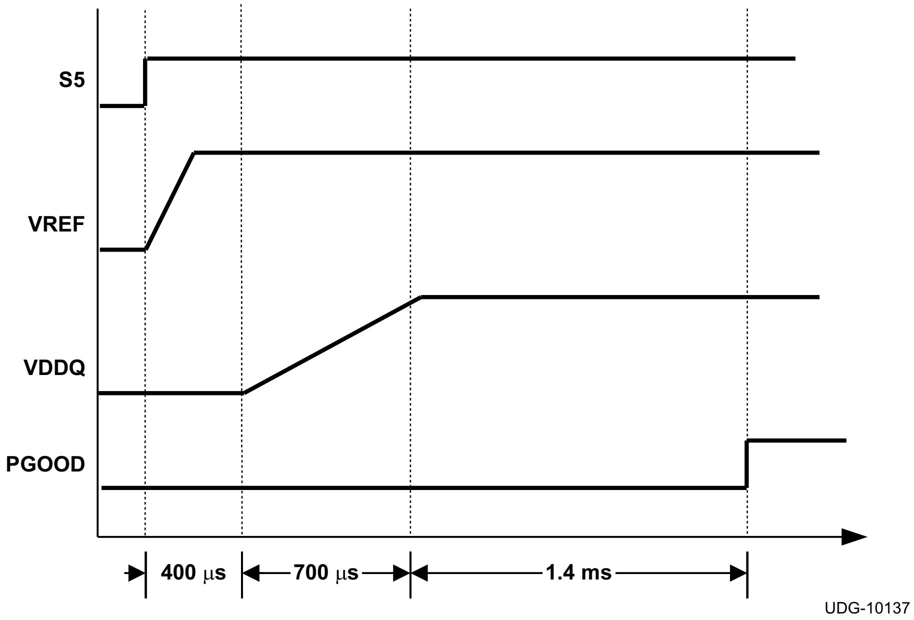

Figure 22. Typical Start-Up Waveforms

Feature Description (continued)

7.3.4 Power State Control

The TPS51716 has two input pins, S3 and S5, to provide simple control scheme of power state. All of VDDQ, VTTREF and VTT are turned on at S0 state (S3=S5=high). In S3 state (S3=low, S5=high), VDDQ and VTTREF voltages are kept on while VTT is turned off and left at high impedance state (high-Z). The VTT output floats and does not sink or source current in this state. In S4/S5 states (S3=S5=low), all of the three outputs are turned off and discharged to GND according to the discharge mode selected by MODE pin. Each state code represents as follow; S0 = full ON, S3 = suspend to RAM (STR), S4 = suspend to disk (STD), S5 = soft OFF. (See Table 1.)

Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S4/S5	LO	LO	OFF	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)

7.3.5 VDDQ Overvoltage and Undervoltage Protection

The TPS51716 sets the overvoltage protection (OVP) when VDDQSNS voltage reaches a level 20% (typ) higher than the REFIN voltage. When an OV event is detected, the controller changes the output target voltage to 0 V. This usually turns off DRVH and forces DRVL to be on. When the inductor current begins to flow through the low-side MOSFET and reaches the negative OCL, DRVL is turned off and DRVH is turned on, for a minimum on-time.

After the minimum on-time expires, DRVH is turned off and DRVL is turned on again. This action minimizes the output node undershoot due to LC resonance. When the VDDQSNS reaches 0 V, the driver output is latched as DRVH off, DRVL on. VTTREF and VTT are turned off and discharged using the non-tracking discharge MOSFETs regardless of the tracking mode.

The undervoltage protection (UVP) latch is set when the VDDQSNS voltage remains lower than 68% (typ) of the REFIN voltage for 1 ms or longer. In this fault condition, the controller latches DRVH low and DRVL low and discharges the VDDQ, VTT and VTTREF outputs. UVP detection function is enabled after 1.2 ms of SMPS operation to ensure startup.

To release the OVP and UVP latches, toggle S5 or adjust the V5IN voltage down and up beyond the undervoltage lockout threshold.

7.3.6 VDDQ Out-of-Bound Operation

When the output voltage rises to 8% above the target value, the out-of-bound operation starts. During the out-of-bound condition, the controller operates in forced PWM-only mode. Turning on the low-side MOSFET beyond the zero inductor current quickly discharges the output capacitor. During this operation, the cycle-by-cycle negative overcurrent limit is also valid. Once the output voltage returns to within regulation range, the controller resumes to auto-skip mode.

7.3.7 VDDQ Overcurrent Protection

The VDDQ SMPS has cycle-by-cycle overcurrent limiting protection. The inductor current is monitored during the off-state using the low-side MOSFET $R_{DS(on)}$, and the controller maintains the off-state when the inductor current is larger than the overcurrent trip level. The current monitor circuit inputs are PGND and SW pins so that those should be properly connected to the source and drain terminals of low-side MOSFET. The overcurrent trip level, V_{OCTRIP}, is determined by Equation 1, where R_{TRIP} is the value of the resistor connected between the TRIP pin and GND, and I_{TRIP} is the current sourced from the TRIP pin. I_{TRIP} is 10 μA typically at room temperature, and has 4700ppm/°C temperature coefficient to compensate the temperature dependency of the low-side MOSFET $R_{DS(on)}$.

$$V_{OCTRIP} = R_{TRIP} \times \frac{I_{TRIP}}{8} \tag{1}$$

Because the comparison is done during the off-state, V_{OCTRIP} sets the valley level of the inductor current. The load current OCL level, I_{OCL}, can be calculated by considering the inductor ripple current as shown in Equation 2.

$$I_{OCL} = \left(\frac{V_{OCTRIP}}{R_{DS(on)}}\right) + \frac{I_{IND(ripple)}}{2} = \left(\frac{V_{OCTRIP}}{R_{DS(on)}}\right) + \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L_X} \times \frac{V_{OUT}}{f_{SW} \times V_{IN}}$$

where

- $I_{IND(ripple)}$ is inductor ripple current (2)

In an overcurrent condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall down. Eventually, it crosses the undervoltage protection threshold and shuts down.

7.3.8 VTT and VTTREF

TPS51716 integrates two high performance, low-dropout linear regulators, VTT and VTTREF, to provide complete DDR2, DDR3, DDR3L, LPDDR3, and DDR4 power solutions. The VTTREF has a 10-mA sink/source current capability, and tracks ½ of VDDQSNS with ±1% accuracy using an on-chip ½ divider. A 0.22-µF (or larger) ceramic capacitor must be connected close to the VTTREF terminal to ensure stable operation. The VTT responds quickly to track VTTREF within ±40 mV at all conditions, and the current capability is 2 A for both sink and source. A 10-µF (or larger) ceramic capacitor(s) need to be connected close to the VTT terminal for stable operation. To achieve tight regulation with minimum effect of wiring resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high-current line to the VTT pin. (Refer to the *Layout Guidelines* section for details.)

When VTT is not required in the design, the following treatment is strongly recommended.

- Connect VLDOIN to VDDQ.
- Tie VTTSNS to VTT, and remove capacitors from VTT to float.
- Connect VTTGND to GND.
- Select MODE2, 3, 4, or 5 shown in Table 2 (Select Non-tracking discharge mode).
- Maintain a 0.22-µF capacitor connected at VTTREF.
- Pull down S3 to GND with 1-kΩ resistance.

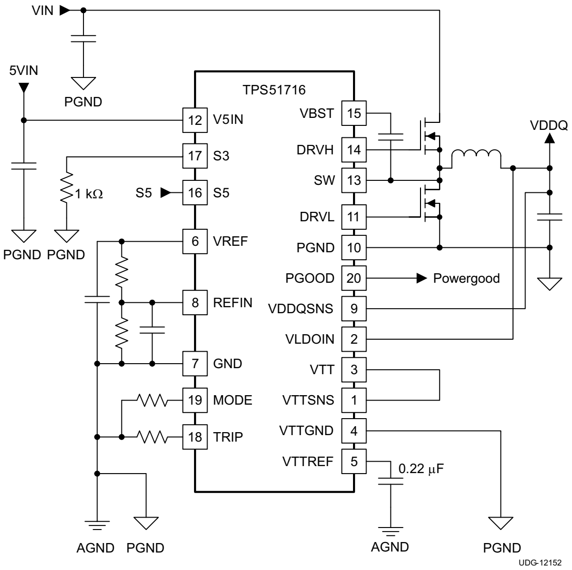

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Figure 23. Application Circuit When VTT is not Required

7.3.9 VTT Overcurrent Protection

The LDO has an internally fixed constant overcurrent limiting of 3-A (typ) for both sink and source operation.

7.3.10 V5IN Undervoltage Lockout (UVLO) Protection

The TPS51716 has a 5-V supply UVLO protection threshold. When the V5IN voltage is lower than UVLO threshold voltage, typically 3.9 V, VDDQ, VTT, and VTTREF are shut off. This is a non-latch protection.

7.3.11 Thermal Shutdown

The TPS51716 includes an internal temperature monitor. If the temperature exceeds the threshold value, 140°C (typ), VDDQ, VTT, and VTTREF are shut off. The state of VDDQ is open, and that of VTT and VTTREF are high impedance (high-Z) at thermal shutdown. The discharge functions of all outputs are disabled. This is a non-latch protection and the operation is restarted with soft-start sequence when the device temperature is reduced by 10°C (typ).

7.4 Device Functional Modes

7.4.1 MODE Pin Configuration

The TPS51716 reads the MODE pin voltage when the S5 signal is raised high and stores the status in a register. A 15-µA current is sourced from the MODE pin during this time to read the voltage across the resistor connected between the pin and GND. Table 2 shows resistor values, corresponding control mode, switching frequency and discharge mode configurations.

Table 2. MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	CONTROL MODE	SWITCHING FREQUENCY (kHz)	DISCHARGE MODE
3	33	D-CAP2	500	Non-Tracking
2	22		670	
1	12		670	Tracking
0	1		500	

7.4.2 Discharge Control

In S4/S5 state, VDDQ, VTT, and VTTREF outputs are discharged based on the respective discharge mode selected above. The tracking discharge mode discharges VDDQ output through the internal VTT regulator transistors enabling quick 13 ms discharge operation. The VTT output maintains tracking of the VTTREF voltage in this mode. (Please refer to Figure 28) After 4 ms of tracking discharge operation, the mode changes to non-tracking discharge. The VDDQ output must be connected to the VLDOIN pin in this mode. The non-tracking mode discharges the VDDQ and VTT pins using internal MOSFETs that are connected to corresponding output terminals. The non-tracking discharge is slow compared with the tracking discharge due to the lower current capability of these MOSFETs. Refer to Figure 29.

7.4.3 D-CAP2 Mode Operation

Figure 24 shows simplified model of D-CAP2 architecture.

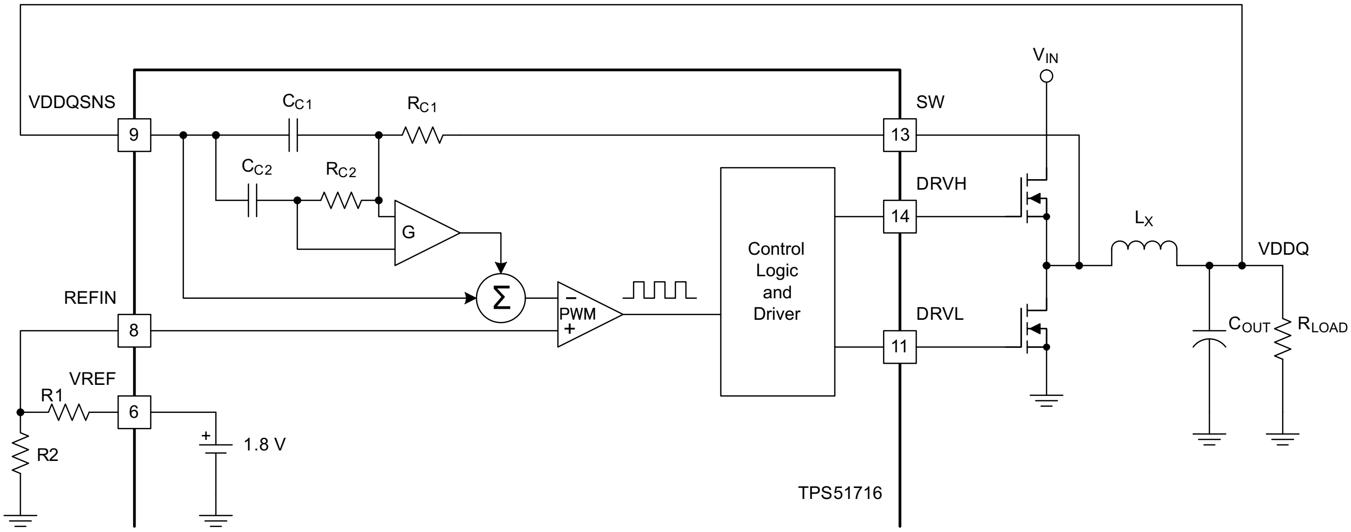


Figure 24. Simplified Modulator Using D-CAP2 Mode

The D-CAP2 mode in the TPS51716 includes an internal feedback network enabling the use of very low ESR output capacitor(s) such as multi-layer ceramic capacitors. The role of the internal network is to sense the ripple component of the inductor current information and combine it with voltage feedback signal. Using $R_{C1} = R_{C2} \equiv R_C$ and $C_{C1} = C_{C2} \equiv C_C$, 0-dB frequency of the D-CAP2 mode is given by Equation 3. It is recommended that the 0-dB frequency (f_0) be lower than 1/3 of the switching frequency to secure the proper phase margin.

$$f_0 = \frac{R_C \times C_C}{2\pi \times G \times L_X \times C_{OUT}} \le \frac{f_{SW}}{3}$$

where

- G is gain of the amplifier which amplifies the ripple current information generated by the compensation circuit (3)

The typical G value is 0.25, and typical $R_C C_C$ time constant values for 500 kHz and 670 kHz operation are 23 µs and 14.6 µs, respectively.

For example, when f_{SW}=500 kHz and L_X=1 µH, C_{OUT} should be larger than 88 µF.

When selecting the capacitor, pay attention to its characteristics. For MLCC use X5R or better dielectric and consider the derating of the capacitance by both DC bias and AC bias. When derating by DC bias and AC bias are 80% and 50%, respectively, the effective derating is 40% because 0.8 x 0.5 = 0.4. The capacitance of specialty polymer capacitors may change depending on the operating frequency. Consult capacitor manufacturers for specific characteristics.

7.4.4 Light-Load Operation

In auto-skip mode, the TPS51716 SMPS control logic automatically reduces its switching frequency to improve light-load efficiency. To achieve this intelligence, a zero cross detection comparator is used to prevent negative inductor current by turning off the low-side MOSFET. Equation 4 shows the boundary load condition of this skip mode and continuous conduction operation.

$$I_{LOAD(LL)} = \frac{\left(V_{IN} - V_{OUT}\right)}{2 \times L_X} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \tag{4}$$

8 Application and Implementation

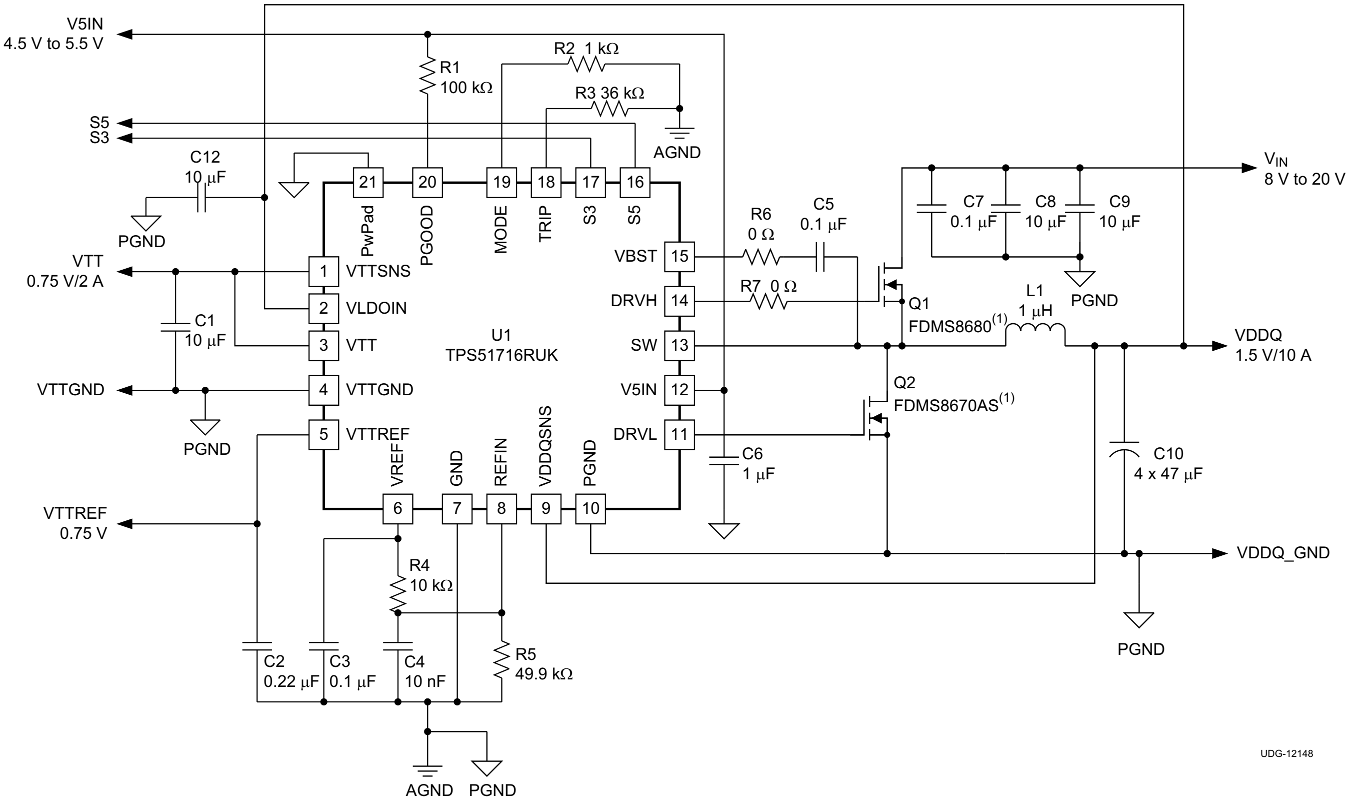
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPS51716 is typically used as step down converters, which converts a voltage from 3V- 28V to 0.7 V to 1.8 V output voltage and provide a total solution to memory system.

8.2 Typical Application



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(1) TI NexFET™ power MOSFETs are available and can be used in this application. Please contact your local TI representative.

Figure 25. DDR3, DCAP-2 500-kHz Application Circuit, Tracking Discharge

Table 3. DDR3, DCAP-2 500-kHz Application Circuit, List of Materials

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURE	PART NUMBER
C8, C9	2	10 µF, 25 V	Taiyo Yuden	TMK325BJ106MM
C10	4	47 µF, 6.3 V	TDK	C2012X5R0J476M
L1	1	1 µH, 18.5 A, 2.3 mΩ	NEC Tokin	MPC1055L1R0C
Q1	1	30 V, 35 A, 8.5 mΩ	Fairchild	FDMS8680
Q2	1	30 V, 42 A, 3.5 mΩ	Fairchild	FDMS8670AS

8.2.1 Design Requirements

To begin the design process, the user must know a few application parameters (see Table 4).

Table 4. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	8 to 20 V
Output voltage	1. 5 V
Transient response, 1.5-A load step	∆Vout = ±5%
Input ripple voltage	400 mV
Output ripple voltage	40 mV
Output current rating	10A
Operating frequency	670 kHz/ 500 kHz

8.2.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS51716.

8.2.2.1 External Components Selection

The external components selection is a simple process.

1. Determine the value of R1 and R2

   The output voltage is determined by the value of the voltage-divider resistor, R1 and R2. R1 is connected between VREF and REFIN pins, and R2 is connected between the REFIN pin and GND. Setting R1 to 10-kΩ is a good starting point. Determine R2 using Equation 5.

   $$R2 = \frac{R1}{\left(\frac{1.8}{V_{OUT} - \frac{V_{OUT(ripple)}}{2}}\right) - 1} \qquad (5)$$

   For an application using organic semiconductor capacitor(s) or specialty polymer capacitor(s) for the output capacitor(s), the output voltage ripple can be calculated as shown in Equation 6.

   $$V_{OUT(ripple)} = I_{IND(ripple)} \times ESR \qquad (6)$$

   For an application using ceramic capacitor(s) as the output capacitor(s), the output voltage ripple can be calculated as shown in Equation 7.

   $$V_{OUT(ripple)} = \frac{I_{IND(ripple)}}{8 \times C_{OUT} \times f_{SW}} \qquad (7)$$

2. Choose the inductor

   The inductance value should be determined to yield a ripple current of approximately ¼ to ½ of maximum output current. Larger ripple current increases output ripple voltage and improves the signal-to-noise ratio and helps stable operation.

   $$L_X = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{O(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \qquad (8)$$

   The inductor needs a low direct current resistance (DCR) to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 9.

   $$I_{IND(peak)} = \frac{R_{TRIP} \times I_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \qquad (9)$$

3. Choose the OCL setting resistance, R_{TRIP}

   Combining Equation 1 and Equation 2, R_{TRIP} can be obtained using Equation 10.

$$R_{TRIP} = \frac{8 \times \left(I_{OCL} - \left(\frac{(V_{IN} - V_{OUT})}{(2 \times L_X)} \right) \times \frac{V_{OUT}}{(f_{SW} \times V_{IN})} \right) \times R_{DS(on)}}{I_{TRIP}} \tag{10}$$

4. Choose the output capacitors

   Determine output capacitance to meet small signal stability as shown in Equation 11.

$$\frac{R_C \times C_C}{2\pi \times G \times L_X \times C_{OUT}} \le \frac{f_{SW}}{3} \tag{11}$$

where

- $R_C \times C_C$ time constant is 23 µs for 500 kHz operation (or 14.6 µs for 670-kHz operation)
- $G = 0.25$

8.2.3 Application Curves

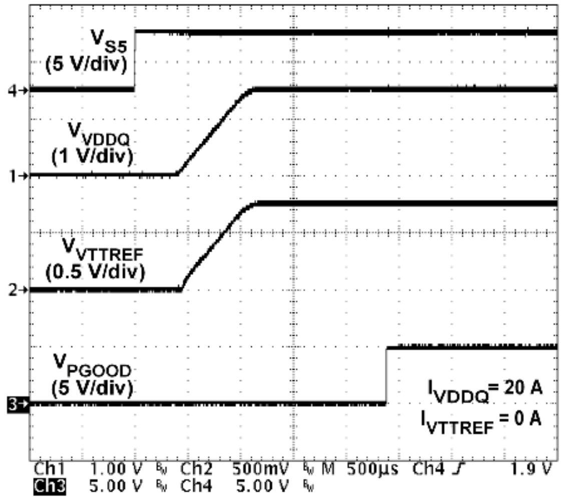

Figure 26. 1.5-V Startup Waveforms

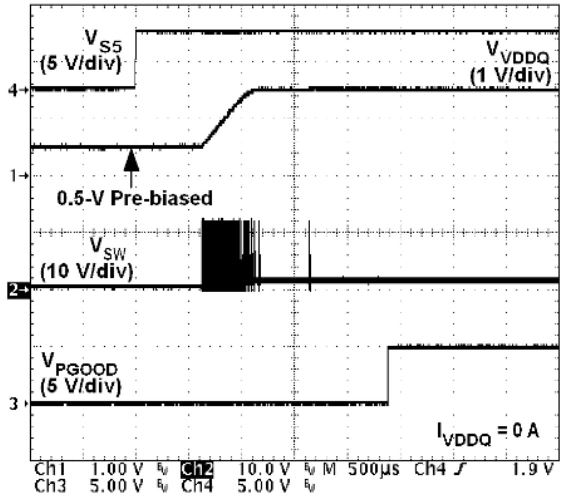

Figure 27. 1.5-V Startup Waveforms (0.5-V Pre-Biased)

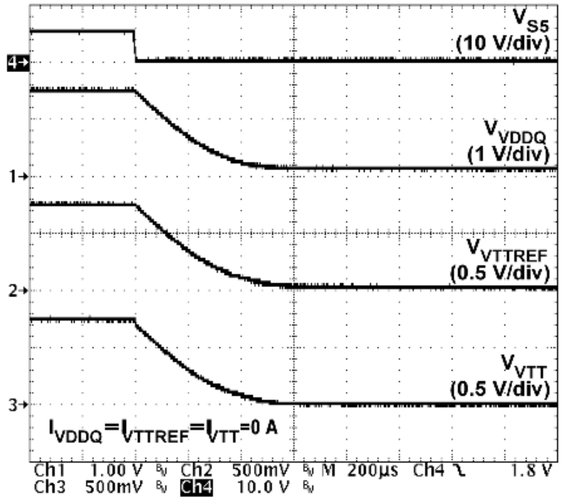

Figure 28. 1.5-V Soft-Stop Waveforms (Tracking Discharge)

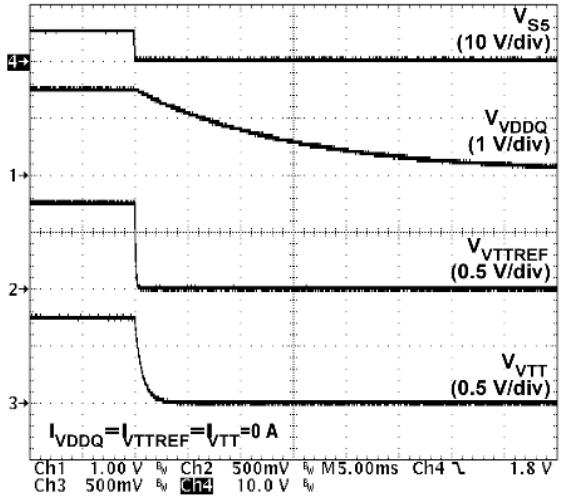

Figure 29. 1.5-V Soft-Stop Waveforms (Non-Tracking Discharge)

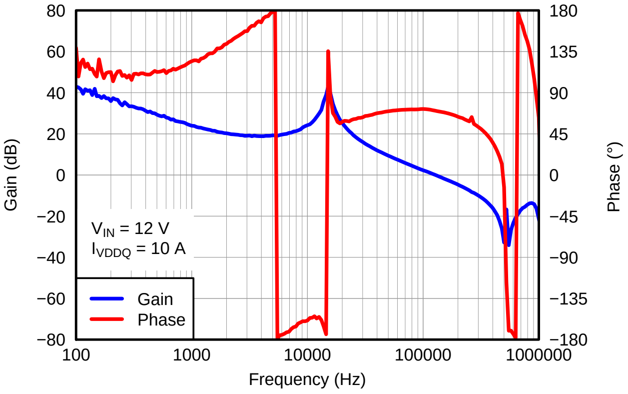

Figure 30. VDDQ Bode Plot

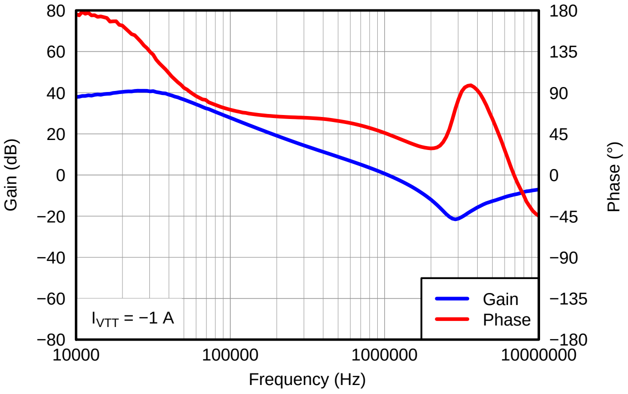

Figure 31. VTT Bode Plot (Sink)

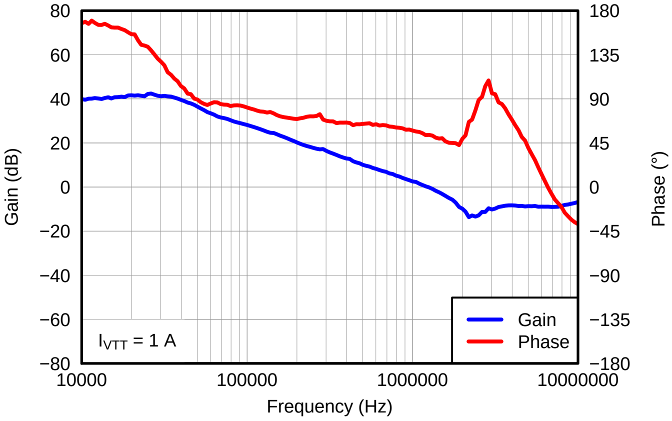

Figure 32. VTT Bode Plot (Source)

9 Power Supply Recommendations

The TPS51367 is designed to operate from input supply voltage in the range of 3 V to 28 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is V_O / 0.75.

10 Layout

10.1 Layout Guidelines

Certain issues must be considered before designing a layout using the TPS51716.

- VIN capacitor(s), VOUT capacitor(s) and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner system GND plane should be inserted, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VDDQSNS, VTTSNS, MODE, REFIN, VREF and TRIP should be placed away from high-voltage switching nodes such as SW, DRVL, DRVH or VBST to avoid coupling. Use internal layer(s) as system GND plane(s) and shield feedback trace from power traces and components.
- The DC/DC converter has several high-current loops. The area of these loops should be minimized in order to suppress generating switching noise.
  - The most important loop to minimize the area of is the path from the VIN capacitor(s) through the high and low-side MOSFETs, and back to the negative node of the VIN capacitor(s). Connect the negative node of the VIN capacitor(s) and the source of the low-side MOSFET as close as possible. (Refer to loop #1 of Figure 33)
  - The second important loop is the path from the low-side MOSFET through inductor and VOUT capacitor(s), and back to source of the low-side MOSFET. Connect the source of the low-side MOSFET and negative node of VOUT capacitor(s) as close as possible. (Refer to loop #2 of Figure 33)
  - The third important loop is of gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from V5IN capacitor through gate driver and the low-side MOSFET, and back to negative node of the capacitor. To turn off the low-side MOSFET, high current flows from gate of the low-side MOSFET through the gate driver and PGND pin, and back to source of the low-side MOSFET. Connect negative node of V5IN capacitor, source of the low-side MOSFET and PGND pin as close as possible. (Refer to loop #3 of Figure 33)
- Connect negative nodes of the VTTREF output capacitor, VREF capacitor and REFIN capacitor and bottom-side resistance of VREF voltage-divider to GND pin as close as possible. The negative node of the VTT output capacitor(s), VTTGND, GND and PGND pins should be connected to system GND plane near the device as shown in Figure 33.
- Because the TPS51716 controls output voltage referring to voltage across VOUT capacitor, VDDQSNS should be connected to the positive node of VOUT capacitor using different trace from that for VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise generative lines. GND pin refers to the negative node of VOUT capacitor.
- Connect the overcurrent setting resistor from TRIP pin to GND pin and make the connections as close as possible to the device to avoid coupling from a high-voltage switching node.
- Connect the frequency and mode setting resistor from MODE pin to GND pin ground, and make the connections as close as possible to the device to avoid coupling from a high-voltage switching node.
- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace and via(s) of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as SW node, which connects to the source of the high-side MOSFET, the drain of the low-side MOSFET and the high-voltage side of the inductor, should be as short and wide as possible.
- VLDOIN should be connected to VOUT with short and wide traces. An input bypass capacitor should be placed as close as possible to the pin with short and wide connections. The negative node of the capacitor should be connected to system GND plane.
- The output capacitor for VTT should be placed close to the pins with a short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- VTTSNS should be connected to the positive node of the VTT output capacitor(s) using a separate trace from the high-current power line. When remote sensing is required attach the output capacitor(s) at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between GND pin and the output capacitor(s).
- Consider adding a low pass filter (LPF) at VTTSNS in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ.

Layout Guidelines (continued)

- In order to effectively remove heat from the package, prepare a thermal land and solder to the package thermal pad. Wide trace of the component-side copper, connected to this thermal land, helps heat spreading. Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to help dissipation. The thermal land can be connected to either AGND or PGND but is recommended to be connected to PGND, the system GND plane(s), which has better heat radiation.

10.2 Layout Example

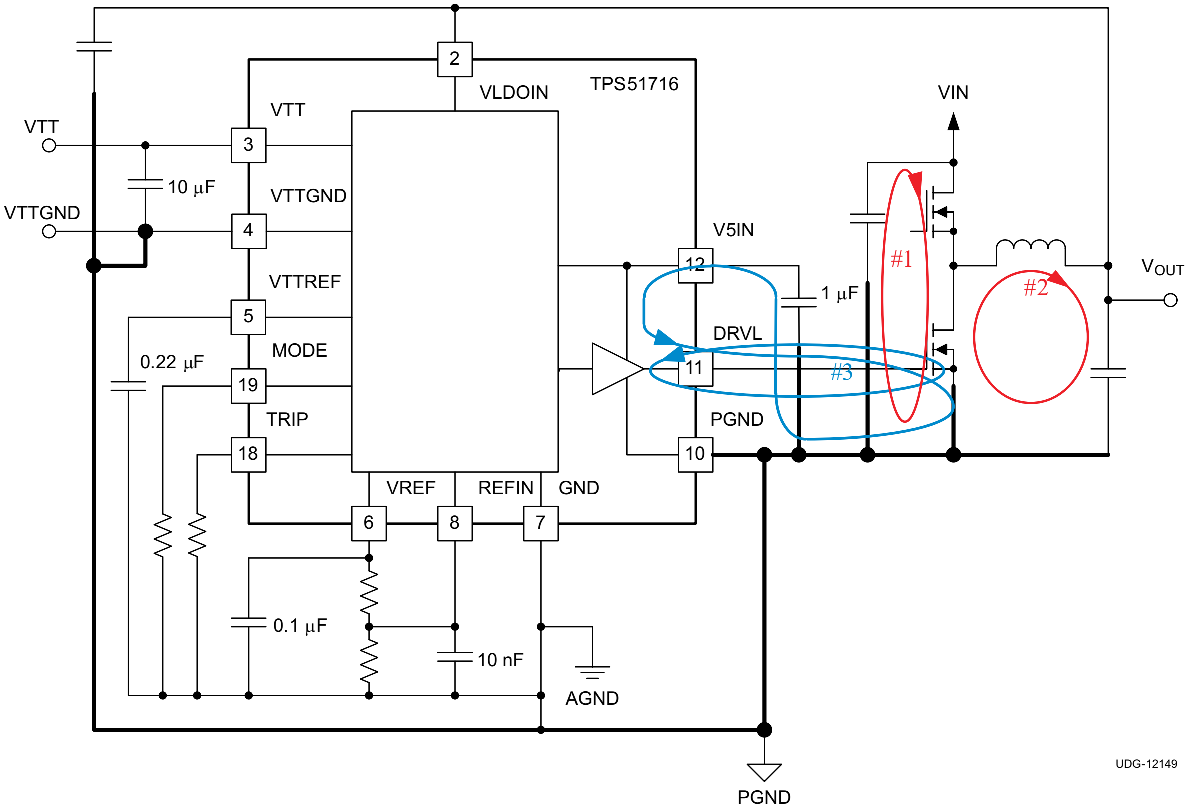

Figure 33. DC/DC Converter Ground System

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

D-CAP2, NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51716RUKR	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	51716	Samples
TPS51716RUKT	ACTIVE	WQFN	RUK	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	51716	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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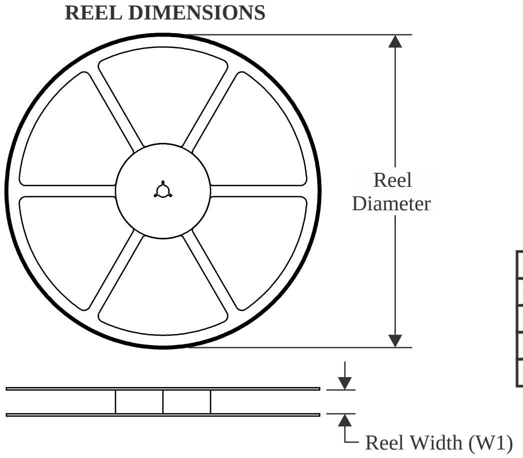
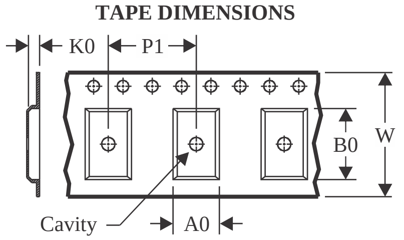
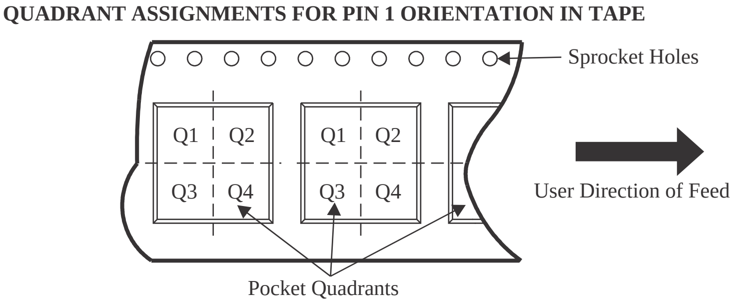
TAPE AND REEL INFORMATION





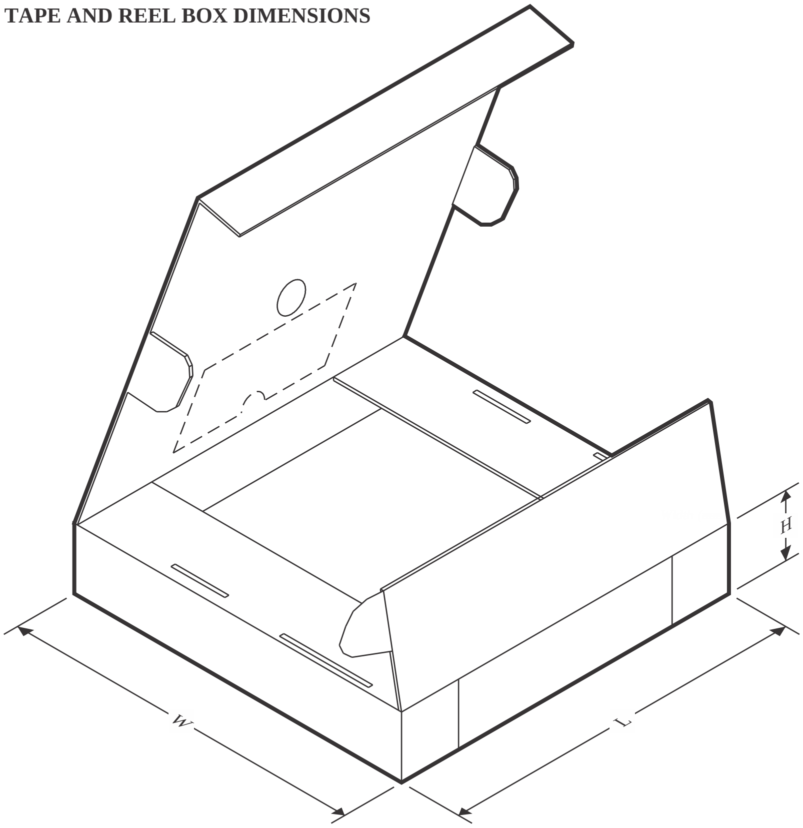
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51716RUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51716RUKT	WQFN	RUK	20	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

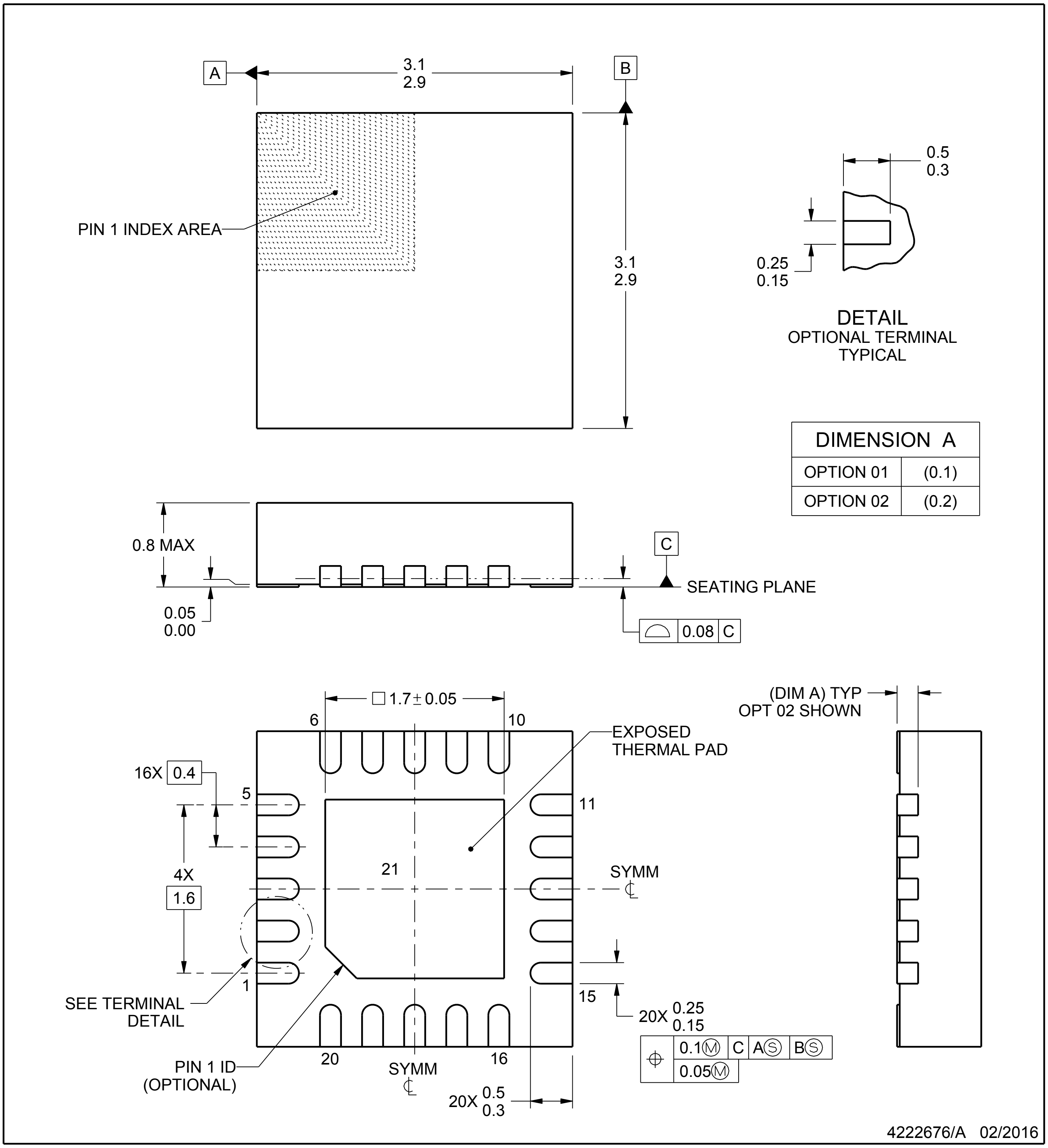
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51716RUKR	WQFN	RUK	20	3000	338.0	355.0	50.0
TPS51716RUKT	WQFN	RUK	20	250	205.0	200.0	33.0

PACKAGE OUTLINE

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

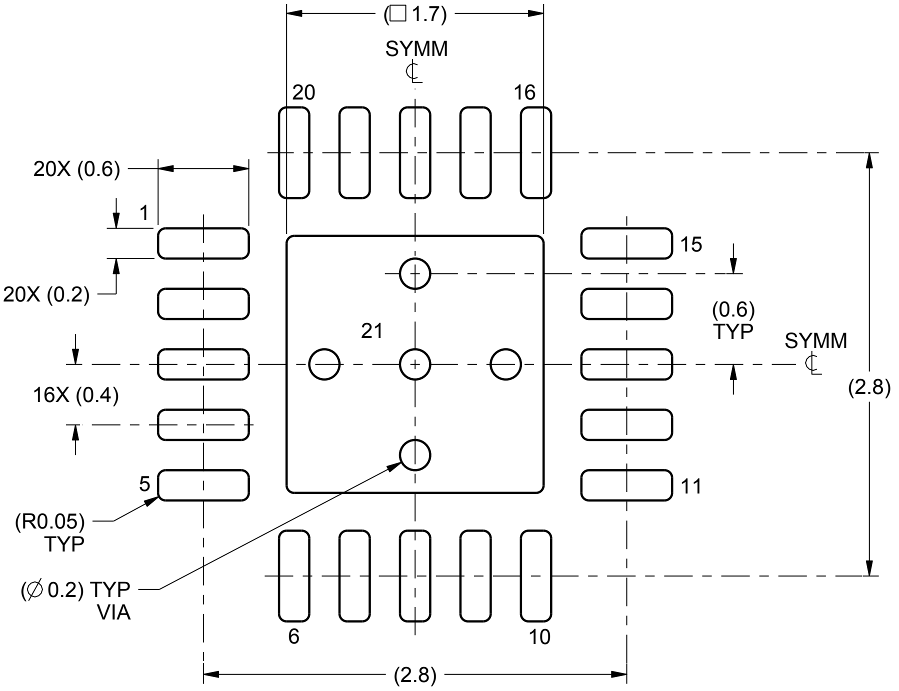


DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)

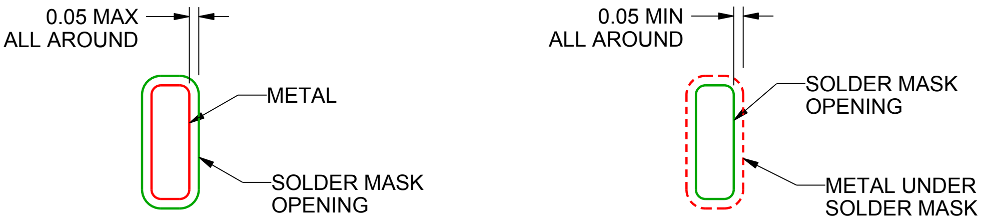
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
SCALE:20X



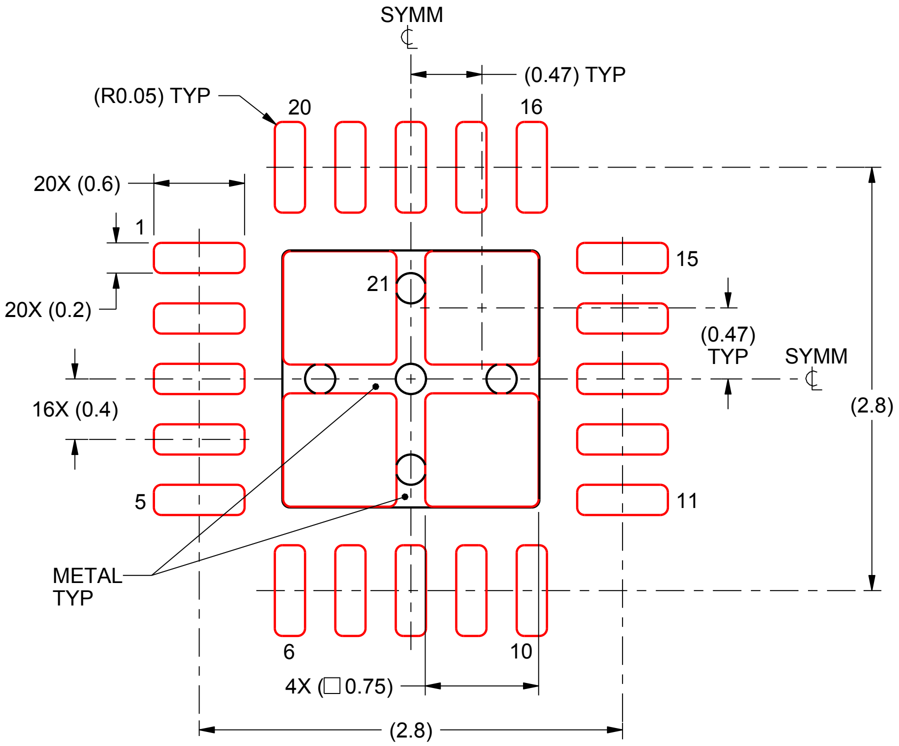
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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