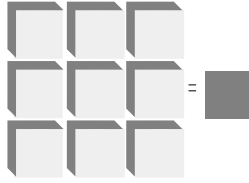


LSI/CSI



LS6511N LS6512 LS6513



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PIR SENSOR INTERFACE

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FEATURES:

- Direct Interface with PIR Sensor
- Two-Stage Differential Amplifier
- Amplifier Gain and Bandwidth externally controlled
- True and Complementary Output Drives
- Separate digital filters for processing positive and negative input signals
- Single Pulse/Dual Pulse/ Concurrent Pulse Detection
- Adjustable Output Pulse Width
- Optional 5V Shunt Regulator Output
- 75 μ A Typical Supply Current
- Undervoltage Detection
- **LS6511N**(DIP); **LS6511N-S** (SOIC) - See Figure 1A
- **LS6512**(DIP); **LS6512-S** (SOIC) - See Figure 1A
- **LS6513**(DIP); **LS6513-S** (SOIC) - See Figure 1B

APPLICATIONS:

Security system intrusion detection, automatic doors, motion triggered events such as remote animal photography, etc.

DESCRIPTION (See Figure 5)

The **LS6511N**, **LS6512** and **LS6513** are CMOS integrated circuits designed for detecting motion from a PIR Sensor and initiating appropriate responses.

DIFFERENTIAL AMPLIFIER

Each stage of the two stage Differential Amplifier can be set to have its own amplification and bandwidth. The two inputs to the first stage allow for single-ended or differential connection to PIR Sensors. This stage can be biased anywhere in its dynamic range. The second stage is internally biased so that the Window Comparator's lower and higher thresholds can be fixed relative to this bias. Signal levels as low as 100 μ V can be detected.

WINDOW COMPARATOR

The Window Comparator provides noise filtering by enabling only those signals equal to or greater than a fixed threshold at the output of the Differential Amplifier to appear at the 2 outputs of the Window Comparator. One output detects positive input signals while the other output detects negative input signals.

COMPARATOR DIGITAL FILTER

The outputs of the Window Comparator are filtered so that motion must be present for a certain duration before it can be recognized and appear as pulses at the Digital Filter outputs. An external RC network sets the duration time. Nominal duration is 50ms.

MODE SELECT

A tristate input pin selects how the detected signals are processed. Single Pulse (SP) Mode is when detection from either a positive or negative input signal at the Digital Filter outputs will cause an LED / RELAY output to occur. Concurrent Pulse (CP) Mode is when detection from a positive and negative input signal must occur within a specific time before an output will occur. Dual Pulse (DP) mode is when any two detections within a specific time will cause an output to occur. SP Mode = 0; CP Mode = Open; DP Mode = 1.

PROGRAMMABLE RETRIGGERABLE ONE-SHOTS

Positive and negative input signals at the digital filter outputs will generate retriggerable one-shot pulses. In the Concurrent Pulse Mode, outputs from each one-shot must occur together at some point in time to cause an output to occur. The one-shot pulse width is programmable using an external RC network. Typical pulse widths used vary between 1 and 12 seconds.

WINDOW TIMER

In the Dual Pulse Mode any two detections must occur within a timing window to cause an output to occur. The timing window is programmable using an external RC network. Typical windows are between 1 and 5 seconds.

ENABLE Input

A low on the Enable input for **LS6513** allows the LED / Relay and LED / Relay outputs to respond to the PIR input detection. If the Enable input is high, then the two outputs remain in their dormant state. The LED / Relay and LED / Relay outputs on **LS6511N** and **LS6512** are always enabled.

SEL UDV Input

For the **LS6513**, a low on this input allows undervoltage to be detected. If left floating, undervoltage detection will not occur.

OUTPUT DURATION TIMER

The duration timer is retriggerable and programmable using an external RC network. Typical duration times are between 0.5 and 15 seconds. Successive input detections will restart the timer.

OUTPUTS

The LED / RELAY Output is an open drain output that will sink current when an input signal is detected and processed. The **LS6511N** will also sink current when the Power Supply drops below 3.5V (Typical) (Undervoltage Detection). The Undervoltage Detection will be removed when the Power Supply rises above 3.7V (Typical). The LED / RELAY Output performs identically but is opposite in polarity. The output can sink current from a relay coil returned to a positive voltage (V_{DD} to 15V maximum). The **LS6512** will not respond to an undervoltage detection. The **LS6513** can be selected to respond or not respond to a power supply undervoltage.

The undervoltage detection feature in the **LS6511N** assures that in security systems tampering with the power supply by loading it and causing it to be reduced in value will be quickly detected.

In battery operated non-security systems applications the undervoltage feature is not desirable because it produces unwanted outputs as the batteries age. The **LS6512** should be selected for these applications.

SHUNT REGULATOR

The **LS6511N** includes a 5V Shunt Regulator Output which can be tied to the V_{DD} Pin so that the circuit can be powered from a higher voltage power supply.

Note: See Figures 2, 3 and 4 for application schematics.

PIN ASSIGNMENT - TOP VIEW

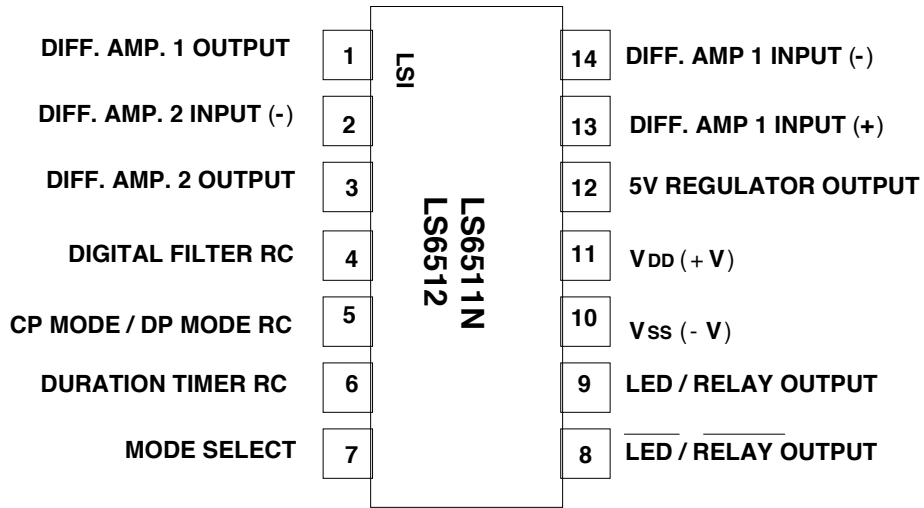


FIGURE 1A

PIN ASSIGNMENT - TOP VIEW

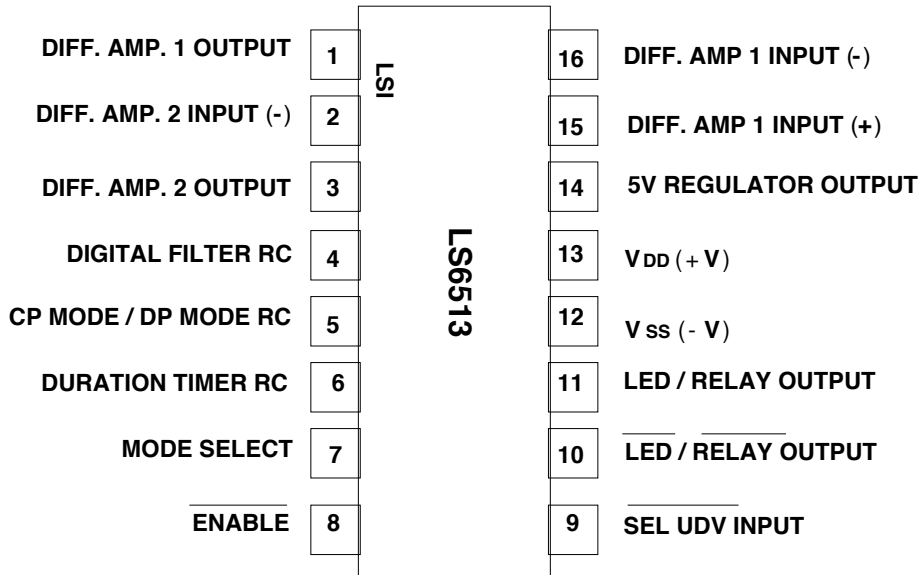


FIGURE 1B

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.

ABSOLUTE MAXIMUM RATINGS:

| PARAMETER | SYMBOL | VALUE | UNIT |
|-----------------------|-----------|------------------------|------|
| DC supply voltage | VDD - VSS | +7 | V |
| Any input voltage | VIN | VSS - 0.3 to VDD + 0.3 | V |
| Operating temperature | TA | -40 to +85 | °C |
| Storage temperature | TSTG | -65 to +150 | °C |

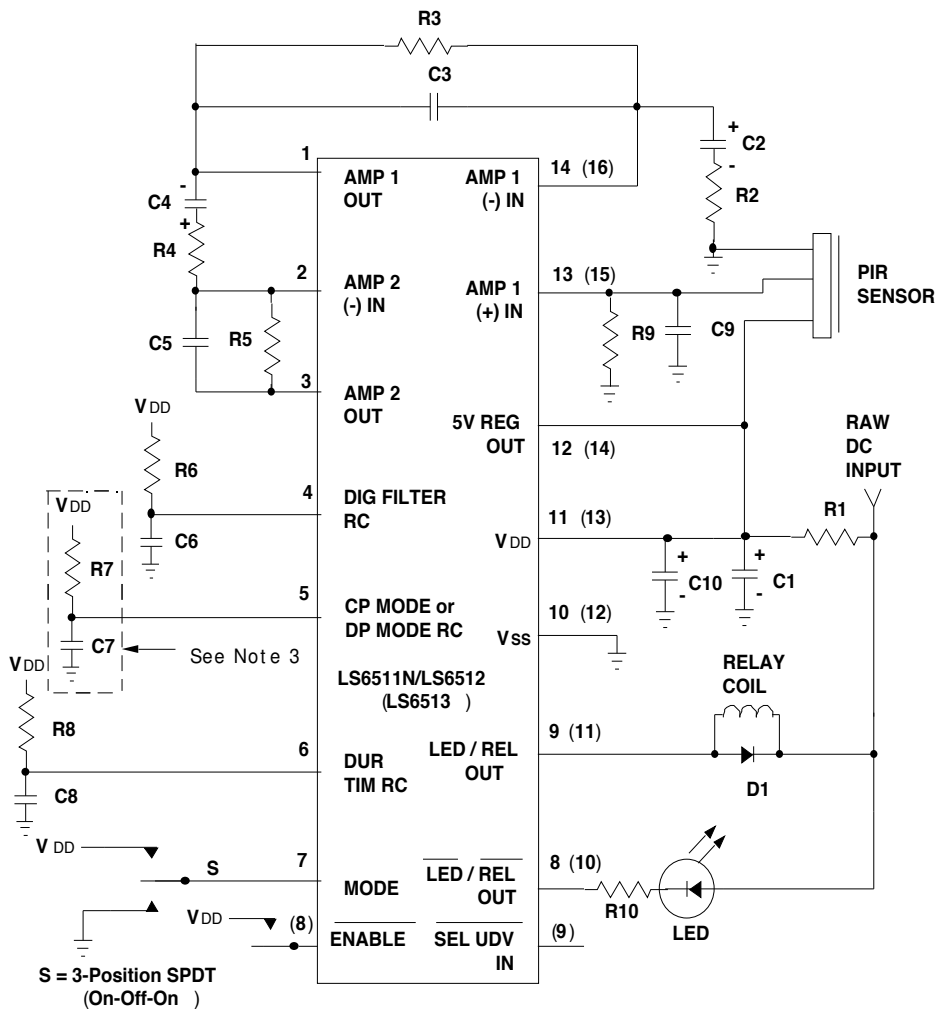
ELECTRICAL CHARACTERISTICS:

(All voltages referenced to VSS, TA = -40°C to +55°C, 4.5V ≤ VDD ≤ 6.5V, unless otherwise specified.)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | CONDITIONS |
|-----------------------------------------------------------------------------------------------------------------------------------------|--------|------|------------|------|-------|-----------------------------------------------------------------------------|
| SUPPLY CURRENT: | | | | | | |
| VDD = 5V | IDD | - | 75 | 100 | μA | LED/RELAY, LED/RELAY |
| VDD = 4.5V - 6.5V | IDD | - | 125 | 160 | μA | and REGULATOR outputs not loaded |
| REGULATOR: | | | | | | |
| Voltage | VR | - | 5 | - | V | - |
| Current | IR | - | - | 15 | mA | - |
| UNDERVOLTAGE: | | | | | | |
| DETECTION | UDV | 2.9 | 3.5 | 4.1 | V | } LS6511N |
| RECOVERY | URV | 3.05 | 3.7 | 4.4 | V | } LS6513 |
| MIN. OPERATING VOLTAGE | VDM | - | - | 3.0 | V | } LS6512 } LS6513 |
| DIFFERENTIAL AMPLIFIERS: | | | | | | |
| Open Loop Gain, Each Stage | G | 70 | - | - | dB | - |
| Common Mode Rejection Ratio | CMRR | 60 | - | - | dB | - |
| Power Supply Rejection Ratio | PSRR | 60 | - | - | dB | - |
| Input Sensitivity (Minimum Detectable Voltage to first amplifier when both amplifiers are cascaded for a net gain of 8,000) | VS | 100 | - | - | μVp-p | TA = 25°C, with Amplifier Bandpass configuration as shown in Figure 3 |
| Input Dynamic Range | - | 0 | - | 1.75 | V | - |
| Diff. Amp 2 Internal Reference | VIR | - | 0.35VDD | - | V | - |
| COMPARATOR: | | | | | | |
| Lower Reference | VTHL | - | VIR - 0.5V | - | V | At VDD = 5.0V |
| Higher Reference | VTHH | - | VIR + 0.5V | - | V | At VDD = 5.0V |
| DIGITAL FILTER: | | | | | | |
| For 50ms Filter Time | RDF | - | 2.2 | - | MΩ | - |
| | CDF | - | 0.01 | - | μF | - |
| ONE SHOT | | | | | | |
| (1 Second) | ROS | - | 2.2 | - | MΩ | - |
| | COS | - | 0.22 | - | μF | - |
| WINDOW TIMER | | | | | | |
| (2.5 Second) | RWT | - | 2.2 | - | MΩ | - |
| | CWT | - | 0.68 | - | μF | - |
| Concurrent Pulse Window | TCP | - | 1 | - | sec | RCP ≤ 2.2MΩ } CCP = 0.22μF } } Pin 5 |
| Dual Pulse Window | TDP | - | 2.5 | - | sec | RDP = 2.2MΩ } CDP = 0.68μF } |
| DURATION TIMER | TDT | - | 4 | - | sec | RDT = 2.2MΩ } Pin 6 CDT = 0.68μF } |
| OUTPUT DRIVE CURRENT | | | | | | |
| (Vo = 0.5V Max.) | Io | -20 | - | - | mA | VDD = 5V |
| | Io | -10 | - | - | mA | VDD = VDM |

FIGURE 2. TYPICAL RELAY APPLICATION

NOTE 1: The relay coil is normally energized and the LED is off. When an alarm occurs, the relay coil becomes de-energized and the LED is turned on.



- R1 = See NOTE 2
- R2 = 36kΩ
- R3 = 1.5MΩ
- R4 = 36kΩ
- R5 = 1.5MΩ
- R6 = 2.2MΩ (Typical)
- R7 = 2.2MΩ (Typical)
- R8 = 2.2MΩ (Typical)
- R9 = 36kΩ
- R10 = 2.2kΩ (Typical)

- C1 = 100μF
- C2 = 10μF
- C3 = 0.003μF
- C4 = 10μF
- C5 = 0.003μF
- C6 = 0.01μF (Typical)
- C7 = 0.22μF (CP Mode; Typical)
- C7 = 0.68μF (DP Mode; Typical)
- C8 = 0.22μF (Typical)
- C9 = 0.1μF
- C10 = 0.1μF
- D1 = 1N4001
- Relay = No typical P/N

PIR = Perkin-Elmer LHi 958, 978 (Typical)
 Nicera RE200B, SDA02-54 (Typical)

All Resistors 1/4W. All Capacitors 10V.

NOTE 2: R1 is selected to provide sufficient current to drive the LS6511N and PIR Sensor. Any surplus current is available to drive additional loads applied to the 5V Shunt Regulator output or is absorbed by the 5V Shunt Regulator. Refer to specifications for current limits.

NOTE 3: In SP Mode, R7 and C7 are not used and Pin 5 is tied to Vss.

NOTE 4: Adjust the value of R9 if the selected PIR Sensor causes the input static voltage at Pin 13 to be out of the Input Dynamic Range of 0V to 1.75V. (See Electrical Characteristics on Page 2)

NOTE 5: Sensitivity can be adjusted to a lower value by increasing the value of R2 or R4 or by decreasing the value of R3 or R5.

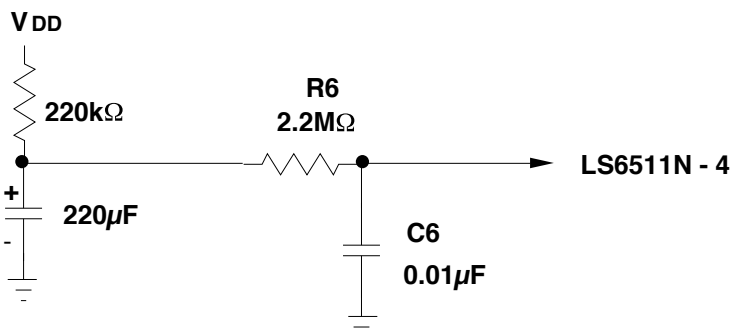
NOTE 6: Pins shown in parentheses and connections shown by broken lines are for LS6513 only.

NOISE CONSIDERATIONS

Layout of any circuit using a high-gain PIR amplifier is critical. The PIR amplifier components should be located close to the amplifier pins on the chip in order to minimize noise pickup. The oscillator and relay drive components should be located away from the amplifier components.

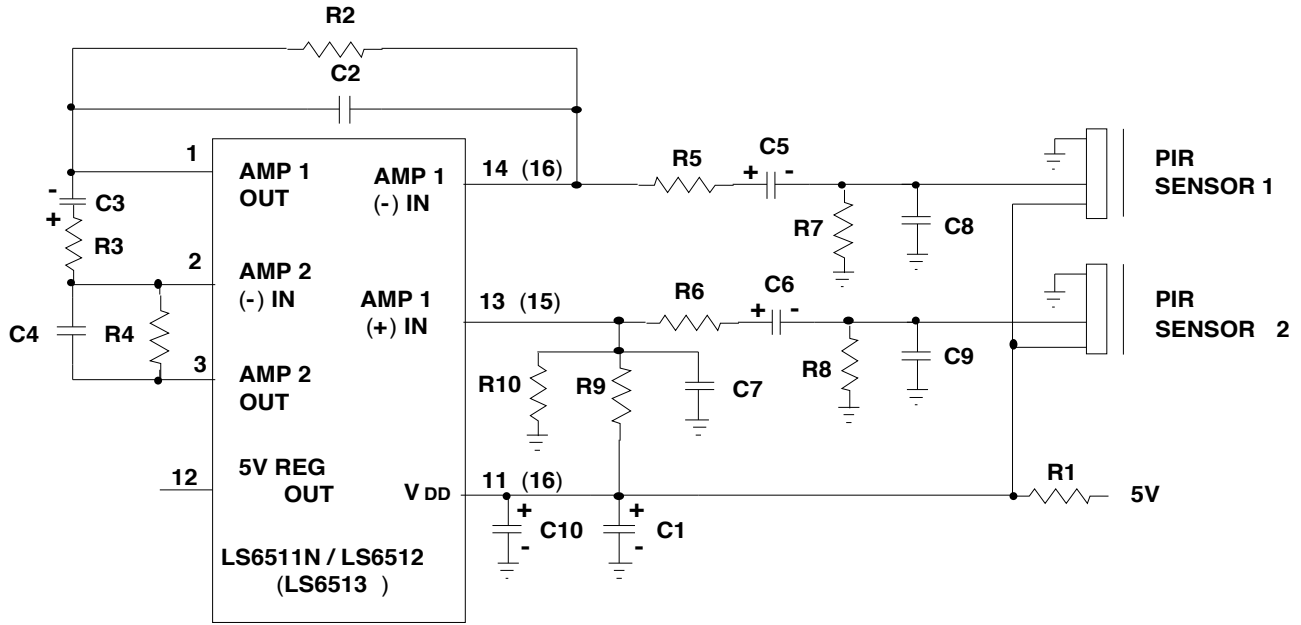
Other steps that can help reduce noise is adding a ground shield backplane to the PCB and enhancing the filtering of VDD; i.e., adding a 0.1uF high frequency capacitor across C1 and increasing C1 to 220 μF.

FIGURE 3. INHIBITING OUTPUTS UPON POWER TURN-ON



Using the typical application circuit as shown in Figure 2, the Outputs on Pins 8 and 9 occur on power-up because of the large settling time in the amplifier stages. In applications where this is not desirable, the digital filter oscillator must be disabled on power-up long enough to enable the PIR amplifiers to stabilize. Replacing the R6-C6 circuit shown in Figure 2 with the circuit shown in Figure 3 will disable the digital filter oscillator until the voltage across the 220μF capacitor reaches a value high enough for the oscillator to begin oscillating. Component values that can be changed to speed up stabilization include C2, C3, C4 and C5. C3 and C5 become 0.001μF and C2 and C4 become 10μF.

FIGURE 4. DIFFERENTIAL INTERFACE TO PIR SENSOR PAIR



| | | | |
|------------|-------------|--------------|-------------|
| R1 = 1kΩ | R6 = 36kΩ | C1 = 100μF | C6 = 10μF |
| R2 = 1.5MΩ | R7 = 36kΩ | C2 = 0.003μF | C7 = 0.01μF |
| R3 = 36kΩ | R8 = 36kΩ | C3 = 10μF | C8 = 0.1μF |
| R4 = 1.5MΩ | R9 = 5.6MΩ | C4 = 0.003μF | C9 = 0.1μF |
| R5 = 36kΩ | R10 = 2.4MΩ | C5 = 10μF | C10 = 0.1μF |

PIRs = **Perkin-Elmer** LHi 954, 958, 978; **Nicera** RE200B, SDA02-54 (Typical)

All Resistors 1/4 W. All Capacitors 10V.

- NOTES:** 1) A pair of PIR Sensors may be used in applications where a wider optical field of view is needed.
 2) External 5V Regulator drives the LS6511N and PIR sensor.

FIGURE 5. BLOCK DIAGRAM

