

# PHD96NQ03LT

## N-channel TrenchMOS logic level FET

Rev. 06 — 15 March 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge

### 1.3 Applications

- DC-to-DC convertors

### 1.4 Quick reference data

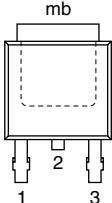
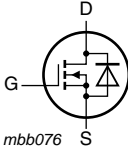
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	25	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V};$ see <a href="#">Figure 1</a> and <a href="#">3</a>	-	-	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	115	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 5\text{ V}; I_D = 50\text{ A};$ $V_{DS} = 15\text{ V}; T_j = 25\text{ °C};$ see <a href="#">Figure 11</a>	-	8.4	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 9</a>	-	4.2	4.95	m $\Omega$
		$V_{GS} = 5\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	5.6	7.5	m $\Omega$



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT428 (DPAK)</p>	 <p>mbb076</p>
2	D	drain <a href="#">[1]</a>		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

## 3. Ordering information

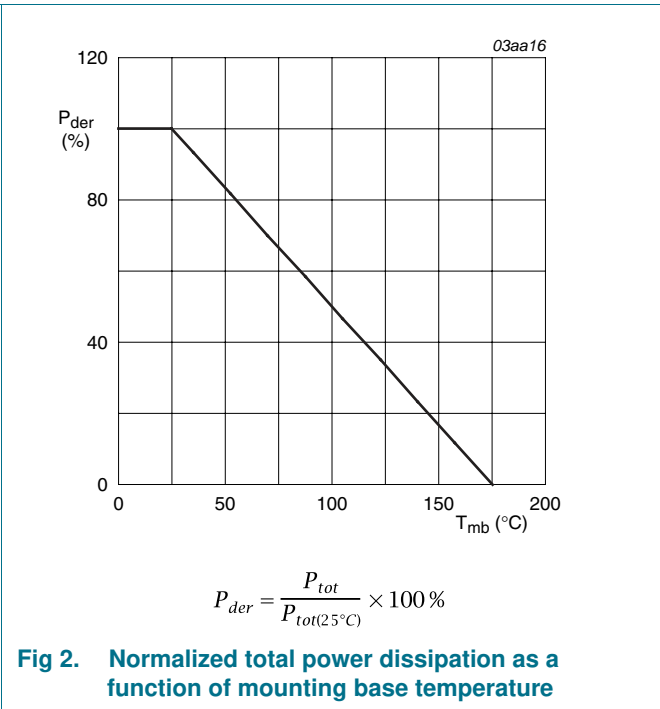
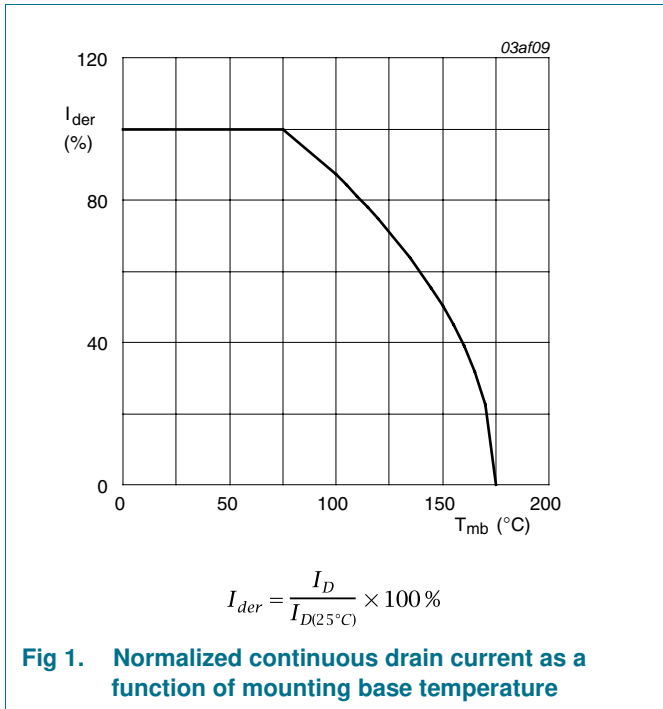
Table 3. Ordering information

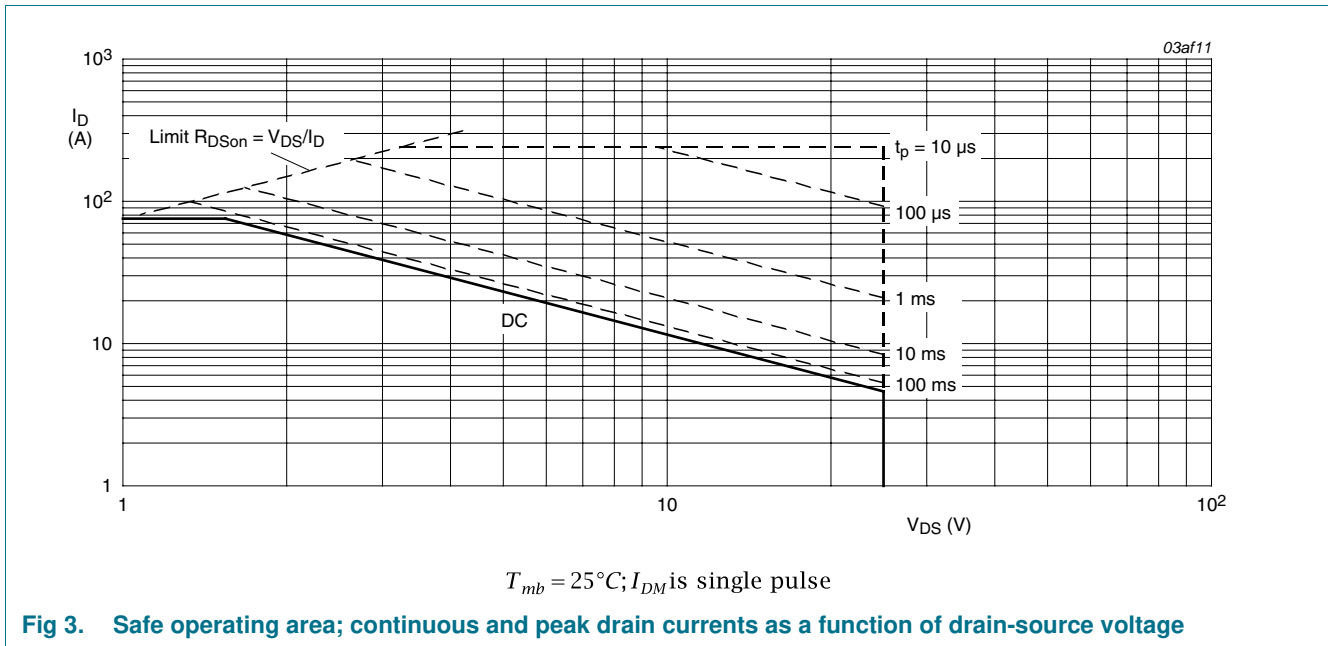
Type number	Package		Version
	Name	Description	
PHD96NQ03LT	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

### 4. Limiting values

**Table 4. Limiting values**  
 In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	25	V
V <sub>DGR</sub>	drain-gate voltage	T <sub>j</sub> ≤ 175 °C; T <sub>j</sub> ≥ 25 °C; R <sub>GS</sub> = 20 kΩ	-	25	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 100 °C; see <a href="#">Figure 1</a> V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 1</a> and <a href="#">3</a>	-	65 75	A A
I <sub>DM</sub>	peak drain current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 3</a>	-	240	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	115	W
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	75	A
I <sub>SM</sub>	peak source current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>mb</sub> = 25 °C	-	240	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = 43 A; V <sub>sup</sub> ≤ 15 V; R <sub>GS</sub> = 50 Ω; t <sub>p</sub> = 0.25 ms; unclamped	-	185	mJ
I <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche current	V <sub>GS</sub> = 10 V; V <sub>sup</sub> ≤ 15 V; R <sub>GS</sub> = 50 Ω; T <sub>j(initial)</sub> = 25 °C; unclamped	-	75	A

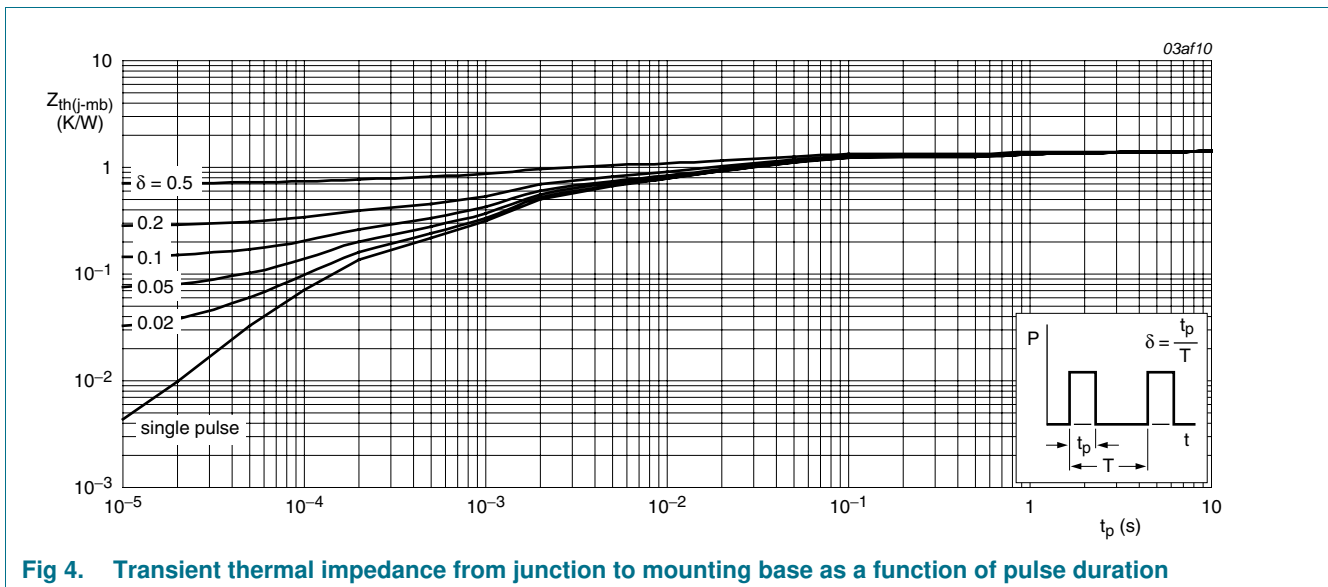




## 5. Thermal characteristics

**Table 5. Thermal characteristics**

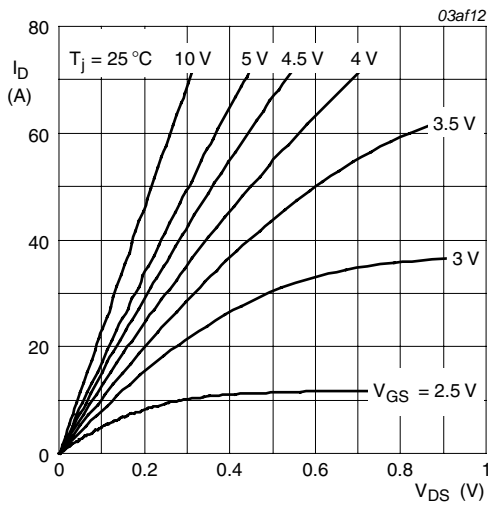
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	75	-	K/W



## 6. Characteristics

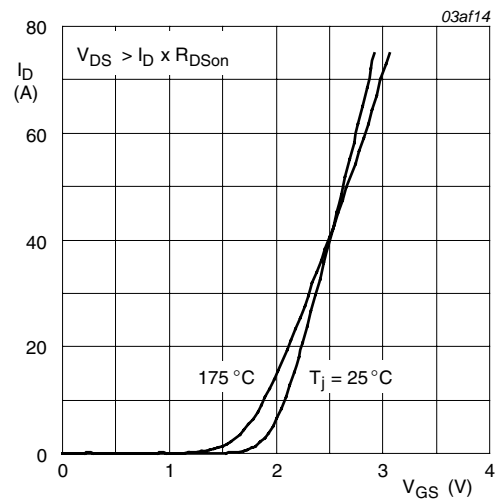
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	22	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a>	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 8</a>	1	1.5	2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	1	$\mu\text{A}$
		$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	10	13.5	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a>	-	4.2	4.95	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	5.6	7.5	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 50 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	-	26.7	-	nC
$Q_{GS}$	gate-source charge		-	8.5	-	nC
$Q_{GD}$	gate-drain charge		-	8.4	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	2200	-	pF
$C_{oss}$	output capacitance		-	725	-	pF
$C_{rss}$	reverse transfer capacitance		-	290	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 5.6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}; I_D = 12.5 \text{ A}$	-	18	-	ns
$t_r$	rise time		-	70	-	ns
$t_{d(off)}$	turn-off delay time		-	75	-	ns
$t_f$	fall time		-	70	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	0.9	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 25 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	43	-	ns
$Q_r$	recovered charge		-	40	-	nC



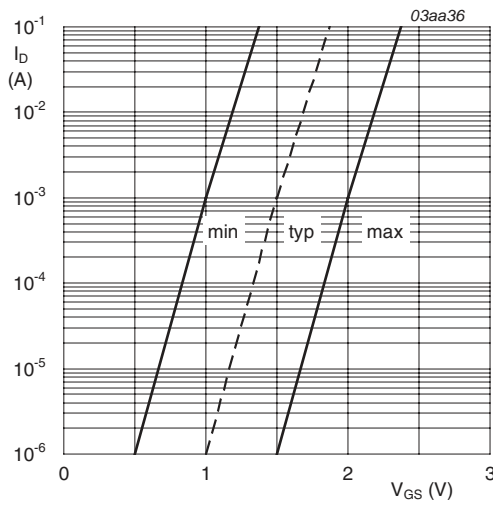
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



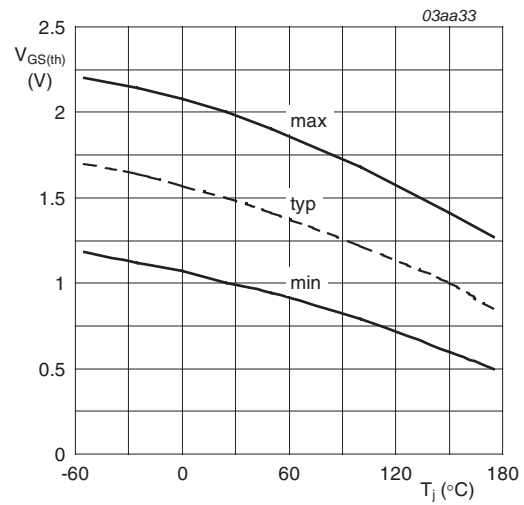
$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}; V_{DS} > I_D \times R_{DS(on)}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



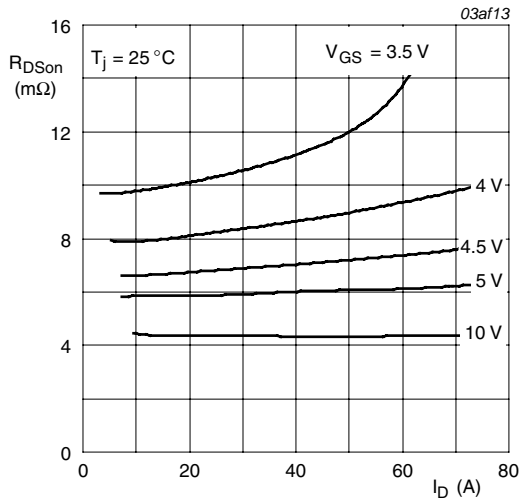
$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



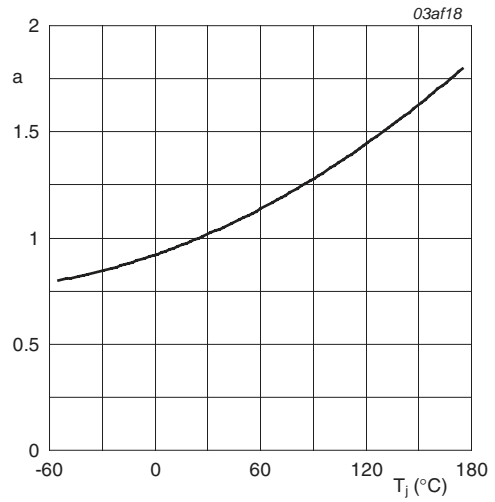
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



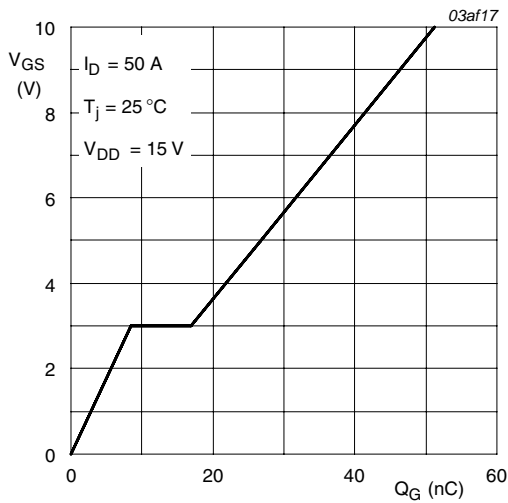
$T_j = 25^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



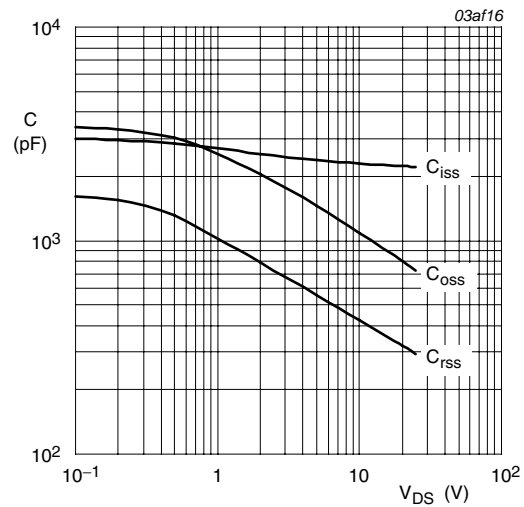
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



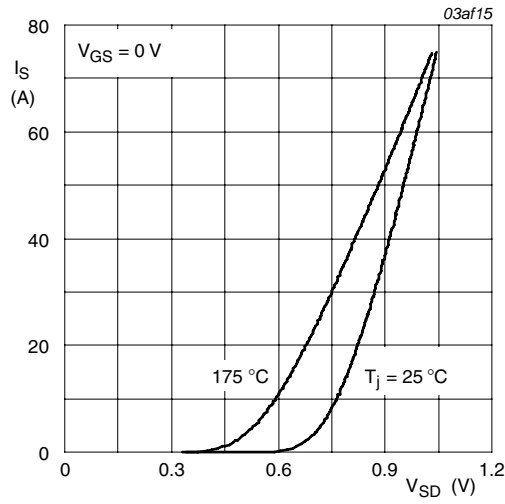
$I_D = 50\text{ A}; V_{DS} = 15\text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ C$  and  $175^\circ C; V_{GS} = 0V$

Fig 13. Source current as a function of source-drain voltage; typical values



7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

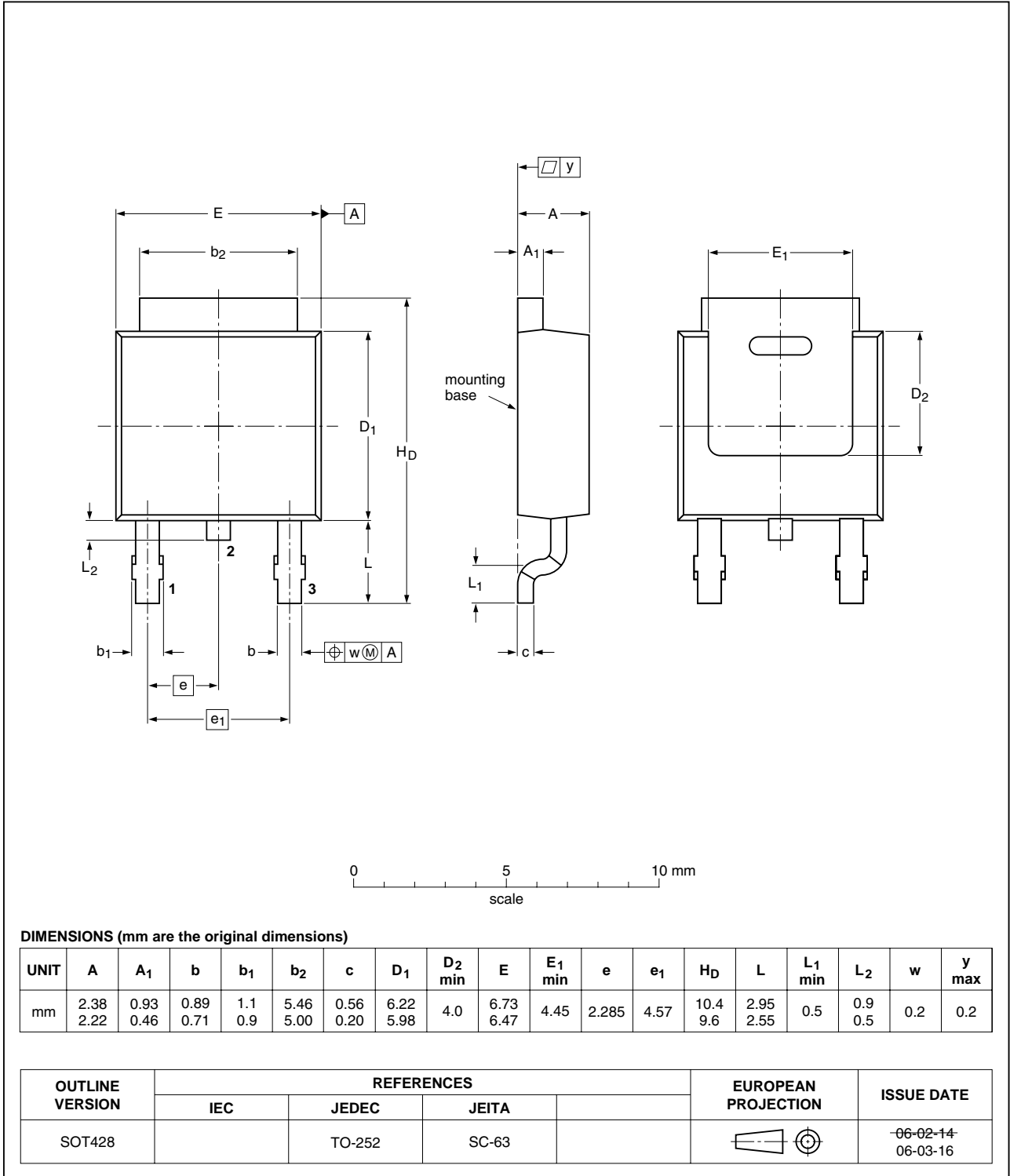


Fig 14. Package outline SOT428 (DPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD96NQ03LT_6	20100315	Product data sheet	-	PHP96NQ03LT-05
Modifications:		<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul>		
PHP96NQ03LT-05 (9397 750 09666)	20020605	Product data	-	PHP96NQ03LT-04
PHP96NQ03LT-04	20020220	Product data	-	PHP96NQ03LT-03
PHP96NQ03LT-03	20011023	Product data	-	PHP96NQ03LT-02
PHP96NQ03LT-02	20011008	Product data	-	PHP96NQ03LT-01
PHP96NQ03LT-01	20010716	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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