

# APDS-9702

## Signal Conditioning IC for Optical Proximity Sensors with Digital I<sup>2</sup>C Interface



### Data Sheet

#### Description

APDS-9702 is a signal conditioning IC that enhances the performance and robustness of the optical sensors used for proximity or object detection.

APDS-9702 is a single chip solution that consists of an I<sup>2</sup>C Write function, oscillation circuit, LED driver circuit and sunlight cancellation circuit integrated into a single chip. APDS-9702 has artificial light immunity and is also operational under the sun. Design flexibility is optimized as APDS-9702 can be paired up with an integrated proximity sensor or discrete pair solution.

APDS-9702 can be disabled to maximize power savings and battery life in applications such as portable or battery-operated devices. The LED current of the optical proximity sensors can be configured to different levels using a limiting resistor at the LEDA pin. APDS-9702 also provides user options in frequency, suitable burst rate, comparator threshold setting and burst off period that can reduce power consumption. These low power consumption features makes it also ideal for low power mobile and handheld devices.

APDS-9702 is capable of operating at voltage supply ranging from 2.4 V to 3.6 V. APDS-9702 has two separate output pins for analog and digital outputs. This provides flexibility to use either the analog or digital output (or both) depending on the requirements of the application.

The device is packaged in 8-pin QFN package measuring 0.55mm(H) x 2mm(W) x 2mm(L).

#### Ordering Information

Part Number	Packaging	Quantity
APDS-9702-020	Tape & Reel	2500 per reel

#### Application Support Information

The Application Engineering Group is available to assist you with the application design associated with APDS-9702 module. You can contact them through your local sales representatives for additional details.

#### Features

- Low power consumption
  - Internal oscillation circuit to drive LED in pulse mode
  - Low shut down current
  - External LED drive-current control
- Complete shutdown mode
  - Low shutdown current
- Supply voltage : 2.4 V to 3.6 V
- Operational in sunlight conditions up to 100klux(with HSDL-9100)
- Artificial light immunity
- Analog & Digital output available
  - Built in comparator for digital output
  - Digital output remains Low during object detected.
- Wide bandwidth Trans-impedance amplifier
- External capacitor and resistor for integration and gain controls
- Flexibility to enhance detection distance up to 200mm with HSDL-9100 or further with external discrete pair
- Small 2mm x 2mm QFN 8-pin package
- Design flexibility to pair with Avago Proximity Sensors or discrete pair solution
- Lead-free & RoHS Compliant

#### Applications

- PDA and mobile phones
- Digital Camera
- Portable and Handheld devices
- Personal Computers/Notebooks
- Amusement/Games/Vending Machines
- Industrial Automation
- Contactless Switches
- Sanitary Automation

# APDS-9702 Block Diagram

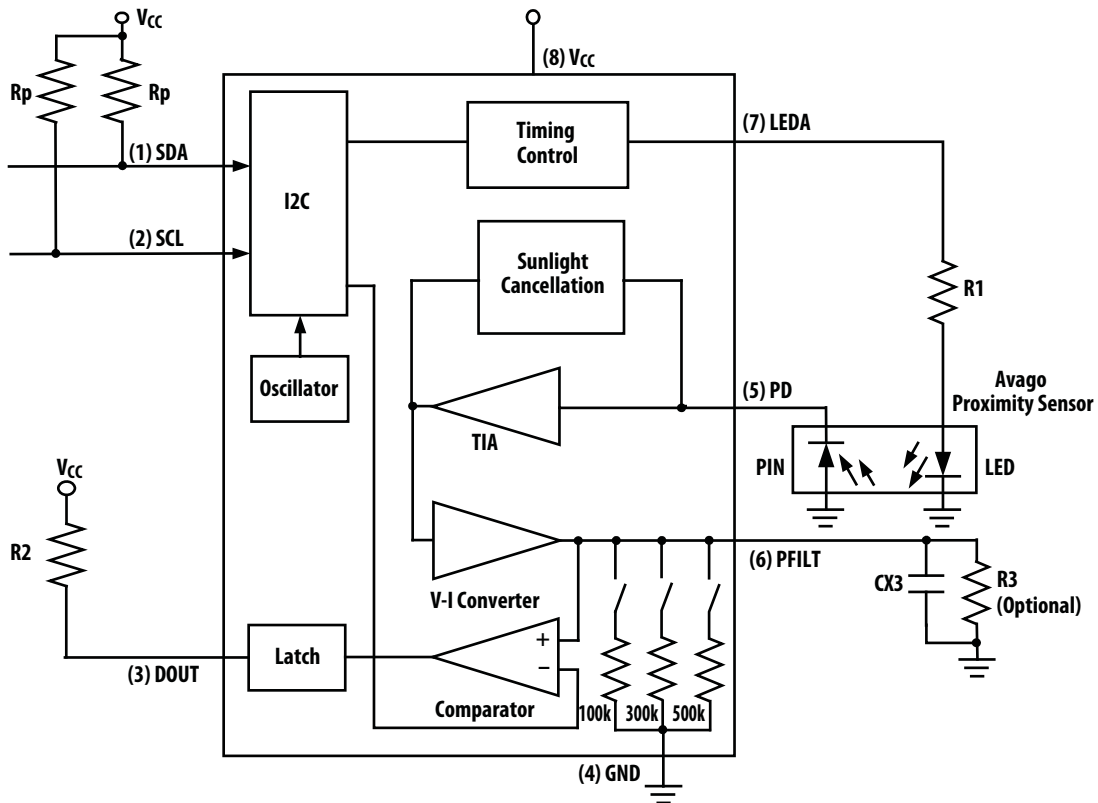
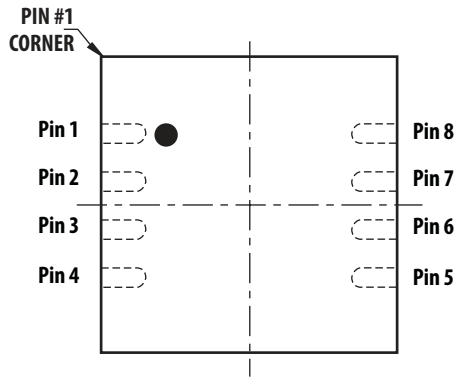


Figure 1. APDS-9702 Block Diagram

## APDS-9702 pin-out and I/O Configurations



**I/O Pins Configuration Table**

Pin	Symbol	Type	Description
1	SDA	Digital I/O	<b>I2C Serial Data I/O terminal</b> I2C input / output signal
2	SCL	Digital I/P	<b>I2C Serial Clock Input terminal</b> I2C clock input signal
3	DOUT	Digital O/P	<b>Digital Output</b> An open drain output that requires a pull-up resistor of recommended value 10k $\Omega$ DOUT = Low at last LED pulse of burst when $V_{PFILT} > V_{TH}$ , DOUT remains Low during object detected. DOUT = High at last LED pulse of burst when $V_{PFILT} < V_{TH}$ , DOUT remains High during object not detected. Please refer to Output Waveforms Definition.
4	GND	Ground	<b>Ground</b>
5	PD	Analog I/P	<b>Photo-Detector Input</b> Connect to Cathode of photo-detector (proximity sensor)
6	PFILT	Analog O/P	<b>Analog Output</b> Connect to integration circuit (R3 & CX3)
7	LEDA	Analog O/P	<b>LED Driver Output</b> Connect to Anode of LED (proximity sensor)
8	VCC	Supply	<b>Voltage Supply</b>

### Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Conditions
Supply Voltage	$V_{CC}$	0	3.6	V	$T_a=25^\circ\text{C}$
Input Logic Voltage	$V_I$	0	3.6	V	$T_a=25^\circ\text{C}$
Reflow Soldering Temperature			260	$^\circ\text{C}$	

### Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Conditions
Operating Temperature	$T_A$	-40	85	$^\circ\text{C}$	
Storage Temperature	$T_S$	-40	125	$^\circ\text{C}$	
Supply Voltage	$V_{CC}$	2.4	3.6	V	

## Electrical & Optical Specifications (Ta=25°C)

Parameters	Symbol	Minimum	Typical	Maximum	Units	Conditions
<b>Input</b>						
Logic High Input Voltage	V <sub>IH</sub>	0.7*V <sub>CC</sub>			V	
Logic Low Input Voltage	V <sub>IL</sub>			0.3*V <sub>CC</sub>	V	
Logic High Input Current	I <sub>IH</sub>		0.1		μA	V <sub>I</sub> ≥ V <sub>IH</sub>
Logic Low Input Current	I <sub>IL</sub>		0.1		μA	V <sub>I</sub> ≤ V <sub>IL</sub>
Shutdown Current	I <sub>SD</sub>			1	μA	V <sub>CC</sub> = 3.0 V, TRG = X, PWR = 0
Standby Current	I <sub>SB</sub>		70	100	μA	V <sub>CC</sub> = 3.0 V, TRG = 0, PWR = 1
<b>Output</b>						
Digital Output Low Level	V <sub>OL</sub>	0		0.3	V	I <sub>DOUT(Low)</sub> = 2 mA, V <sub>CC</sub> = 3.0 V
Digital Output High Level	V <sub>OH</sub>	V <sub>CC</sub> - 0.3			V	V <sub>CC</sub> = 3.0 V, R <sub>2</sub> = 10kΩ
Built-in Resistor at PFILT	R <sub>FILT</sub>		100k, 300k, 500k		Ω	Through I <sup>2</sup> C set.
<b>Transmitter</b>						
I <sub>LED</sub> Pulse Current	I <sub>LED</sub>		125	235	mA	V <sub>CC</sub> = 3.0 V, R <sub>1</sub> = 10Ω
Number of LED Pulse			16 x (1, 2, ..., 16 times)			Through I <sup>2</sup> C set.
LED Pulse Frequency			12.5, 25, 50, 100		kHz	Through I <sup>2</sup> C set. Pulse Duty Cycle = 50%.
LED Burst Duration vs. OFF Period			1/16, 1/64, 1/128, 1/256			Through I <sup>2</sup> C set.
<b>Receiver</b>						
Photodiode Input Current (PD)	I <sub>PD</sub>	0		3	μA	
Current Gain	I <sub>PFILT</sub> /I <sub>PD</sub>		20		times	V <sub>CC</sub> = 3.0 V [1]
<b>Comparator Threshold</b>						
Threshold voltage	V <sub>TH</sub>		0.12 0.17 0.22 0.27 0.32 0.37 0.42 0.47 0.52 0.57 0.62 0.67 0.72 0.77 0.82 0.87		V	TH = 0000, TH = 0001, TH = 0010, TH = 0011, TH = 0100, TH = 0101, TH = 0110, TH = 0111, TH = 1000, TH = 1001, TH = 1010, TH = 1011, TH = 1100, TH = 1101, TH = 1110, TH = 1111
<b>Sunlight Cancellation</b>						
DC Current, PD	I <sub>DC</sub>		100		μA	V <sub>CC</sub> = 3.0 V [1]

Note:

1. Specified by design, not production tested.

## Typical Application Circuit

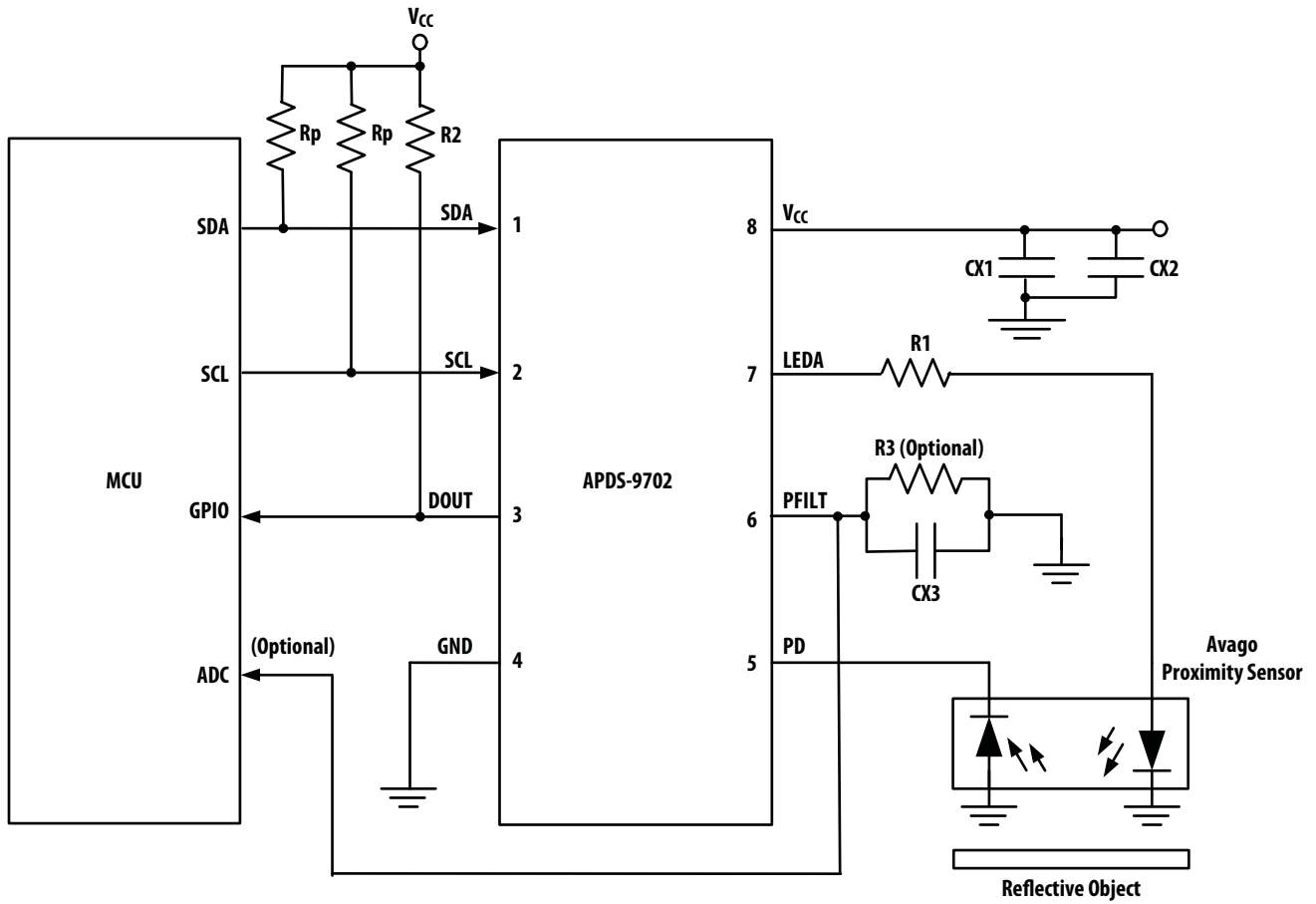


Figure 2. Typical Application Circuit for APDS-9702

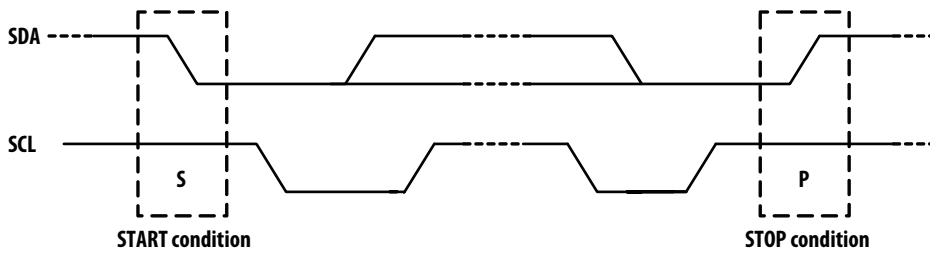
### Recommended Avago

Proximity Sensor	Description
HSDL-9100	Integrated Reflective Proximity Sensor

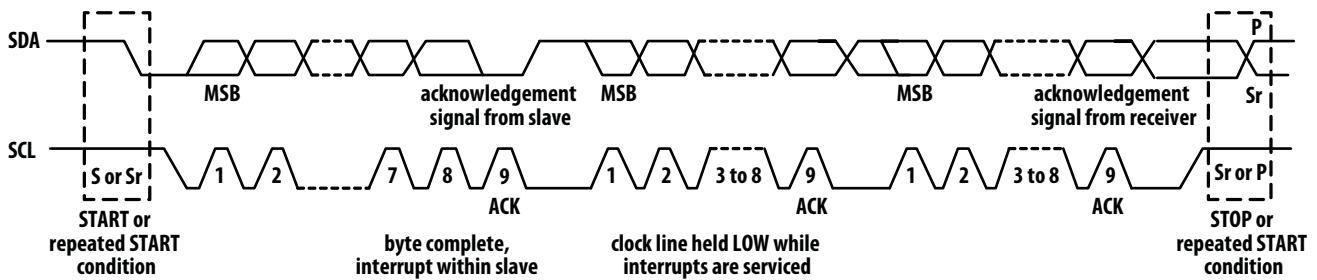
Component	Recommended Values ( with HSDL-9100)
R1	10 $\Omega$ $\pm$ 5%, 0.25W
R2	10k $\Omega$ $\pm$ 5%
R3	1M $\Omega$ $\pm$ 5%
Rp	10k $\Omega$ $\pm$ 5%
CX1	100 nF $\pm$ 20% X 7R, Ceramic,
CX2	6.8 $\mu$ F $\pm$ 20%, Tantalum
CX3	3.3 nF $\pm$ 20% X 7R, Ceramic

## I<sup>2</sup>C Definition

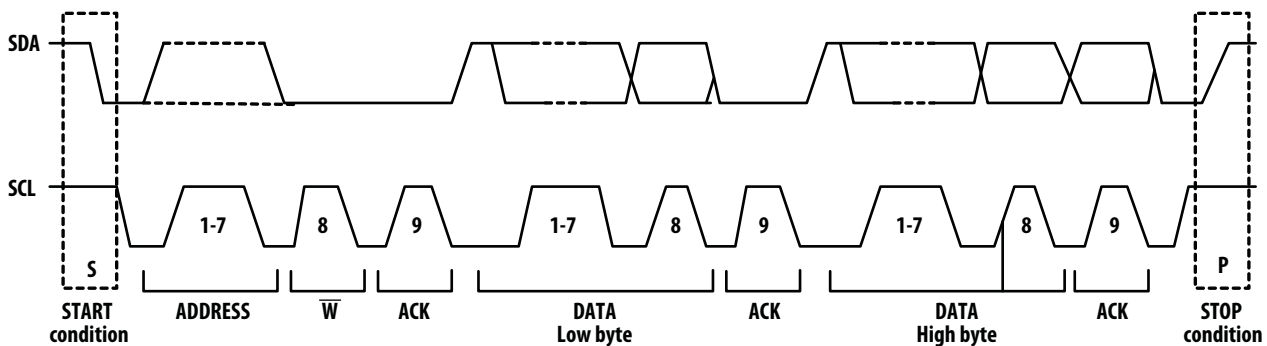
APDS-9702 operates as slave device on I<sup>2</sup>C bus for clock frequency (SCL) up to 400 kHz. The basic protocol of I<sup>2</sup>C bus is described below, for more details and specifications, please refer to *I<sup>2</sup>C-bus specification and user manual*.



**START and STOP conditions**



**Data transfer on I<sup>2</sup>C bus**



**A complete data transfer**

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Data Byte	A	Data Byte	A	P

S Start Condition

Wr Write "0"

A Acknowledge (0 for ACK)

P Stop Condition

□ Master-to-Slave

■ Slave-to-Master

Slave Address: 1010100 (Default)

## Register Definition

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRG	PWR	NB3	NB2	NB1	NB0	F1	F0	DC1	DC0	TH3	TH2	TH1	TH0	R1	R0
Default	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0

Register	Type	Description	Remark
TRG	Trigger	This pin is active high. TRG = 1 → Normal proximity sensing operations TRG = 0 → No operation (Default)	
PWR	Power	PWR = 0 → Power Shut Down (Default) PWR = 1 and TRG = 0 → Standby PWR = 1 and TRG = 1 → Active Operations	
NB<3:0>	NBurst	Number of LED Pulse per Burst = 16 x (1, 2, ..., 16 times); 0x0 = 16-pulse, 0x1 = 32-pulse (Default), ..., 0xE = 240-pulse, 0xF = 256-pulse	Figure 3
F<1:0>	Frequency	00 = 12.5kHz (Default), 01 = 25kHz, 10 = 50kHz, 11 = 100kHz; Wave is fixed at 50% Duty Cycle	Figure 3
DC<1:0>	Duration Cycle	LED Burst Duration versus OFF period; 00 = 1:16, 01 = 1:64, 10 = 1:128 (Default) and 11 = 1:256	Figure 3
TH<3:0>	Threshold, VTH	16 options of Comparator Threshold Setting; 0000 = 0.12V, 0001 = 0.17V, 0010 = 0.22V, 0011 = 0.27V, 0100 = 0.32V (Default), 0101 = 0.37V, 0110 = 0.42V, 0111 = 0.47V, 1000 = 0.52V, 1001 = 0.57V, 1010 = 0.62V, 1011 = 0.67V, 1100 = 0.72V, 1101 = 0.77V, 1110 = 0.82V, 1111 = 0.87V	Figure 4
R<1:0>	RFLIT	Programmable Filter Register; 00 = No resistor (Default), 01 = 100k, 10 = 300k, 11 = 500k	Figure 5

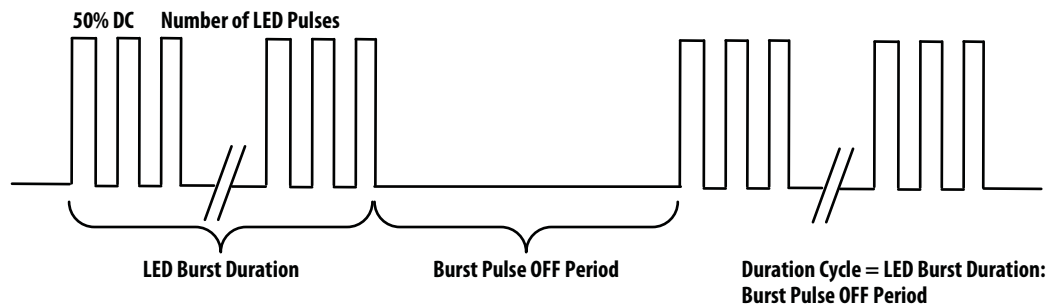


Figure 3. LEDA Burst Pulses Definition

## Transmit Burst Pulses Definition

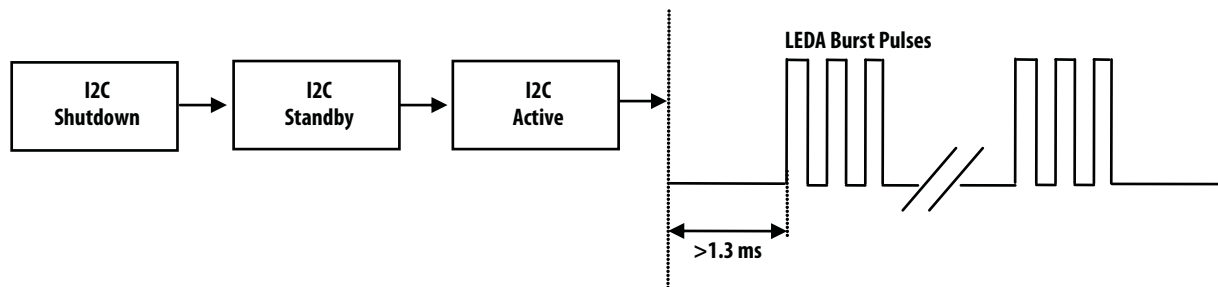
Operation ON/OFF condition is shown in the following table:

TRG	PWR	Condition
X	0	Shut down
0	1	Standby Mode
1	1	Active Mode, pulses sent

The burst pulses at LEDA pin will be activated under 2 state conditions with 2 different start-up timing. The following diagrams explained these 2 scenarios.

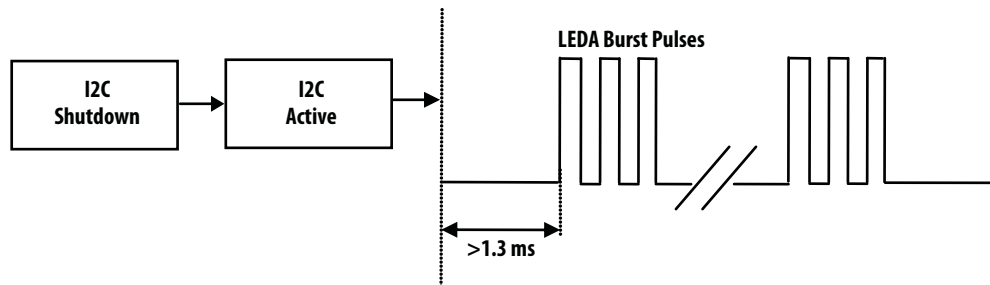
### (a) State condition 1:

From Shut down -> Standby Mode -> Active Mode: Burst pulses at LEDA pin are activated after 1.3 ms



### (b) State condition 2:

From Shut down -> Active Mode: Burst pulses at LEDA pin are activated after 1.3 ms





## Output Waveforms Definition

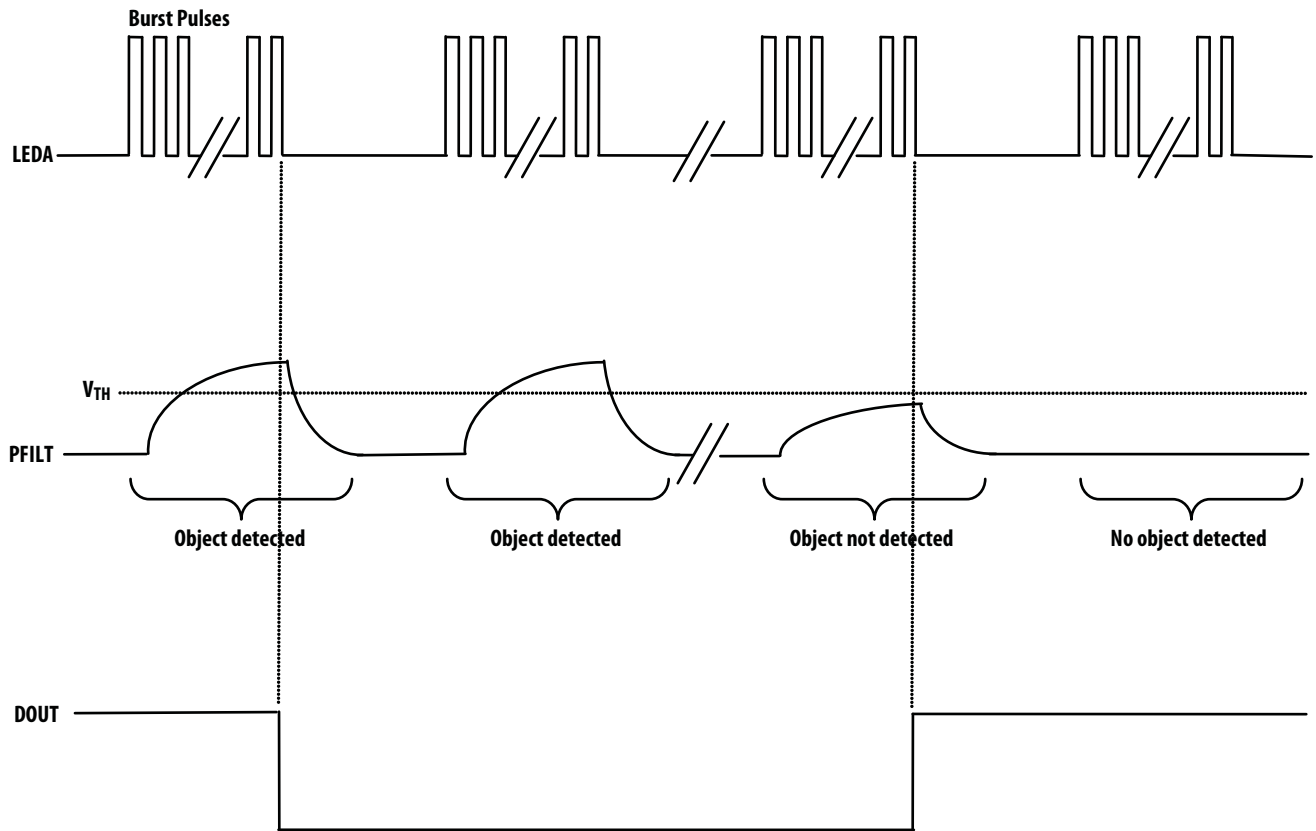


Figure 4. Output Waveforms Definition

## R<sub>FILT</sub> Definition

There are built-in resistors at PFILT (pin 6) to provide 4 options to set the desired resistor for integrated RC circuit.

R0	R1	Resistor Value
0	0	Open. External resistor R3 is required to be in parallel with CX3
0	1	100k ohm. R3 become optional.
1	0	300k ohm. R3 become optional.
1	1	500k ohm. R3 become optional.

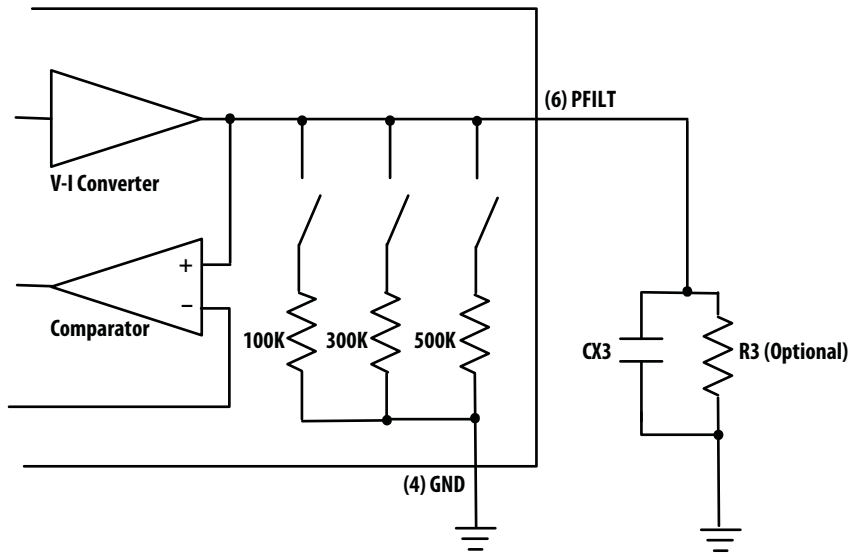
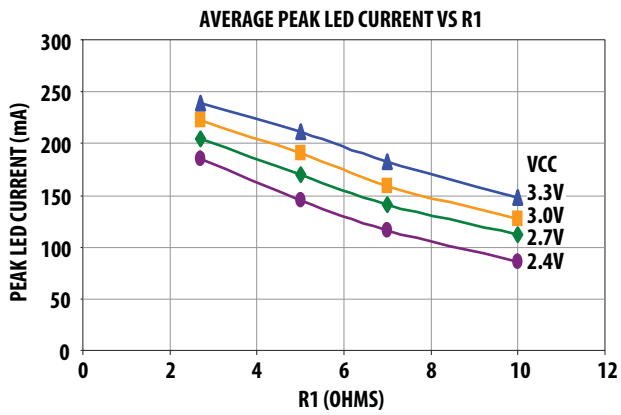
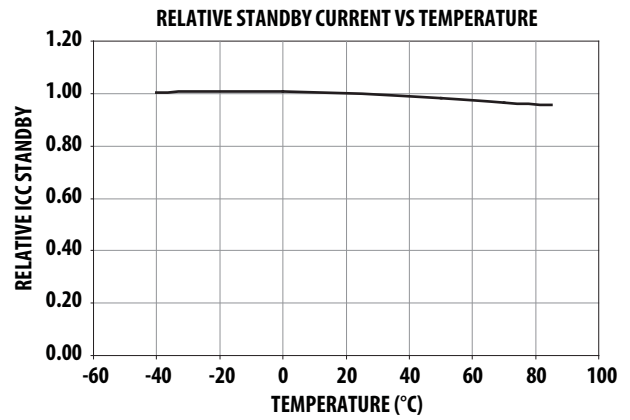
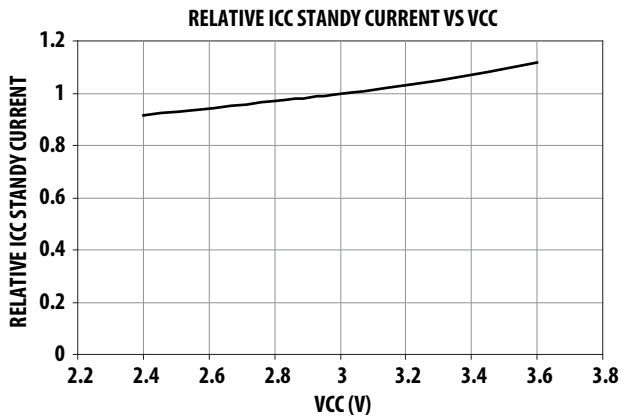
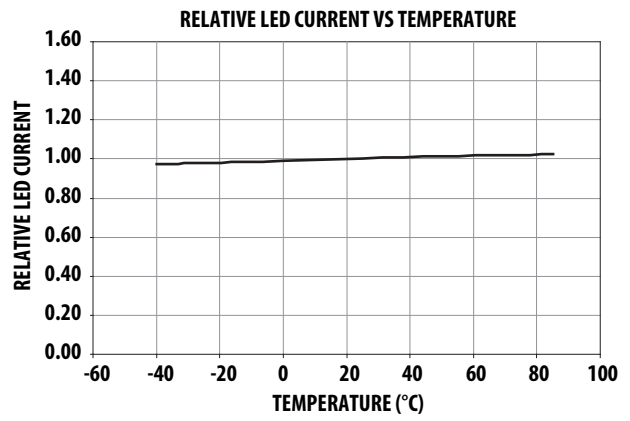
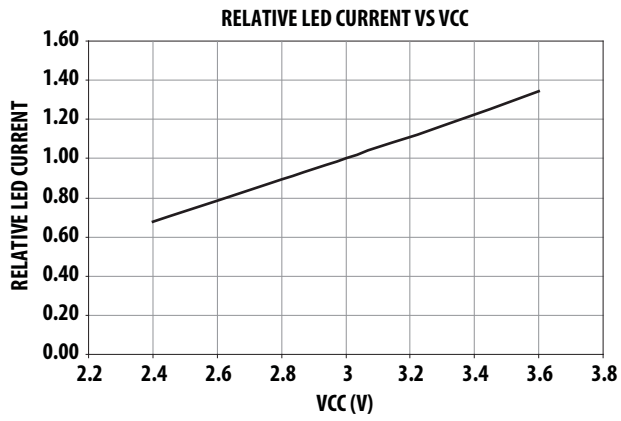


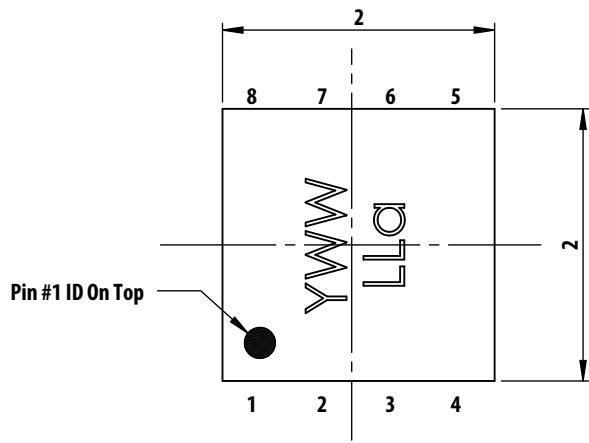
Figure 5. R<sub>FILT</sub> definition

## APDS 9702 Performance Charts

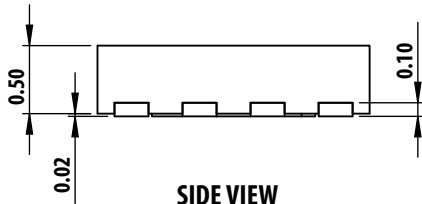


# APDS-9702 Package Dimensions

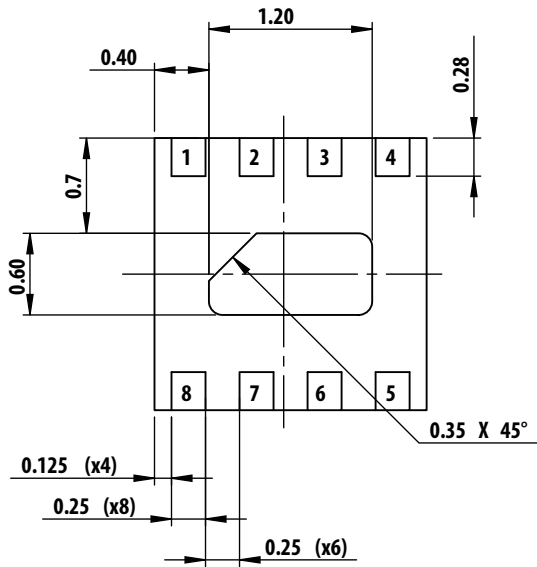
## QFN 8-Pin Package



**TOP VIEW**



**SIDE VIEW**

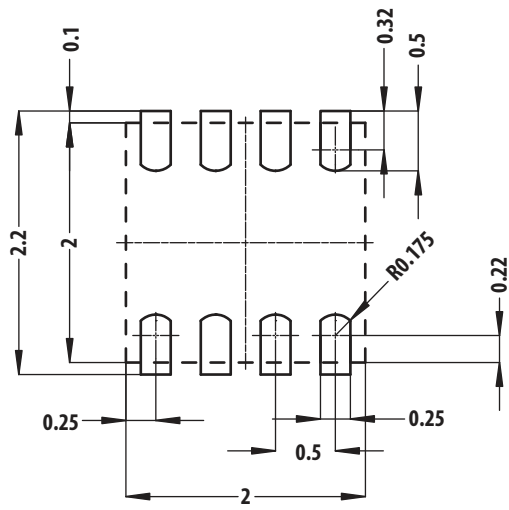


**BOTTOM VIEW**

Note:

1. All Dimensions in mm. Tolerance  $\pm 0.1$ mm unless specified.
2. Marking Information:  
 The unit is marked 'YWW LLa' on the chip.  
 Y = Year (Last digit of the year)  
 WW = work week (1-54)  
 LL = Lot number (01-99)  
 a = Denote this is an I<sup>2</sup>C part.

## Recommended Minimum Land pattern and Keep-out Area



**SOLDER LAND PATTERN**

Dimension in mm.  
Recommended tolerances +/-0.1mm

### Keep-out Area Recommendations:

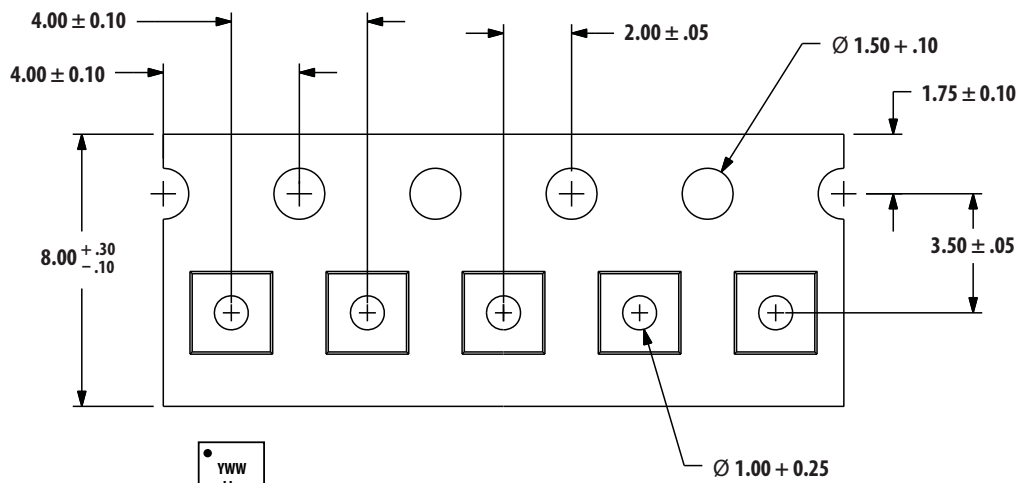
Area of Solder Land pattern = 2.3mm x 2.1mm

Module placement tolerance & keep out on each side with no lead = 0.55mm & keep out on each side solder lead = 0.8mm

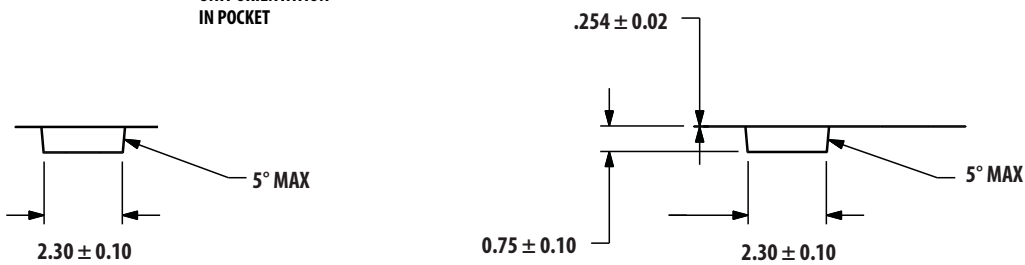
Keep-out area = 3.9mm x 3.2mm

# APDS-9702 Tape and Reel Dimensions

## Tape Dimensions



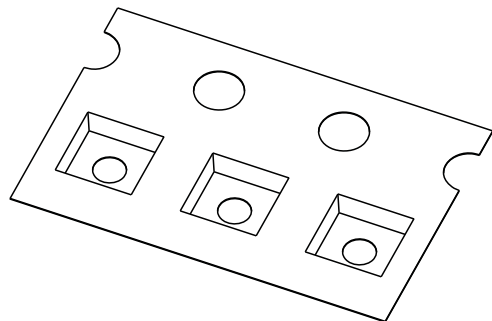
UNIT ORIENTATION  
IN POCKET



**A.**

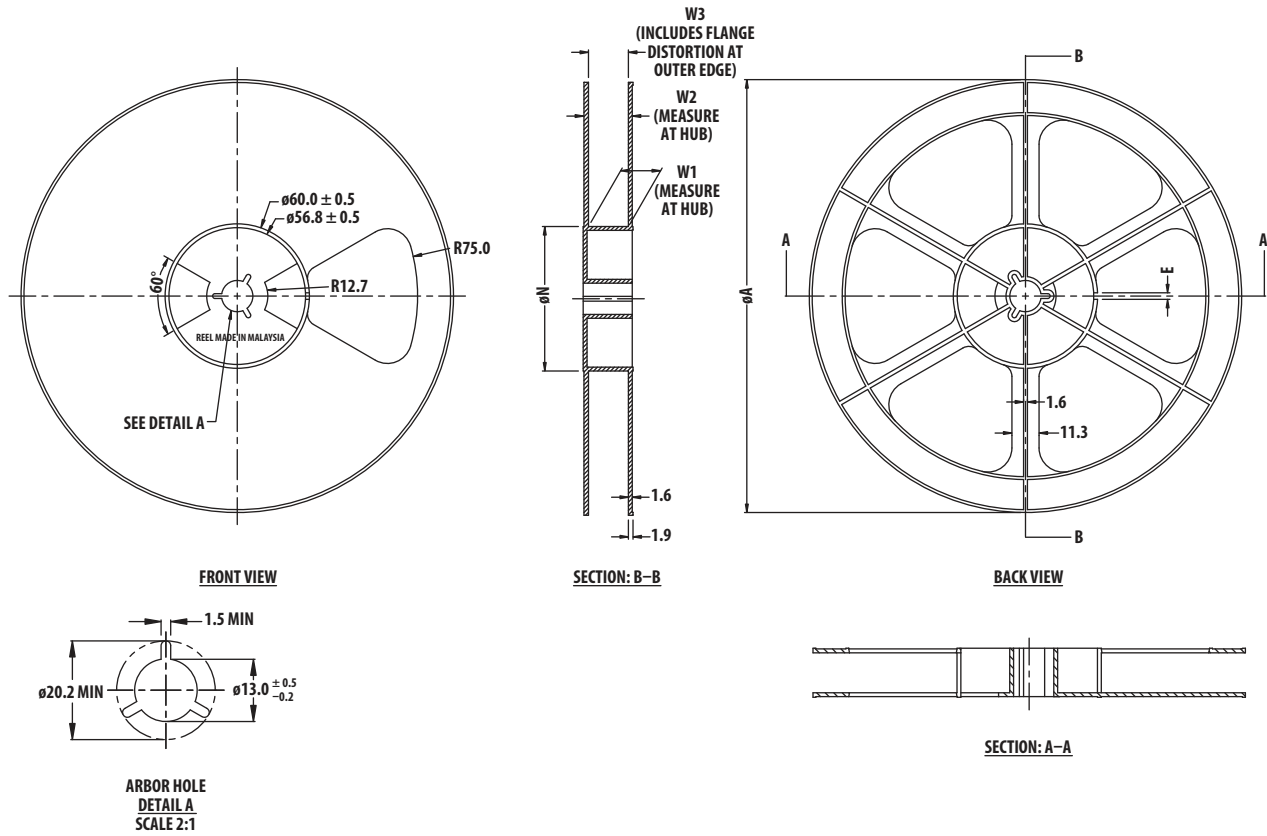
**K.**

**B.**



ALL DIMENSIONS IN mm.

## Reel Dimensions



Product Specifications						
TAPE WIDTH	$\phi A$	$\phi N$	WT	W2 (MAX)	W3	E
08MM	$180^{+0.0}_{-2.0}$	$60 \pm 2.0$	$8.4^{+1.5}_{-0.0}$	14.4	$8.4^{+2.5}_{-0.5}$	$4.0 \pm 0.1$

All Dimensions in mm.

## Packaging

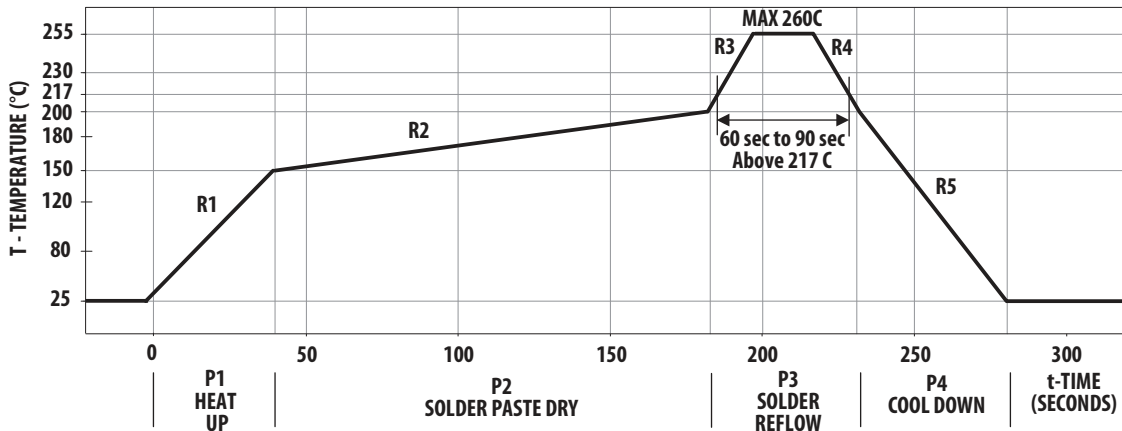
All APDS-9702 options are shipped in ESD proof packaging.

This part is compliant to JEDEC MSL 1.

## Recommended Storage Conditions

Storage Temperature	The units in tape and reel are recommended to be kept in a controlled climate environment, with temp at $25 \pm 5/-10^\circ\text{C}$ and relative humidity at $55 \pm 15\%$ .
Time from unsealing to soldering	This part is compliant to JEDEC MSL-1 (unlimited floor life at $< 30^\circ\text{C} / 85\%RH$ )

## Recommended Reflow Profile



The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different  $\Delta T/\Delta \text{time}$  temperature change rates or duration. The  $\Delta T/\Delta \text{time}$  rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and APDS-9702 pins are heated to a temperature of 150°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3°C per second to allow for even heating of both the PC board and APDS-9702 pins.

**Process zone P2** should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 200°C (392°F).

**Process zone P3** is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 255°C (491°F) for optimum results. The dwell time above the liquidus point of solder should be between 20 and 40 seconds. It usually takes about 20 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 40 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 200°C (392°F), to allow the solder within the connections to freeze solid.

**Process zone P4** is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and APDS-9702 pins to change dimensions evenly, putting minimal stresses on the APDS-9702.

It is recommended to perform reflow soldering no more than twice.

For product information and a complete list of distributors, please go to our web site: [www.avagotech.com](http://www.avagotech.com)

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TECHNOLOGIES