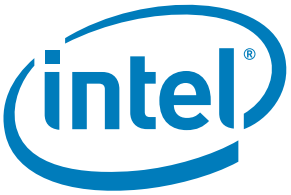

Intel® 82552V Fast Ethernet PHY

Datasheet

Product Features

- **General**
  - — Physical layer interface 10BASE-T/ 100BASE-TX IEEE 802.3 compliant.
  - — IEEE 802.3u Auto-Negotiation support for 10BASE-T/100BASE-TX
  - — Automatic MDI/MDI-X switch-over
  - — XOR tree support
  - — 10BASE-T auto-polarity correction
  - — Auto-detection of "Unplugged mode".
  - — 3.3 V device
  - — Reverse auto negotiation .
  - — LCI Interface Support
  - — Loop back support
  - — PXE Support
- **Power**
  - — Low Power: 310 mW at fastest speed
  - — Reduced power in "Unplugged mode"
- **Technology**
  - — 82552V - 32 pins, QfN 5 mm x 5 mm package
  - — Two Port LED support (Speed, Link and Activity)

Order Number: 322322-001EN
Revision 1.9

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Revision History

Date	Revision	Description
September 2008	0.5	Initial public release.
February 2009	0.75	Added power delivery diagram. Added reset effects table. Updated Reference Documents list. Removed preliminary oscillator information. Added magnetics specifications. Corrected pinout diagram and pin description table. Updated power consumption table.
April 2009	1.0	Corrected pinout diagram and pin description table. Updated power consumption table.
May 2009	1.1	Updated power value. Updated RBIAS value. Removed chipset reference and added platform chipset name, Tiger Point. Updated Signal Definition table. Updated mechanical drawing and assembly information. Updated Low-Power Link Up section. Corrected signal name in Figure 8.
July 2009	1.9	Updated measured power table; removed Intel Confidential designation.

1.0 Introduction

1.1 Scope

This document describes the external architecture for the 82552V. It's intended to be a reference for software developers of device drivers, board designers, test engineers, or anyone else who might need specific technical or programming information about the 82552V.

1.2 Overview

The Intel® 82552V 10/100 Mbps Platform LAN Connect is a highly-integrated device designed for 10 or 100 Mbps Ethernet systems. It is based on the IEEE 10BASE-T and 100BASE-TX standards.

The IEEE 802.3u standard for 100BASE-TX defines networking over two pairs of Category 5 unshielded twisted pair cable or Type 1 shielded twisted pair cable.

The 82552V conforms with the IEEE 802.3u Auto-Negotiation standard and the IEEE 802.3x Full Duplex Flow Control standard. The 82552V also includes a PHY interface compliant to the current platform LAN connect interface.

The 82552V only operates with the ITiger Point chipset that incorporates the MAC. An interface for a Platform Controller Hub (PCH) is also available--contact your Intel representative for more information.

The 82552V is packaged in a small footprint QFN package with 32 pins, 5 mm x 5 mm with 0.5 mm pitch, making it very useful for small form-factor platforms.

The 82552V interfaces with its MAC through the LCI-based interface.

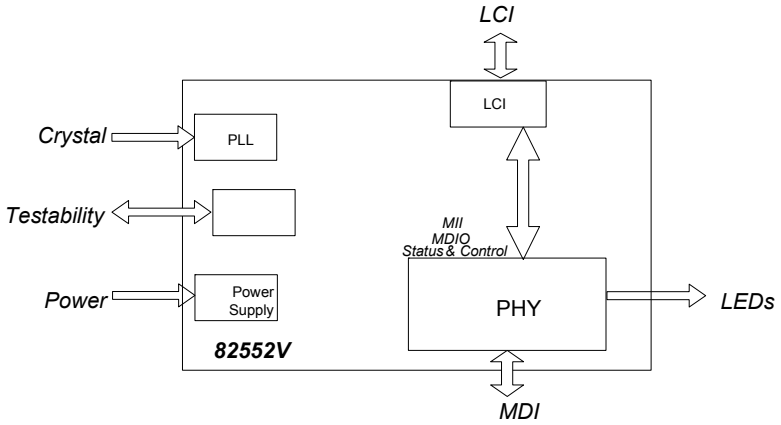

Figure 1. 82552V Block Diagram

1.3 References

- IEEE 802.3 Standard for Local and Metropolitan Area Networks, Institute of Electrical and Electronics Engineers.
- • LAN Connect Interface Specification. Intel Corporation.
- • I/O Control Hub 2, 3, and 4 EEPROM Map and Programming Information. Intel Corporation.
- • I/O Control Hub 5, 6, and 7 EEPROM Map and Programming Information. Intel Corporation

Programming information can be obtained through your local Intel representatives.

1.4 Product Codes

Table 1 lists the product ordering codes for the 82552V Ethernet controller.

Table 1. Product Ordering Code

Device	Product Code
82552V	WG82552V

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2.0 Interconnects

2.1 Introduction

The 82552V implements the LCI interconnect to the MAC:

It is an eight-pin interface that incorporates all MII management functionality. The interface includes reset functionality as well.

2.2 JCLK Clock

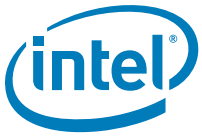
The 82552V drives a 50 Mhz clock or a 5 Mhz clock to the MAC depending on the selected technology: 100base-TX or 10Base-T respectively. The 82552V does not stop the LCI clock in any case. During reduced power mode, the 82552V drives a 5 Mhz clock.

2.3 JRSTSYNC

The 82552V filters out any JRSTSYNC pulses with width less than 200 ns to distinguish between a RESET and a SYNC pulse. For resetting the 82552V, the reset should be longer than 500 us.

2.4 XOR Test Interface

Signal	Type
LED_10_100n	XOR output
LED_ACTn	XOR input
JRXD0	XOR input
JRXD1	XOR input
JRXD2	XOR input
JTXD0	XOR input
JTXD1	XOR input
JTXD2	XOR input
JCLK	XOR input
JRSTSYNC	XOR input
RSVD _IN_1	XOR input
RSVD _IN_32	XOR input



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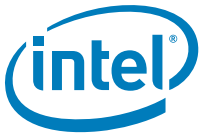
3.0 Pin Interface

3.1 Pin Assignment

The 82552V is packaged in a 32-pin package, 5 x 5 mm with a 0.5 mm lead pitch. There are 32 pins on the periphery and a die pad (Exposed Pad*) for ground.

3.1.1 Signal Type Definitions

Signal Type	Definition
I	A standard input-only signal.
O	Totem pole output is a standard active driver.
T/s	Tri-state is a bi-directional, tri-state input/output pin.
S/t/s	Sustained tri-state is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives an s/t/s pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving an s/t/s signal any sooner than one clock after the previous owner tri-states it.
O/d	Open drain enables multiple devices to share as a wire-OR.
Analog	Analog input/output signal.
AI	Analog input signal.
AO	Analog output signal.
B	Input bias
P	Power
PD	Pull down
PU	Pull up
IH	Digital input with hysteresis



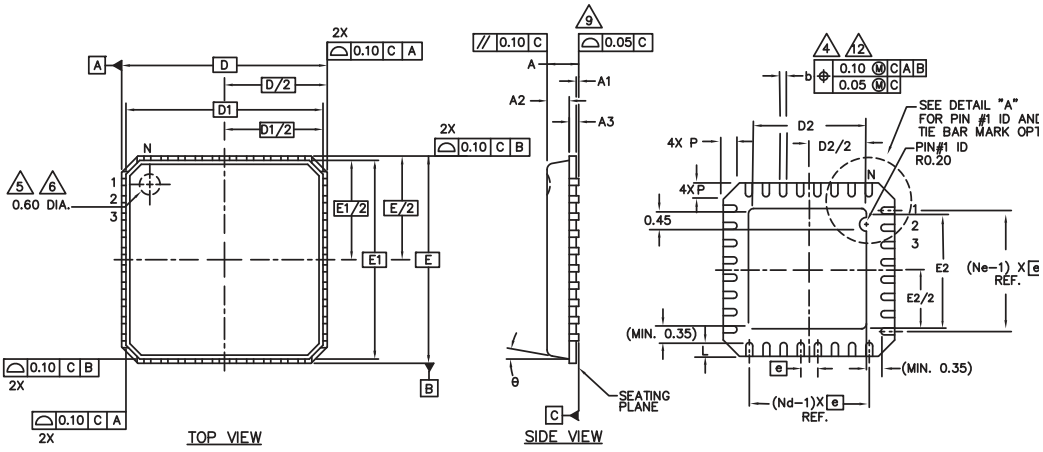
3.2 Pin Descriptions

Pin Name	Pin #	Pin type	Description
VDD2P5_OUT	1	AO	2.5V regulator output. A 1uF plus several 0.1uF cap needed to stabilize the output. It is for analog, digital I/O and the transformer center taps
VDD3P3_IN	2	P	3.3 V
DVDD1P2_3	3	P	Digital 1.2V
RSVD_IN_4	4	I, PU (low voltage)	Select either 25 MHz or 48 MHz external clock source. Float=25 MHz, GND=48 MHz
XTAL_OUT	5	AO	Crystal oscillator output. 27pF to GND. An external clock source with 0-1.2V swing can inject to this pin when crystal is not used
XTAL_IN	6	AI	Crystal oscillator input, 27pF to GND.
VDD1P2_OUT	7	P	1.2V regulator output. Two 0.1uF caps or one 1uF cap needed to stabilize the output.
RBIAS	8	AO	Connect 2.26 kOhm ±1% to GND
MDI_PLUS0/ MDI_MINUS0	9, 10	AI, AO	Media Dependent interface 0, terminated with two 49.9Ω resistors and connect to XFMR
MDI_PLUS1/ MDI_MINUS1	11, 12	AI, AO	Media Dependent interface 1, terminated with two 49.9Ω resistors and connect to XFMR
AVDD2P5_13	13	P	Analog 2.5 V
RSVD _IN_14	14	I/O, PU	Reserved input pin. Tie to 3.3V through a 10 kOhm resistor.
RSVD _IN_15	15	I/O, PU	Reserved input pin. Tie to 3.3V through a 10 kOhm resistor
TEST_EN	16	I, PD	Test enable.
LED_10_100#	17	I/O, PU, input is only for test	Parallel LED output for 10/100BASE-T, 0 = 100 BT 1 = 10 BT
LED_ACT#	18	I/O, PU, input is only for test	Parallel LED activity indicator, active low
JTAG_TDI	19	I/O, PU,	Jtag data in
JTAG_TMS	20	I/O, PU,	Jtag tms
JTAG_TDO	21	I/O, PU,	Jtag data out
JTAG_TCK	22	I/O, PU,	Jtag clk
DVDD2P5_23	23	P	Digital I/O 2.5V
JRXD2	24	I/O, PU, input is only for test	50 Mbps receive out
JRXD1	25	I/O, PU, input is only for test	50 Mbps receive out
JRXD0	26	I/O, PU, input is only for test	50 MHz receive out
JCLK	27	I/O, PU, input is only for test	Clock out
JTXD2	28	I, PU,	Transmit input
JTXD1	29	I, PU,	Transmit input
JTXD0	30	I, PU,	Transmit input
JRSTSYNC	31	IH, PU,	System reset input
RSVD _IN_32	32	IH, PU,	Reserved input pin. Tie to 3.3 V through a 10 kOhm resistor

4.0 Package

4.1 Package Type and Epad Size

The 82552V is a 5 mm x 5 mm, 32-pin QFN package with a pad size of 2.7 mm x 2.7 mm.



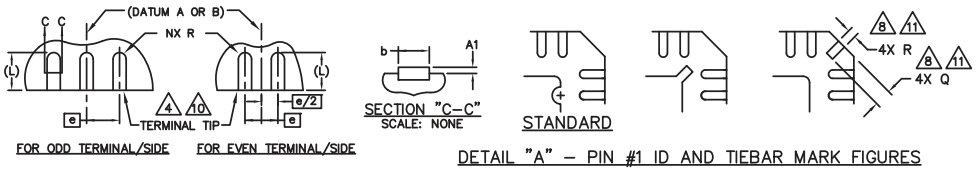
Symbol	Package Dimensions			Note
	MIN	NOM	MAX	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
Q	-	-	-	
D2	See Exposed Pad Dimensions			
E2	See Exposed Pad Dimensions			

Exposed Pad

SYMBOL	D2			E2			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD	2.60	2.70	2.80	2.60	2.70	2.80	

Symbol	Common Dimensions			Note
	MIN	NOM	MAX	
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	10
A2	0.60	0.65	0.70	
A3		0.20 REF		
D		500 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ	0	–	12'	
P	0.24	0.42	0.60	
O	0.30	0.40	0.65	8,11
R	0.13	0.17	0.23	8,11

Tolerance Requirement for D1/E1: +/- 0.1 mm



DETAIL "A" – PIN #1 ID AND TIEBAR MARK FIGURES

4.2 Package Electrical and Thermal Characteristics

Max temperature junction is 120 degrees C.

Velocity (m/s)	Theta Ja (c/w)	Theta Jb (c/w)	Theta Jc (c/w)	Psi jt (c/w)	Psi jb (c/w)
0	52.5	33	11.2	0.9	31.7
1	45.9	33	11.2	1.4	31.3
2.5	41.1	33	11.2	1.9	30.9

No heat sink is required.

4.3 Power and Ground Requirements

The 82552V requires one power supply.

Note: Power delivery can be customized based on a specific OEM platform configuration.

4.3.1 Power Delivery

The 82552V operates from a 3.3 V DC external power rail and internally generates the 2.5 V and 1.2 V supplies.

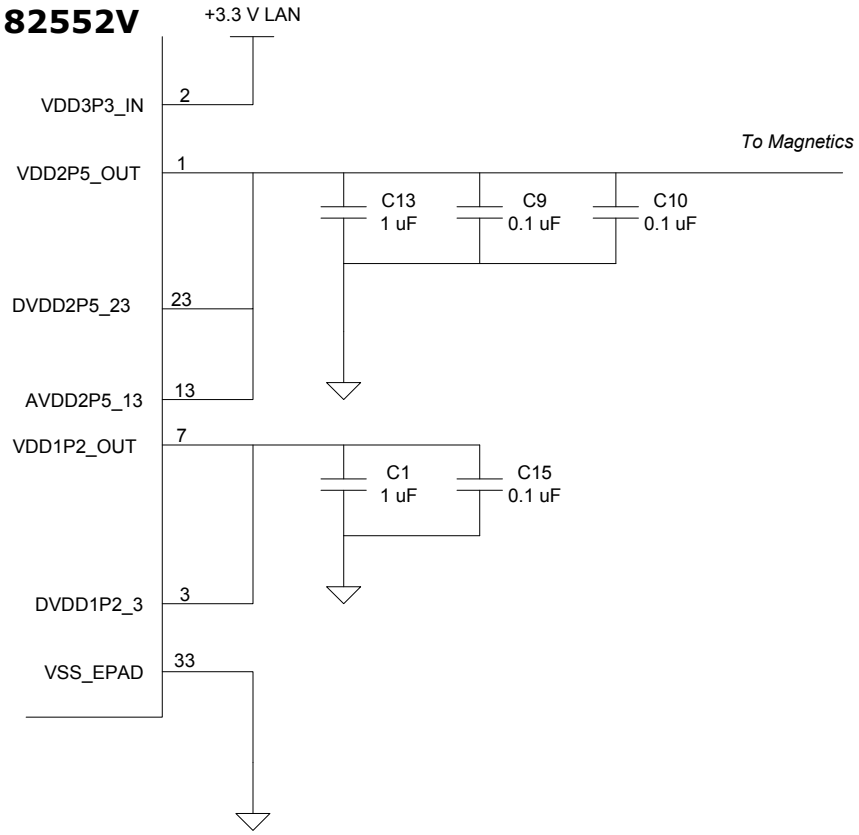


Figure 2. 82552V Power Delivery Diagram

4.4 Pinouts (Top View, Pins Down)

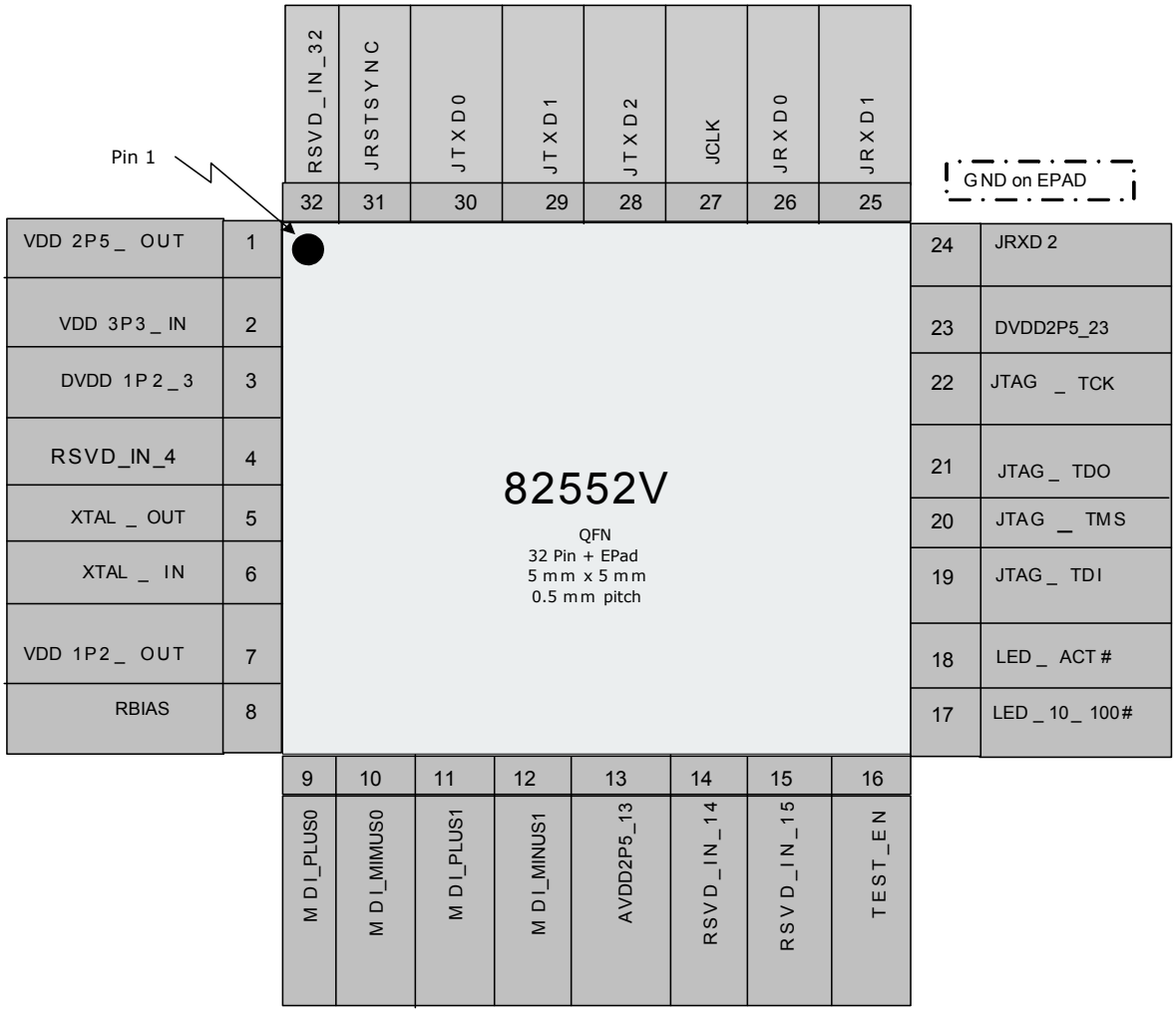


Figure 3. 82552V Pinouts

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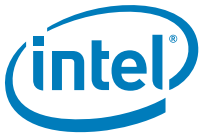


5.0 Initialization

5.1 Power Up Sequence

The 82552V uses a 3.3 V power rail. The rail must meet the LCI power ramp requirements. The following flowchart shows the power up sequence for the 82552V.

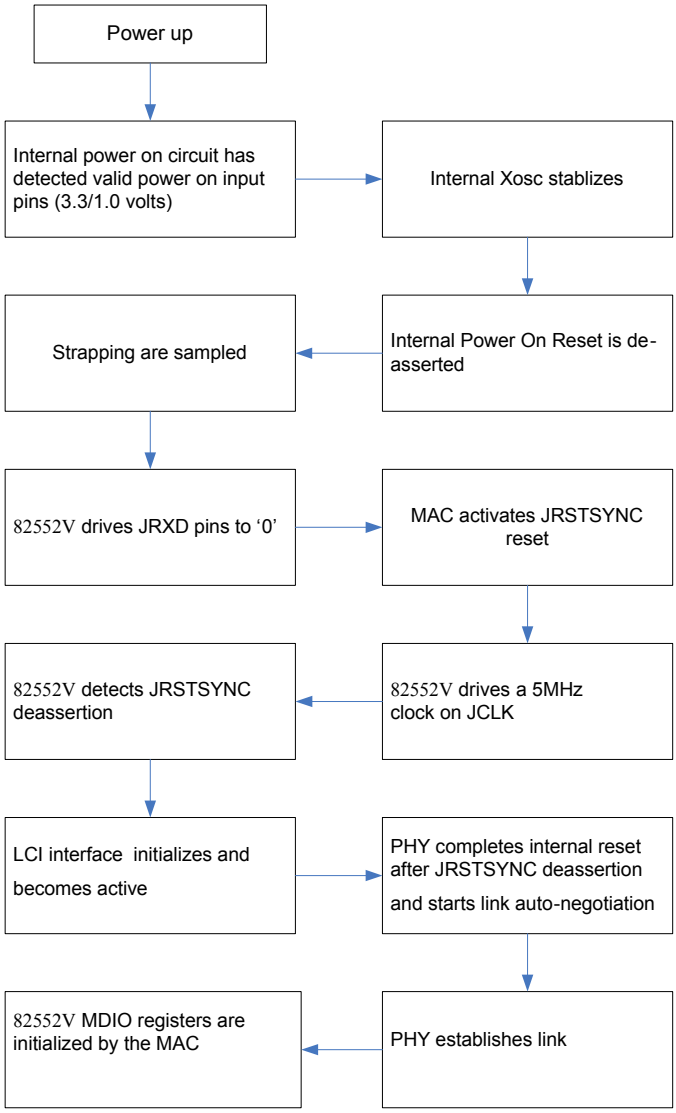


Figure 4. Power Up Sequence Flowchart

5.2 Reset Operation

Three resets are available:

- Internal Power On Reset (POR)--the 82552V has an internal mechanism for sensing the power pins. Until power is up and stable, the 82552V generates an internal active low reset. This reset acts as a master reset for the device.

  Strapping values are latched after Internal POR is de-asserted.

- LCI Reset--Reset from JRSTSYNC pin causing complete reset of the 82552V, including the PHY.
- PHY Soft Reset--A PHY reset caused by writing to bit 15 in MDIO register 0.

  Setting the bit resets the PHY, but does not reset non-PHY parts.

The effect/impact of these various reset options on these and other registers is listed in the following table. A (√) indicates that these areas are affected.

Effects/Sources	PHY Registers and States	Strapping Options
Internal POR	√	√
LCI Reset	√	
PHY Soft Reset	√	

6.0 Power Management and Delivery

This section describes how power management is implemented in the 82552V.

6.1 Power Consumption

The following table lists the measured power:

Table 2. Measured Power

Mode	Description	Intel® 82552V PHY Power + internal regulator (mW)	Intel® NM10 Express Chipset incremental power (mW)	Total Solution Power (mW)
S0	100 Mbit active	310	86	396
	100 Mbit idle	307	8	315
	10 Mbit active	413	17	430
	10 Mbit idle	59	0	59
	Cable Disconnect	20	0	20
	LAN disable (BIOS or driver)	13	-	13
Sx	WOL disabled	13	-	13
	10 Mbit WOL	59	0	59
	100 Mbit WOL	307	8	315

† The values for power consumption with WOL enabled depend on the link partner autonegotiation or forced speed and whether LPLU (described below) is enabled .

†† The incremental chipset power is the difference between the chipset power measured at the various LAN connection speeds (active and idle) and the chipset power when the LAN has been disabled via the BIOS.

††† To disable WOL, set “Enable PME” to Disabled.

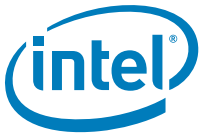
6.2 Power Saving Feature

This section provides information about the low power configuration for the 82552V.

6.2.1 Low-Power Link Up (LPLU)

LPLU is a software-based (Windows*-only) feature that instructs the PHY to negotiate to the lowest possible connection speed when going from the S0 state to an Sx state. This power saving feature can be used when power is more important than performance in the Sx state. See the power consumption table for the amount of power drawn in idle when at different connection speeds.

LPLU is enabled for non-D0a states by the Low Power Link Up option in the Advanced driver properties tab.



- Disabled = LPLU is disabled.
- Enabled = LPLU is enabled in all non-D0a states.

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7.0 Electrical and Timing Specifications

7.1 Introduction

This section describes the 82552V's recommended operating conditions, power delivery, DC electrical characteristics, power sequencing and reset requirements, LCI, reference clock, and packaging information.

7.2 Operating Conditions

7.2.1 Absolute Maximum Operating Conditions

- Case Temperature Under Bias ..... 0 ^{o}C to + 130 ^{o}C
- Storage Temperature ..... -65 ^{o}C to +150 ^{o}C
- Supply Voltage with respect to V_{SS} ..... -0.5 V to + 4.6 V
- Outputs Voltages ..... -0.5 V to + 3.45 V
- Input Voltages ..... -1.0 V to + VCC

Note: Case temperature should not exceed junction temperature.

7.2.2 3.3 V Rail Requirements

Title	Description	Min	Max	Units
Rise Time	Time from 10% to 90% mark	0.1	100	mS
Monotonicity	Voltage dip allowed in ramp	N/A	0	mV
Slope	Ramp rate at any given time between 10% and 90% Min: 0.8*V(min)/Rise time (max) Max: 0.8*V(max)/Rise time (min)	24	28800	V/S
Operational Range	Voltage range for normal operating conditions	3	3.6	V
Ripple	Maximum voltage ripple (peak to peak)	N/A	70	mV
Overshoot	Maximum overshoot allowed	N/A	100	mV

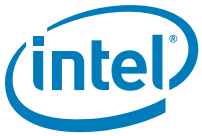

Table 3. Power Detection Threshhold

Symbol	Parameter	Specifications			Units
		Min	Typ	Max	
V1a	High-threshold for 3.3V supply	2.4	2.5	2.6	V
V2a	Low-threshold for 3.3V supply	2.1	2.2	2.3	V

7.2.3 DC Characteristics

Table 4. General DC Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
T	Temperature	Min - Case Temp; Max - Case Temp	0		85	C
P	Power Dissipation	10 Mbps, 100 Mbps (transmitter on)		415		mW
		Reduced Power		20		mW

7.2.4 3.3 V I/O Interfaces DC Characteristics

Table 5. 3.3 V I/O Interfaces DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VCC3p3_IN	I/O Supply Voltage		3.0		3.6	V
V_{IH}	Input High Voltage		0.6Vccj		Vccj+0.5	V
V_{IL}	Input Low Voltage		-0.5		0.3Vccj	V
I_{IL}	Input Leakage Current	0 < Vin < Vccj			±10	µA
V_{OH}	Output High Voltage	Iout = -500 µA	.9Vccj			V
V_{OL}	Output Low Voltage	Iout = 1500 µA			.1Vccj	V
C_{IN}	Input Pin Capacitance				8	pF

7.2.5 LED DC Characteristics

Table 6. LED DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OLLED}	Output Low Voltage	Iout = 10 mA			0.7	V
V_{OHLED}	Output High Voltage	Iout = -10 mA	2.4			V

7.2.6 AC Characteristics

7.2.6.1 LCI buffer load

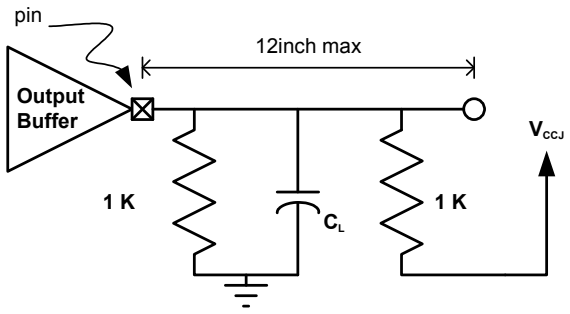

Figure 5. Load for Testing Output Timings

7.2.6.2 LCI Clock and Signals Timings

Table 7. LCI Clock and Signals Timings

	Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
T1	T_{CYC}	JCLK cycle time		20		200	ns	2,6
T2	T_{HIGH}	JCLK high time		8.5			Ns	8
T3	T_{LOW}	JCLK low time		8.5			ns	8
	---	JCLK Slew Rate		1.0		4.0	V/ns	3
T4	t_{VALP}	**JCLK** to valid delay, PHY		2.0		13.0	ns	1,4,5
T5	t_{SUP}	PHY setup time to **JCLK**		5.0			ns	4,5
T6	t_{HP}	PHY signals hold time to **JCLK**		1.0			ns	4
	---	Output Signals slew rate		0.25		4.0	V/ns	7
T7	$t_{CLK-RST}$	**JCLK** stable time before Reset deassertion		0.5			ms	

Notes:

1. Output delays into a capacitive load of 10 pF. For a slow slew rate output driver 0pF load must be used for minimum delays and 50 pF for maximum delays.

2. The LCI active frequency is defined by the protocol – as high 50 MHz and as low as 5MHz. Dynamic changes of the normal operating frequency are not allowed. Only a change between the normal operating state and a clock stopped state are supported. The clock may only be stopped in a low state. During clock stop, LCI iinterface signals must not be allowed to float.
3. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.
4. Input and output timings are measured relative to JCLK timing at the respective component's pin (JCLK is output from PHY and input into MAC).
5. In a PHY that is designed for lower than 50 MHz frequency, t_{SUP} and maximum t_{VALP} can be extended, by as much as half of the cycle-time difference between that frequency and 50 MHz. This will also allow some added leniency for the system designer as well. Example: max frequency for the designed PHY is 25 MHz. The cycle time difference is 20ns. t_{SUP} and maximum t_{VALP} can be extended by 10ns each.
6. JCLK must never be stopped while in operation mode. The frequency of JCLK must be stable once initiated during reset.
7. Signal slew rates are measured between V_{TL} and V_{TH}.
8. V_{TEST} 0.5Vccj

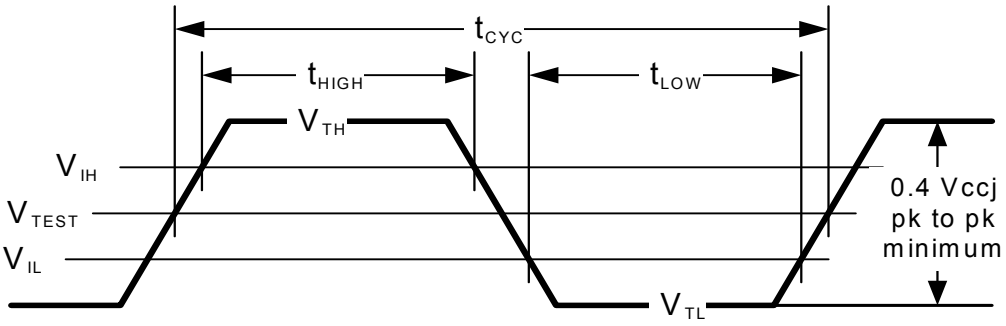

Figure 6. Clock Input Measurement Conditions

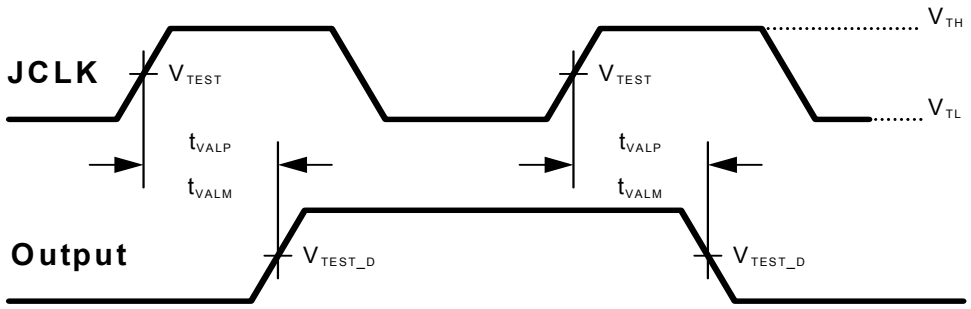

Figure 7. Output Timing Measurement Conditions

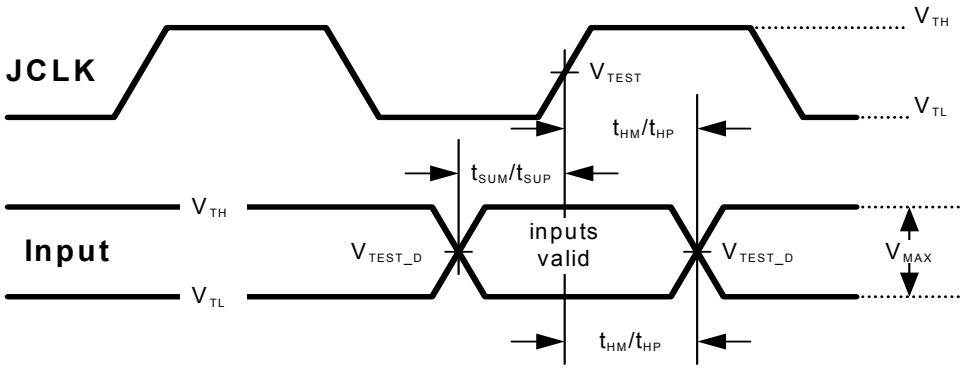

Figure 8. Input Timing Measurement Conditions

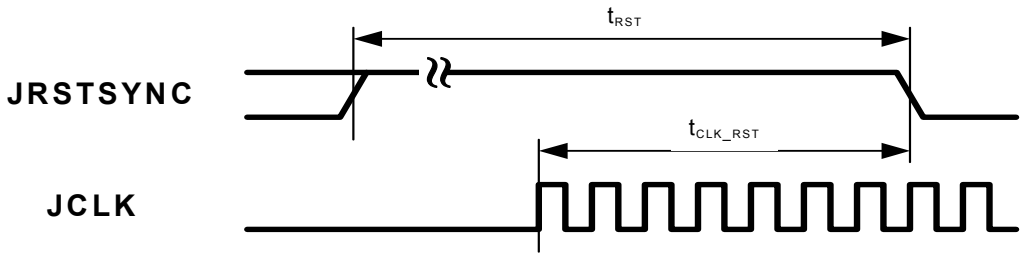

Figure 9. Reset and JCLK timings

7.2.7 Reset (JRSTSYNC) Timing Parameters

Table 8. Reset (JRSTSYNC) Timing Parameters

	Symbol	Parameter	Condition	Min	Typ	Max	Units
T17	T_{RST_WID}	Reset pulse width		500			µs
T18	T_{POP_RST}	Power Up to falling edge of Reset		1000			µs

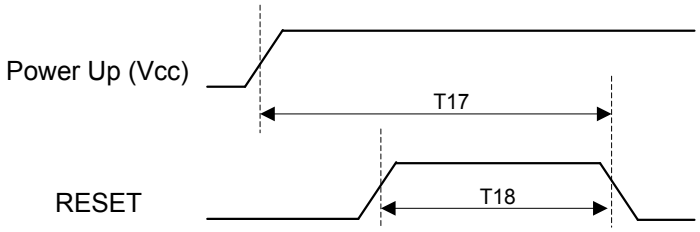

Figure 10. Reset Timing Parameters

7.2.8 Crystal Information

The schematics for the intended crystal design options are shown below:

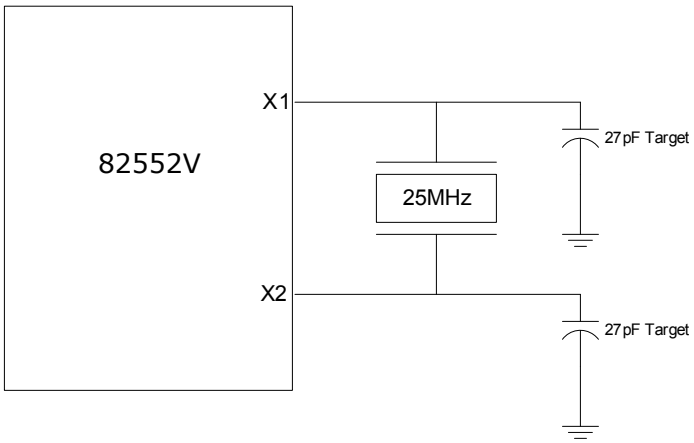

Figure 11. Crystal Connection Diagram

7.2.9 Crystal Specifications

Table 9. Crystal Specifications

Vibrational mode	Fundamental
Nominal frequency	25.000 MHz @ 25 C
Frequency Tolerance	±30ppm
Temperature Stability	±30ppm @ 0 C to 70 C
Calibration mode	Parallel
Crystal Load Capacitance	18 pF
Shunt Capacitance	6 pF maximum

Series Resistance, Rs	50 Ω maximum
Drive Level	200 uW maximum
Aging	±5.0 ppm per year maximum
Insulation Resistance	500 MΩ minimum @ DC 100 V

7.3 Discrete/Integrated Magnetics Specification

Table 10. Discrete/Integrated Magnetics Specification

Criteria	Condition	Values (Min/Max)
Voltage Isolation	At 50 to 60 Hz for 60 seconds	1500 Vrms (min)
	For 60 seconds	2250 V dc (min)
Open Circuit Inductance (OCL) or OCL (alternate)	With 8 mA DC bias at 25 °C	400 µH (min)
	With 8 mA DC bias at 0 °C to 70 °C	350 µH (min)
Insertion Loss	100 kHz through 999 kHz 1.0 MHz through 60 MHz 60.1 MHz through 80 MHz 80.1 MHz through 100 MHz 100.1 MHz through 125 MHz	1 dB (max) 0.6 dB (max) 0.8 dB (max) 1.0 dB (max) 2.4 dB (max)
Return Loss	1.0 MHz through 40 MHz 40.1 MHz through 100 MHz When reference impedance si 85 Ω, 100 Ω, and 115 Ω. Note that return loss values might vary with MDI trace lengths. The LAN magnetics might need to be measured in the platform where it is used.	18 dB (min) 12 to 20 * LOG (frequency in MHz / 80) dB (min)
Crosstalk Isolation Discrete Modules	1.0 MHz through 29.9 MHz 30 MHz through 250 MHz 250.1 MHz through 375 MHz	-50.3+(8.8*(freq in MHz / 30)) dB (max) -26-(16.8*(LOG(freq in MHz / 250)))) dB (max) -26 dB (max)
Crosstalk Isolation Integrated Modules	1.0 MHz through 10 MHz 10.1 MHz through 100 MHz 100.1 MHz through 375 MHz	-50.8+(8.8*(freq in MHz / 10)) dB (max) -26-(16.8*(LOG(freq in MHz / 100)))) dB (max) -26 dB (max)
Diff to CMR	1.0 MHz through 29.9 MHz 30 MHz through 500 MHz	-40.2+(5.3*((freq in MHz / 30)) dB (max) -22-(14*(LOG((freq in MHz / 250)))) dB (max)
CM to CMR	1.0 MHz through 270 MHz 270.1 MHz through 300 MHz 300.1 MHz through 500 MHz	-57+(38*((freq in MHz / 270)) dB (max) -17-2*((300-(freq in MHz) / 30) dB (max) -17 dB (max)

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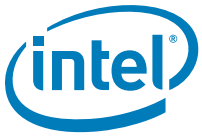


8.0 Programmers' Visible State

Table 11. PHY Register Bit Type

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to a one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to a zero and remains cleared until a read operation is performed through the management interface or a reset occurs.
Retain	Value written to a register field does take effect without a software reset.
RES	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RO	Read only
ROC	Read only clear; After read, register field is cleared to zero.
R/W	Read/write
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register is read, the register field is cleared to zero.
RWR	Read/Write reset. All bits are readable and writable. After reset the register field is cleared to zero.
RWS	Read/Write set. All bits are readable and writable. After reset the register field is set to a non-zero value specified in the text.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is cleared to zero when the function is complete.
Update	Value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.
WO	Write only. Reads to this type of register field return undefined data.

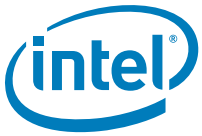


Table 12. Base PHY Register Summary

Offset	Name
0	Control Register
1	Status Register
2	PHY identifier
3	PHY identifier2
4	Auto negotiation Advertisement Register
5	Link Partner Ability Register
6	Auto negotiation Expansion Register
16	PHY Specific Control Register
17	PHY Specific Status Register
18	Interrupt Enable Register
19	Interrupt Status Register
20	SmartSpeed Control Register
21	Receive Error Counter Register
22	Virtual Cable Tester Control Register
24	LED Control Register
25	Manual LED Override Register
28	Virtual Cable Tester Status Register
29	Adresss Port of Extended Register
30	Data Port of Extended Register

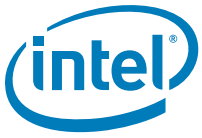
Table 13. Control PHY Register Descriptions (Address Offset = 0x00, or 0d00)

Bits	Symbol	Type		Description
15	Reset	Mode	R/W	PHY Software Reset. Writing a "1" to this bit causes the PHY to be partially reset. This bit is cleared after Write operation. The reset takes effect immediately after the bit is set. 1= PHY reset 0 =Normal operation
		HW Rst	0	
		SW Rst	SC	
14	Loopback	Mode	R/W	When loopback is activated, the transmitter data presented on MII TXD is looped back to MII RXD internally. Link is broken when loopback is enabled. 1 = Enable Loopback 0 = Disable Loopback
		HW Rst	0	
		SW Rst	0	
13	Speed Selection (LSB)	Mode	R/W	Upon hardware reset, this bit and 0.6 bit are determined by anen (bit0.12) and speed_i (phycore interface pin): anen {0.6 , 0.13} 0 {1'b0, speed_i} 1 2'b01 (00:10Mbps; 01:100Mbps; 10,11:Reserved)
		HW Rst	See Desc.	
		SW Rst		
12	Auto-negotiation	Mode	R/W	This bit determined by ANEN_i (phycore interface pin) upon hardware reset. 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
		HW Rst	See Desc.	
		SW Rst		
11	Power Down	Mode	R/W	When PHY is switched from power down to normal operation, software reset and Auto-Negotiation Restart are performed even bit Reset (0.15) or bit Restart Auto-Negotiation (0.9) is not set. 1 = Power down 0 = Normal operation
		HW Rst	0	
		SW Rst	0	
10	Isolate	Mode	R/W	Not implemented. (The GMII/MII/TBI output pins are tri-stated when this bit is set to 1. The GMII/MII/TBI inputs are ignored. 1 = Isolate 0 = Normal operation)
		HW Rst	0	
		SW Rst	0	
9	Restart Auto-negotiation	Mode	R/W,SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
		HW Rst	0	
		SW Rst	SC	
8	Duplex Mode	Mode	RW,SC	Upon hardware reset , this bit depends on duplex_i (phycore interface signal) and anen bit(0.12): 0.12 0.8 0 0 1 duplex_i 1:Full Duplex 0 :Half Duplex
		HW Rst	See Desc.	
		SW Rst		

7	Collision Test	Mode	R/W	Setting this bit to 1 will cause the COL pin to assert whenever the TX_EN pin is asserted. 1 = Enable COL signal test 0 = Disable COL signal test
		HW Rst	0	
		SW Rst	0	
6	Speed Selection (MSB)	Mode	R/W	See bit 0.13
		HW Rst	See Desc.	
		SW Rst		
5:0	Reserved	Mode	RO	Will always be 00000.
		HW Rst	00000	
		SW Rst	00000	

Table 14. Status PHY Register (Address Offset = 0x01, or 0d01)

Bits	Symbol	Type		Description
15	100BASE-T4	Mode	RO	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
		HW Rst	Always 0	
		SW Rst	Always 0	
14	100BASE-X Full-Duplex	Mode	RO	Capable of 100-Tx Full Duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
13	100BASE-X Half-Duplex	Mode	RO	Capable of 100-Tx Half Duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
12	10 Mbps Full-Duplex	Mode	RO	Capable of 10Base-T full duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
11	10 Mbs Half-Duplex	Mode	RO	Capable of 10Base-T half duplex operation
		HW Rst	Always 1	
		SW Rst	Always 1	
10	100BASE-T2 Full-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst	Always 0	
		SW Rst	Always 0	
9	100BASE-T2 Half-Duplex	Mode	RO	Not able to perform 100BASE-T2
		HW Rst	Always 0	
		SW Rst	Always 0	
8	Extended Status	Mode	RO	Extended status information in register15
		HW Rst	Always 1	
		SW Rst	Always 1	
7	Reserved	Mode	RO	
		HW Rst	Always 0	
		SW Rst	Always 0	



6	MF Preamble Suppression	Mode	RO	PHY accepts management frames with preamble suppressed
		HW Rst	Always 1	
		SW Rst	Always 1	
5	Auto-Negotiation Complete	Mode	RO	1: Auto negotiation process complete 0:Auto negotiation process not complete
		HW Rst	0	
		SW Rst	0	
4	Remote Fault	Mode	RO,LH	1: Remote fault condition detected 0:Remote fault condition not detected
		HW Rst	0	
		SW Rst	0	
3	Auto-Negotiation Ability	Mode	RO	1 : PHY able to perform auto negotiation
		HW Rst	Always 1	
		SW Rst	Always 1	
2	Link Status	Mode	RO,LL	This register bit indicates whether the link was lost since the last read operation of this bit. Register bit 17.10 (Link Real Time) reflects real-time link status. 1 = Link is up 0 = Link is down or lost since last Read Operation
		HW Rst	0	
		SW Rst	0	
1	Jabber Detect	Mode	RO,LH	1: Jabber condition detected 0: Jabber condition not detected
		HW Rst	0	
		SW Rst	0	
0	Extended Capbility	Mode	RO	1: Extended register capabilities
		HW Rst	Always 1	
		SW Rst	Always 1	

Table 15. PHY Identifier (Address Offset = 0x02, or 0d02)

Bits	Symbol	Type		Description
15:0	Organizationally Unique Identifier (OUI) Bit 3:18	Mode	RO	Organizationally Unique Identifier bits 3:18
		HW Rst	Always	
		SW Rst	Always	

Table 16. PHY iIdentifier2 (Address Offset = 0x03, or 0d03)

Bits	Symbol	Type		Description
15: 0	OUI bit 19:24 Model Number Revision Number	Mode	RO	Organizationally Unique Identifier bits 19:24 Bit 9:0 is set by PHY interface pins mn[5:0] and rn[3:0].
		HW Rst	Always	
		SW Rst	Always	

Table 17. Auto-Negotiation Advertisement PHY Register (Address Offset = 0x04, or 0d04)

Bits	Symbol	Type		Description
15	Reserved	Mode	R/W	Reserved
		HW Rst	0	
		SW Rst	Update	
14	Ack	Mode	RO	Must be 0
		HW Rst	Always 0	
		SW Rst	Always 0	
13	Remote Fault	Mode	R/W	1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
		HW Rst	0	
		SW Rst	Update	
12	Reserved	Mode	RO	Always 0.
		HW Rst	Always 0	
		SW Rst	Always 0	
11	Asymmetric Pause	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: • Software reset is asserted (register 0.15) • Restart Auto-Negotiation is asserted (register 0.9) • Power down (register 0.11) transitions from power down to normal operation • Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause (this bit has added the pad control and can be set from the F001 top, its default value is one)
		HW Rst	1	
		SW Rst	Update	
10	PAUSE	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: • Software reset is asserted (register 0.15) • Restart Auto-Negotiation is asserted (register 0.9) • Power down (register 0.11) transitions from power down to normal operation • Link goes down 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented (this bit has added the pad control and can be set from the F001 top, its default value is one)
		HW Rst	1	
		SW Rst	Update	
9	100BASE-T4	Mode	RO	Not able to perform 100BASE-T4
		HW Rst	Always 0	
		SW Rst	Always 0	

8	100BASE-TX Full Duplex	Mode	RW	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: • Software reset is asserted (register 0.15) • Restart Auto-Negotiation is asserted (register 0.9) • Power down (register 0.11) transitions from power down to normal operation • Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
7	100BASE-TX Half Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: • Software reset is asserted (register 0.15) • Restart Auto-Negotiation is asserted (register 0.9) • Power down (register 0.11) transitions from power down to normal operation • Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
6	10BASE-TX Full Duplex	Mode	R/W	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: • Software reset is asserted (register 0.15) • Restart Auto-Negotiation is asserted (register 0.9) • Power down (register 0.11) transitions from power down to normal operation • Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
5	10BASE-TX Half Duplex	Mode	RW	The value of this bit will be updated immediately after writing this register. But the value written to this bit does not takes effect until any one of the following occurs: • Software reset is asserted (register 0.15) • Restart Auto-Negotiation is asserted (register 0.9) • Power down (register 0.11) transitions from power down to normal operation • Link goes down 1 = Advertise 0 = Not advertised
		HW Rst	1	
		SW Rst	Update	
4:0	Selector field	Mode	RO	Selector Field mode 00001 = 802.3
		HW Rst	Always 00001	
		SW Rst	Always 00001	

Table 18. Link partner ability PHY register, base page (Address Offset = 0x05, or 0d05)

Bits	Symbol	Type		Description
15	Reserved	Mode	RO	Reserved
		HW Rst	0	
		SW Rst	0	
14	Ack	Mode	RO	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
		HW Rst	0	
		SW Rst	0	

13	Remote Fault	Mode	RO	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
		HW Rst	0	
		SW Rst	0	
12	Reserved	Mode	RO	Technology Ability Field Received Code Word Bit 12
		HW Rst	0	
		SW Rst	0	
11	Asymmetric Pause	Mode	RO	Technology Ability Field Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
		HW Rst	0	
		SW Rst	0	
10	PAUSE	Mode	RO	Technology Ability Field Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
		HW Rst	0	
		SW Rst	0	
9	100BASE-T4	Mode	RO	Technology Ability Field Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
		HW Rst	0	
		SW Rst		
8	100BASE-TX Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
		HW Rst	0	
		SW Rst	0	
7	100BASE-TX Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
		HW Rst	0	
		SW Rst	0	
6	10BASE-TX Full Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
		HW Rst	0	
		SW Rst	0	
5	10BASE-TX Half Duplex	Mode	RO	Technology Ability Field Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
		HW Rst	0	
		SW Rst	0	

4:0	Selector field	Mode	RO	Selector Field Received Code Word Bit 4:0
		HW Rst	00000	
		SW Rst	00000	

Note: The values contained in reg5 are only guaranteed to be valid once auto-negotiation has successfully completed, as indicated by bit 1.5.

Table 19. Auto-Negotiation expansion PHY register (Address Offset = 0x06, or 0d06)

Bits	Symbol	Type		Description
15:5	Reserved	Mode	RO	Reserved. Must be 0.
		HW Rst	Always 0x000	
		SW Rst	Always 0x000	
4	Parallel Detection fault	Mode	RO,LH	1: a fault has been detect 0: no fault has been detected
		HW Rst	0	
		SW Rst	0	
3	Reserved	Mode	RO	
		HW Rst	0	
		SW Rst	0	
2	Reserved	Mode	R/W	
		HW Rst	1	
		SW Rst	1	
1	Page received	Mode	RO,LH	1: A new page has been received 0: No new page has been received
		HW Rst	0	
		SW Rst	0	
0	Link Partner Auto negotiation able	Mode	RO	1: Link partner is auto negotiation able 0: Link partner is not auto negotiation able
		HW Rst	0	
		SW Rst	0	

Table 20. Function Control PHY register (Address Offset = 0x10, or 0d16)

Bits	Symbol	Type		Description
15:12	Reserved	h/s w	0	Always 0
11	Assert CRS on Transmit	Mode	R/W	11
		HW Rst	0	
		SW Rst	Retain	

10	Reserved	h/s w	0	Always 0
9:8	Energy Detect	Mode	R/W	0x = Off 10 = Sense only on Receive (Energy Detect) 11 = Sense and periodically transmit NLP
		HW Rst	0	
		SW Rst	Retain	
6:5	MDI Crossover Mode	Mode	R/W	Changes to these bits are disruptive to the normal operation; therefore any changes to these registers must be followed by a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
		HW Rst	11	
		SW Rst	Update	
4:3	Reserved	h/s w	0	Always 0
2	SQE Test	Mode	R/W	SQE Test is automatically disabled in full-duplex mode regardless of the state of register 16.2 1 = SQE test enabled 0 = SQE test disabled
		HW Rst	0	
		SW Rst	Retain	
1	Polarity Reversal	Mode	R/W	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled
		HW Rst	0	
		SW Rst	Retain	
0	Disable Jabber	Mode	R/W	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function
		HW Rst	0	
		SW Rst	Retain	

Table 21. PHY specific status PHY register (Address Offset = 0x11, or 0d17)

Bits	Symbol	Type		Description
15:14	Speed	Mode	RO	These status bits are valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = Reserved 01 = 100 Mbps 00 = 10 Mbps
		HW Rst	00	
		SW Rst	Retain	
13	Duplex	Mode	RO	This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
		HW Rst	0	
		SW Rst	Retain	
12	Page Received (real-time)	Mode	RO	1 = Page received 0 = Page not received
		HW Rst	0	
		SW Rst	Retain	

11	Speed and Duplex Resolved	Mode	RO	1 = Resolved 0 = Not resolved When Auto-Negotiation is disabled, this bit will be set for force speed mode.
		HW Rst	0	
		SW Rst	0	
10	Link (real-time)	Mode	RO	1 = Link up 0 = Link down
		HW Rst	0	
		SW Rst	0	
9：7	reserved	Mode	RO	Always 0
		HW Rst	0	
		SW Rst	0	
6	MDI Crossover Status	Mode	RO	This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual configuration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI
		HW Rst	0	
		SW Rst	Retain	
5	Smartspeed downgrade	Mode	RO	1 = Downgrade 0 = No Downgrade
		HW Rst	0	
		SW Rst	0	
4	Energy Detect Status	Mode	RO	1 = Sleep 0 = Active
		HW Rst	0	
		SW Rst	0	
3	Transmit Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disabled
		HW Rst	0	
		SW Rst	Retain	
2	Receive Pause Enabled	Mode	RO	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
		HW Rst	0	
		SW Rst	Retain	
1	Polarity (real time)	Mode	RO	1 = Reversed 0 = Normal
		HW Rst	0	
		SW Rst	0	
0	Jabber (real time)	Mode	RO	1 = Jabber 0 = No jabber
		HW Rst	0	
		SW Rst	Retain	

Table 22. Interrupt enable PHY register (Address Offset = 0x12, or 0d18)

Bits	Symbol	Type		Description
15	Auto-Negotiation Error Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
14	Speed Changed Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
13	Duplex Changed Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
12	Page Received Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
11	Auto-Negotiation Completed Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
10	Link Status Changed Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
9	Symbol Error Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
8	False Carrier Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
7	FIFO Over/ Underflow Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
6	MDI Crossover Changed Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	

5	Smartspeed-downgrade Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
4	Energy Detect Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
3:2	Reserved	h/s w	0	Always 00.
1	Polarity Changed Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	
0	Jabber Interrupt Enable	Mode	RW	1 = Interrupt enable 0 = Interrupt disable
		HW Rst	0	
		SW Rst	Retain	

Table 23. Interrupt status PHY register (Address Offset = 0x13, or 0d19)

Bits	Symbol	Type		Description
15	Auto-Negotiation Error	Mode	RO, LH	An error will occur if there are parallel detect fault, no common HCD, or link failure after negotiation completes. 1 = Auto-Negotiation Error 0 = No Auto-Negotiation Error
		HW Rst	0	
		SW Rst	Retain	
14	Speed Changed	Mode	RO, LH	1 = Speed changed 0 = Speed not changed
		HW Rst	0	
		SW Rst	Retain	
13	Duplex Changed	Mode	RO, LH	1 = Duplex changed 0 = Duplex not changed
		HW Rst	0	
		SW Rst	Retain	
12	Page Received	Mode	RO	1 = Page received 0 = Page not received
		HW Rst	0	
		SW Rst	Retain	
11	Auto-Negotiation Completed	Mode	RO	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
		HW Rst	0	
		SW Rst	Retain	

10	Link Status Changed	Mode	RO, LH	1 = Link status changed 0 = Link status not changed
		HW Rst	0	
		SW Rst	Retain	
9	Symbol Error	Mode	RO, LH	1 = Symbol error 0 = No symbol error
		HW Rst	0	
		SW Rst	Retain	
8	False Carrier	Mode	RO, LH	1 = False carrier 0 = No false carrier
		HW Rst	0	
		SW Rst	Retain	
7	Reserved	Mode	RO, LH	
		HW Rst	0	
		SW Rst	Retain	
6	MDI Crossover Changed	Mode	RO, LH	1 = Crossover changed 0 = Crossover not changed
		HW Rst	0	
		SW Rst	Retain	
5	Smartspeed-downgrade Interrupt	Mode	RO, LH	1 = Smartspeed-downgrade detected. 0 = No Smartspeed-downgrade.
		HW Rst	0	
		SW Rst	Retain	
4	Energy Detect Changed	Mode	RO, LH	1 = Energy Detect state changed 0 = No Energy Detect state change detected
		HW Rst	0	
		SW Rst	Retain	Not implement, always 0.
3:2	reserved	h/s w	0	Always 00
1	Polarity Changed	Mode	RO, LH	1 = Polarity Changed 0 = Polarity not changed
		HW Rst	0	
		SW Rst	Retain	
0	Jabber	Mode	RO, LH	1 = Jabber 0 = No jabber
		HW Rst	0	
		SW Rst	Retain	

Table 24. SmartSpeed Control PHY Register (Address Offset = 0x14, or 0d20)

15:11	reserved	Mode	RO	Reserved. Must be 00000000.
		HW Rst	0	
		SW Rst	0	

9	aneg_now_qual	Mode	R/W	Set this bit to 1 to cause the PHY to restart autonegotiation.
		HW Rst	1'b0	
		SW Rst	Retain	
9	Rev_aneg_qual	Mode	R/W	Make PHY to auto-negotiate in reversed mode.
		HW Rst	1'b0	
		SW Rst	Update	
8	Reserved	Mode	R/W	Reserved
		HW Rst	1'b0	
		SW Rst	Update	
7	Cfg_pad_en	Mode	R/W	The default value is zero; if this bit is set to one, then the auto negotiation Arbitration FSM will bypass the LINK_STATUS_CHECK state when the 10BASE-T/100BASE-TX ready signal is asserted.
		HW Rst	0	
		SW Rst	Update	
6	Mr_ltdis	Mode	R/W	The default value is zero; if this bit is set to one, then the NLP Receive Link Integrity Test FSM will stays at the NLP_TEST_PASS state.
		HW Rst	0	
		SW Rst	Update	
5	SmartSpeed_en	Mode	R/W	The default value is one; if this bit is set to one and cable inhibits completion of the training phase, then After a few failed attempts, PHY automatically downgrades the highest ability to the next lower speed: from 100 to 10.
		HW Rst	1	
		SW Rst	Update	
4:2	SmartSpeed_retry_limit	Mode	R/W	The default value is three; if these bits are set to three, then the PHY will attempt five times before downgrading; The number of attempts can be changed through setting these bits.
		HW Rst	011	
		SW Rst	Update	
1	Bypass_smartSpeed_timer	Mode	R/W	The default value is zero; if this bit is set to one, the SmartSpeed FSM will bypass the timer used for stability.
		HW Rst	0	
		SW Rst	Update	
0	reserved	Mode	RO	Reserved. Must be 0.
		HW Rst	0	
		SW Rst	0	

Table 25. Receive error counter PHY register (Address Offset = 0x15, or 0d21)

15:0	Receive Error Count	Mode	RO	Counter will peg at 0xFFFF and will not roll over. (when rx_dv is valid, count rx_er numbers) (in this version, only for 100Base-TX)
		HW Rst	0x0000	
		SW Rst	Retain	

Table 26. Virtual cable tester control PHY register (Address Offset = 0x16, or 0d22)

15:10	Reserved	Mode	RO	Reserved.
		HW Rst	Always 0	
		SW Rst	Always 0	
9:8	MDI Pair Select	Mode	RW	Virtual Cable Tester™ Control registers. Use the Virtual Cable Tester Control Registers to select which MDI pair is shown in the Virtual Cable Tester Status register. 00 = MDI[0] pair 01 = MDI[1] pair 10 = Reserved 11 = Reserved
		HW Rst	00	
		SW Rst	Retain	
7:1	Reserved	h/s w	0	Always 0
0	Enable Test	Mode	RW	When set, hardware automatically disables this bit when VCT is done. 1 = Enable VCT Test 0 = Disable VCT Test
		HW Rst	0	
		SW Rst	Retain	

Table 27. LED control PHY register (Address Offset = 0x18, or 0d24)

Bits	Symbol	Type		Description
15	Disable LED	Mode	R/W	0 = Enable 1 = Disable
		HW Rst	0	
		SW Rst	Retain	
14:12	Led on time	Mode	R/W	001 = 10ms 010 = 21 ms 011 = 42ms 100 = 84 ms 101 = 168ms 110 to 111 = 42ms
		HW Rst	100	
		SW Rst	Retain	

11	Force Interrupt	Mode	RO	Always 0.
		HW Rst	0	
		SW Rst	0	
10:8	Led off time	Mode	R/W	000 = 21 ms 001 = 42 ms 010 = 84 ms 011 =168 ms 100 =330 ms 101 to 111 = 168ms
		HW Rst	001	
		SW Rst	Retain	
7:5	Reserved	Mode	RO	Reserved
		HW Rst	000	
		SW Rst	Always 0	
4:3	LED_LINK control	Mode	R/W	00 = Direct LED mode 11 = Master/Slave LED mode 01, 10 = Combined LED modes
		HW Rst	0	
		SW Rst	Retain	
2	LED_DUPLEX control	Mode	R/W	0 = Duplex 1 = Duplex/Collision
		HW Rst	0	
		SW Rst	Retain	
1	LED_RX control	Mode	R/W	1 = Receive activity/Link 0 = Receive activity
		HW Rst	0	
		SW Rst	Retain	
0	LED_TX Control	Mode	R/W	1 = Activity/Link 0 = Transmit activity
		HW Rst	0	
		SW Rst	Retain	

Table 28. Manual LED override PHY register (Address Offset = 0x19, or 0d25)

Bits	Symbol	Type		Description
15:12	Reserved	Mode	RO	Reserved.
		HW Rst	Always 0	
		SW Rst	Always 0	
11:10	LED_ DUPLEX	Mode	R/W	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
		HW Rst	00	
		SW Rst	Retain	

9:8	LED_LINK10	Mode	R/W	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
		HW Rst	00	
		SW Rst	Retain	
7:6	LED_LINK100	Mode	R/W	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
		HW Rst	00	
		SW Rst	Retain	
5:4	Reserved	Mode	R/W	Reserved
		HW Rst	00	
		SW Rst	Retain	
3:2	LED_RX	Mode	R/W	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
		HW Rst	00	
		SW Rst	Retain	
1:0	LED_TX	Mode	R/W	LED "Off" means LED pin output equals high. LED "On" means LED pin output equals low. 00 = Normal 01 = Blink 10 = LED Off 11 = LED On
		HW Rst	00	
		SW Rst	Retain	

Table 29. Virtual cable tester status PHY register (Address Offset = 0x1c, or 0d28)

Bits	Symbol	Type		Description
15:10	Reserved	Mode	RO	Reserved.
		HW Rst	Always 0	
		SW Rst	Always 0	
9:8	Status	Mode	RO	The content of the Virtual Cable Tester Status Registers applies to the cable pair selected in the Virtual Cable Tester™ Control Registers. 11 = Test Fail 00 = Valid test, normal cable (no short or open in cable) 10 = Valid test, open in cable (Impedance > 333 ohms) 01 = Valid test, short in cable (Impedance < 33 ohms)
		HW Rst	00	
		SW Rst	00	
7:0	Delta_Time	Mode	R/W	Delta time to indicate distance.
		HW Rst	0	
		SW Rst	0	

Table 30. Address Port of Extended PHY Register (Address Offset = 0x1d, or 0d29)

Bits	Symbol	Type		
15:6	Reserved	Mode	RO	The address index of the register will be write or Read.
		HW Rst	0	
		SW Rst	0	
5:0	Address Offset	Mode	R/W	The address index of the register will be Write or Read.
		HW Rst	0	
		SW Rst	0	

Table 31. Data Port of Extended PHY Register (Address Offset = 0x1e, or 0d20)

15:0	Data	Mode	R/W	The data port of extended register. address offset must be set before accessing this register.
		HW Rst	0	
		SW Rst	0	

8.1 Extended Register description

Table 32. System Mode Control 0 (Address Offset = 0x00 (Hex), or 0(Decimal))

15:6	Reserved	Mode	R/W	
		HW Rst	10'h009	
		SW Rst		
5:4	TXDAC Class AB enable	Mode	R/W	[5]: 1 enable 100BASE-TX TXDAC Class AB Mode [4]: 1 enable 10BASE-T TXDAC Class AB Mode
		HW Rst	0	
		SW Rst	Retain	
		HW Rst	2'b01	
		SW Rst	Retain	

3:0	reserved	Mode	R/W	
		HW Rst	4'hE	
		SW Rst	Retain	

Table 33. System mode control 3 (Address Offset = 0x03 (Hex), or 3(Decimal))

15	Reserved	Mode	R/W	
		HW Rst	0	
		SW Rst	0	
14	First_LUFrame_TX	Mode	R/W	1 = the frame with link_status(register17.10) asserted in the middle of the frame will not be transmitted at all; 0 = frames will be transmitted when link is up.
		HW Rst	0	
		SW Rst	Retain	
13	Phy_pll_on	Mode	R/W	PLL control bit, makes AND connection with input pin phy_pll_on to control PLL, 1 = PLL is always on, except iddq mode; 0 = PLL is control by hibernate module.
		HW Rst	1	
		SW Rst	Retain	
12:11	reesrved	Mode	R/W	
		HW Rst	2'b11	
		SW Rst	Retain	
10	LED test control	Mode	R/W	1: when power on reset, the LED will not light. 0: when power on reset, the LED will light for 2.5s.
		HW Rst	0	
		SW Rst	Retain	
9:0	reserved	Mode	R/W	
		HW Rst	10'h3FF	
		SW Rst	Retain	

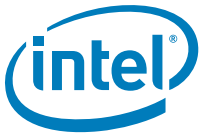


Table 34. Hibernation Mode Control Register (Address Offset = 0x0b (Hex), or 11 (Decimal))

15	Ps_hib_en	Mode	R/W	Power hibernate control bit; 1: hibernate enable 0: hibernate disable
		HW Rst	1	
		SW Rst	retain	
14	Wake_mode	Mode	R/W	1:PHY wake up by energy detect or wake up pin 0:PHY wake up only by energy detect
		HW Rst	0	
		SW Rst	retain	
13	reserved	Mode	R/W	
		HW Rst	1	
		SW Rst	retain	
12	Hib_pulse_sw	Mode	R/W	1: when hibernate, PHY sends NLP pulse and detects signal from cable. 0: when hibernate, PHY doesn't send NLP pulse and only detects signal from cable.
		HW Rst	1	
		SW Rst	retain	
11	Gate_25m_en_sw	Mode	R/W	1:when hibernate, shut off 25m clock of auto-negotiation 0:25m clock to auto-negotiation is not controlled by hibernate
		HW Rst	1	
		SW Rst	retain	
10:0	reserved	Mode	R/W	
		HW Rst	11'h400	
		SW Rst	retain	

Table 35. 100BASE-TX Test Mode Register (Address Offset = 0x10 (Hex), or 16 (Decimal))

15	TM100_ENA	Mode	R/W	Enable 100BASE-TX loopback test mode.
		HW Rst	0	
		SW Rst	Retain	
14:8	Reversed	Mode	R/W	Always 0.
		HW Rst	7'h00	
		SW Rst	0	

7	Jitter_test	Mode	R/W	100BASE-TX jitter test
		HW Rst	0	
		SW Rst	Retain	
6	Os_test	Mode	R/W	100BASE-TX over-shoot test
		HW Rst	0	
		SW Rst	Retain	
5	Dcd_test	Mode	R/W	100BASE-TX DCD test
		HW Rst	0	
		SW Rst	Retain	
4	PMD_LPBK_2	Mode	R/W	PMA loopback, test MLT-3 Encoder and MLT-3 Decoder
		HW Rst	0	
		SW Rst	0	
3	PMD_LPBK_1	Mode	R/W	PMD loopback, test Scrambler and Descrambler
		HW Rst	0	
		SW Rst	0	
2	PMA_LPBK_2	Mode	R/W	PMA loopback, test Carrier Detect and Link Monitor
		HW Rst	0	
		SW Rst	0	
1	PMA_LPBK_1	Mode	R/W	PMA loopback, test FEF Generator and FEF Detector
		HW Rst	0	
		SW Rst	0	
0	PCS_LPBK	Mode	R/W	PCS loopback, test pcs_tx and pcs_rx
		HW Rst	0	
		SW Rst	0	

Table 36. 10BASE-T Test Mode Register (Address Offset = 0x12 (Hex), or 18 (Decimal))

15:14	reserved	Mode	R/W	
		HW Rst	10'h120	
		SW Rst	Retain	
5	Test_mode[2]	Mode	R/W	bit2 of 3-bit test_mode[2:0]. See bit 1:0 of this register.
		HW Rst	0	
		SW Rst	0	
4:3	reserved	HW Rst	2'b00	
		SW Rst	0	
		SW Rst	retain	
2	Loopback mode select	Mode	R/W	1: lpbk2—deep in Loopback mode 0: lpbk1—shallow in Loopback mode (connect to dig10.test_mode_i[0])
		HW Rst	0	
		SW Rst	0	
1:0	Test_mode[1:0]	Mode	R/W	Combined with bit5: [001]: packet with all ones, 10MHz sine wave [010]: pseudo random, [011]: normal link pulse only, [100]: 5MHz sin wave. Others: normal mode.
		HW Rst	0	
		SW Rst	0	

Table 37. Power Saving Control (Address Offset = 0x29 (Hex), or 41 (Decimal))

15	Top_ps_en	Mode	RO	1: top level power saving enable 0: top level power saving disable
		HW Rst	1	
		SW Rst	retained	
14:12	Reserved	Mode	R/W	
		HW Rst	3'h3	
		SW Rst	retained	

11:9	Dac_amp_100	Mode	R/W	Control amplitude of transmit signal in 100BT mode
		HW Rst	3'h3	
		SW Rst	retained	
8:6	Dac_amp_10	Mode	R/W	Control amplitude of transmit signal in 100BT mode
		HW Rst	3'h3	
		SW Rst	retained	
5:1	reserved	Mode	R/W	
		HW Rst	0	
		SW Rst	0	
0	Reserved	Mode	R/W	
		HW Rst	1	
		SW Rst	retained	

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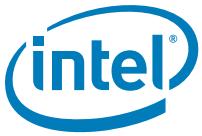


9.0 Non-Volatile Memory (NVM)

9.1 Introduction

This section is intended for designs using a 10/100 Mb/s LAN controller that is integrated into an Intel® Platform Control Hub (PCH) device in conjunction with an the 82552V Physical Layer Transceiver (PHY).

There are several LAN clients that might access the NVM such as hardware, LAN driver, and BIOS. Refer to the *I/O Control Hub 5, 6, and 7 EEPROM Map and Programming Information.* and the *Intel®10/100 Mbps Ethernet Controller Family Software Technical Reference Manual*, both from Intel, for more details.

Unless otherwise specified, all numbers in this section use the following numbering convention:

- Numbers that do not have a suffix are decimal (base 10).
- Numbers with a prefix of "0x" are hexadecimal (base 16).
- Numbers with a suffix of "b" are binary (base 2).

9.2 EEUPDATE Utility

Intel has created an EEUPDATE utility that can be used to update NVM LAN images. The tool uses two basic data files outlined in the following section (image file and MACaddress file). The EEUPDATE utility is flexible and can be used to update the entire NVM LAN region image or just the Ethernet controller MAC address. In addition, it also updates the checksum field after the region is modified. Note that other Flash programming utilities (such as FITC) might not have this capability. For more information on how to use EEUPDATE, refer to the eeupdate.txt file that is included with the EEUPDATE utility.

To obtain a copy of this program, contact your Intel representative.

9.2.1 Command Line Parameters

The DOS command format is as follows:

```
EEUPDATE Parameter_1 Parameter_2
```

where:

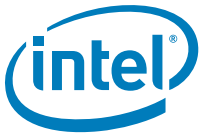
Parameter_1 = /D or /A

/D is used to update the entire region image.

/A is used to update just the Ethernet Individual Address.

Parameter_2 = filename

In Example 1, Parameter_2 is `file1.eep`, which contains the complete NVM image in a specific format used to update the complete region. All comments in the `.eep` file must be preceded by a semicolon (;).



Example 1. EEUPDATE /D file1.eep

In Example 1, Parameter 2 is `file2.dat`, which contains a list of IA addresses. The EEUPDATE utility finds the first unused address from this file and uses it to update the NVM. An address is marked used if it is followed by a date stamp. When the utility uses a specific address, a log file called eelog.dat is updated with that address. This updated file should be used as the `.dat` file for the next update.

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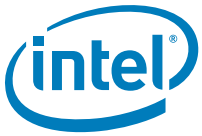
10.0 Checklists

Contact your Intel Representative for access to the 82552V Design and Board Layout Checklists.



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11.0 Reference Schematics

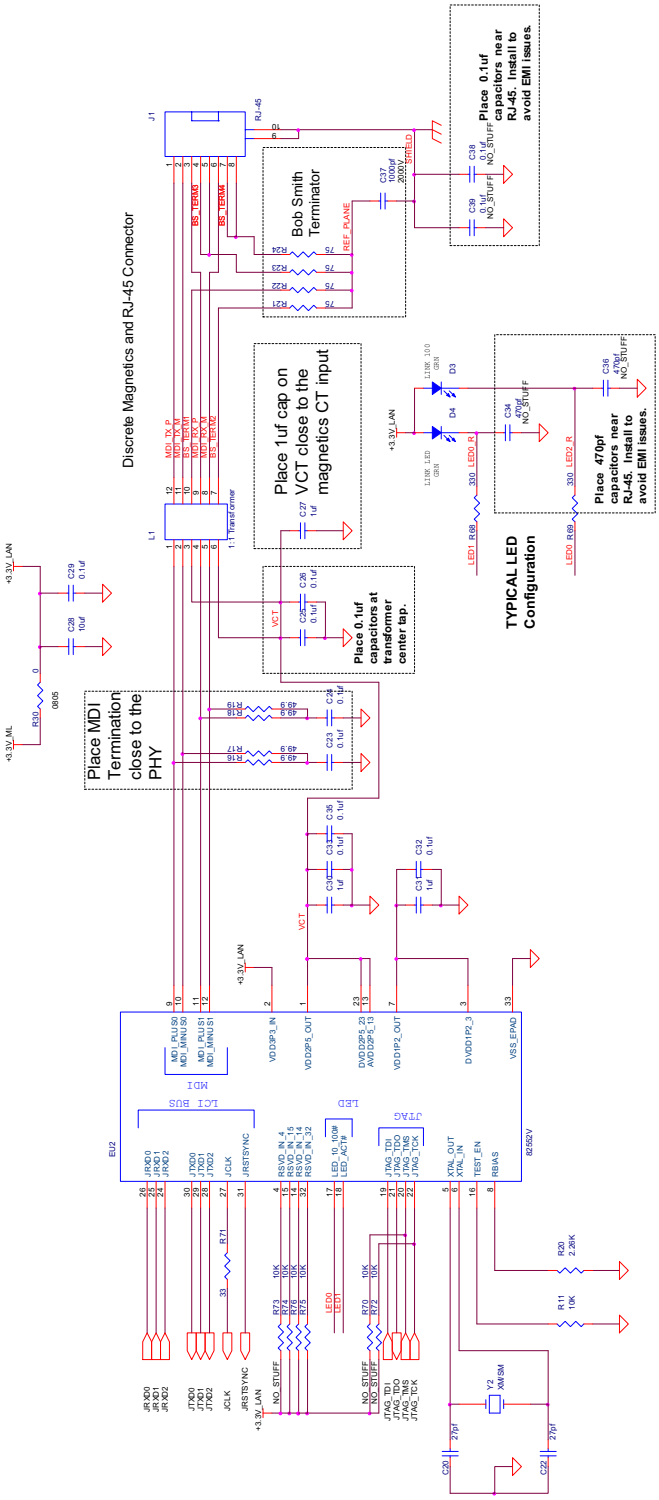


Figure 12. 82552V Reference Schematic--Discrete Magnetics

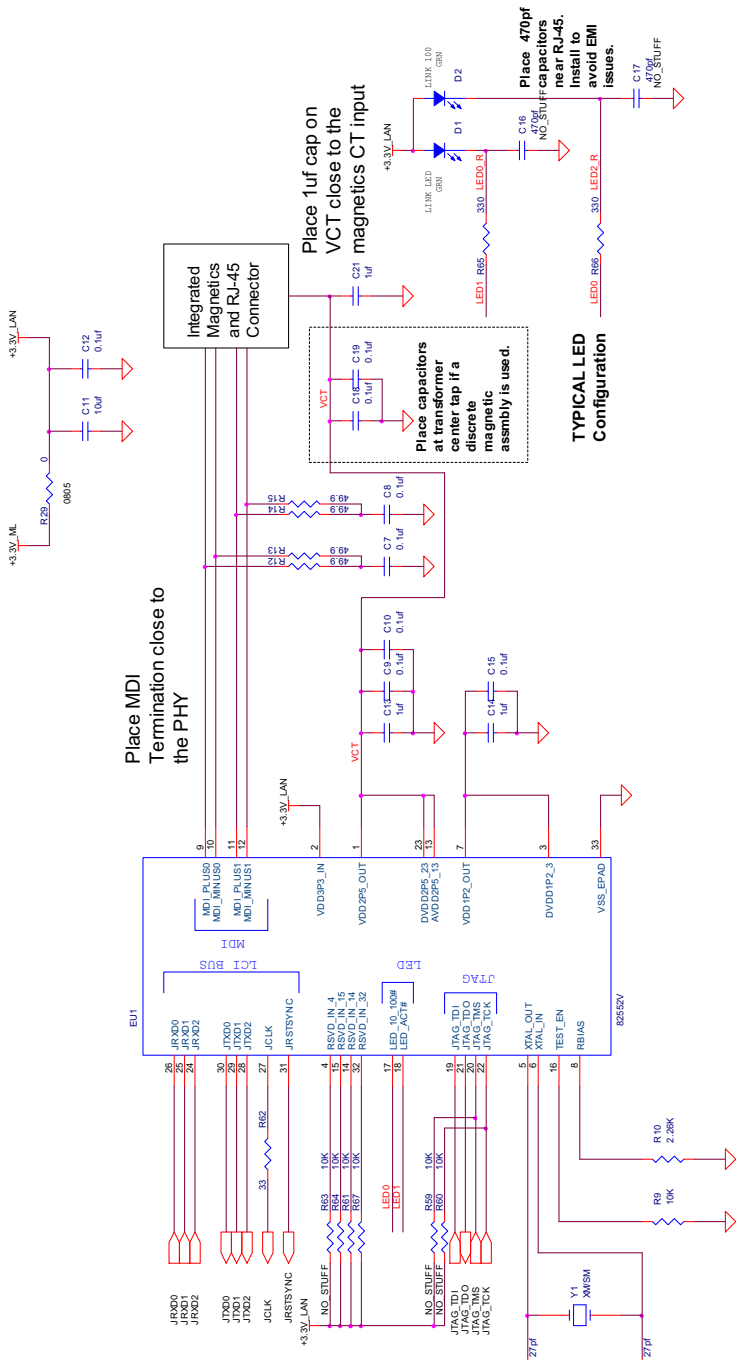
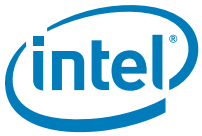


Figure 13. 82552V Schematic--Integrated Magnetics



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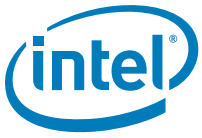
12.0 Models

Contact your Intel Representative for access to the 82552V XOR model.



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