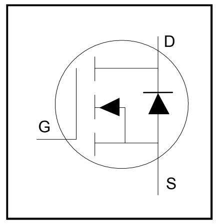
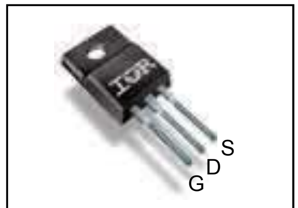
StrongIRFET™
IRFI7440GPbF

HEXFET® Power MOSFET

Application
- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters



V_{DSS}		40V
$R_{DS(on)}$	typ.	2.0mΩ
	max	2.5mΩ
I_D		95A



TO-220AB Full-Pak

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFI7440GPbF	TO-220 Full-Pak	Tube	50	IRFI7440GPbF

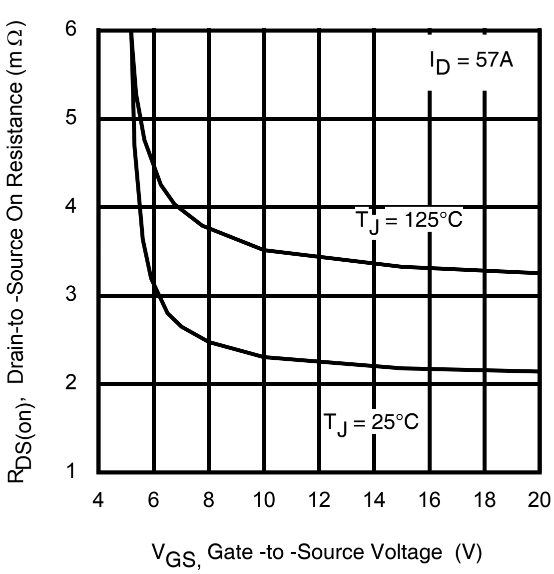


Fig 1. Typical On-Resistance vs. Gate Voltage

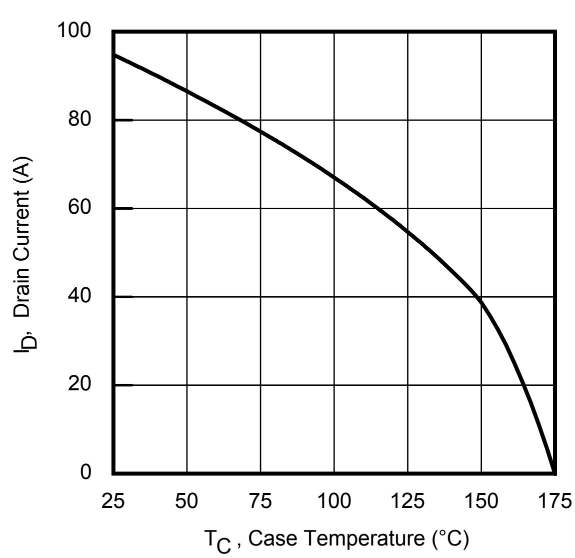


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximium Rating

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	95	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	67	
I_{DM}	Pulsed Drain Current ①	380	
P_D @T_C = 25°C	Maximum Power Dissipation	42	W
	Linear Derating Factor	0.28	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	201	mJ
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ⑧	407	
I_{AR}	Avalanche Current ①	See Fig. 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	——	3.6	°C/W
$R_{\theta JA}$	Junction-to-Ambient	——	65	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	37	——	mV/°C	Reference to 25°C, I_D = 2mA ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	2.0	2.5	mΩ	V_{GS} = 10V, I_D = 57A
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	V_{DS} = V_{GS}, I_D = 100μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	μA	V_{DS} = 40V, V_{GS} = 0V
		——	——	150		V_{DS} = 40V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
R_G	Gate Resistance	——	2.3	——	Ω	

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 124μH, R_G = 50Ω, I_{AS} = 57A, V_{GS} =10V.

③ $I_{SD} \leq$ 57A, di/dt $\leq$ 962A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.

④ Pulse width $\leq$ 400μs; duty cycle $\leq$ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

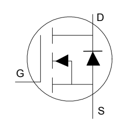
⑦ R_θ is measured at T_J approximately 90°C.

⑧ Limited by T_{Jmax}, starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 29A, V_{GS} =10V.

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	144	——	——	S	V_{DS} = 10V, I_D =57A
Q_g	Total Gate Charge	——	88	132	nC	I_D = 57A
Q_{gs}	Gate-to-Source Charge	——	22	——		V_{DS} = 20V
Q_{gd}	Gate-to-Drain Charge	——	30	——		V_{GS} = 10V
Q_{sync}	Total Gate Charge Sync. (Qg – Qgd)	——	58	——		
$t_{d(on)}$	Turn-On Delay Time	——	11	——	ns	V_{DD} = 20V
t_r	Rise Time	——	42	——		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	——	56	——		R_G= 2.7Ω
t_f	Fall Time	——	36	——		V_{GS} = 10V④
C_{iss}	Input Capacitance	——	4549	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	689	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	450	——		f = 1.0MHz, See Fig.7
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	——	835	——		V_{GS} = 0V, V_{DS} = 0V to 32V⑥
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	——	981	——		V_{GS} = 0V, V_{DS} = 0V to 32V⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)①	——	——	95	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	380		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C,I_S = 57A,V_{GS} = 0V ④
dv/dt	Peak Diode Recovery dv/dt③	——	5.1	——	V/ns	T_J = 175°C,I_S =57A, V_{DS} = 40V④
t_{rr}	Reverse Recovery Time	——	36	——	ns	T_J = 25°C V_{DD} = 34V
		——	38	——		T_J = 125°C I_F = 57A,
Q_{rr}	Reverse Recovery Charge	——	45	——	nC	T_J = 25°C di/dt = 100A/μs ④
		——	49	——		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	2.1	——	A	T_J = 25°C

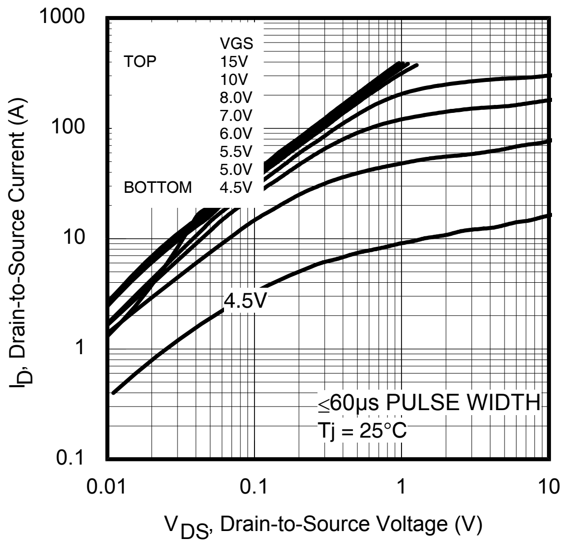


Fig 3. Typical Output Characteristics

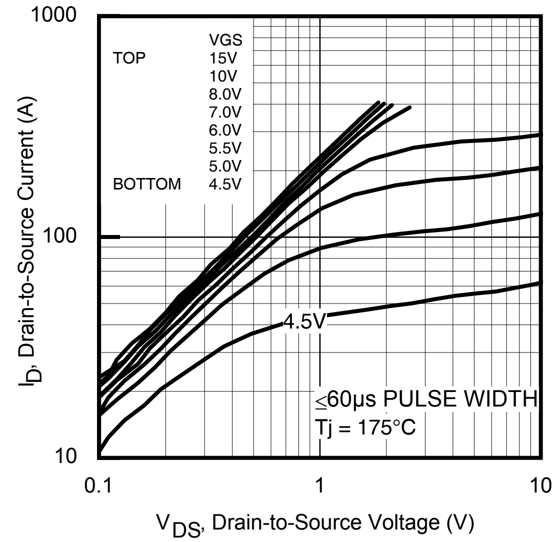


Fig 4. Typical Output Characteristics

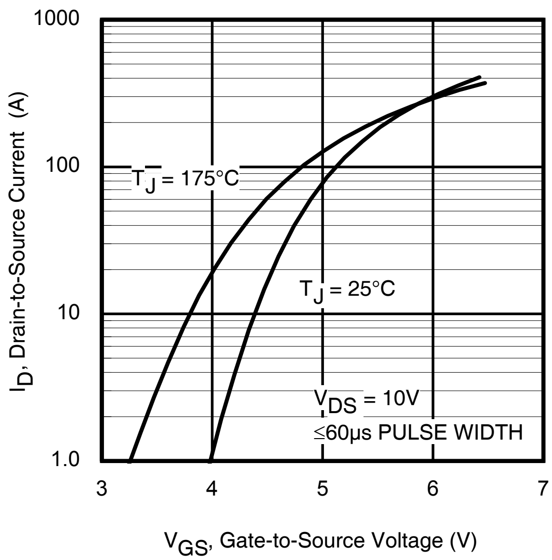


Fig 5. Typical Transfer Characteristics

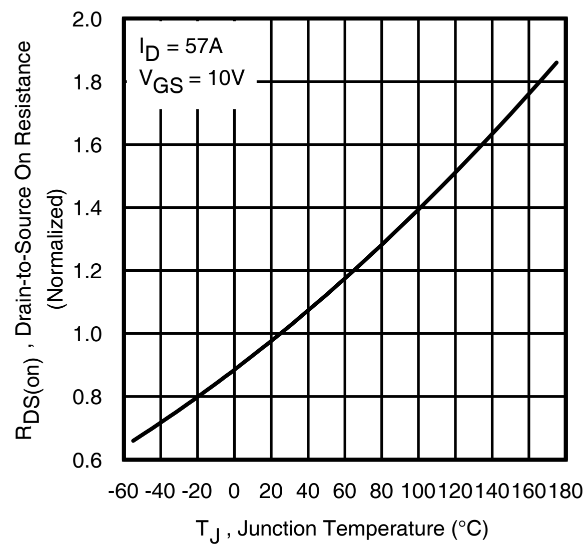


Fig 6. Normalized On-Resistance vs. Temperature

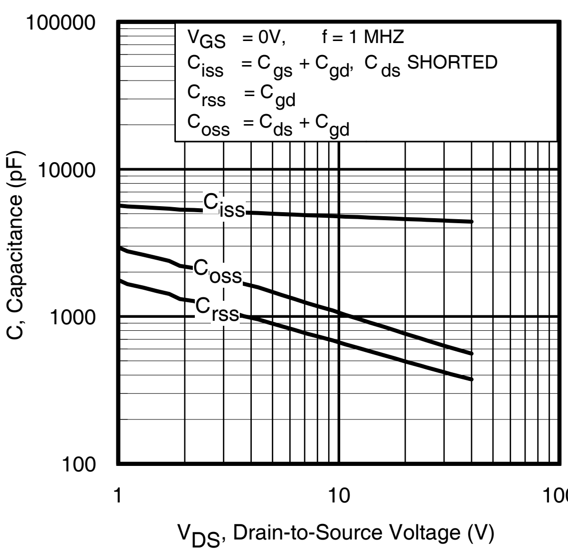


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

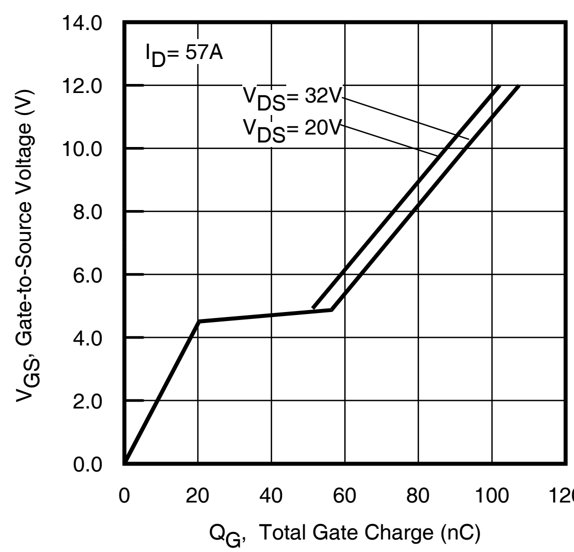


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

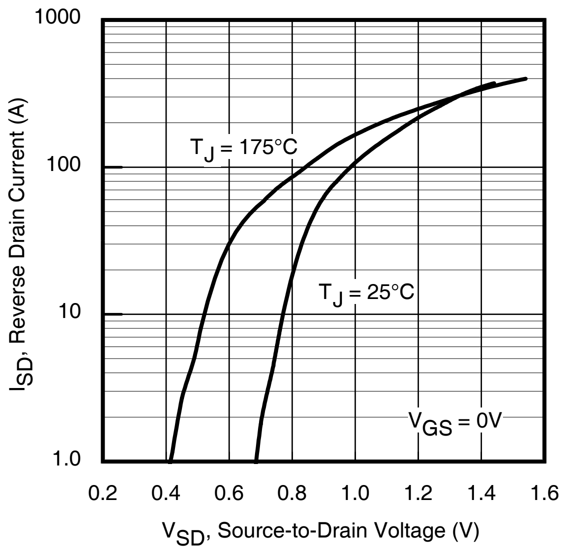


Fig 9. Typical Source-Drain Diode Forward Voltage

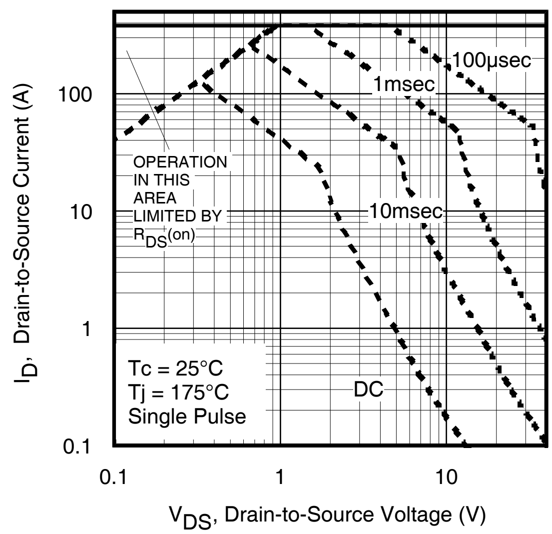


Fig 10. Maximum Safe Operating Area

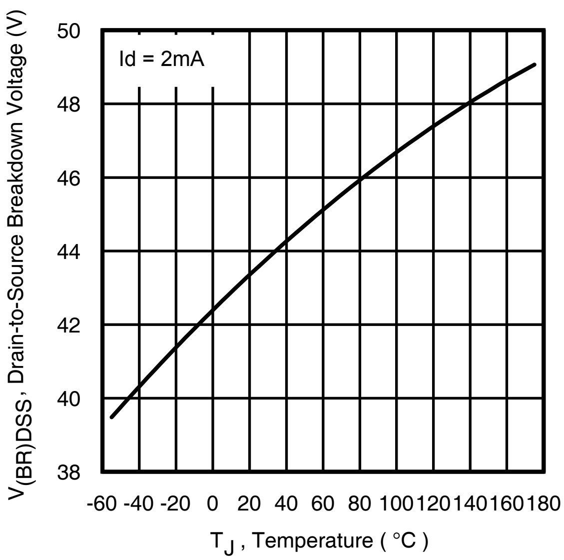


Fig 11. Drain-to-Source Breakdown Voltage

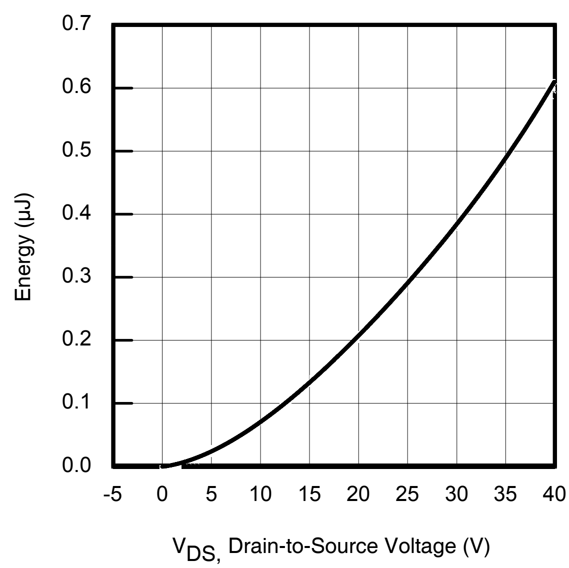


Fig 12. Typical C_{oss} Stored Energy

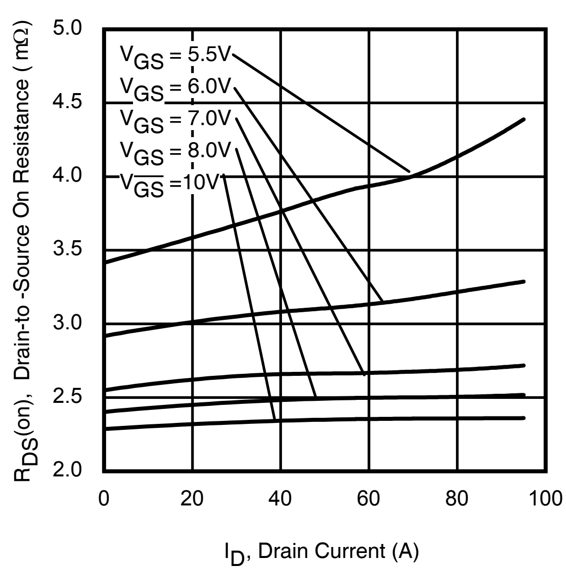


Fig 13. Typical On-Resistance vs. Drain Current

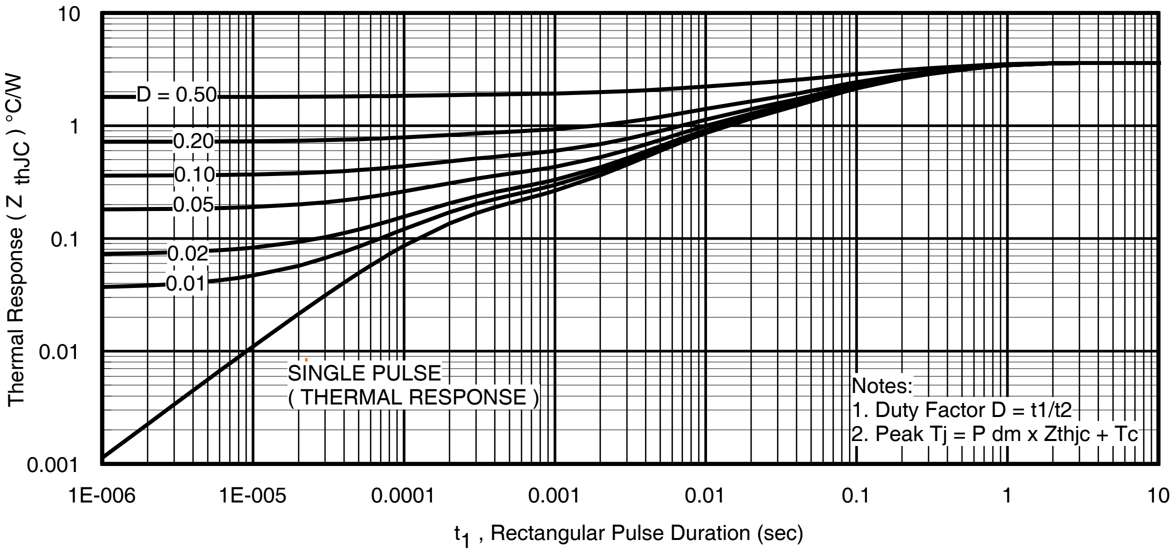


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

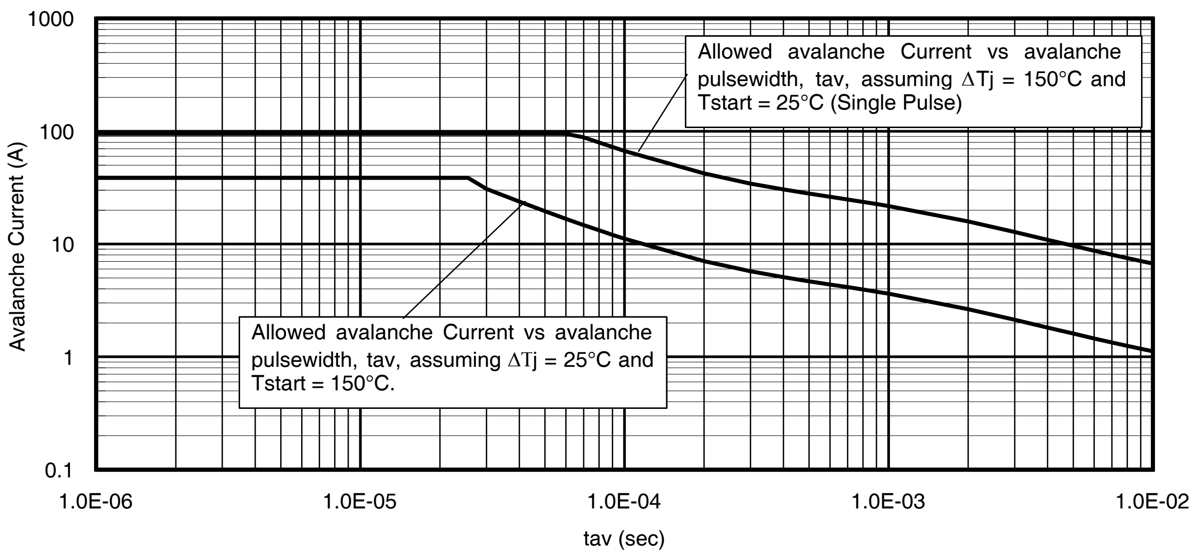


Fig 15. Avalanche Current vs. Pulse Width

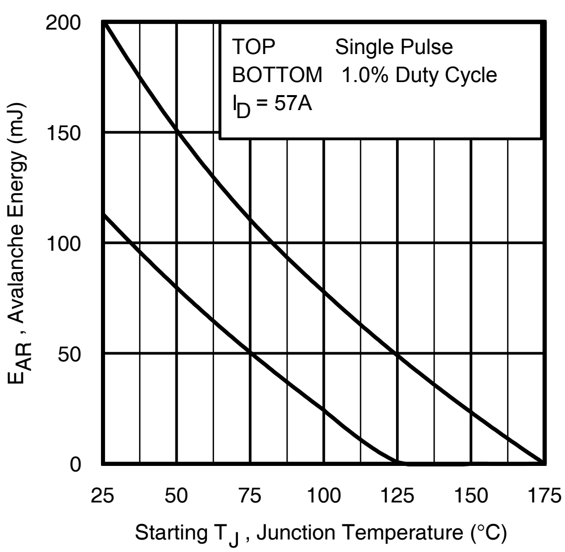


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1.Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
t_{av} = Average time in avalanche.
D = Duty cycle in avalanche = tav ·f
$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$PD\ (ave) = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$

$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$

$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$

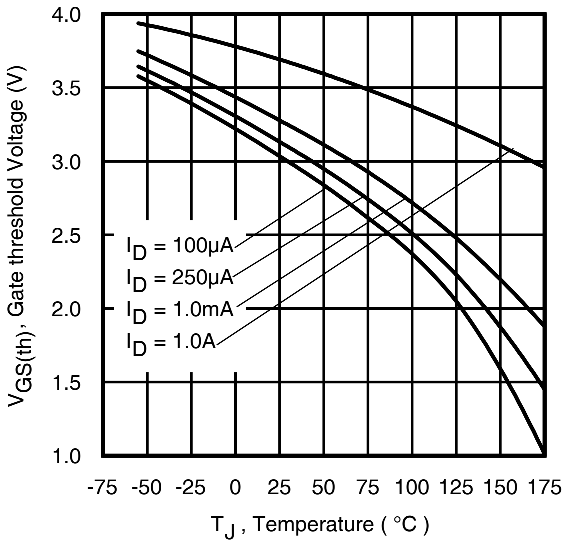


Fig 17. Threshold Voltage vs. Temperature

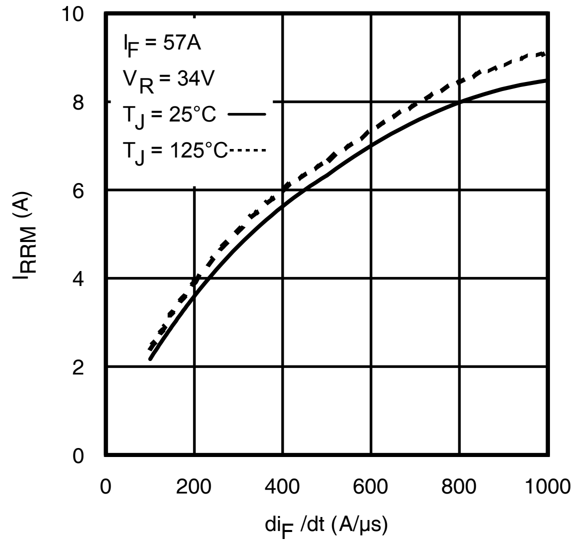


Fig 18. Typical Recovery Current vs. dif/dt

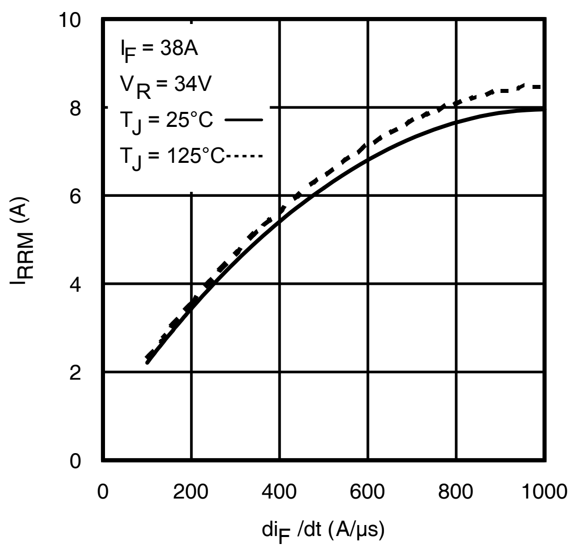


Fig 19. Typical Recovery Current vs. dif/dt

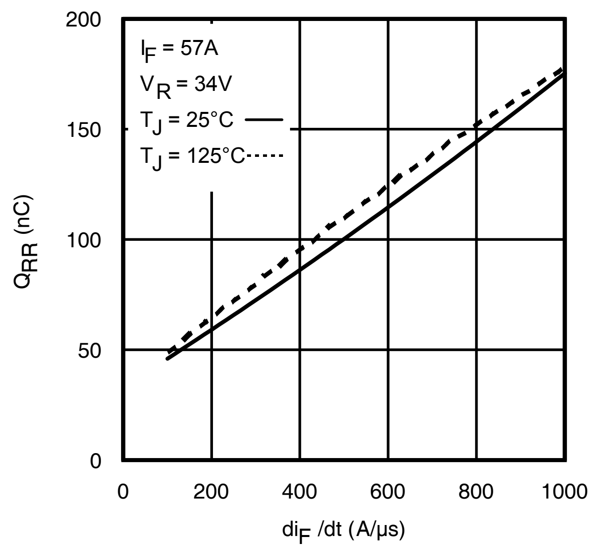


Fig 20. Typical Stored Charge vs. dif/dt

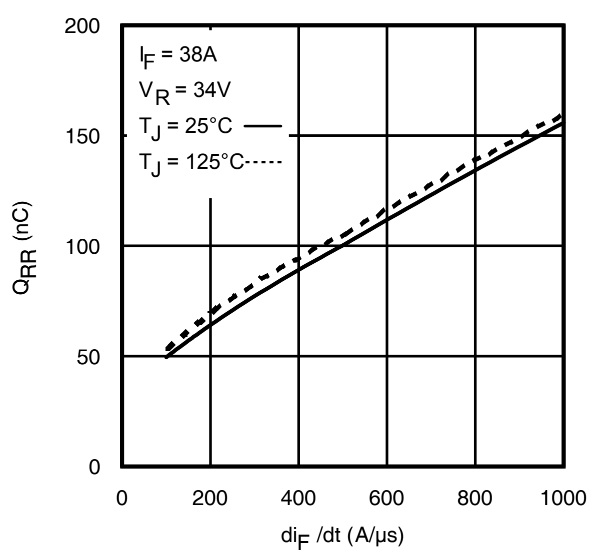


Fig 21. Typical Stored Charge vs. dif/dt

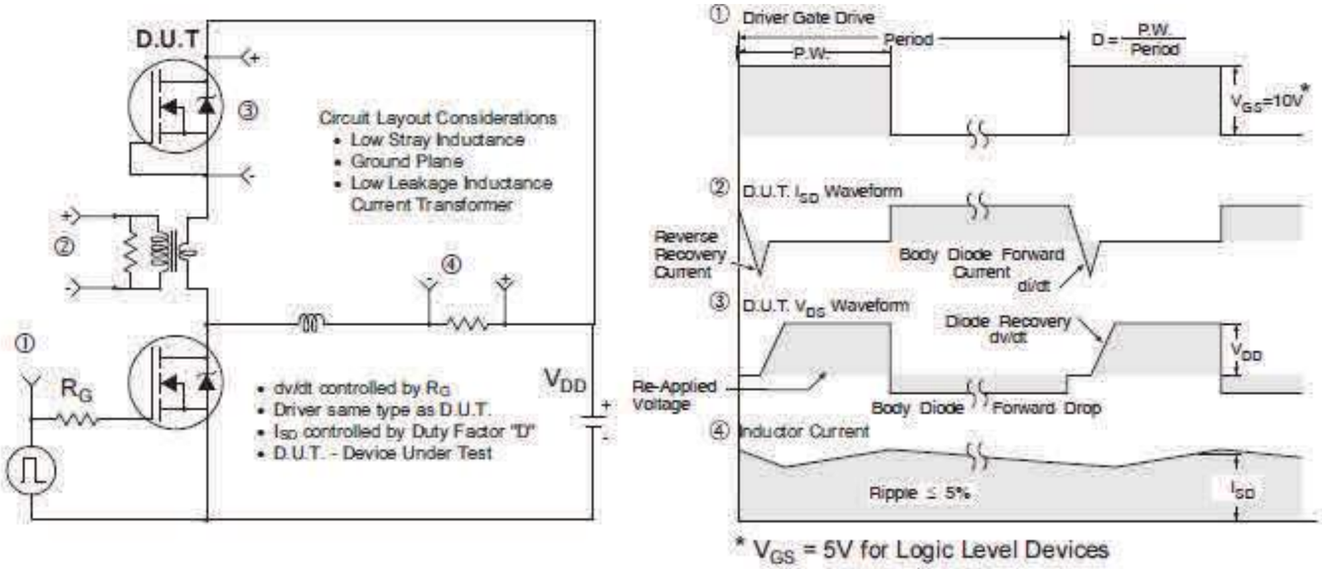


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

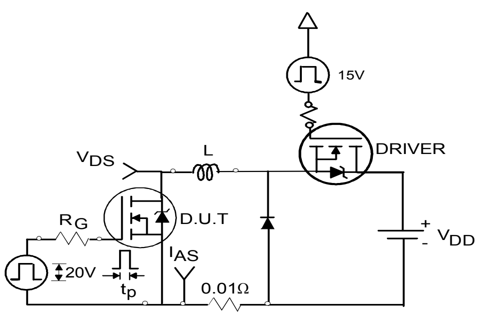


Fig 23a. Unclamped Inductive Test Circuit

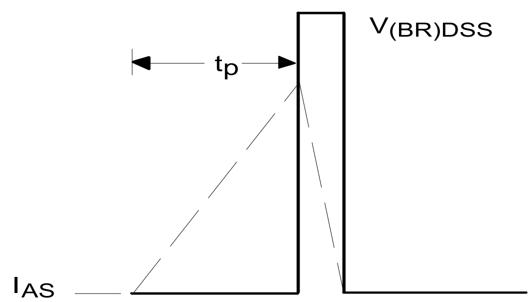


Fig 23b. Unclamped Inductive Waveforms

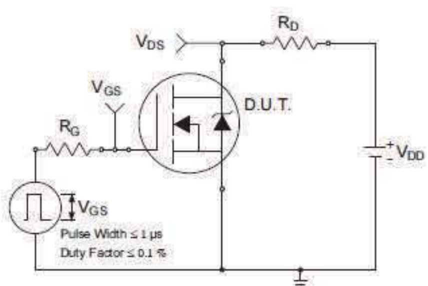


Fig 24a. Switching Time Test Circuit

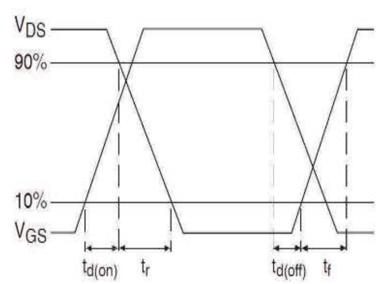


Fig 24b. Switching Time Waveforms

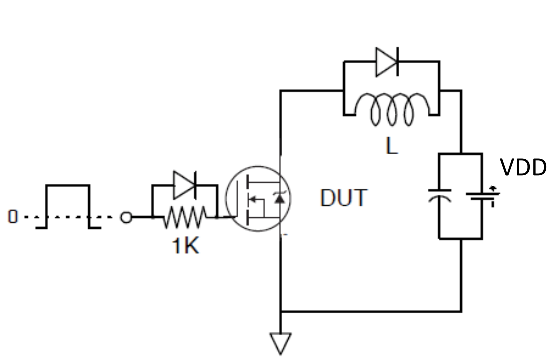


Fig 25a. Gate Charge Test Circuit

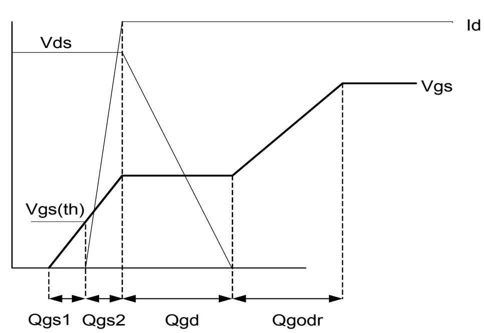
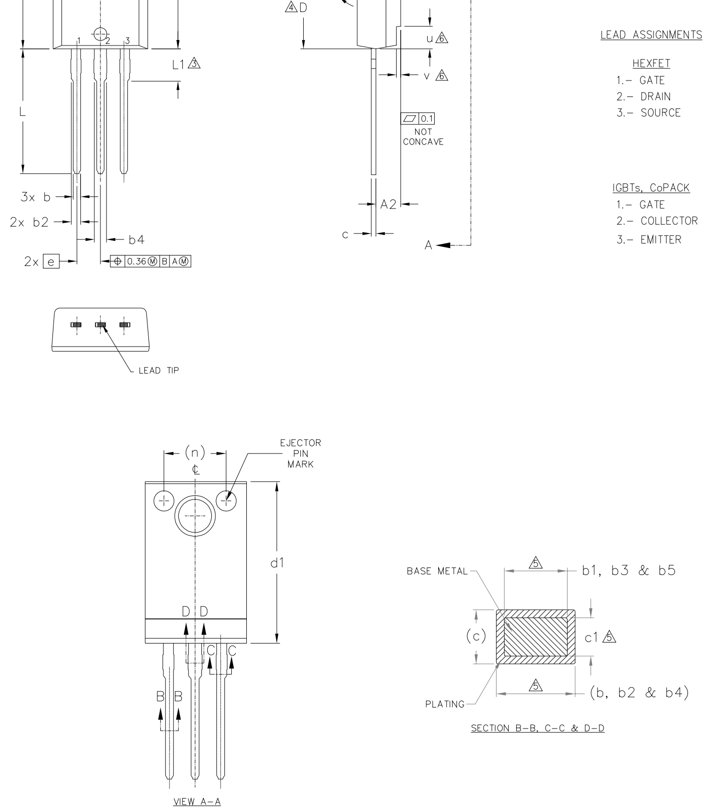


Fig 25b. Gate Charge Waveform

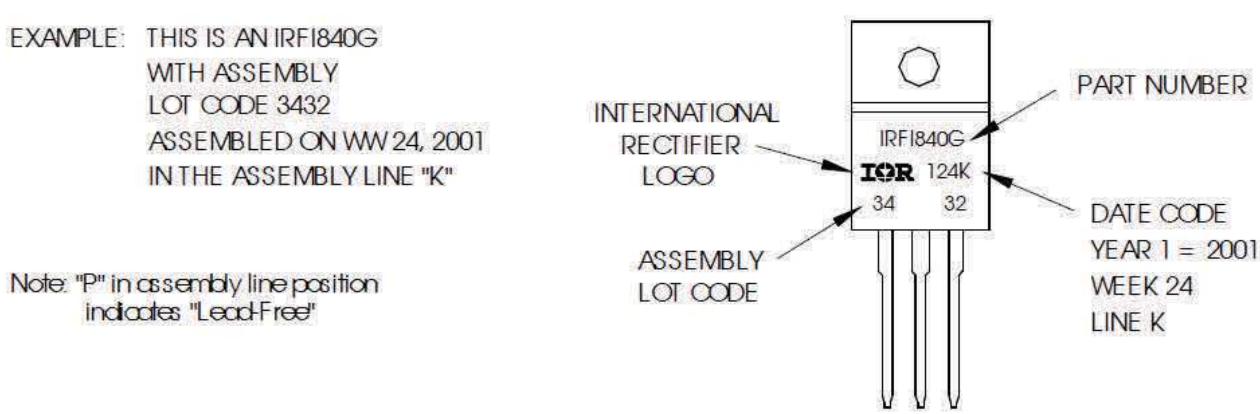
TO-220 Full–Pak Package Outline (Dimensions are shown in millimeters (inches))

NOTES:
1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M– 1994.
2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
7.0 CONTROLLING DIMENSION : INCHES.



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	
A1	2.57	2.82	.101	.111	
A2	2.51	2.92	.099	.115	
b	0.61	0.94	.024	.037	
b1	0.61	0.89	.024	.035	5
b2	0.76	1.27	.030	.050	
b3	0.76	1.22	.030	.048	5
b4	1.02	1.52	.040	.060	
b5	1.02	1.47	.040	.058	5
c	0.33	0.63	.013	.025	
c1	0.33	0.58	.013	.023	5
D	8.66	9.80	.341	.386	4
d1	15.80	16.13	.622	.635	
d2	13.97	14.22	.550	.560	
d3	12.29	12.93	.484	.509	
E	9.63	10.74	.379	.423	4
e	2.54 BSC		.100 BSC		
L	13.21	13.72	.520	.540	
L1	3.10	3.68	.122	.145	3
n	6.05	6.60	.238	.260	
øP	3.05	3.45	.120	.136	
u	2.39	2.49	.094	.098	6
v	0.41	0.51	.016	.020	6
ø1	–	45°	–	45°	

TO-220 Full-Pak Part Marking Information



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	TO-220 Full-Pak	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
11/18/2014	• Updated $E_{AS\ (L=1mH)}$ = 407mJ on page 2 • Updated note 8 "Limited by T_{Jmax}, starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 29A, V_{GS} =10V". on page 2
12/16/2015	• Updated datasheet with corporate template • Corrected typo test condition for Switch time ID from "57A" to "30A" on page 3.

Published by
Infineon Technologies AG
81726 München, Germany