FDMS86500L

MOSFET, N-Channel, POWERTRENCH®

60 V, 158 A, 2.5 mΩ

ON Semiconductor®

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General Description

This N–Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Features

- Max $r_{DS(on)} = 2.5$ mΩ at $V_{GS} = 10$ V, $I_D = 25$ A
- Max $r_{DS(on)} = 3.7$ mΩ at $V_{GS} = 4.5$ V, $I_D = 20$ A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

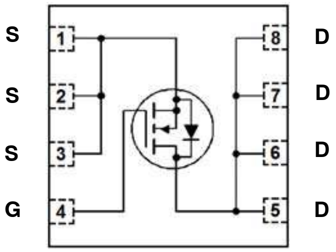
Applications

- Primary Switch in Isolated DC–DC
- Synchronous Rectifier
- Load Switch

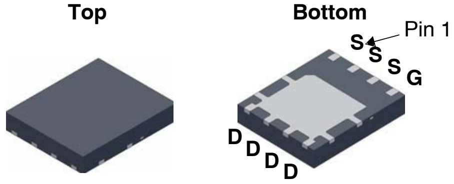
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: – Continuous T_C = 25°C (Note 5) – Continuous T_C = 100°C (Note 5) – Continuous T_A = 25°C (Note 1a) – Pulsed (Note 4)	 158 100 25 799	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	240	mJ
P_D	Power Dissipation: T_C = 25°C T_A = 25°C (Note 1a)	 104 2.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

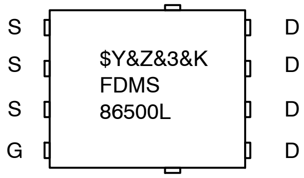


N-Channel MOSFET



Power 56
(PQFN8)
CASE 483AE

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FDMS86500L	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Quantity
FDMS86500L	FDMS86500L	Power 56 (PQFN8) (Pb-Free / Halogen Free)	3000/Tape&Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	60			V
ΔBV_{DSS} /ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		30		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1	1.8	3	V
$\Delta V_{GS(th)}$ /ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		−7		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 25 A		2.1	2.5	mΩ
		V_{GS} = 4.5 V, I_D = 20 A		2.9	3.7	
		V_{GS} = 10 V, I_D = 25 A, T_J = 125°C		3.1	3.7	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 20 A		95		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz		9420	12530	pF
C_{oss}	Output Capacitance			1470	1955	pF
C_{rss}	Reverse Transfer Capacitance			50	80	pF
R_g	Gate Resistance	f = 1MHz	0.1	1.1	3.0	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30 V, I_D = 25 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		27	43	ns
t_r	Rise Time			16	28	ns
$t_{d(off)}$	Turn-Off Delay Time			63	100	ns
t_f	Fall Time			7.8	16	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 30 V, I_D = 25 A		117	165	nC
		V_{GS} = 0 V to 4.5 V, V_{DD} = 30 V, I_D = 25 A		54	108	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 30 V, I_D = 25 A		26.6		nC
Q_{gd}	Gate to Drain “Miller” Charge			11.5		nC

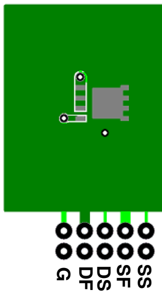
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_s	Continuous Drain to Source Diode Forward Current	T_C = 25°C			80	A
$I_{s,pulse}$	Pulse Drain to Source Diode Forward Current	T_C = 25°C			799	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		0.68	1.2	V
		V_{GS} = 0 V, I_S = 25 A (Note 2)		0.79	1.3	
t_{rr}	Reverse Recovery Time	I_F = 25 A, di/dt = 100 A/μs		54	87	ns
Q_{rr}	Reverse Recovery Charge			42	67	nC
t_{rr}	Reverse Recovery Time	I_F = 25 A, di/dt = 300 A/μs		46	73	ns
Q_{rr}	Reverse Recovery Charge			84	134	nC

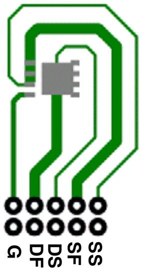
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 220 mJ is based on starting T_J = 25°C, L = 0.3 mH, I_{AS} = 40 A, V_{DD} = 54 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 66 A.
4. Pulsed Id please refer to Figure 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

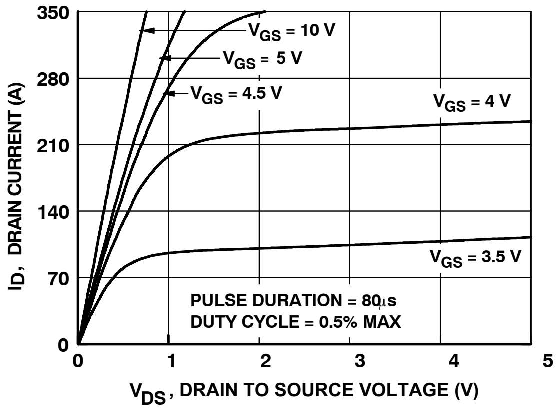


Figure 1. On Region Characteristics

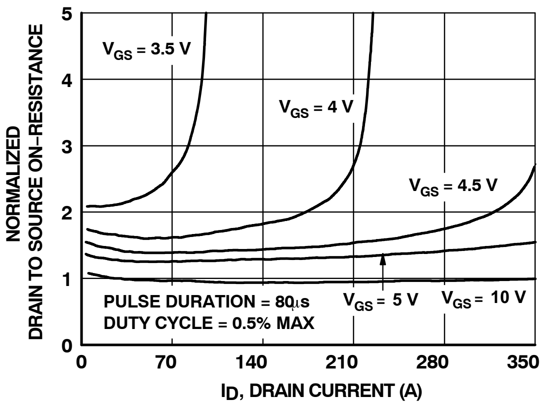


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

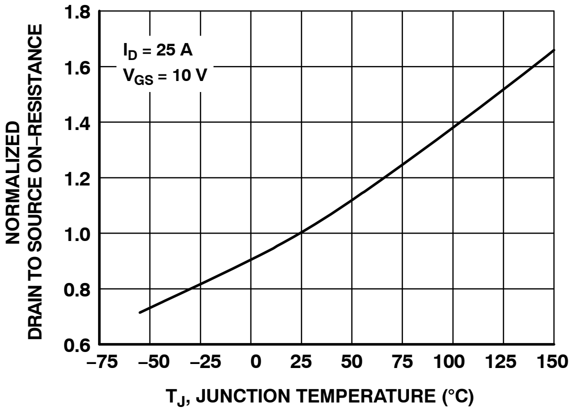


Figure 3. Normalized On Resistance vs. Junction Temperature

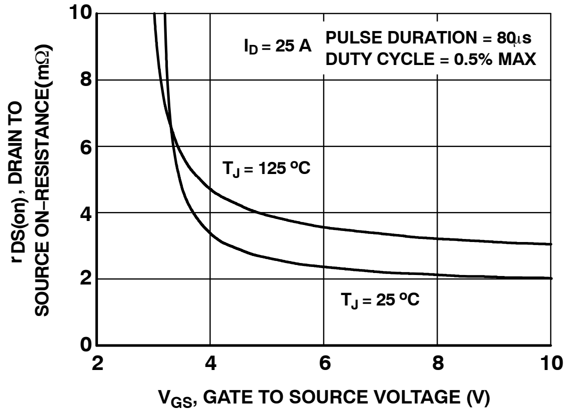


Figure 4. On−Resistance vs. Gate to Source Voltage

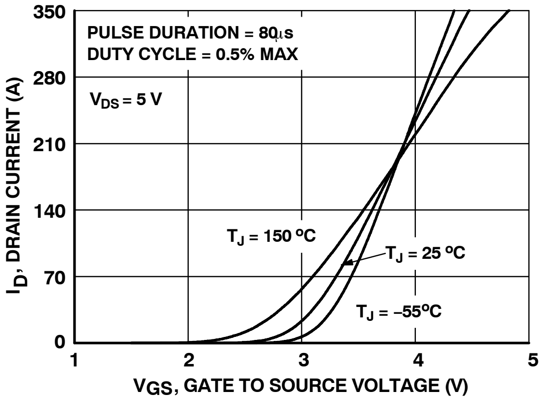


Figure 5. Transfer Characteristics

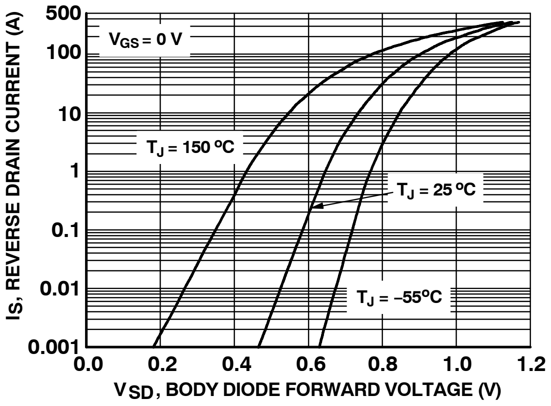


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

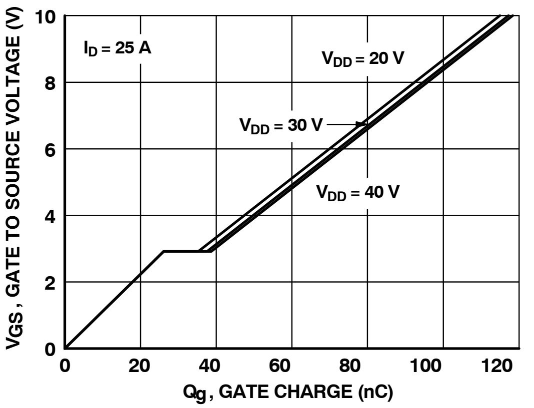


Figure 7. Gate Charge Characteristics

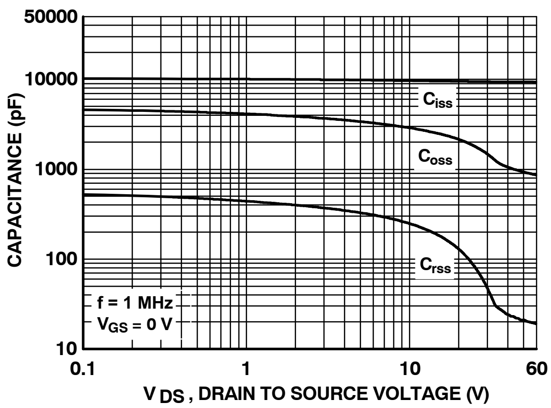


Figure 8. Capacitance vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

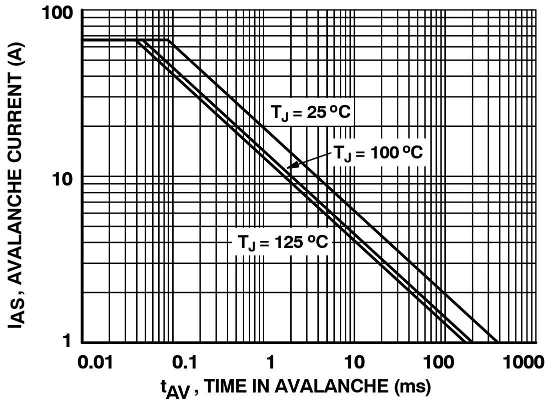


Figure 9. Unclamped Inductive Switching Capability

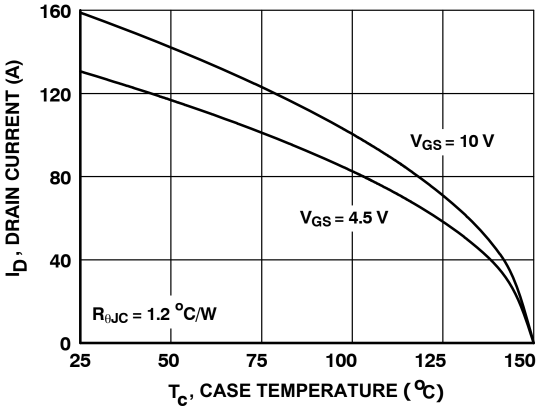


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

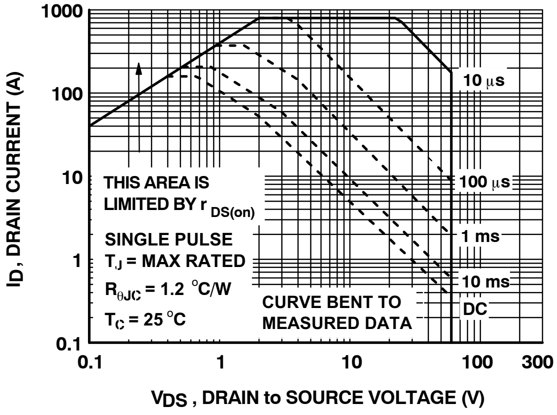


Figure 11. Forward Bias Safe Operating Area

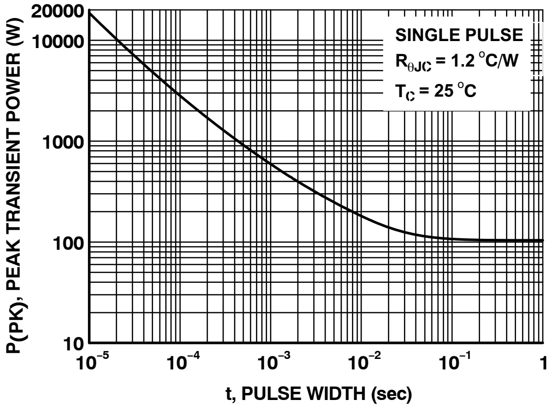


Figure 12. Single Pulse Maximum Power Dissipation

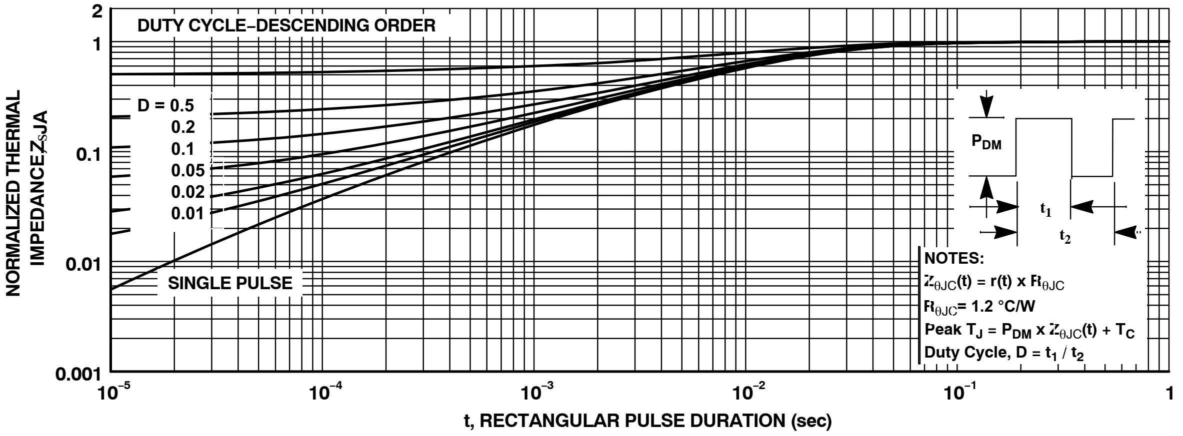


Figure 13. Transient Thermal Response Curve

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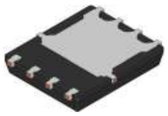
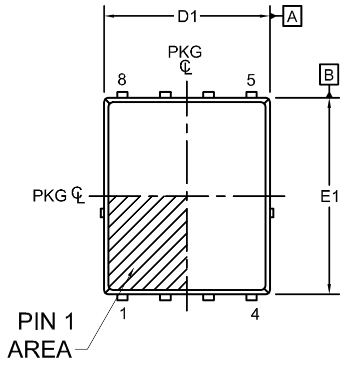
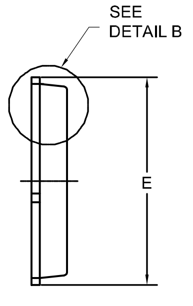


PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

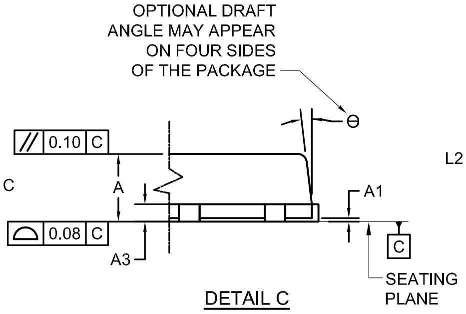


TOP VIEW

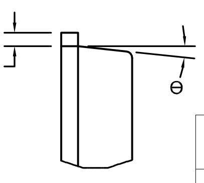


NOTES:

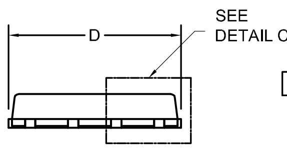
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DETAIL C
SCALE: 2:1

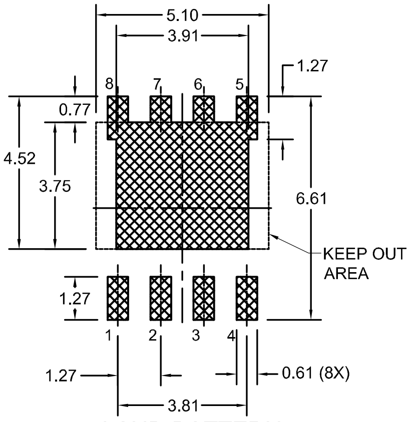


DETAIL B
SCALE: 2:1

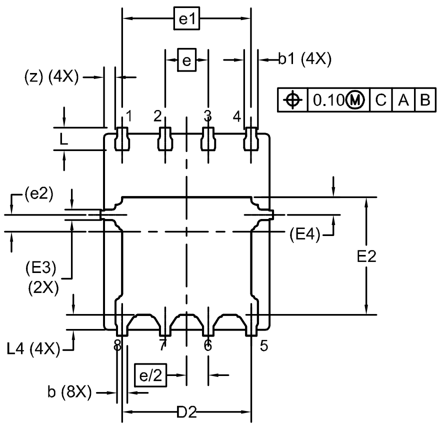


SIDE VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°



LAND PATTERN
RECOMMENDATION



BOTTOM VIEW

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