STR6S161HXD

Data Sheet

Description

The STR6S161HXD is power IC for switching power supplies, incorporating a power MOSFET and a current mode PWM controller IC.

The operation mode is automatically changed, in response to load, to the fixed switching frequency, to the switching frequency control, and to the burst oscillation mode. Thus, the power efficiency is improved.

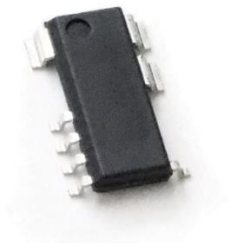
The product achieves high cost-effective power supply systems with few external components.

Features

- Pb-free (RoHS compliant)
- Improving circuit efficiency (Since the step drive control can keep V_{RM} of secondary rectification diodes low, the circuit efficiency can be improved by low V_F)
- Current Mode Type PWM Control
- AC Input Voltage Detection Function
  - Overvoltage Protection Function (HVP)
  - Brown-In and Brown-Out Function
- No Load Power Consumption, P_{IN} < 40 mW
- Automatically changed operation mode in response to load conditions
  - Fixed switching frequency mode, 100 kHz (typ.) in normal operation.
  - Green mode, 25 kHz (typ.) to 100 kHz (typ.) in middle to light load.
  - Burst oscillation mode in light load.
- Random Switching Function
- Slope Compensation Function
- Leading Edge Blanking Function
- Bias Assist Function
- Protections
  - Two Types of Overcurrent Protection (OCP): Pulse-by-Pulse, built-in compensation circuit to minimize OCP point variation on AC input voltage
  - Overload Protection with timer (OLP): Auto-restart
  - Overvoltage Protection (OVP): Auto-restart
  - Thermal Shutdown (TSD): Auto-restart

Package

SOIC16



Not to scale

Electrical Characteristics

- V_{DSS} = 700 V (min.)
- $R_{DS(ON)}$ = 3.95 Ω (max.)
- $f_{OSC(AVG)}$ = 100 kHz
- Output Power, P_{OUT}*

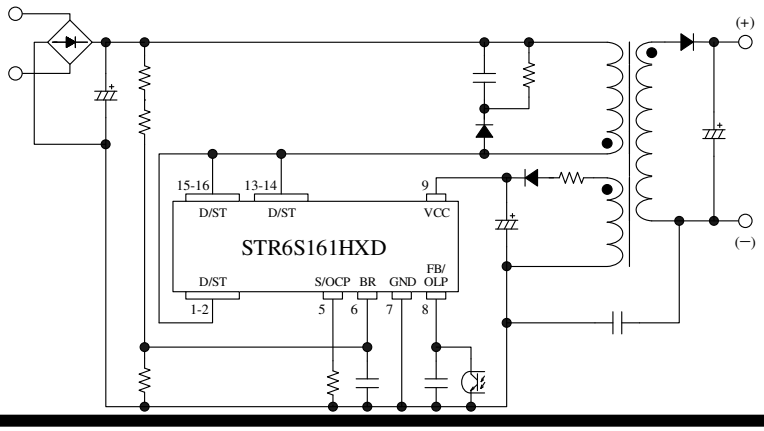
Part Number	Adapter		Open frame	
	230VAC	85 to 265VAC	230VAC	85 to 265VAC
STR6S161HXD	19.6W	14.3W	33.5W	22.5W

* The output power is actual continues power that is measured at 50 °C ambient. The peak output power can be 120 to 140 % of the value stated here. Core size, duty cycle, and thermal design affect the output power. It may be less than the value stated here.

Applications

- White Goods
- Office Automation Equipment
- Audio Visual Equipment
- Industrial Equipment
- Other Switched Mode Power Supplies

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25°C, all D/ST pins are shorted on the PCB.

Parameter	Symbol	Conditions	Pins	Rating	Units
Drain Peak Current (1)	I_{DPEAK}	Single pulse	1 − 5	2.5	A
Maximum Switching Current (2)	I_{DMAX}	T_A = − 40 to 125 °C	1 − 5	2.5	A
Avalanche Energy (3)(4)	E_{AS}	I_{LPEAK}=1.78A	1 − 5	36	mJ
S/OCP Pin Voltage	$V_{S/OCP}$		5 – 7	−2 to 6	V
BR Pin Voltage	V_{BR}		6 – 7	−0.3 to 7.5	V
BR Pin Sink Current	I_{BR}		6 – 7	1.0	mA
FB/OLP Pin Voltage	V_{FB}	$I_{FB} \leq$ 1mA	8 – 7	−0.3 to 14	V
FB/OLP Pin Sink Current	I_{FB}		8 – 7	1.0	mA
VCC Pin Voltage	V_{CC}		9 – 7	−0.3 to 32	V
D/ST Pin Voltage	$V_{D/ST}$		1 – 7	−1 to V_{DSS}	V
Power MOSFET Power Dissipation(5)	P_{D1}	(6)	1 − 5	1.25	W
Control Part Power Dissipation	P_{D2}		9 – 7	1.1	W
Operating Ambient Temperature	T_{OP}		—	−40 to 125	°C
Storage Temperature	T_{STG}		—	−40 to 125	°C
Junction Temperature	T_J		—	150	°C

(1) See Section 5.1.
(2) The Maximum Switching Current is the drain current determined by the drive voltage of the IC and threshold voltage of the power MOSFET, $V_{GS(TH)}$.
(3) See Figure 4-2.
(4) Single pulse, V_{DD} = 99 V, L = 20 mH.
(5) See Figure 4-3.
(6) When embedding this hybrid IC onto the printed circuit board (copper area in a 15 mm × 15 mm).

2. Electrical Characteristics

- Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (−).
- Unless specifically noted, T_A = 25°C and V_{CC} = 18 V.

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Units
Power Supply Startup Operation							
Operation Start Voltage	$V_{CC(ON)}$		9 – 7	13.8	15.0	16.2	V
Operation Stop Voltage(*)	$V_{CC(OFF)}$		9 – 7	7.6	8.5	9.2	V
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC} = 12 V	9 – 7	—	1.5	3.0	mA
Startup Circuit Operation Voltage	$V_{ST(ON)}$		1 – 7	40	47	55	V
Startup Current	$I_{CC(ST)}$	V_{CC} = 13.5 V $V_{D/ST}$ = 100 V	9 – 7	−4.05	−2.50	−1.08	mA
Startup Current Biasing Threshold Voltage	$V_{CC(BIAS)}$	I_{CC} = −500 µA	9 – 7	8.0	9.6	10.5	V
Normal Operation							
Average Switching Frequency	$f_{OSC(AVG)}$		1 – 7	90	100	110	kHz
Switching Frequency Modulation Deviation	Δf		1 – 7	—	8.4	—	kHz
Maximum Feedback Current	$I_{FB(MAX)}$	V_{CC} = 12 V	8 – 7	−170	−130	−85	µA
Minimum Feedback Current	$I_{FB(MIN)}$		8 – 7	−21	−13	−5	µA
Light Load Operation							
FB/OLP Pin Starting Voltage of Frequency Decreasing	$V_{FB(FDS)}$	$f_{OSC(AVG)}$× 0.9	8 – 7	2.88	3.60	4.32	V
FB/OLP Pin Ending Voltage of Frequency Decreasing	$V_{FB(FDE)}$	$f_{OSC(MIN)}$× 1.1	8 – 7	2.48	3.10	3.72	V
Minimum Switching Frequency	$f_{OSC(MIN)}$		1 − 7	18	25	32	kHz
Standby Operation							
FB/OLP Pin Oscillation Stop Threshold Voltage	$V_{FB(OFF)}$		8 – 7	1.62	1.77	1.92	V
Brown-In / Brown-Out Function							
AC Input Overvoltage Protection (HVP) Threshold Voltage(†)	$V_{BR(HVP)}$		6 – 7	5.34	5.51	5.68	V
AC Input Overvoltage Protection (HVP) Release Threshold Voltage	$V_{BR(HVPR)}$		6 – 7	5.23	5.39	5.55	V
Brown-In Threshold Voltage	$V_{BR(IN)}$		6 – 7	1.02	1.11	1.20	V
Brown-Out Threshold Voltage	$V_{BR(OUT)}$		6 – 7	0.76	0.85	0.94	V
Protection							
Maximum Duty Cycle	D_{MAX}		1 − 7	70	75	80	%
Leading Edge Blanking Time	t_{BW}		—	—	330	—	ns
OCP Compensation Coefficient	DPC		—	—	25.8	—	mV/µs
OCP Compensation Duty Cycle	D_{DPC}		—	—	36	—	%
OCP Threshold Voltage at Zero Duty Cycle	$V_{OCP(L)}$		5 − 7	0.735	0.795	0.855	V

(*) $V_{CC(BIAS)} > V_{CC(OFF)}$ always.
(†) $V_{BR(HVP)} > V_{BR(HVPR)}$

Parameter	Symbol	Conditions	Pins	Min.	Typ.	Max.	Units
OCP Threshold Voltage at 36% Duty Cycle	$V_{OCP(H)}$		1 − 7	0.843	0.888	0.933	V
OCP Threshold Voltage in Leading Edge Blanking Time	$V_{OCP(LEB)}$		1 − 7	—	1.69	—	V
OLP Threshold Voltage	$V_{FB(OLP)}$		8 – 7	6.8	7.3	7.8	V
OLP Delay Time	t_{OLP}		8 – 7	55	75	90	ms
OLP Operation Current	$I_{CC(OLP)}$		9 – 7	—	260	—	µA
FB/OLP Pin Clamp Voltage	$V_{FB(CLAMP)}$		8 – 7	10.5	11.8	13.5	V
OVP Threshold Voltage	$V_{CC(OVP)}$		9 – 7	27.0	29.1	31.2	V
Thermal Shutdown Operating Temperature(‡)	$T_{J(TSD)}$		—	127	145	—	°C
Thermal Shutdown Temperature Hysteresis	$T_{J(TSD)HYS}$		—	—	80	—	°C
Power MOSFET							
Drain-to-Source Breakdown Voltage	V_{DSS}	I_{DS} = 300 µA	1 − 5	700	—	—	V
Drain Leakage Current	I_{DSS}	V_{DS} = 700 V	1 − 5	—	—	50	µA
On-resistance	$R_{DS(ON)}$	I_{DS} = 0.4 A	1 − 5	—	—	3.95	Ω
Switching Time	t_f		1 − 5	—	—	250	ns
Thermal Resistance							
Junction to Case Thermal Resistance	θ_{J-C}		—	—	—	25	°C/W

(‡) The junction temperature of the internal control chip is measured.

3. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	0.17	—	g

4. Derating Curves

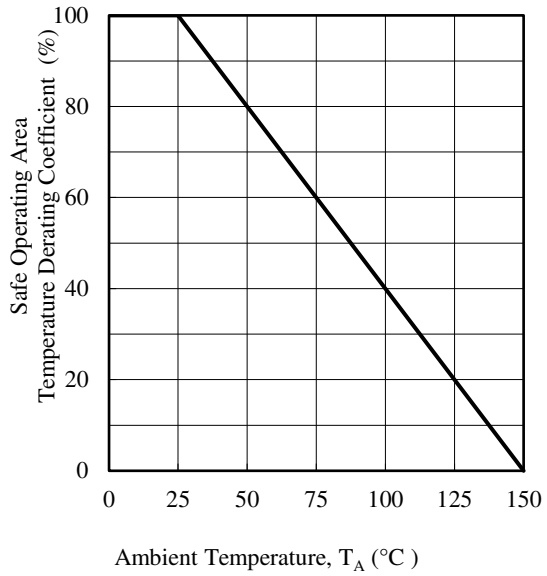


Figure 4-1. SOA Temperature Derating Coefficient Curve

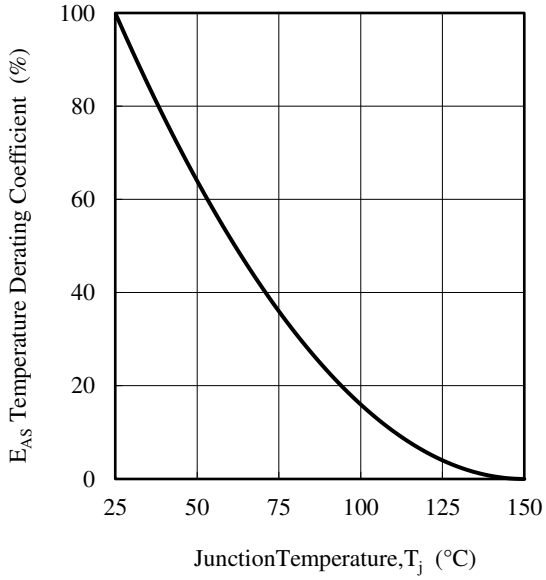


Figure 4-2. Avalanche Energy Derating Coefficient Curve

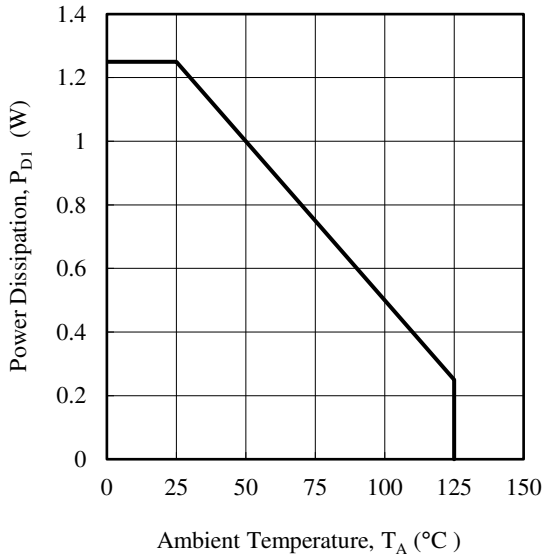


Figure 4-3. Power Dissipation Temperature Derating Curve

5. Performance Curves

5.1. Power MOSFET Safe Operating Area Curves

- When the IC is used, the safe operating area curve should be multiplied by the temperature derating coefficient derived from Figure 4-1.
- The broken line in the safe operating area curve is the drain current curve limited by on-resistance.
- Unless otherwise specified, T_A = 25 °C, Single pulse.

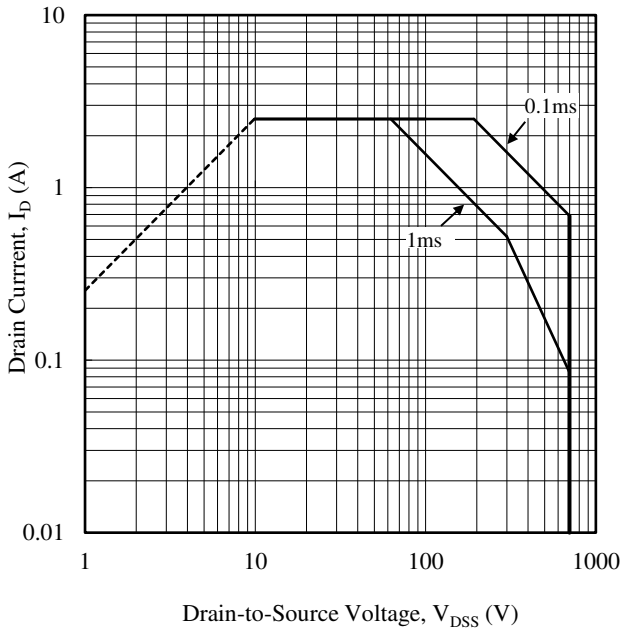


Figure 5-1. Power MOSFET Safe Operating Area Curves

5.2. Transient Thermal Resistance Curves

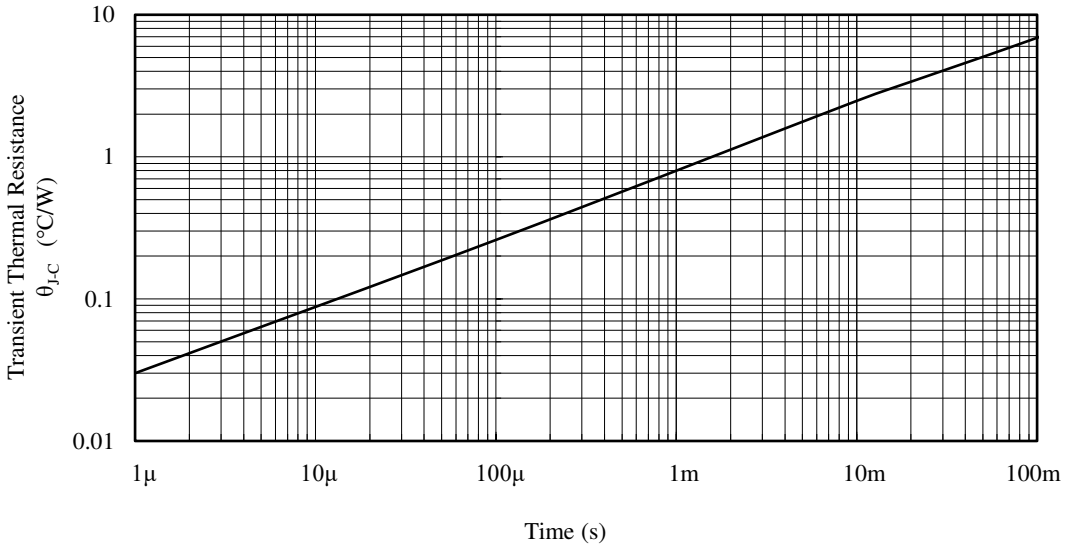
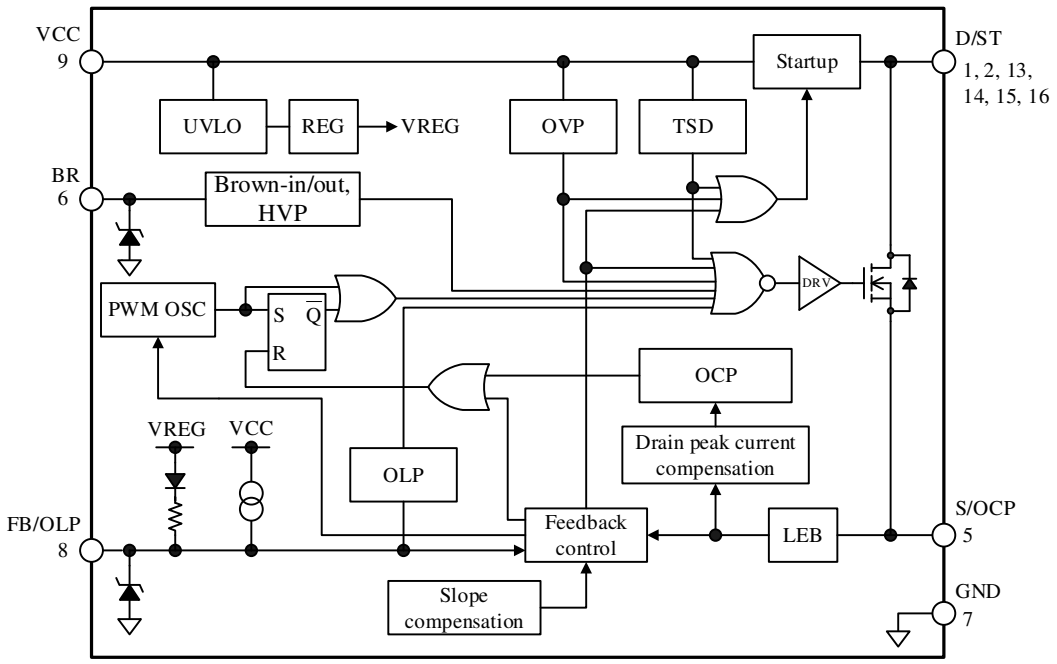
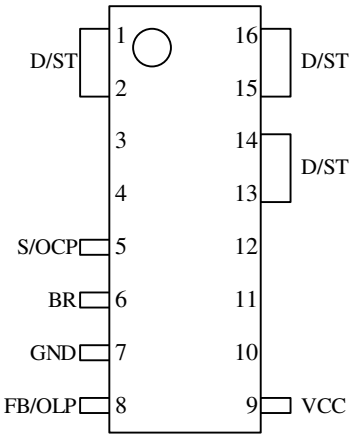


Figure 5-2. Junction to Case Transient Thermal Resistance

6. Block Diagram



7. Pin Configuration Definitions



Pin	Name	Descriptions
1	D/ST	Power MOSFET drain and startup current input
2		
3	—	(Pin removed)
4	—	(Pin removed)
5	S/OCP	Power MOSFET source and Overcurrent Protection (OCP) signal input
6	BR	AC input voltage detection signal input
7	GND	Ground
8	FB/OLP	Constant voltage control signal input and Overload Protection (OLP) signal input
9	VCC	Power supply voltage input for control part and Overvoltage Protection (OVP) signal input
10	—	(Pin removed)
11	—	(Pin removed)
12	—	(Pin removed)
13	D/ST	Power MOSFET drain and startup current input
14		
15		
16		

8. Typical Application

The PCB traces of the D/ST pins (Pin 1, 2, 13 to 16) should be as wide as possible, in order to enhance thermal dissipation. In applications having a power supply specified such that the D/ST pins have large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.

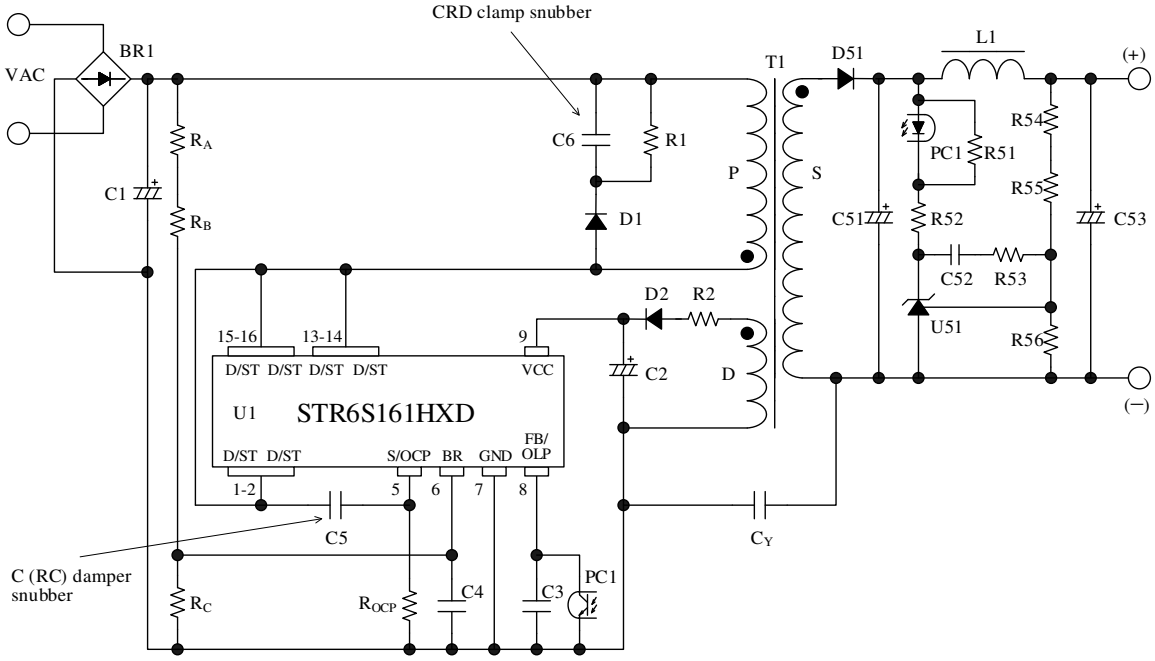
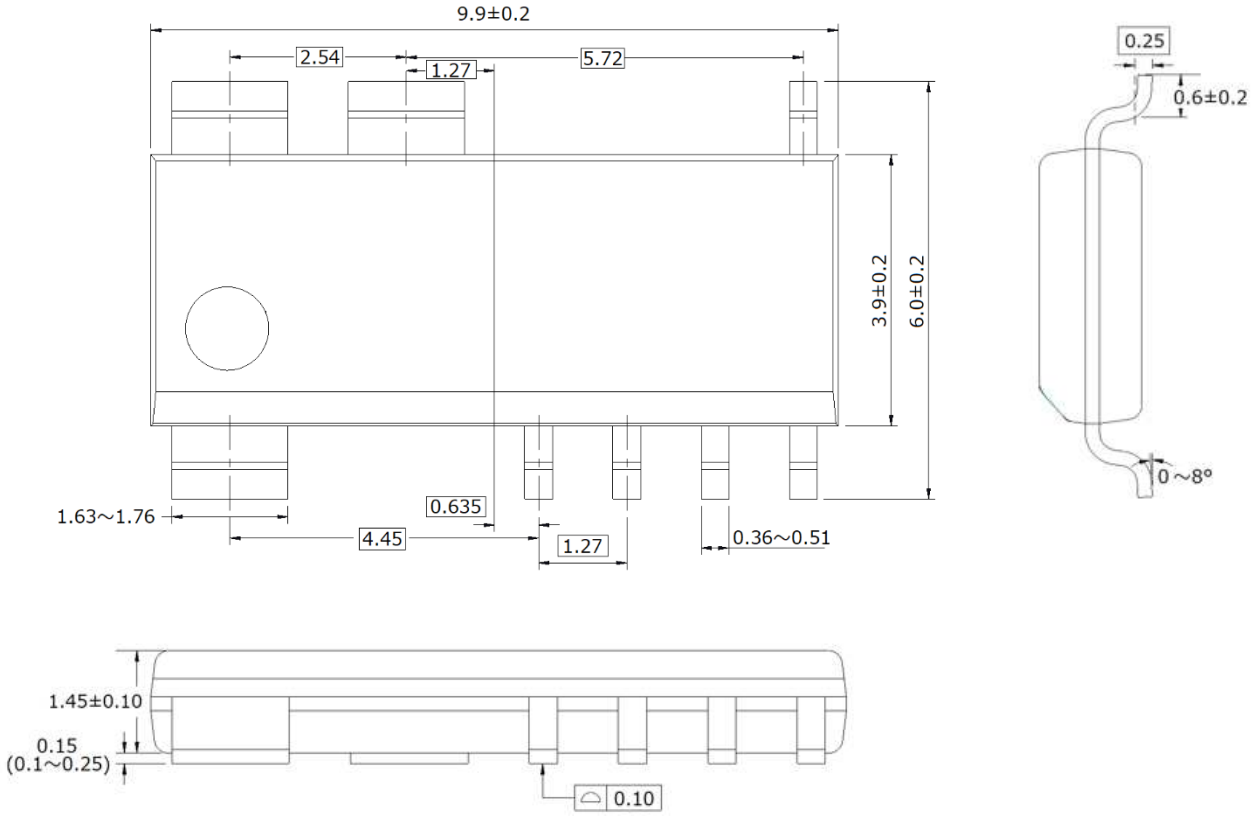


Figure 8-1. Typical Application Circuit

9. Physical Dimensions

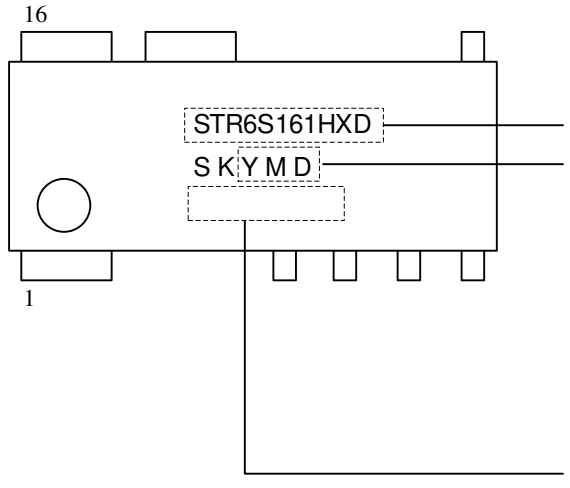
- SOIC16



NOTES:

- Dimension in millimeters
- Dimensions do not include mold burrs.
- Pb-free (RoHS compliant)
- MSL 1 (Moisture Sensitivity Level 1)
- When soldering the products, it is required to minimize the working time within the following limits:
  Flow: 260 °C / 10 s, 1 time
  Reflow
  Preheat: 150 °C to 200 °C / 60 s to 120 s
  Solder heating: 255 °C / 30s, 3 times (260 °C peak)
  Soldering iron: 350 °C / 3.5 s, 1 time

10. Marking Diagram



Part Number

Lot Number:
Y is the last digit of the year of manufacture (0 to 9)
M is the month of the year (1 to 9, O, N, or D)
D is the period of days represented by:
1: the first 10 days of the month (1st to 10th)
2: the second 10 days of the month (11th to 20th)
3: the last 10–11 days of the month (21st to 31st)

Control Number

11. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum.

Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (−).

11.1. Startup Operation

Figure 11-1 shows the circuit around IC. Figure 11-2 shows the start up operation.

The IC incorporates the startup circuit. The circuit is connected to D/ST pin. When D/ST pin voltage reaches to Startup Circuit Operation Voltage $V_{ST(ON)}$ = 47 V, the startup circuit starts operation.

During the startup process, the constant current, $I_{CC(ST)}$ = −2.50 mA, charges C2 at VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V, the control circuit starts operation.

The startup time of control circuit is determined by C2 capacitor value. The approximate startup time, t_{START} (shown in Figure 11-2) is calculated as follows:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{\left| I_{CC(ST)} \right|} \quad (1)$$

Where:

t_{START} : Startup time of IC (s)

$V_{CC(INT)}$: Initial voltage on VCC pin (V)

When BR pin voltage is less than $V_{BR(IN)}$ = 1.11 V, the Bias Assist Function (refer to Section 11.3) is disabled. Thus, VCC pin voltage repeats increasing to $V_{CC(ON)}$ and decreasing to $V_{CC(OFF)}$ (shown in Figure 11-2). When BR pin voltage becomes $V_{BR(IN)}$ or more, the IC starts switching operation. During the switching operation, the voltage rectified the auxiliary winding voltage, V_D, of Figure 11-1 becomes a power source to the VCC pin. After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero.

The approximate value of auxiliary winding voltage is about 18 V, taking account of the winding turns of D winding so that VCC pin voltage becomes Equation (2) within the specification of input and output voltage variation of power supply.

$$V_{CC(BIAS)}(\max.) < V_{CC} < V_{CC(OVP)}(\min.)$$

$$\Rightarrow 10.5\ (V) < V_{CC} < 27.0\ (V) \quad (2)$$

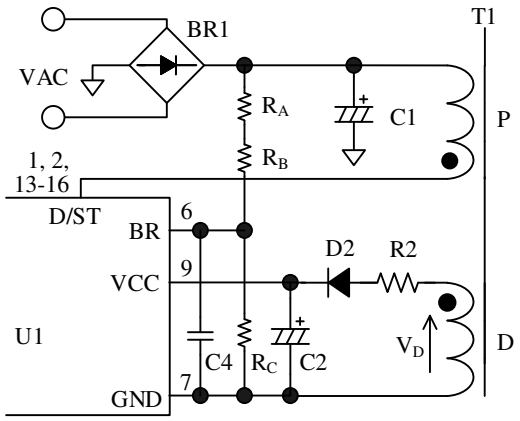


Figure 11-1. VCC Pin Peripheral Circuit

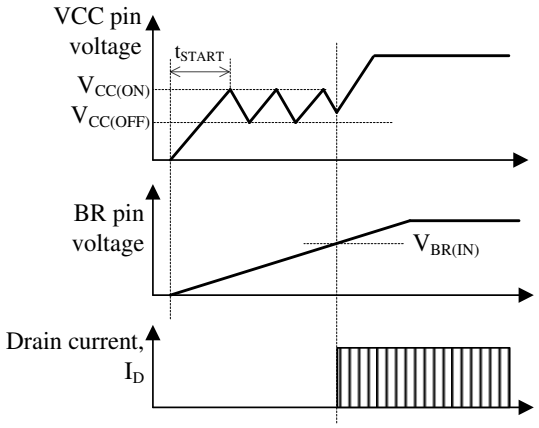


Figure 11-2. Startup Operation

11.2. Undervoltage Lockout (UVLO)

Figure 11-3 shows the relationship of VCC pin voltage and circuit current I_{CC}. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.5 V, the control circuit stops operation by Undervoltage Lockout (UVLO) circuit, and reverts to the state before startup.

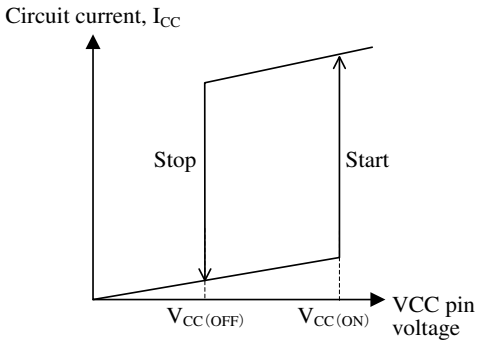


Figure 11-3. Relationship Between VCC pin voltage and I_{CC}

11.3. Bias Assist Function

By the Bias Assist Function, the startup failure is prevented. The Bias Assist Function is activated, in both of following condition:

the FB pin voltage is FB/OLP Pin Oscillation Stop Threshold Voltage, $V_{FB(OFF)}$= 1.77 V or less

and the VCC voltage decreases to the Startup Current Biasing Threshold Voltage, $V_{CC(BIAS)}$ = 9.6 V.

When the Bias Assist Function is activated, the VCC pin voltage is kept almost constant voltage, $V_{CC(BIAS)}$ by providing the startup current, $I_{CC(ST)}$, from the startup circuit. Thus, the VCC pin voltage is kept more than $V_{CC(OFF)}$.

Since the startup failure is prevented by the Bias Assist Function, the value of C2 connected to VCC pin can be small. Thus, the startup time and the response time of the OVP become shorter.

The operation of the Bias Assist Function in startup is as follows. It is necessary to check and adjust the startup process based on actual operation in the application, so that poor starting conditions may be avoided.

Figure 11-4 shows VCC pin voltage behavior during the startup period.

After VCC pin voltage increases to $V_{CC(ON)}$ = 15.0 V at startup, the IC starts the operation. Then circuit current increases and VCC pin voltage decreases. At the same time, the auxiliary winding voltage V_D increases in proportion to output voltage. These are all balanced to produce VCC pin voltage.

When VCC pin voltage is decrease to $V_{CC(OFF)}$ = 8.5 V in startup operation, the IC stops switching operation and a startup failure occurs.

When the output load is light at startup, the output voltage may become more than the target voltage due to the delay of feedback circuit. In this case, the FB pin voltage is decreased by the feedback control. When the FB pin voltage decreases to $V_{FB(OFF)}$ or less, the IC stops switching operation and VCC pin voltage decreases. When VCC pin voltage decreases to $V_{CC(BIAS)}$, the Bias Assist Function is activated and the startup failure is prevented.

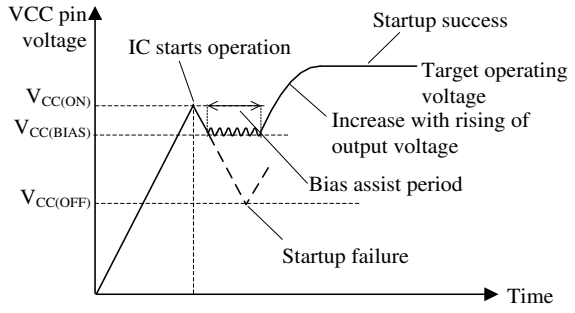


Figure 11-4. VCC Pin Voltage during Startup Period

11.4. Soft Start Function

Figure 11-5 shows the behavior of VCC pin voltage and drain current during the startup period.

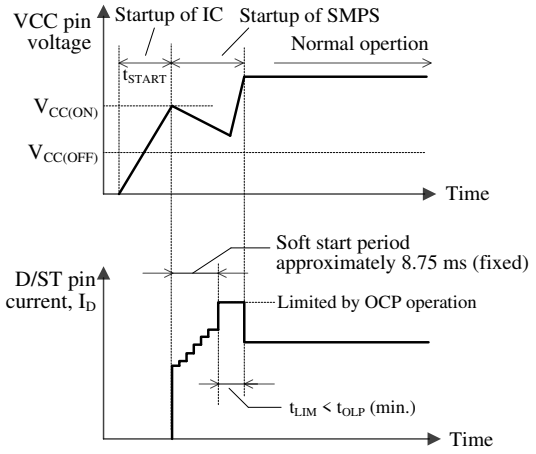


Figure 11-5. V_{CC} and I_D Behavior during Startup

The IC activates the soft start circuitry during the startup period. Soft start time is fixed to around 8.75 ms. during the soft start period, over current threshold is increased step-wisely (7 steps). This function reduces the voltage and the current stress of power MOSFET and secondary side rectifier diode.

Since the Leading Edge Blanking Function (see Section 11.6) is deactivated during the soft start period, there is the case that on time is less than the leading edge blanking time, t_{BW} = 330 ns.

After the soft start period, D/ST pin current, I_D, is limited by the Overcurrent Protection (OCP), until the output voltage increases to the target operating voltage. This period is given as t_{LIM}.

When t_{LIM} is longer than the OLP Delay Time, t_{OLP}, the output power is limited by the Overload Protection (OLP).

Thus, it is necessary to adjust the value of output capacitor and the turn ratio of auxiliary winding D so that the t_{LIM} is less than t_{OLP} = 55 ms (min.).

11.5. Constant Output Voltage Control

The IC achieves the constant voltage control of the power supply output by using the current-mode control method, which enhances the response speed and provides the stable operation.

The FB/OLP pin voltage is internally added the slope compensation at the feedback control (see Section 0.Functionnal Block Diagram), and the target voltage, V_{SC}, is generated. The IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}, as

shown in Figure 11-6 and Figure 11-7.

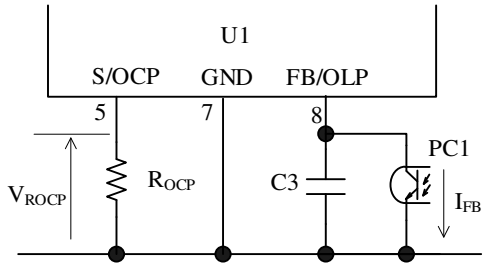


Figure 11-6. FB/OLP Pin Peripheral Circuit

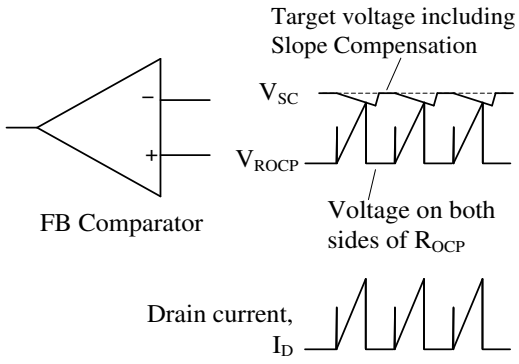


Figure 11-7. Drain Current, I_D, and FB Comparator Operation in Steady Operation

- Light load conditions
  When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases.
  This control prevents the output voltage from increasing.

- Heavy load conditions
  When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases.
  This control prevents the output voltage from decreasing.

In the current mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based on the initial value of the drain current.

This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in Figure 11-8. This is called the subharmonics phenomenon.

In order to avoid this, the IC incorporates the Slope Compensation Function. Because the target voltage is added a down-slope compensation signal, which reduces the peak drain current as the on-duty gets wider relative to the FB/OLP pin signal to compensate V_{SC}, the subharmonics phenomenon is suppressed.

Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance of normal operation.

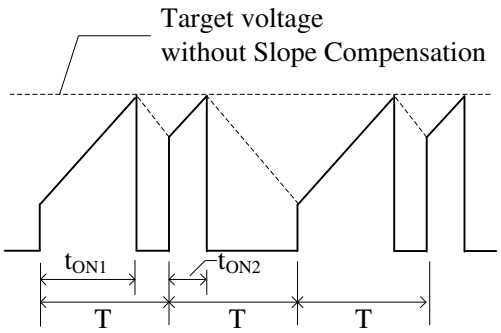


Figure 11-8. Drain Current, I_D, Waveform in Subharmonic Oscillation

11.6. Leading Edge Blanking Function

The constant voltage control of output of the IC uses the peak-current-mode control method.

In peak-current-mode control method, there is a case that the power MOSFET turns off due to unexpected response of FB comparator or Overcurrent Protection circuit (OCP) to the steep surge current in turning on a power MOSFET.

In order to prevent this response to the surge voltage in turning-on the power MOSFET, the Leading Edge Blanking, t_{BW} = 330 ns is built-in. During t_{BW}, the OCP threshold voltage becomes $V_{OCP(LEB)}$ = 1.69 V which is higher than the normal OCP threshold voltage (see Section 11.10).

11.7. Random Switching Function

The IC modulates its switching frequency randomly by superposing the modulating frequency on $f_{OSC(AVG)}$ in normal operation. This function reduces the conduction noise compared to others without this function, and simplifies noise filtering of the input lines of power supply.

11.8. Step Drive Control

Figure 11-9 shows a flyback control circuit. The both end of secondary rectification diode (D51) is generated surge voltage when a power MOSFET turns on. Thus, V_{RM} of D51 should be set in consideration of the surge.

The IC optimally controls the gate drive of the internal power MOSFET (Step drive control) depending on the load condition. The step drive control reduces the surge voltage of D51 when the power MOSFET turns on (See Figure 11-10). Since V_{RM} of D51 can be set to lower value than usual, the price reduction and the increasing circuit efficiency are achieved by using a diode of low V_F.

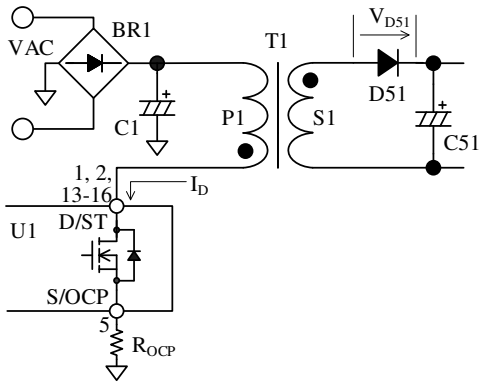


Figure 11-9. Flyback Control Circuit

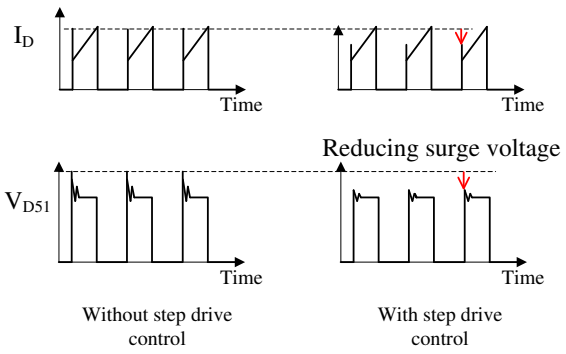


Figure 11-10. I_D and V_{D51} Waveforms

11.9. Operation Mode

As shown in Figure 11-11, when the output power is decreasing, together with the decrease of the drain current I_D of the internal power MOSFET, the operation mode is automatically changed to the fixed switching frequency mode (100 kHz), to the Green mode controlled the switching frequency (25 kHz to 100 kHz), and to the burst oscillation mode controlled by an internal oscillator. In the Green mode, the number of switching is reduced. In the burst oscillation mode, the switching operation is stopped during a constant period. Thus, the switching loss is reduced, and the power efficiency is improved.

When the output load becomes lower, FB/OLP pin voltage decreases. When FB/OLP pin voltage decreases to $V_{FB(FDS)}$ = 3.60 V or less, the green mode is activated and the oscillation frequency starts decreasing. When FB/OLP pin voltage becomes $V_{FB(FDE)}$ = 3.10 V, the oscillation frequency stops decreasing. At this point, the oscillation frequency becomes $f_{OSC(MIN)}$ = 25 kHz.

When FB/OLP pin voltage further decreases and becomes the standby operation point, the burst oscillation mode is activated. As shown in Figure 11-12, the burst oscillation mode consists of switching period and non-switching period. The oscillation frequency during switching period is the Minimum Frequency, $f_{OSC(MIN)}$ = 25 kHz.

Generally, to improve efficiency under light load conditions, the frequency of the burst mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst mode, audible noises can be reduced.

The OCP detection usually has some detection delay time. The higher the AC input voltage is, the steeper the slope of I_D is. Thus, the peak drain current at the burst oscillation mode becomes high at a high AC input voltage.

It is necessary to consider that the burst frequency becomes low at a high AC input.

If the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.6 V during the transition to the burst mode, the Bias Assist function is activated and stabilizes the standby mode, because the Startup Current, $I_{CC(ST)}$, is provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$. However, if the Bias Assist function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and secondary-side winding and/or reducing the value of R2 (see Section 12.1).

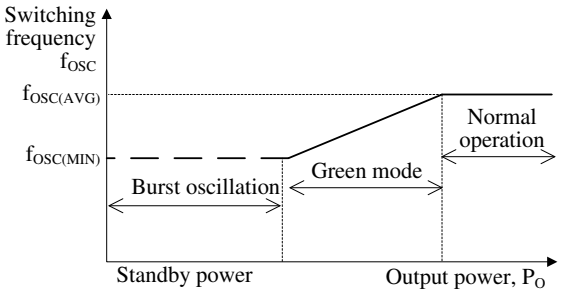


Figure 11-11. Relationship between P_O and f_{OSC}

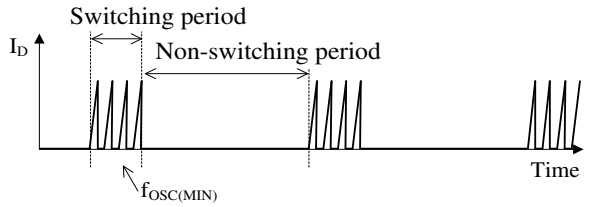


Figure 11-12. Switching Waveform at Burst Oscillation

11.10. AC Input Voltage Detection Function

This function has the following:

- AC Input Overvoltage Function (HVP)
- Brown-In and Brown-Out Function

This function turns on and off switching operation according to the BR pin voltage detecting the AC input voltage, and thus prevents excessive input current and over heating.

Section 11.10.1 shows HVP, Section 11.10.2 shows Brown-In and Brown-Out Function. Figure 11-13 shows waveforms of the BR pin voltage and the drain currnet.

There are two types of detection method as shown in Section 11.10.3 and Section 11.10.4.

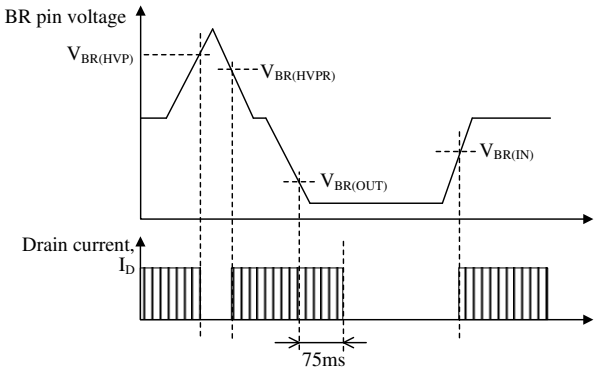


Figure 11-13. BR Pin Voltage and Drain Current Waveforms

11.10.1. AC Input Overvoltage Function (HVP)

When the AC input voltage increases from steady state and the BR pin voltage reaches $V_{BR(HVP)}$ = 5.51 V or more, the IC stops switching operation.

After that, when the AC input voltage decreases and the BR pin voltage falls to $V_{BR(HVPR)}$ = 5.39 V or less, the IC starts switching operation.

By the hysteresis of the HVP threshold voltage, the HVP operation can keep stable without the response of small voltage fluctuations at the BR pin.

11.10.2. Brown-In and Brown-Out Function

Even if the IC is in the operating state that the VCC pin voltage is $V_{CC(OFF)}$ or more, when the AC input voltage decreases from steady-state and the BR pin voltage falls to $V_{BR(OUT)}$ = 0.85 V or less for the OLP Delay Time, t_{OLP} = 75 ms, the IC stops switching operation. When the AC input voltage increases and the BR pin voltage reaches $V_{BR(IN)}$ = 1.11 V or more in the operating state that the VCC pin voltage is $V_{CC(OFF)}$ or more, the IC starts switching operation. The function is disabled during switching operation stop in burst oscillation mode. When the BR pin voltage falls to $V_{BR(OUT)}$ or less in burst oscillation mode and the sum of switching operation period becomes t_{OLP} or more, the IC stops switching operation.

11.10.3. DC Line Detection

Figure 11-14 shows BR pin peripheral circuit of DC line detection. There is a ripple voltage on C1 occurring at a half period of AC cycle. In order to detect each peak of the ripple voltage, the time constant of RC and C4 should be shorter than a half period of AC cycle.

Since the period of the ripple voltage is shorter than t_{OLP}, the switching operation does not stop when only the bottom part of the ripple voltage becomes lower than $V_{BR(OUT)}$.

Thus, it minimizes the influence of load conditions on the voltage detection.

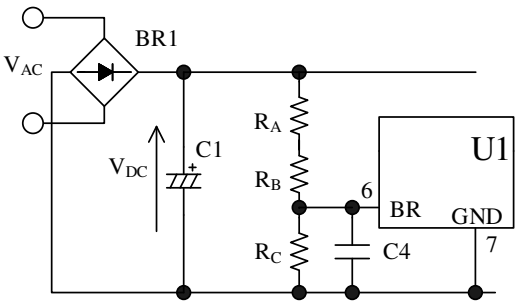


Figure 11-14. DC Line Detection

The components around BR pin:

- R_A and R_B are a few megohms. Because of high voltage applied and high resistance, it is recommended to select a resistor designed against electromigration or use a combination of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
- R_C is a few hundred kilohms
- C4 is 470 pF to 2200 pF for high frequency noise rejection

Neglecting the effect of both input resistance and forward voltage of rectifier diode, the reference value of C1 voltage when HVP and Brown-In and Brown-Out function is activated is calculated as follows:

$$V_{DC(OP)} = V_{BR(TH)} \times \left(1 + \frac{R_A + R_B}{R_C}\right) \quad (3)$$

Where:

$V_{DC(OP)}$: C1 voltage when HVP and Brown-In and Brown-Out function is activated

$V_{BR(TH)}$: Any one of threshold voltage of BR pin (see Table 11-1)

Table 11-1 BR pin threshold voltage

Parameter	Symbol	Value (Typ.)
AC Input Overvoltage Protection (HVP) Threshold Voltage	$V_{BR(HVP)}$	5.51 V
AC Input Overvoltage Protection (HVP) Release Threshold Voltage	$V_{BR(HVPR)}$	5.39 V
Brown-In Threshold Voltage	$V_{BR(IN)}$	1.11 V
Brown-Out Threshold Voltage	$V_{BR(OUT)}$	0.85 V

$V_{DC(OP)}$ can be expressed as the effective value of AC input voltage using Equation (4).

$$V_{AC(OP)RMS} = \frac{1}{\sqrt{2}} \times V_{DC(OP)} \quad (4)$$

R_A, R_B, R_C and C4 should be selected based on actual operation in the application.

11.10.4. AC Line Detection

Figure 11-15 shows BR pin peripheral circuit of AC line detection. In order to detect the AC input voltage, the time constant of RC and C4 should be longer than the period of AC cycle. Thus the response of BR pin detection becomes slow compared with the DC line detection. This method detects the AC input voltage, and thus it minimizes the influence from load conditions. Also, this method is free of influence from C1 charging and discharging time.

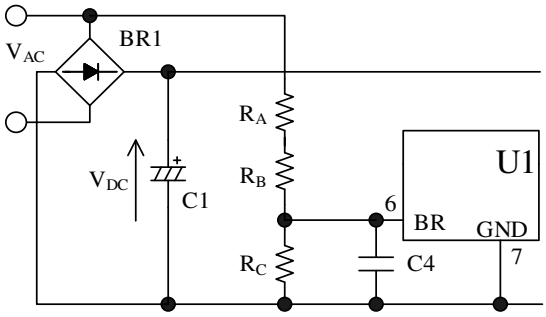


Figure 11-15. AC Line Detection

The components around BR pin:

- R_A and R_B are a few megohms. Because of high voltage applied and high resistance, it is recommended to select a resistor designed against electromigration or use a combination of resistors in series for that to reduce each applied voltage, according to the requirement of the application.
- R_C is a few hundred kilohms
- C4 is 0.22 µF to 1 µF for averaging AC input voltage and high frequency noise reduction. rejection

Neglecting the effect of input resistance is zero, the reference effective value of AC input voltage when HVP and Brown-In and Brown-Out function is activated is calculated as follows:

$$V_{AC(OP)RMS} = \frac{\pi}{\sqrt{2}} \times V_{BR(TH)} \times \left(1 + \frac{R_A + R_B}{R_C}\right) \quad (5)$$

Where:

$V_{AC(OP)RMS}$:the effective value of AC input voltage when HVP and Brown-In and Brown-Out function is activated

$V_{BR(TH)}$:Any one of threshold voltage of BR pin (see Table 11-1)

R_A, R_B, R_C and C4 should be selected based on actual operation in the application.

11.11. Overcurrent Protection (OCP)

11.11.1. Overcurrent Protection Operation

Overcurrent Protection (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to OCP threshold voltage.

During Leading Edge Blanking Time, the OCP threshold voltage becomes $V_{OCP(LEB)}$ = 1.69 V which is higher than the normal OCP threshold voltage as shown in Figure 11-16. Changing to this threshold voltage

prevents the IC from responding to the surge voltage in turning-on the power MOSFET. This function operates as protection at the condition such as output windings shorted or unusual withstand voltage of secondary-side rectifier diodes.

When power MOSFET turns on, the surge voltage width of S/OCP pin should be less than t_{BW}, as shown in Figure 11-16. In order to prevent surge voltage, pay extra attention to R_{OCP} trace layout (see Section 12.2).

In addition, if a C (RC) damper snubber of Figure 11-17 is used, reduce the capacitor value of damper snubber.

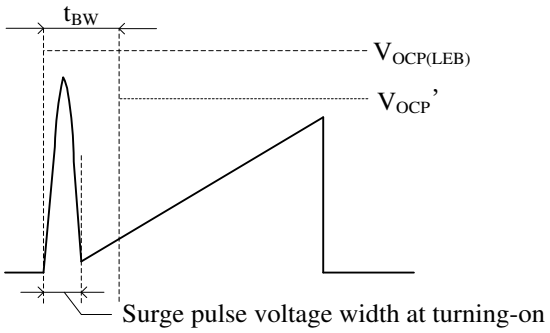


Figure 11-16. S/OCP Pin Voltage

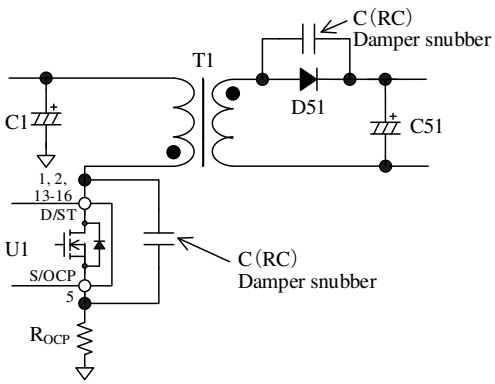


Figure 11-17. Damper Snubber

When AC input voltage is low (Duty cycle is broad), the OCP threshold voltage is controlled to become high. The difference of peak drain current become small compared with the case where the AC input voltage is high (Duty cycle is narrow).

The compensation signal depends on duty cycle. The relation between the duty cycle and the OCP threshold voltage after compensation V_{OCP}' is expressed as Equation (6). When duty cycle is broader than 36 %, the V_{OCP}' becomes a constant value $V_{OCP(H)} = 0.888$ V

$$V_{OCP}' = V_{OCP(L)} + DPC \times ONTime$$

$$= V_{OCP(L)} + DPC \times \frac{ONDuty}{f_{OSC(AVG)}} \quad (6)$$

where,
$V_{OCP(L)}$: OCP Threshold Voltage at zero duty cycle
DPC: OCP Compensation Coefficient
ONTime: On-time of power MOSFET
ONDuty: Duty cycle of power MOSFET
$f_{OSC(AVG)}$: Average PWM Switching Frequency

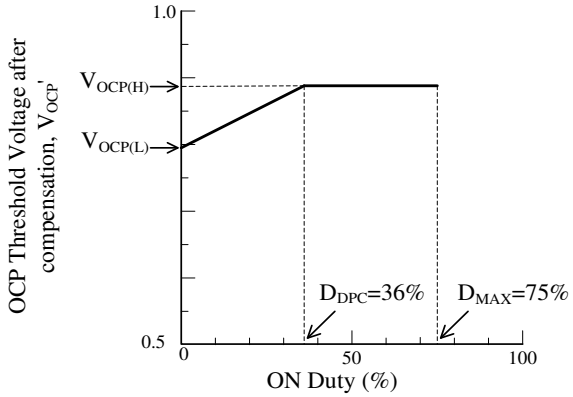


Figure 11-18 Relationship between Duty Cycle and Drain Current Limit after compensation

11.11.2. Input Compensation Function

ICs with PWM control usually have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the detection voltage of actual drain peak current is, compared to V_{OCP}. Thus, the peak current has some variation depending on the AC input voltage in OCP state.

In order to reduce the variation of peak current in OCP state, the IC incorporates a built-in Input Compensation Function.

The Input Compensation Function is the function of correction of OCP threshold voltage depending with AC input voltage, as shown in Figure 11-18.

11.12. Overload Protection (OLP)

Figure 11-19 shows the FB/OLP pin peripheral circuit, and Figure 11-20 shows each waveform for OLP operation.

When the peak drain current of I_D is limited by OCP operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler becomes zero. Thus, the feedback current, I_{FB}, charges C3 connected to the FB/OLP pin and the FB/OLP pin voltage increases. When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ = 7.3 V or more for the OLP delay time, t_{OLP} = 75 ms or more, the OLP function is activated, the IC stops switching operation.

During OLP operation, the intermittent operation by VCC pin voltage repeats and reduces the stress of parts such as the power MOSFET and secondary side rectifier diode.

When the OLP function is activated, the IC stops switching operation, and the VCC pin voltage decreases.

During OLP operation, the Bias Assist Function is disabled. When the VCC pin voltage decreases to $V_{CC(OFF)SKP}$ (about 9 V), the startup current flows, and the VCC pin voltage increases. When the VCC pin voltage increases to $V_{CC(ON)}$, the IC starts operation, and the circuit current increases. After that, the VCC pin voltage decreases. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.5 V, the control circuit stops operation.

Skipping the UVLO operation of $V_{CC(OFF)}$ (see Section 0), the intermittent operation makes the non-switching interval longer and restricts the temperature rise of the power MOSFET.

When the abnormal condition is removed, the IC returns to normal operation automatically.

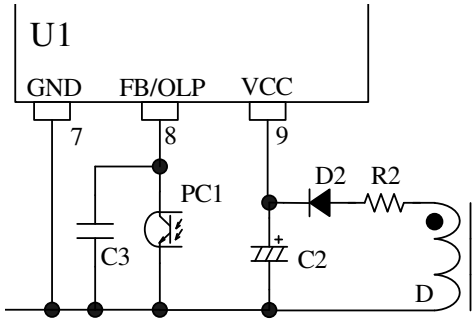


Figure 11-19. FB/OLP Pin Peripheral Circuit

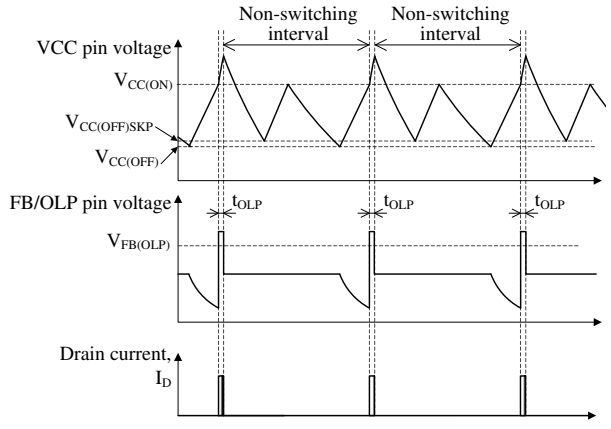


Figure 11-20. OLP Operational Waveforms

11.13. Overvoltage Protection (OVP)

When a voltage between VCC pin and GND pin increases to $V_{CC(OVP)}$ = 29.1 V or more, Overvoltage Protection (OVP) is activated, the IC stops switching operation. During OVP operation, the Bias Assist function is disabled, the intermittent operation by UVLO is repeated (refer to Section 11.12). When the fault condition is removed, the IC returns to normal operation automatically (refer to Figure 11-21).

In case the VCC pin voltage is provided by using auxiliary winding of transformer, the overvoltage conditions such as output voltage detection circuit open can be detected because the VCC pin voltage is proportional to output voltage. The approximate value of output voltage $V_{OUT(OVP)}$ in OVP condition is calculated by using Equation (7).

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 29.1\ (V) \quad (7)$$

where,
$V_{OUT(NORMAL)}$: Output voltage in normal operation
$V_{CC(NORMAL)}$: VCC pin voltage in normal operation

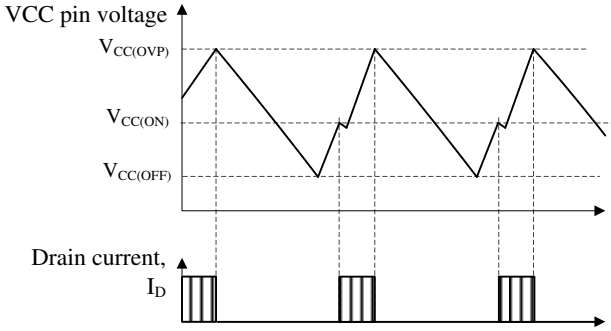


Figure 11-21. OVP Operational Waveforms

11.14. Thermal Shutdown (TSD)

Figure 11-22 shows the Thermal Shutdown (TSD) operational waveforms.

When the temperature of control circuit increases to $T_{J(TSD)}$ = 145 °C or more, TSD is activated, and the IC stops switching operation.

After that, VCC pin voltage decreases. When the VCC pin voltage decreases $V_{CC(BIAS)}$, the bias assist function is activated and VCC pin voltage is kept to over the $V_{CC(OFF)}$.

When the temperature reduces to less than $T_{J(TSD)}$–$T_{J(TSD)HYS}$, the Bias Assist function is disabled and the VCC pin voltage decreases to $V_{CC(OFF)}$. At that time, the IC stops operation by the UVLO circuit and reverts to the state before startup. After that, the startup circuit is activated, the VCC pin voltage increases to $V_{CC(ON)}$, and the IC starts switching operation again.

In this way, the intermittent operation by TSD and UVLO is repeated while there is an excess thermal condition.

When the fault condition is removed and the temperature reduces to less than $T_{J(TSD)}$–$T_{J(TSD)HYS}$, the IC returns to normal operation automatically.

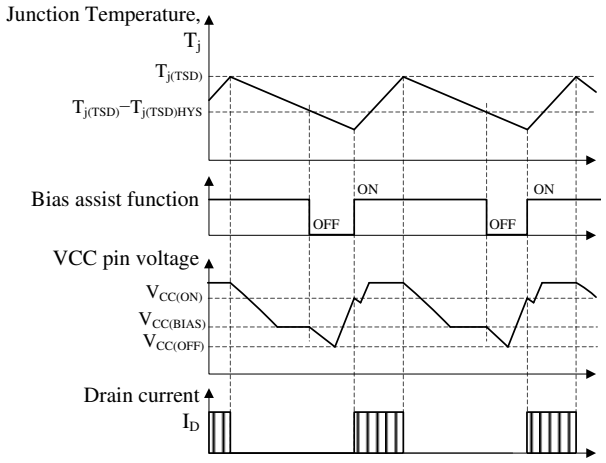


Figure 11-22. TSD Operational Waveforms

12. Design Notes

12.1. External Components

Take care to use properly rated, including derating as necessary and proper type of components.

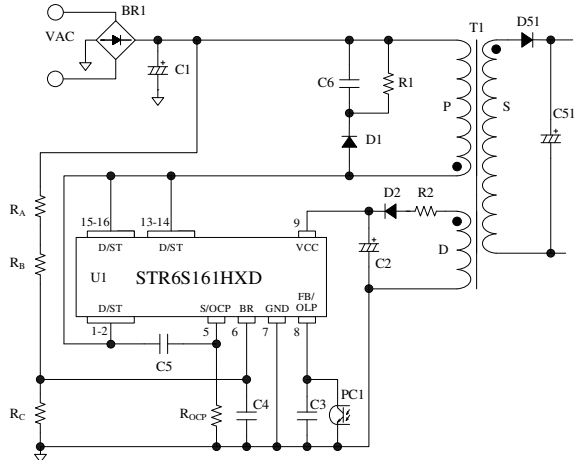


Figure 12-1. The IC Peripheral Circuit

12.1.1. Input and Output Electrolytic Capacitor

Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

12.1.2. S/OCP Pin Peripheral Circuit

In Figure 12-1, R_{OCP} is the resistor for the current detection. A high frequency switching current flows to ROCP, and may cause poor operation if a high inductance resistor is used. Choose a low inductance and high surge-tolerant type.

12.1.3. BR Pin peripheral circuit

Because R_A and R_B (see Figure 12-1) are applied high voltage and are high resistance, the following should be considered according to the requirement of the application:

- Select a resistor designed against electromigration, or
- Use a combination of resistors in series for that to reduce each applied voltage

See the section 11.10 about the AC input voltage detection function and the components around BR pin.

12.1.4. FB/OLP Pin Peripheral Circuit

C3 is for high frequency noise reduction and phase compensation, and should be connected close to these pins. The value of C3 is recommended to be about 2200 pF to 0.01 µF, and should be selected based on actual operation in the application.

12.1.5. VCC Pin Peripheral Circuit

The value of C2 is generally recommended to be 10 µF to 47 µF (see Section 11.1, because the startup time is determined by the value of C2).

In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, IOUT (see Figure 12-2), and the Overvoltage Protection (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.

For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 12-1). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design。

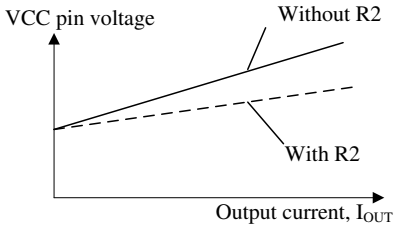


Figure 12-2. Variation of VCC Pin Voltage and Output Current

12.1.6. Snubber Circuit

If the surge voltage of V_{DS} is large, the circuit should be added as follows (see Figure 12-1);

- A clamp snubber circuit of a capacitor-resistor- diode (CRD) combination should be added on the primary winding P.
- A damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin. When the damper snubber circuit is added, this components should be connected near D/ST pin and S/OCP pin.

12.1.7. Phase Compensation

A typical phase compensation circuit with a secondary shunt regulator (U51) is shown in Figure 12-3. C52 and R53 are for phase compensation. The value of C52 and R53 are recommended to be around 0.047µF to 0.47µF and 4.7 kΩ to 470 kΩ, respectively. They should be selected based on actual operation in the application.

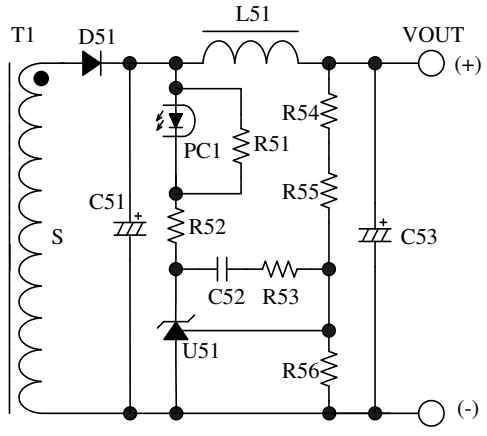


Figure 12-3. Peripheral Circuit around Secondary Shunt Regulator (U51)

12.1.8. Transformer

Apply proper design margin to core temperature rise by core loss and copper loss.

Because the switching currents contain high frequency currents, the skin effect may become a consideration.

Choose a suitable wire gauge in consideration of the RMS current and a current density of 4 to 6 A/mm^2.
If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

- Increase the number of wires in parallel.
- Use litz wires.
- Thicken the wire gauge.

In the following cases, the surge of VCC pin voltage becomes high.

- The surge voltage of primary main winding, P, is high (low output voltage and high output current power supply designs)
- The winding structure of auxiliary winding, D, is susceptible to the noise of winding P.

When the surge voltage of winding D is high, the VCC pin voltage increases and the Overvoltage Protection (OVP) may be activated. In transformer design, the following should be considered;

- The coupling of the winding P and the secondary output winding S should be maximized to reduce the leakage inductance.
- The coupling of the winding D and the winding S should be maximized.
- The coupling of the winding D and the winding P should be minimized.

In the case of multi-output power supply, the coupling of the secondary-side stabilized output winding, S1, and the others (S2, S3···) should be maximized to improve the line-regulation of those outputs.

Figure 12-4 shows the winding structural examples of two outputs.

- Winding structural example (a):
  S1 is sandwiched between P1 and P2 to maximize the coupling of them for surge reduction of P1 and P2.
  D is placed far from P1 and P2 to minimize the coupling to the primary for the surge reduction of D.

- Winding structural example (b)
  P1 and P2 are placed close to S1 to maximize the coupling of S1 for surge reduction of P1 and P2.
  D and S2 are sandwiched by S1 to maximize the coupling of D and S1, and that of S1 and S2. This structure reduces the surge of D, and improves the line-regulation of outputs.

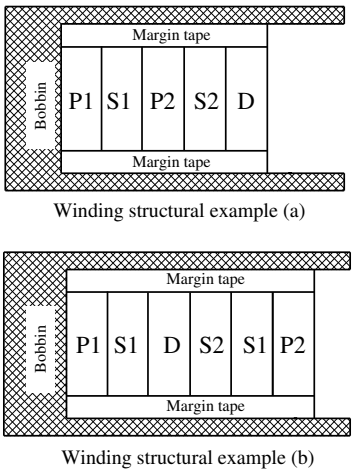


Figure 12-4. Winding Structural Examples

12.2. PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 12-5 shows the circuit design example.

(1) Main Circuit Trace Layout

This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground Trace Layout

Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 12-5 as close to the R_{OCP} pin as possible.

(3) VCC Trace Layout

This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C2 and the IC are distant from each other, placing a capacitor such as film capacitor C_f (about 0.1 μF to 1.0 μF) close to the VCC pin and the GND pin is recommended.

(4) R_{OCP} Trace Layout

R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 12-5) which is close to the base of R_{OCP}.

(5) Peripheral components of the IC

The components for control connected to the IC should be placed as close as possible to the IC, and should be connected as short as possible to the each pin.

(6) Secondary Rectifier Smoothing Circuit Trace Layout

This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(7) Thermal Considerations

Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design.

Since the copper area under the IC and the D/ST pin trace act as a heatsink, its traces should be as wide as possible.

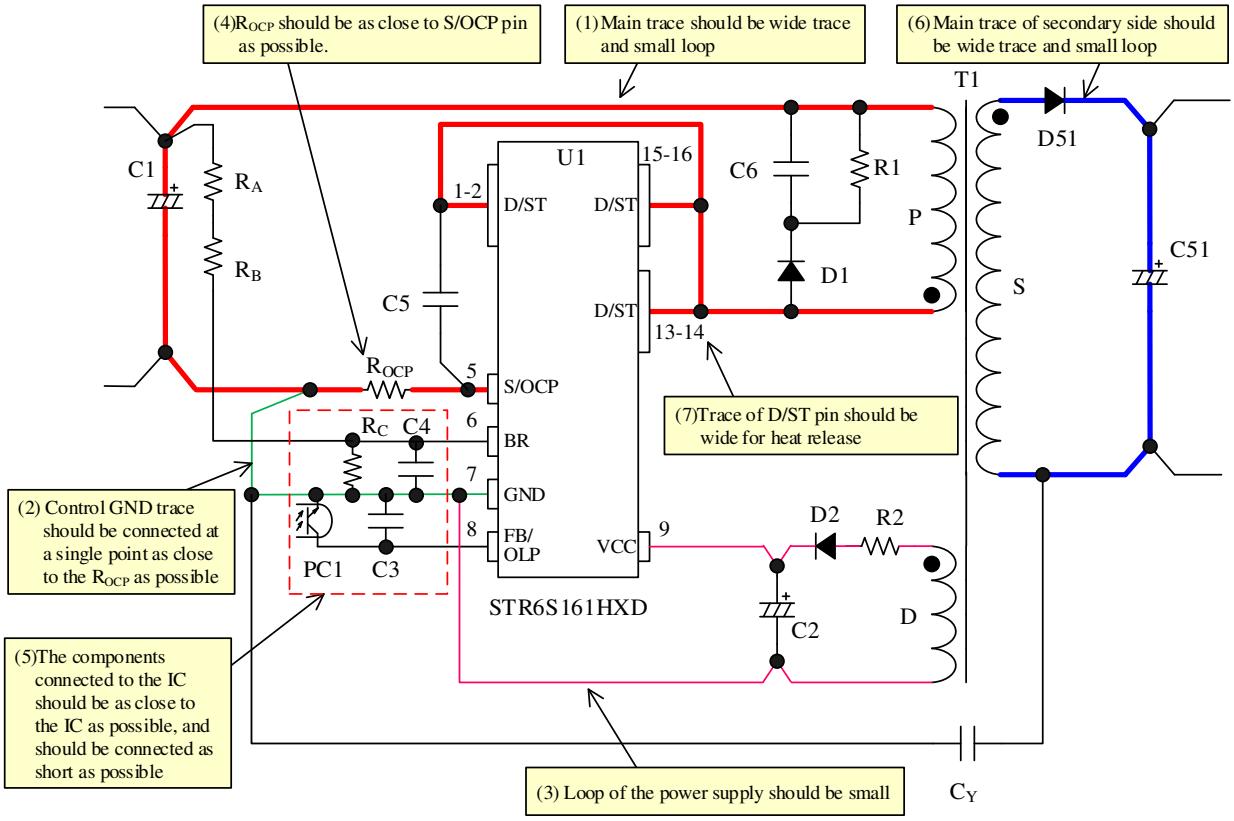
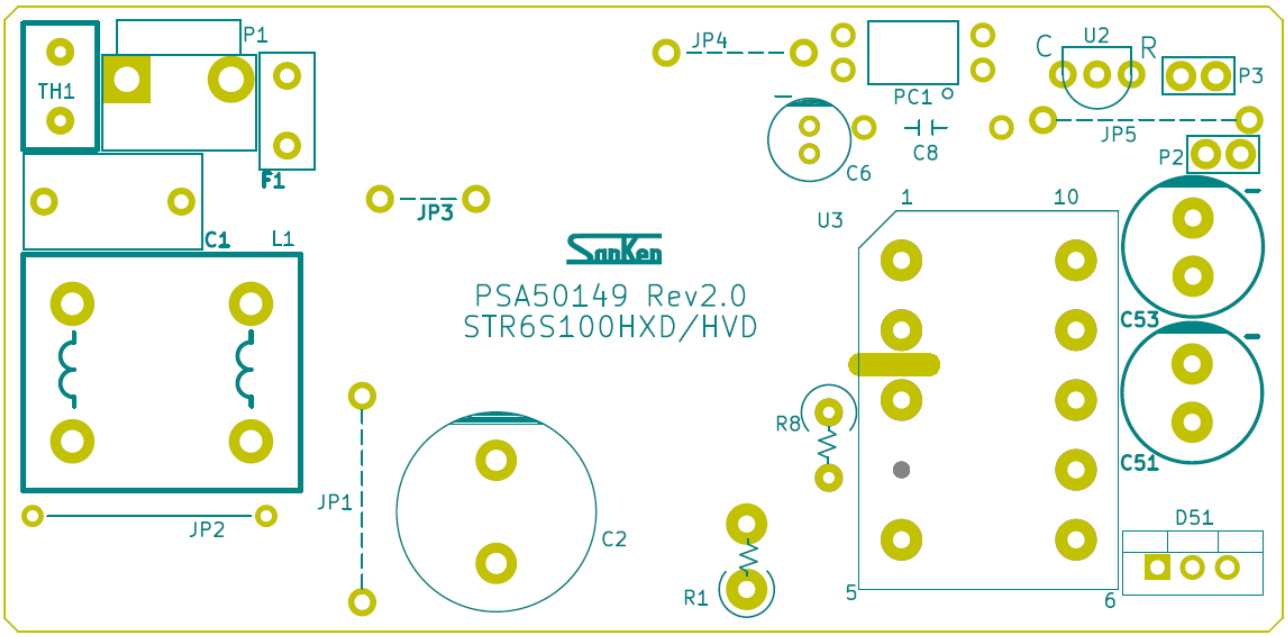


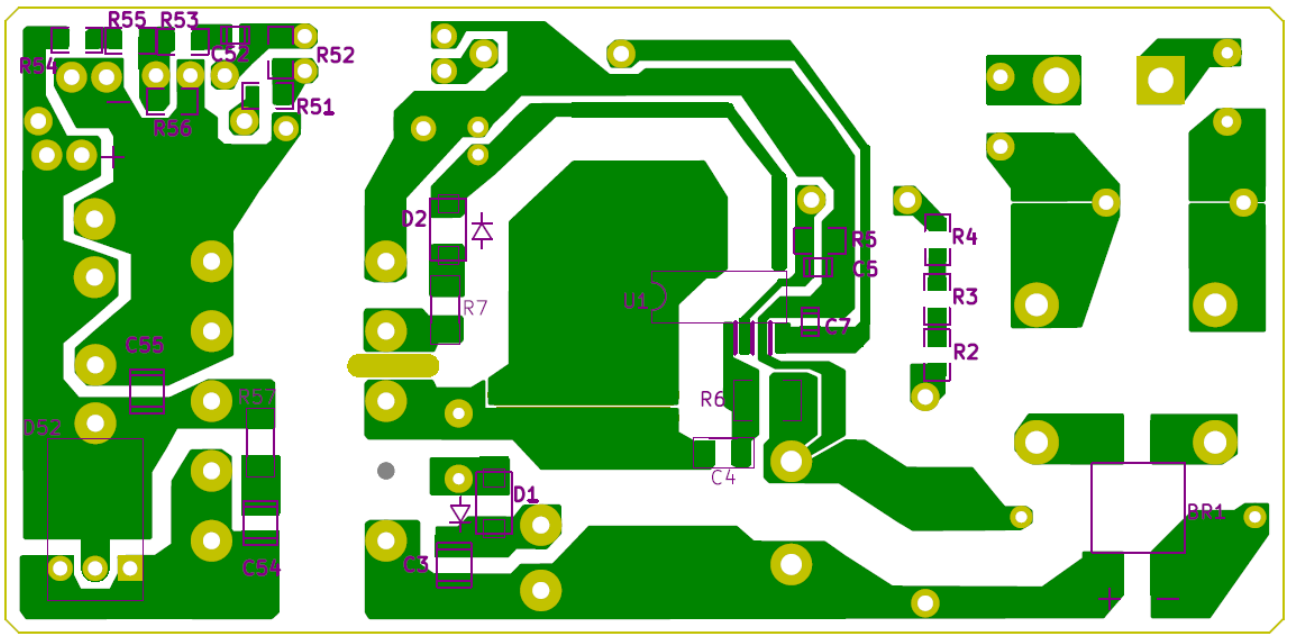
Figure 12-5. Peripheral Circuit Example around the IC

13. Pattern Layout Example

The following show the PCB pattern layout example and the schematic of circuit using



(a) Top View



(b) Bottom View

Figure 13-1. PCB Circuit Trace Layout Example

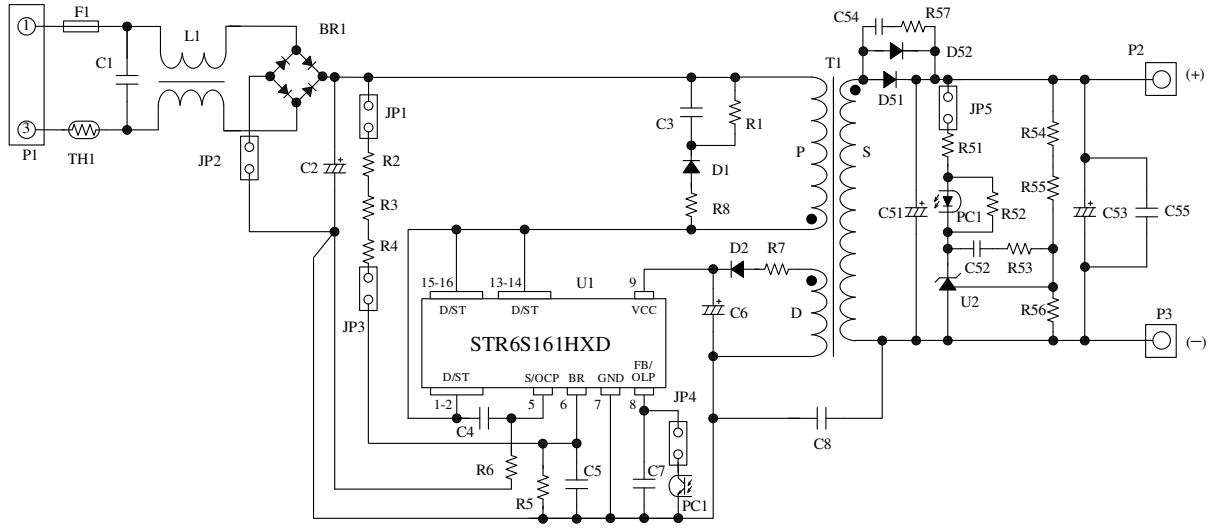


Figure 13-2. Circuit Schematic for PCB Circuit Trace Layout

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