HARRIS SEMICONDUCTOR

CDP1824
CDP1824C

32-Word x 8-Bit Static RAM

February 1992

Features

- **Fast Access Time**
  - V_{DD} = 5V 710ns
  - V_{DD} = 10V 320ns
- **No Precharge or Clock Required**

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V
Plastic DIP	-40°C to +85°C	CDP1824CE	CDP1824E
Burn-In		CDP1824CEX	CDP1824EX
Ceramic DIP	-40°C to +85°C	CDP1824CD	CDP1824D
Burn-In		CDP1824CDX	-
*883B	-55°C to +125°C	CDP1824CD3	CDP1824D3

*Respective specifications are included at the end of this datasheet.

Description

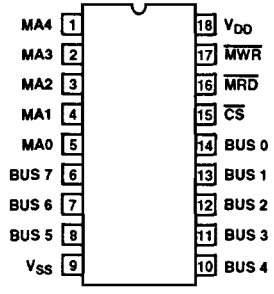
The CDP1824 and CDP1824C are 32-word x 8-bit fully static CMOS random-access memories for use in CDP-1800 series microprocessor systems. These parts are compatible with the CDP1802 microprocessor and will interface directly without additional components.

The CDP1824 is fully decoded and does not require a precharge or clocking signal for proper operation. It has common input and output and is operated from a single voltage supply. The $\overline{MRD}$ signal (output disable control) enables the three-state output drivers, and overrides the $\overline{MWR}$ signal. A $\overline{CS}$ input is provided for memory expansion.

The CDP1824C is functionally identical to the CDP1824. The CDP1824 has an operating range of 4 volts to 10.5 volts, and the CDP1824C has an operating voltage range of 4 volts to 6.5 volts. The CDP 1824 and CDP1824C are supplied in 18 lead hermetic dual-in-line ceramic packages (D suffix), and in 18 lead dual-in-line plastic packages (E suffix).

Pinout

18 LEAD DIP
TOP VIEW



OPERATIONAL MODES

FUNCTION	$\overline{CS}$	$\overline{MRD}$	$\overline{MWR}$	DATA PINS STATUS
Read	0	0	X	Output: High/Low Dependent on Data
Write	0	1	0	Input: Output Disabled
Not Selected	1	X	X	Output Disabled: High Impedance State
Standby	0	1	1	Output Disabled: High Impedance State

Logic 1 = High, Logic 0 = Low, X = Don't Care

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1103.1**

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}):
(All Voltages Referenced to V_{SS} Terminal)
CDP1824 ..... −0.5V to +11V
CDP1824C ..... −0.5V to +7V
Input Voltage Range, All Inputs ..... −0.5V to V_{DD} +0.5V
DC Input Current, Any One Input ..... ±10mA
Operating Temperature Range (T_A):
Package Type D ..... −55°C to +125°C
Package Type E ..... −40°C to +85°C
Storage Temperature Range (T_{stg}) ..... −65°C to +150°C
Lead Temperature (During Soldering):
At distance 1/16 ±1/32 in. (1.59 ± 0.79mm)
from case for 10s max ..... +265°C

Recommended Operating Conditions

At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	CONDITION	LIMITS				UNITS
		CDP1824D		CDP1824CD		
	V_{DD} (V)	MIN	MAX	MIN	MAX	
Supply Voltage Range	-	4	10.5	4	6.5	V
Recommended Input Voltage Range	-	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V
Input Signal Rise or Fall Time (Note 1)	5	-	5	-	5	µs
t_r, t_f	10	-	2	-	-	µs

NOTE:
1. Input signal rise or fall times longer than these maxima can cause loss of stored data in either the selected or deselected mode.

Static Electrical Characteristics

At T_A = -40°C to +85°C, Except as Noted:

CHARACTERISTIC	SYMBOL	CONDITIONS			LIMITS						UNITS
					CDP1824			CDP1824C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(Note 1) TYP	MAX	MIN	(Note 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	-	5	-	25	50	-	100	200	µA
		-	-	10	-	250	500	-	-	-	µA
Output Low (Sink) Current	I_{OL}	0.4	0, 5	5	1.8	2.2	-	1.8	2.2	-	mA
		0.5	0, 10	10	3.6	4.5	-	-	-	-	mA
Output High (Source) Current	I_{OH}	4.6	0, 5	5	-0.9	-1.1	-	-0.9	-1.1	-	mA
		9.5	0, 10	10	-1.8	-2.2	-	-	-	-	mA
Output Voltage Low-Level	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		1.9	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 9.5	-	5	3.5	-	-	3.5	-	-	V
		1.9	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	± 0.1	± 1	-	± 0.1	± 1	µA
			0, 10	10	-	± 0.1	± 1	-	-	-	µA
Operating Current (Note 2)	I_{DD1}	-	0, 5	5	-	4	8	-	4	8	mA
		-	0, 10	10	-	8	16	-	-	-	mA
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	± 0.2	±2.0	-	± 0.2	± 2	µA
		0, 10	0, 10	10	-	± 0.2	±2.0	-	-	-	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	-	10	15	pF

NOTES:
1. Typical values are for T_A = +25°C and nominal V_{DD}.
2. Outputs open circuited; Cycle time = 1µs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ; See Fig. 1.

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1824D CDP1824E			CDP1824CD CDP1824CE			
		Min.#	Typ.●	Max.	Min.#	Typ.●	Max.	
Read Operation								
Access Time From Address Change, t_{AA}	5	–	400	710	–	400	710	ns
	10	–	200	320	–	–	–	
Access Time From Chip Select, t_{DOA}	5	–	300	710	–	300	710	ns
	10	–	150	320	–	–	–	
Output Active From $\overline{MRD}$, t_{AM}	5	–	300	710	–	300	710	ns
	10	–	150	320	–	–	–	

= Time required by a limit device to allow for the indicated function.

● Time required by a typical device to allow for the indicated function. Typical values are for T_A = 25°C and nominal V_{DD}.

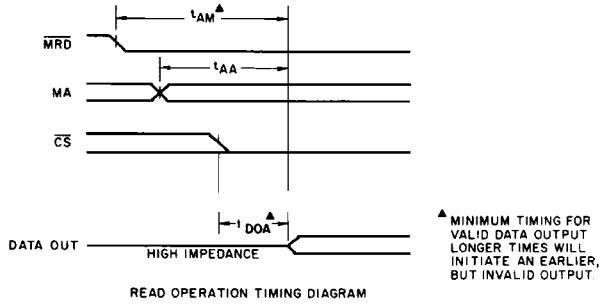


Fig. 1 - Read cycle timing diagram.

Note:

The dynamic characteristics and timing diagrams indicate maximum performance capability of the CDP1824. When used directly with the CDP1802 microprocessor, timing will be determined by the clock frequency and internal delays of the microprocessor.

The following general timing relationships will hold when the CDP1824 is used with the CDP1802 microprocessor:

$t_{WW} = 2\ t_c$

$t_{AH} = 1.0\ t_c$

$t_{AS} = 4.5\ t_c$

$t_{DH} = 1.0\ t_c$ } Data transfers from

$t_{DS} = 5.5\ t_c$ } CDP1802 to memory

$\overline{MRD}$ occurs one clock period (t_c) earlier than the address bits MA0-MA7.

where $t_c = \dfrac{1}{\text{CDP1802 clock frequency}}$

The CDP1824 is capable of operating at the maximum clock frequency of the CDP1802 microprocessor.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = –40 to +85°C, V_{DD} ±5%, Input t_r, t_f = 10 ns, C_L = 50 pF, R_L = 200 kΩ; See Fig. 2.

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS						UNITS
		CDP1824D CDP1824E			CDP1824CD CDP1824CE			
		Min.#	Typ.•	Max.	Min.#	Typ.•	Max.	
Write Operation								
Write Pulse Width, t_{WRW}	5	390	200	–	390	200	–	ns
	10	180	150	–	–	–	–	
Data Setup Time, t_{DS}	5	390	100	–	390	100	–	ns
	10	180	50	–	–	–	–	
Data Hold Time, t_{DH}	5	70	40	–	70	40	–	ns
	10	35	20	–	–	–	–	
Chip Select Setup Time, t_{CS}	5	425	210	–	425	210	–	ns
	10	215	110	–	–	–	–	
Address Setup Time, t_{AS}	5	640	500	–	640	500	–	ns
	10	390	300	–	–	–	–	

= Time required by a limit device to allow for the indicated function.

• Time required by a typical device to allow for the indicated function. Typical values are for T_A = 25°C and nominal V_{DD}.

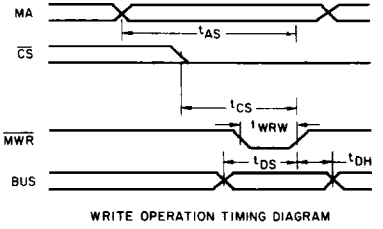


Fig. 2 - Write cycle timing diagram.

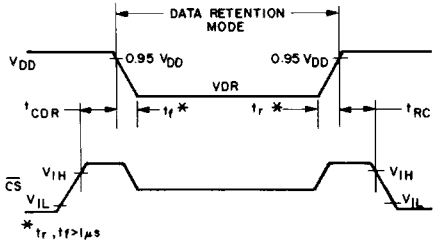


Fig. 3 - Low V_{DD} data retention waveforms and timing diagram.

DATA RETENTION CHARACTERISTICS at T_A = −40 to +85°C; See Fig. 3.

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	CDP1824		CDP1824C		UNITS
			Min.	Max.	Min.	Max.	
Data Retention Voltage, V_{DR}		–	2.5	–	2.5	–	V
Data Retention Quiescent Current, I_{DD}	V_{DR} = 2.5 V	–	–	10	–	40	μA
Chip Deselect to Data Retention Time, t_{CDR}	V_{DR} = 2.5 V	5	600	–	600	–	ns
		10	300	–	–	–	
Recovery to Normal Operation Time, t_{RC}	V_{DR} = 2.5 V	5	600	–	600	–	
		10	300	–	–	–	

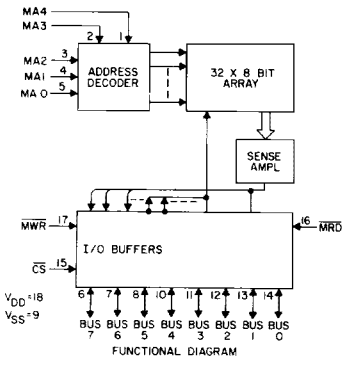


Fig. 4 - Functional diagram.

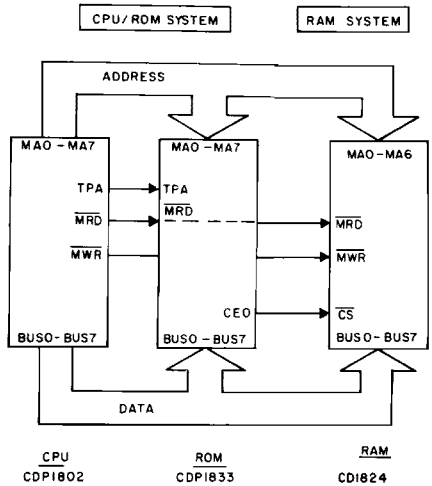


Fig. 5 - CDP1824 (128 x 8) minimum system (128 x 8)