LVDS ZERO DELAY BUFFER w/ JITTER ATTENUATION FOR VIDEO APPLICATIONS

ICS864S004I

General Description

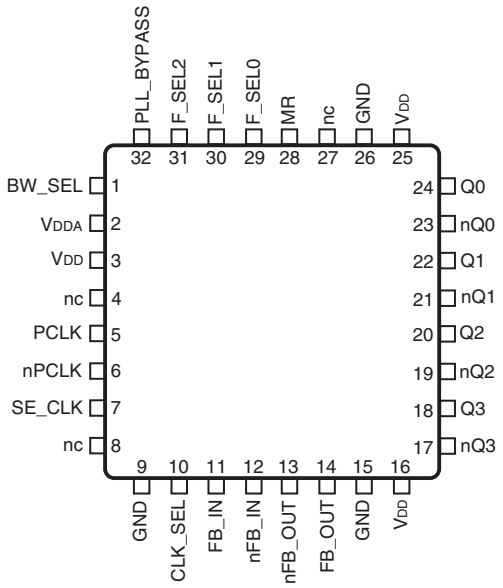
The ICS864S004I is Zero-Delay Buffer with four differential LVDS output pairs, and uses external feedback for “zero delay” clock regeneration. Another feature of the device is the ability to select different bandwidth modes during normal operation to allow for additional clock jitter attenuation.

The output frequency range is specified to include the most common video rates used in professional video systems. With a wide frequency range, the ICS864S004I is ideal for use in video applications where zero-delay, low skew and jitter attenuation are critical factors.

Features

- Four LVDS differential output pairs, and one feedback output pair
- One differential clock input pair PCLK, nPCLK can accept the following differential input levels: LVDS, LVPECL, CML, SSTL
- Maximum output frequency: 333.33MHz
- VCO range: 1.2GHz – 2GHz
- Cycle-to-cycle jitter: TBD
- 3.3V operating supply voltage
- Two bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- External feedback for “zero delay” clock regeneration
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Pin Assignment



32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Block Diagram

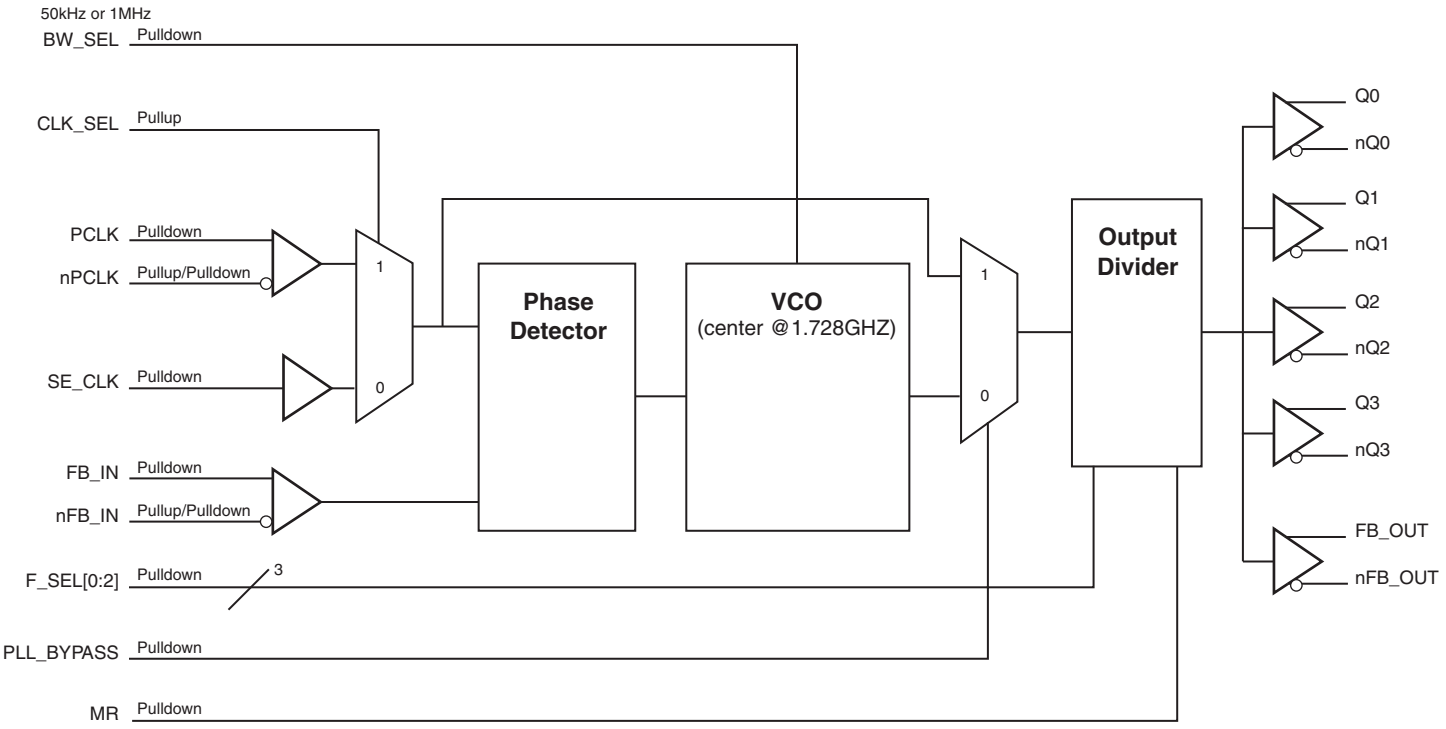


Table 1. Pin Descriptions

Number	Name	Type		Description
1	BW_SEL	Input	Pulldown	Selects between 50kHz and 1MHz PLL bandwidth modes. When HIGH selects 1MHz PLL bandwidth. When LOW selects 50kHz PLL bandwidth. LVCMOS/LVTTL interface levels.
2	V_{DDA}	Power		Analog supply pin.
3, 16, 25	V_{DD}	Power		Core supply pins.
4, 8, 27	nc	Unused		No-Connect.
5	PCLK	Input	Pulldown	Non-inverting differential clock input. LVPECL interface levels.
6	nPCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating. LVPECL interface levels.
7	SE_CLK	Input	Pulldown	Single-ended clock input.
9, 15, 26	GND	Power		Power suply ground.
10	CLK_SEL	Input	Pullup	Selects the reference clock. When LOW selects SE_CLK as clock source. When HIGH selects PCLK, nPCLK as clock source. LVCMOS/LVTTL interface levels.
11	FB_IN	Input	Pulldown	Non-inverting feedback input to phase detector for regenerating clocks with “zero delay”. Connect to FB_OUT.
12	nFB_IN	Input	Pullup/ Pulldown	Inverting feedback input to phase detector for regenerating clocks with “zero delay”. Connect to nFB_OUT.
13, 14	nFB_OUT, FB_OUT	Output		Differential output pair. LVDS interface levels.
17, 18	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
19, 20	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
21, 22	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
23, 24	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
28	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
29, 30, 31	F_SEL0, F_SEL1, F_SEL2	Input	Pulldown	Feedback divider control pins. LVCMOS/LVTTL interface levels.
32	PLL_BYPASS	Input	Pulldown	Selects between the PLL and reference clock as the input to the dividers. When HIGH, selects reference clock. When LOW, selects PLL. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to intenal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Feedback Divider Configuration Table

F_SEL2	F_SEL1	F_SEL0	Feedback Divider	Input/Output Frequency (MHz)	
				Minimum	Maximum
0	0	0	64	18.75	31.25
0	0	1	32	37.5	62.5
0	1	0	24	50	83.33
0	1	1	12	100	166.67
1	0	0	6	200	333.33
1	0	1	Not Used		
1	1	0			
1	1	1			

Table 3B. PLL Bandwidth Configuration Table

BW_SEL	PLL Bandwidth
0	~50kHz (default)
1	~1MHz

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characterisitcs* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.16	3.3	V_{DD}	V
I_{DD}	Power Supply Current			160		mA
I_{DDA}	Analog Supply Current			16		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		3.3V	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		3.3V	-0.3		0.8	V
I_{IH}	Input High Current	SE_CLK, BW_SEL, F_SEL[0:2], MR, PLL_BYPASS	V_{DD} = V_{IN} = 3.465V			150	µA
		CLK_SEL	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	SE_CLK, BW_SEL, F_SEL[0:2], MR, PLL_BYPASS	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. LVPECL Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK/nPCLK, FB_IN/nFB_IN	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK, FB_IN	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nPCLK, nFB_IN	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.3		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			GND + 1.5		V_{DD}	V

NOTE 1: Common mode input voltage is defined as V_{IH}.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

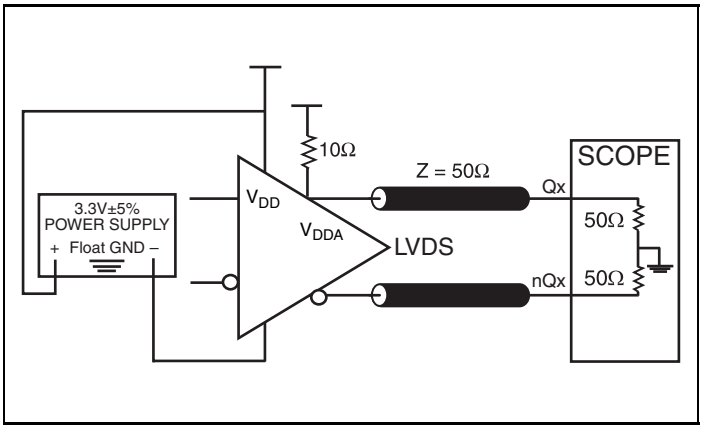
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			380		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.22		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

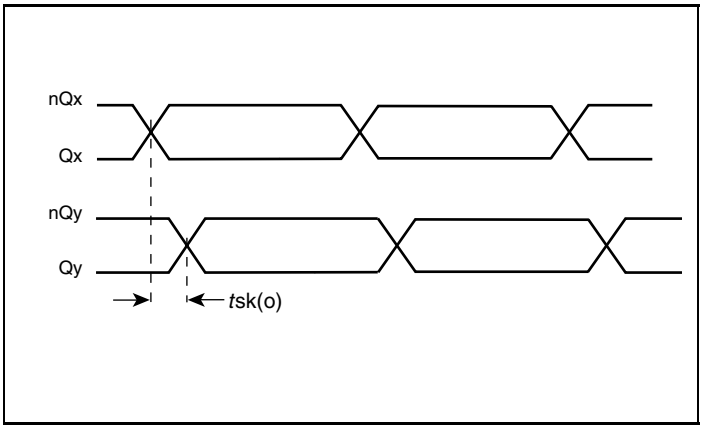
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		18.75		333.33	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			TBD		ps
*t*sk(o)	Output Skew; NOTE 2, 3			15		ps
*t*jit(per)	Period Jitter, RMS; NOTE 1			TBD		ps
t(Ø)	Static Phase Offset, NOTE 1, 4			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		245		ps
odc	Output Duty Cycle			50		%

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at V_{DDO}/2.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: Defined as the time difference between the input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable.

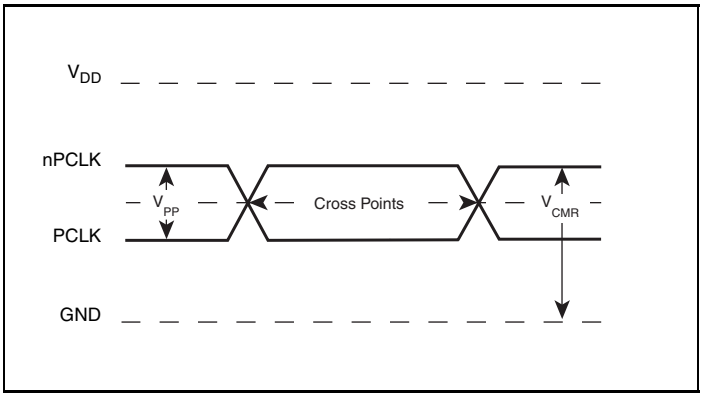
Parameter Measurement Information



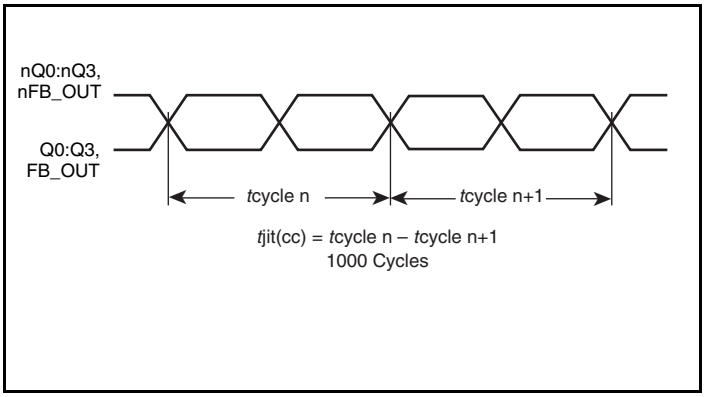
3.3V Output Load AC Test Circuit



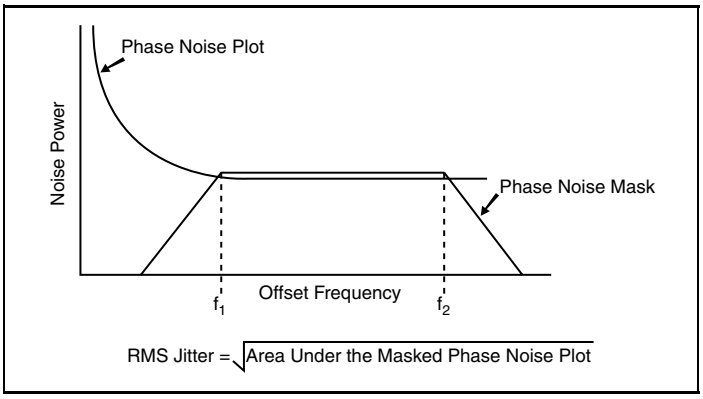
Output Skew



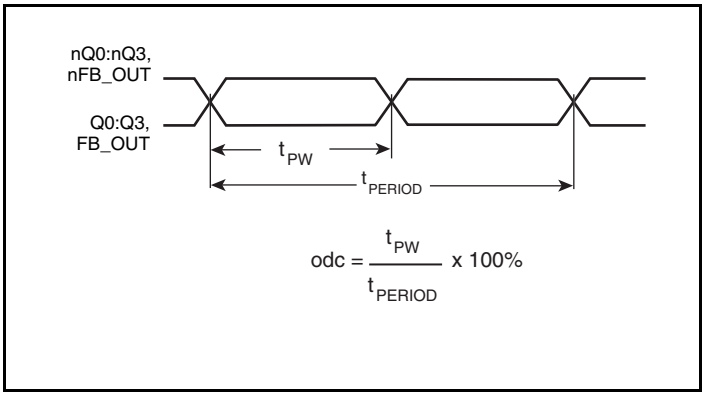
Differential Input Level



Cycle-to-Cycle Jitter

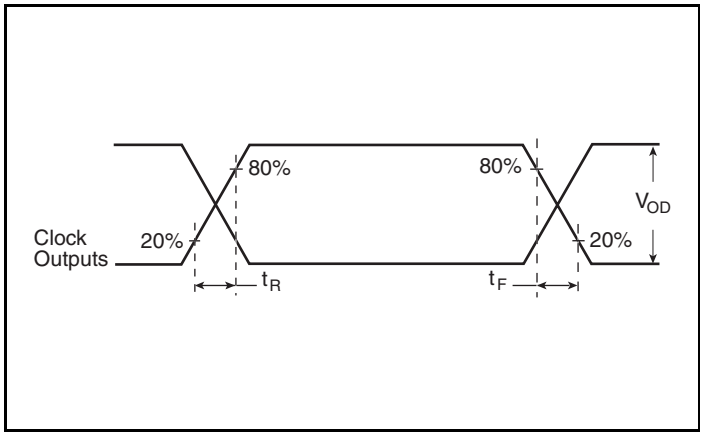


RMS Period Jitter

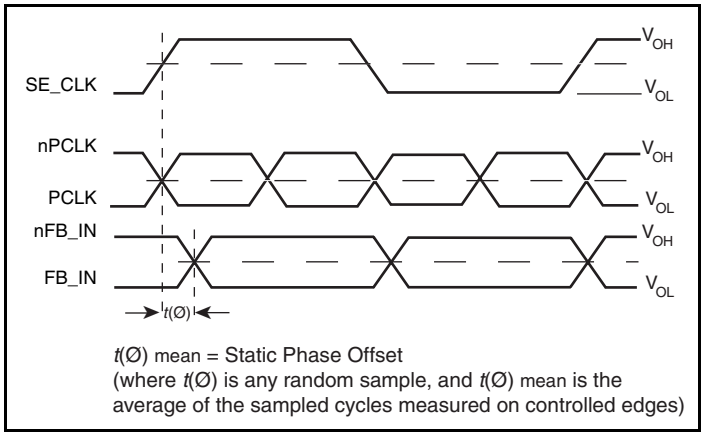


Output Duty Cycle/Pulse Width/Period

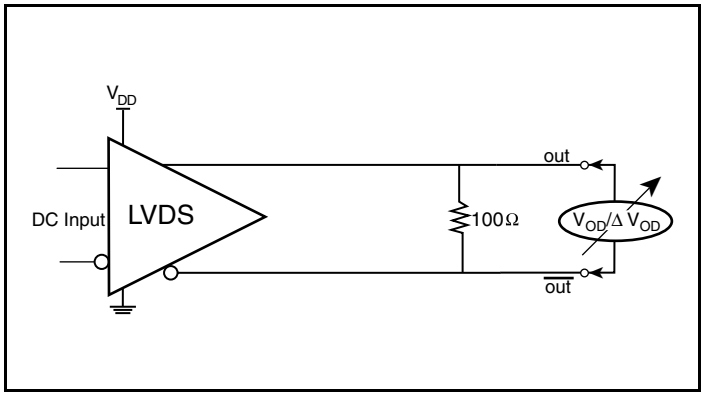
Parameter Measurement Information, continued



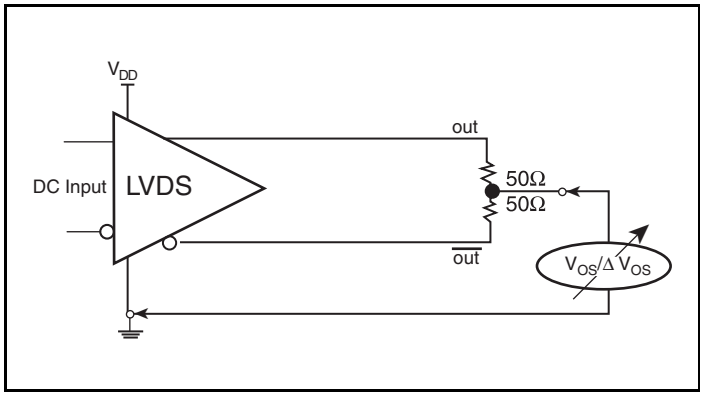
LVDS Output Rise/Fall Time



Static Phase Offset



Differential Output Voltage Setup



Offset Voltage Setup

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

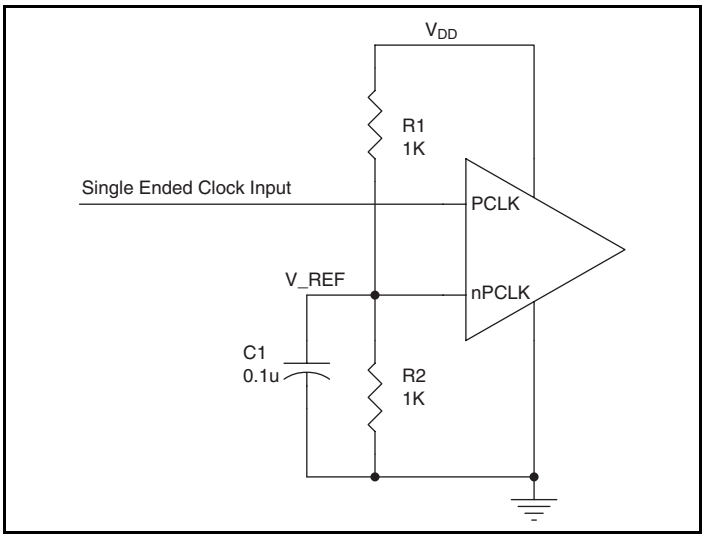


Figure 1. Single-Ended Signal Driving Differential Input

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS864S004I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10μF and a 0.01μF bypass capacitor should be connected to each V_{DDA} pin.

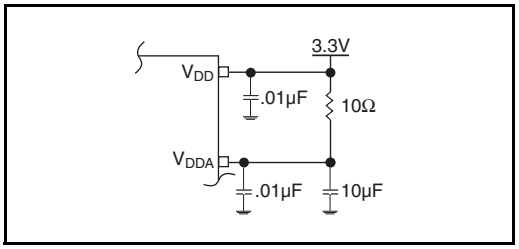


Figure 2. Power Supply Filtering

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

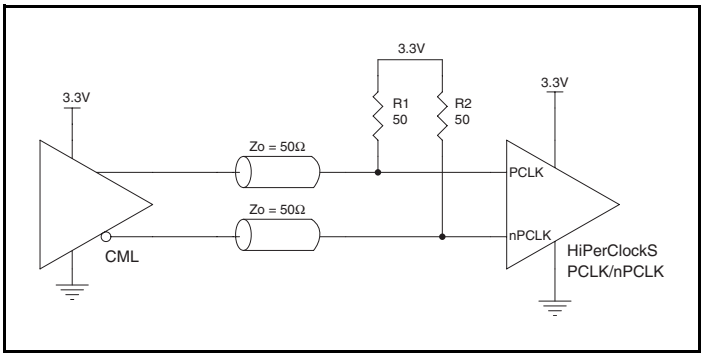


Figure 3A. HiPerClockS PCLK/nPCLK Input Driven by an Open Collector CML Driver

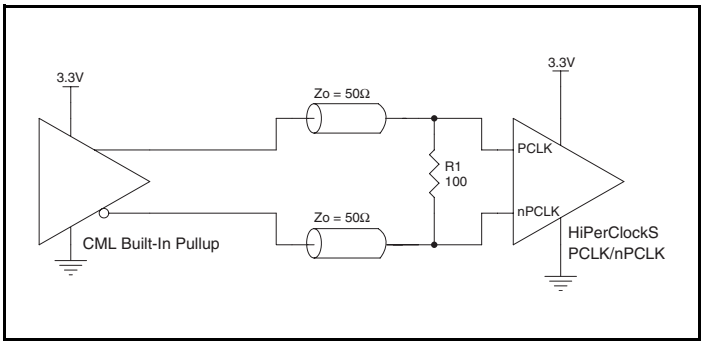


Figure 3B. HiPerClockS PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

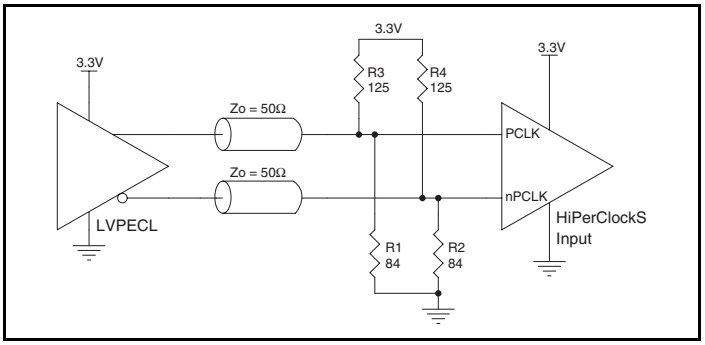


Figure 3C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

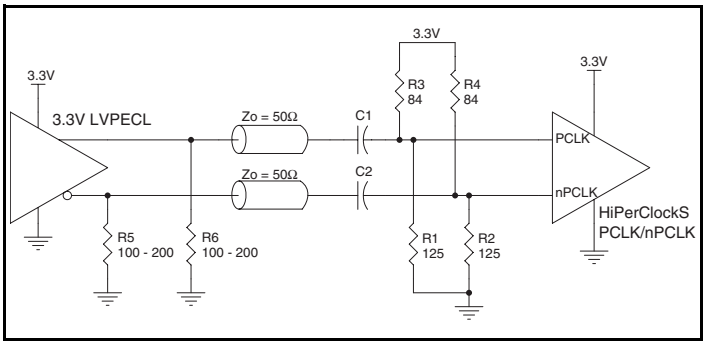


Figure 3D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

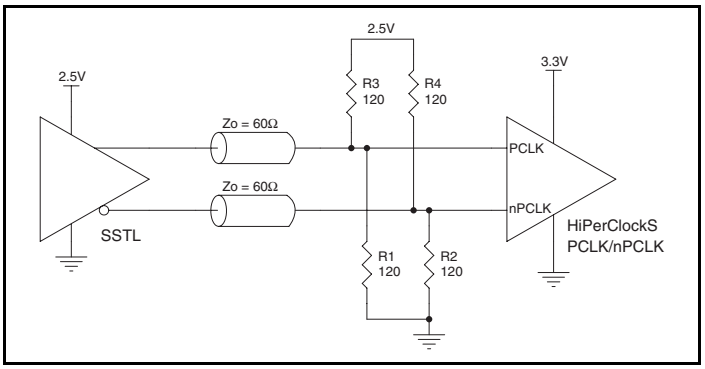


Figure 3E. HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

SE_CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the SE_CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

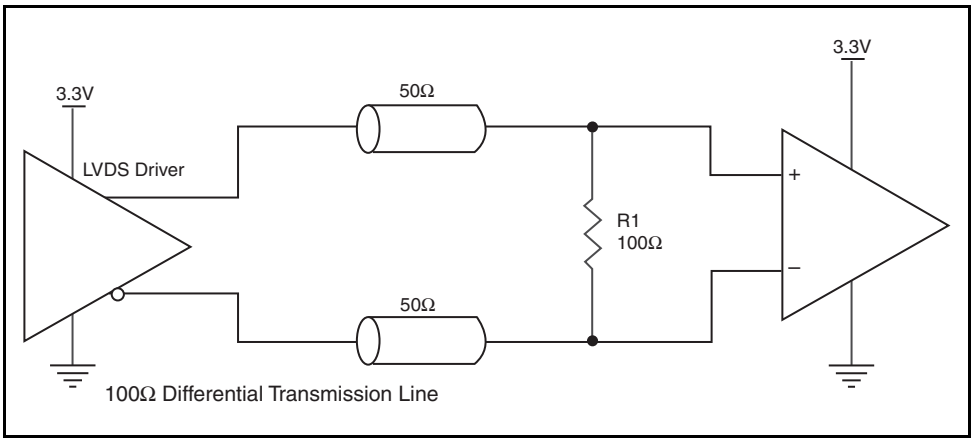


Figure 4. Typical LVDS Driver Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

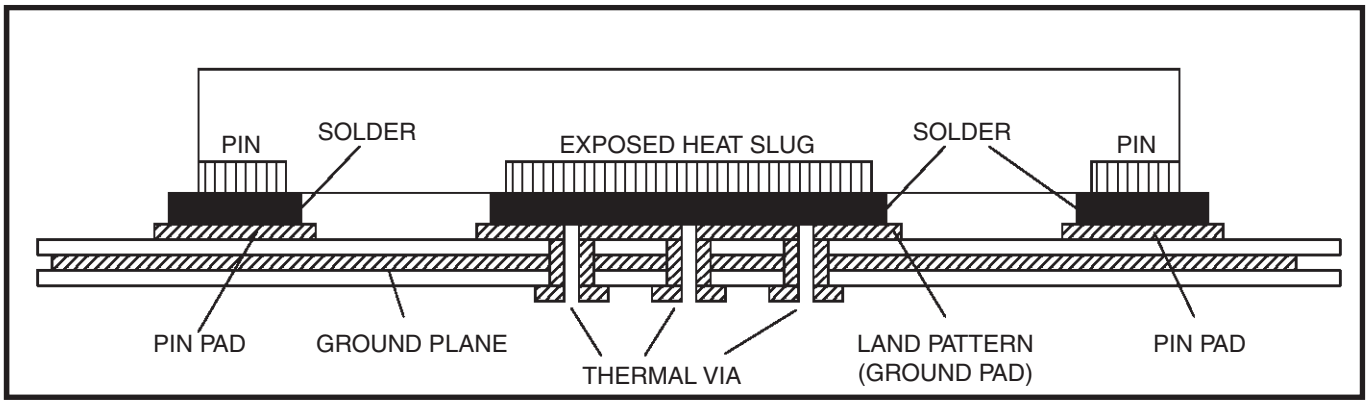


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS864S004I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS864S004I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (160mA + 16mA) = **609.84mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 42.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.610W * 42.7°C/W = 111°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

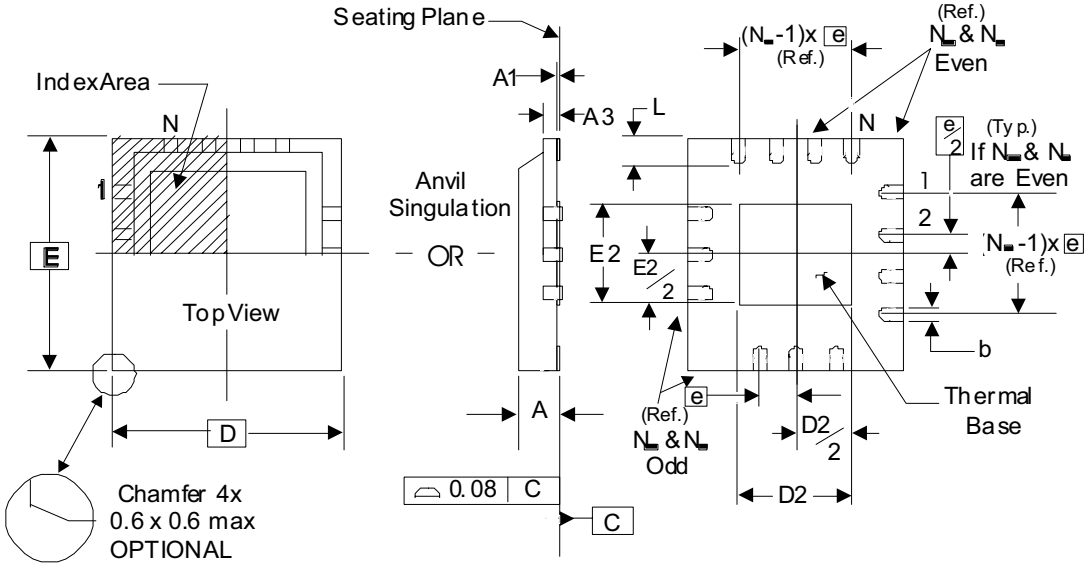
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	42.7°C/W	37.3°C/W	33.5°C/W

Transistor Count

The transistor count for ICS864S004I is: 1852

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN



The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

Table 8. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
864S004AKI	TBD	32 Lead VFQFN	Tray	-40°C to 85°C
864S004AKIT	TBD	32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
864S004AKILF	ICS4S004AIL	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
864S004AKILFT	ICS4S004AIL	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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