ITS42008-SB-D

Smart Octal High-Side NMOS-Power Switch

Data Sheet

Rev 1.01, 2014-05-19

Standard Power

RoHS

1 Overview

PG-DSO-36

Features

- Programmable Input thresholds: CMOS or V_S / 2
- Switching all types of resistive, inductive and capacitive loads
- Fast demagnetization of inductive loads
- Very low standby current
- Optimized Electromagnetic Compatibility (EMC)
- Constant current source diagnostic output for overtemperature
- Overload protection
- Undervoltage shutdown with hysteresis
- Current limitation
- Short circuit protection
- Thermal shutdown with restart
- Overvoltage protection (including load dump)
- Reverse battery protection with external resistor
- Loss of GND and loss of Vbb protection
- Electrostatic Discharge Protection (ESD)
- Green Product (RoHS compliant)

ITS42008-SB-D is not qualified and manufactured according to the requirements of Infineon Technologies with regards to automotive and/or transportation applications.

Description

The ITS42008-SB-D is a protected 200mΩ Smart Octal High-Side NMOS-Power Switch in a PG-DSO-36 power package with charge pump, CMOS or supply-rationmetric compatible input and constant current diagnostic feedback indicating overtemperature of the device.

Product Summary

Overvoltage protection V_{SAZmin}= 47V
Operating voltage range: 11V < V_S< 45V
On-state resistance R_{DSON} = typ 150mΩ
Operating Temperature range: Tj = -25°C to 125°C

Application

- All types of resistive, inductive and capacitive loads.
- Driver for electromagnetic relays
- Power switch for 12V, 24V and 42V DC applications with CMOS compatible or high voltage control interface
- Micro controller or opto coupler compatible power switch with diagnosis feedback for overtemperature
- Power managment for high-side-switching with low current consumption in OFF-mode

Type	Package	Marking
ITS42008-SB-D	PG-DSO-36	I2008D

2 Block Diagram and Terms

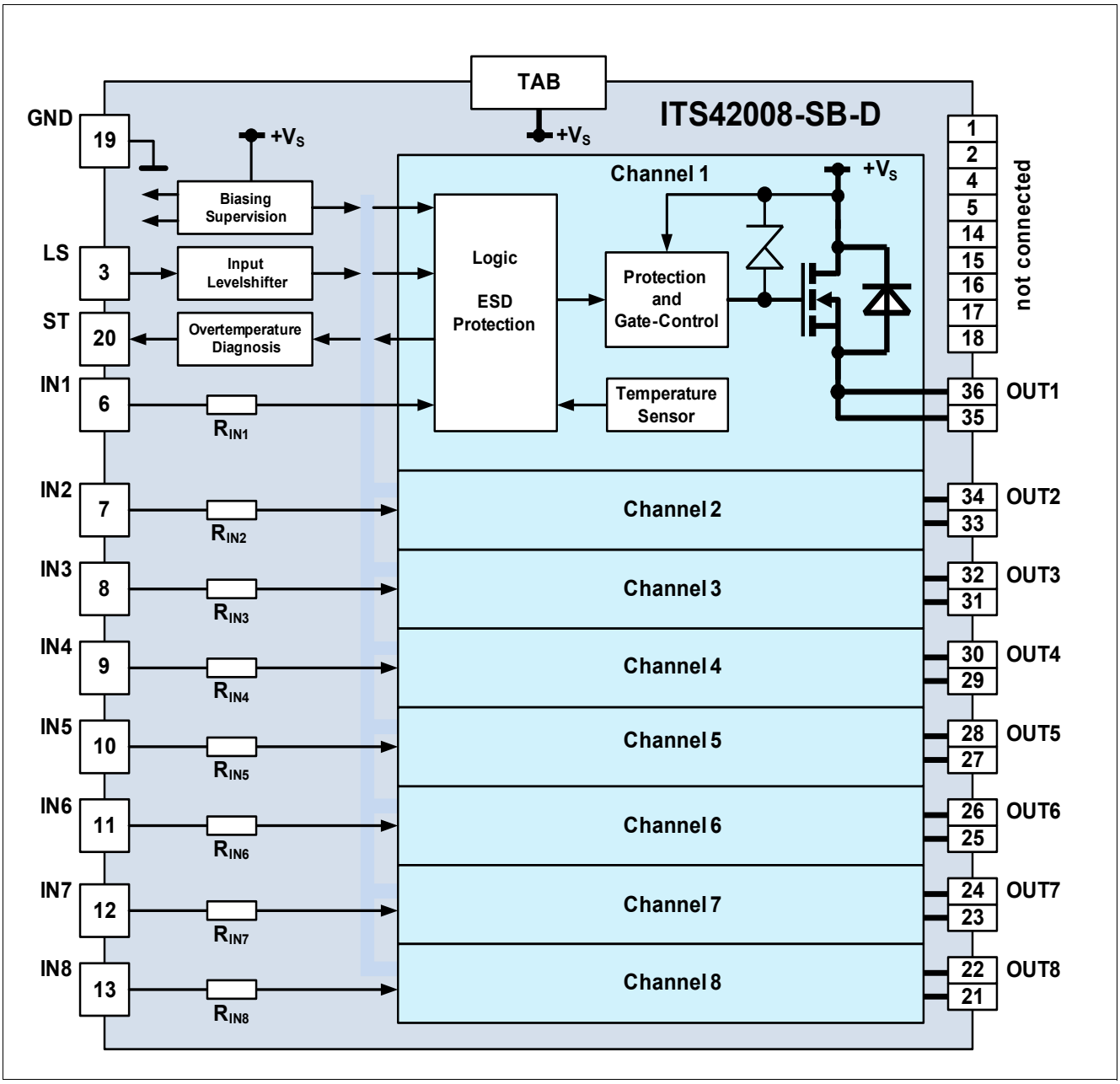
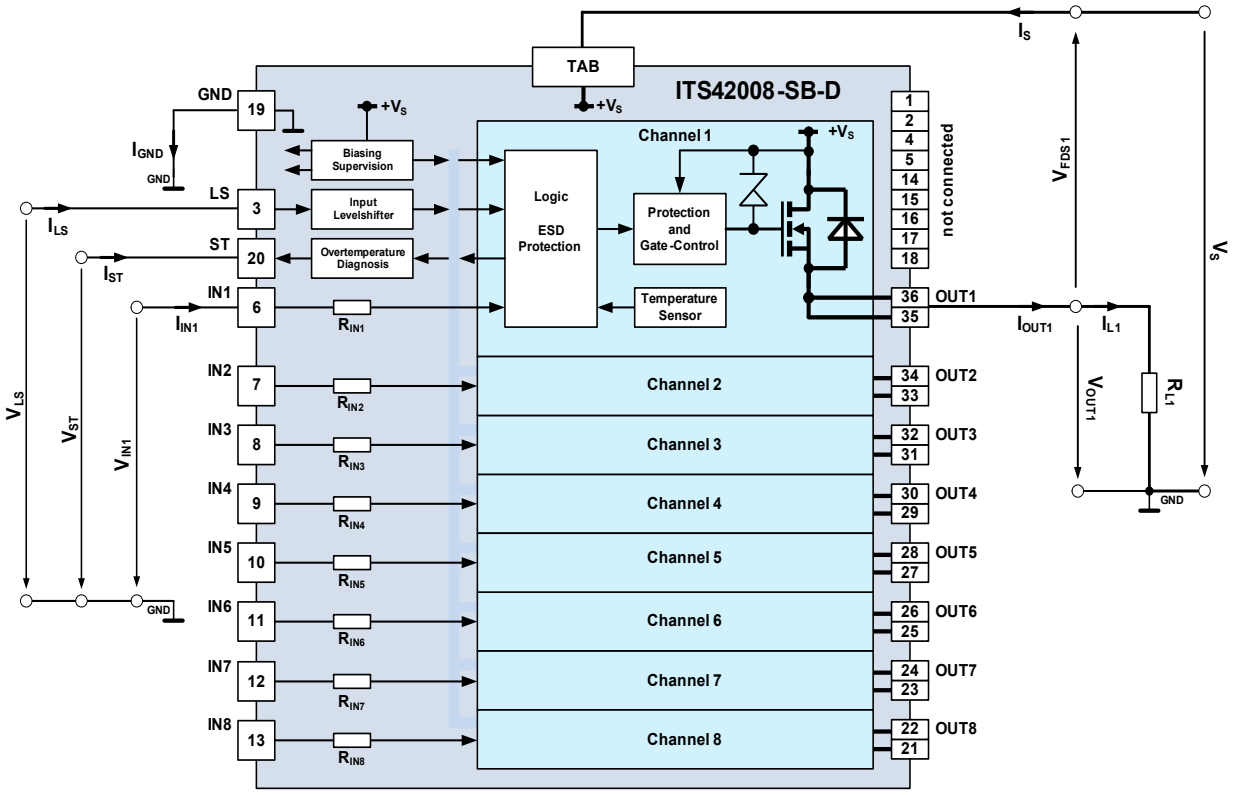


Figure 1 Block diagram

Voltage- and Current-Definitions:



Switching Times and Slew Rate Definitions:

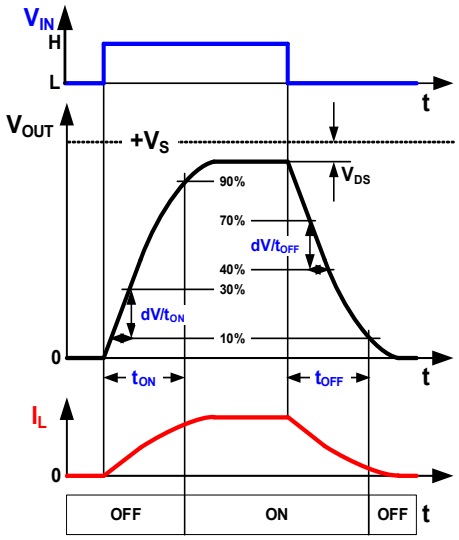


Figure 2 Terms - parameter definition

3 Pin Configuration

3.1 Pin Assignment

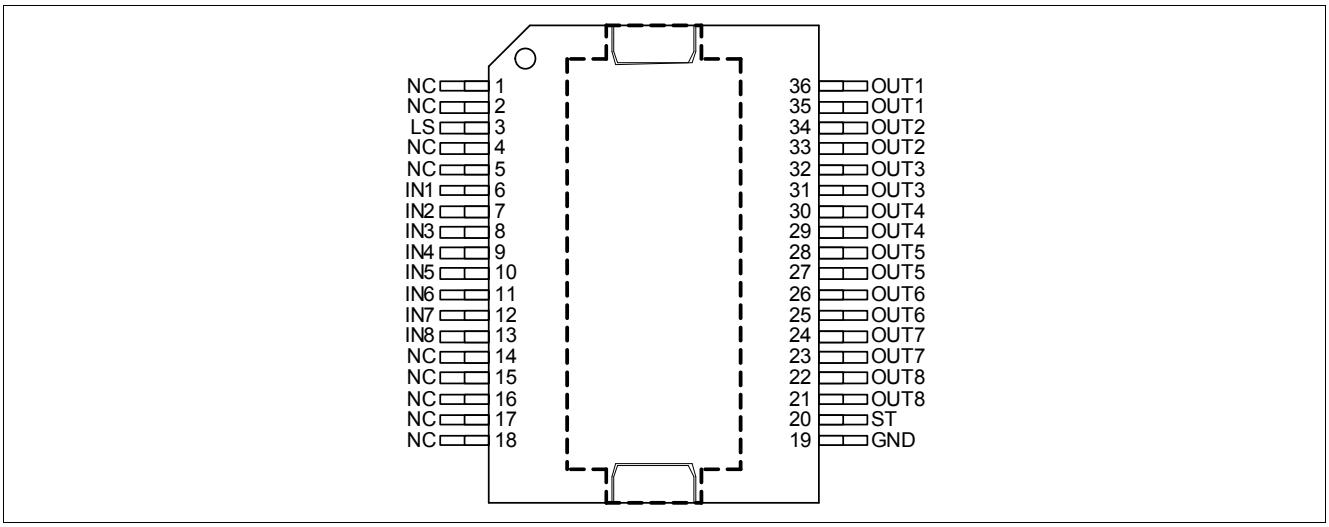


Figure 3 Pin configuration top view, PG-DSO-36

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1, 2, 4, 5	NC	not connected
3	LS	Input level progamming pin; Level: CMOS if LS=L; VS/2 if LS=H
6	IN1	Input channel 1, controles the power switch; the powerswitch is ON when IN1=H
7	IN2	Input channel 2, controles the power switch; the powerswitch is ON when IN2=H
8	IN3	Input channel 3, controles the power switch; the powerswitch is ON when IN3=H
9	IN4	Input channel 4, controles the power switch; the powerswitch is ON when IN4=H
10	IN5	Input channel 5, controles the power switch; the powerswitch is ON when IN5=H
11	IN6	Input channel 6, controles the power switch; the powerswitch is ON when IN6=H
12	IN7	Input channel 7, controles the power switch; the powerswitch is ON when IN7=H
13	IN8	Input channel 8, controles the power switch; the powerswitch is ON when IN8=H
14, 15, 16, 17, 18	NC	not connected
19	GND	Logic ground
20	ST	Status output (common diagnostic output); current source on in case of overtemperature; integrated pull down resistor to GND
21 and 22	OUT8	Output to the load of channel 8 (source of the DMOS power switch)
23 and 24	OUT7	Output to the load of channel 7 (source of the DMOS power switch)
25 and 26	OUT6	Output to the load of channel 6 (source of the DMOS power switch)
27 and 28	OUT5	Output to the load of channel 5 (source of the DMOS power switch)

Pin	Symbol	Function
29 and 30	OUT4	Output to the load of channel 4 (source of the DMOS power switch)
31 and 32	OUT3	Output to the load of channel 3 (source of the DMOS power switch)
33 and 34	OUT2	Output to the load of channel 2 (source of the DMOS power switch)
35 and 36	OUT1	Output to the load of channel 1 (source of the DMOS power switch)
TAB	VS	Supply voltage (design the wiring for the maximum short circuit current and also for low thermal resistance)

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute maximum ratings [1] at T_j = 25°C unless otherwise specified. Currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms"

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage VS							
Voltage	V_S			45	V		4.1.1
Voltage for short circuit protection	V_{SSC}			V_S	V		4.1.2
Output stage OUTx							
Output Current; (Short circuit current see electrical characteristics)	I_{OUTx}	- 2			A	self limited	4.1.3
Reverse current through GND							
Current	I_{RGND}			1.6	A	self limited	4.1.4
Input INx (channel 1 to 8)							
Voltage	V_{INx}	- 10		V_S	V		4.1.5
Current	I_{IN}	- 5		5	mA		4.1.6
Input level progamming LS							
Voltage	V_{LS}	- 1		V_S	V		4.1.7
Status ST							
Voltage	I_{LS}	- 0.3			V	self limited	4.1.8
Current	I_{LS}			1	mA	self limited	4.1.9
Temperatures							
Junction Temperature	T_j	-40		125	°C		4.1.10
Storage Temperature	T_{stg}	-55		125	°C		4.1.11
Power dissipation							
Ta = 25 °C[2]	P_{tot}			3.3	W		4.1.12
Inductive load switch-off energy dissipation							
Tj = 125 °C; IL= 625mA[1]; all channels active	E_{AS}			1	J	single pulse	4.1.13
Tj = 125 °C; IL= 625mA[1]; one channel active	E_{AS}			10	J	single pulse	4.1.14
ESD Susceptibility							
ESD susceptibility (pins INx; LS and ST)	V_{ESD}	-1		1	kV	HBM[3]	4.1.15
ESD susceptibility (all other pins)	V_{ESD}	-5		5	kV	HBM[3]	4.1.16

1) Not subject to production test, specified by design

2) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm2 (one layer, 70mm thick) copper area for Vbb connection. PCB is vertical without blown air

3) ESD susceptibility HBM according to EIA/JESD 22-A 114.

Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" the normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal Operating Voltage	V_S	11		45	V	V_S increasing	4.2.1

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistance - Junction to tab	$R_{thj\text{-}tab}$		2.8		K/W		4.3.1
Thermal Resistance - Junction to Ambient - 1s0p, minimal footprint	R_{thJA_1s0p}		44.1		K/W	2)	4.3.2
Thermal Resistance - Junction to Ambient - 1s0p, 300mm^2	$R_{thJA\_1s0p\_300mm}$		26.5		K/W	3)	4.3.3
Thermal Resistance - Junction to Ambient - 1s0p, 600mm^2	$R_{thJA\_1s0p\_600mm}$		23.8		K/W	4)	4.3.4
Thermal Resistance - Junction to Ambient - 2s2p	R_{thJA_2s2p}		19.9		K/W	5)	4.3.5
Thermal Resistance - Junction to Ambient with thermal vias - 2s2p	R_{thJA_2s2ptv}		18.8		K/W	6)	4.3.6

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, footprint; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

3) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, Cu, 300mm^2; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

4) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, 600mm^2; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

5) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

6) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board with two thermal vias; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu. The diameter of the two vias are equal 0.3mm and have a plating of 25um with a copper heatsink area of 3mm x 2mm). JEDEC51-7: The two plated-through hole vias should have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter.

5 Electrical Characteristics

Table 4 **V_S = 15V to 30V; Tj = -25°C to 125°C; V_{LS}= 0V; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms". Typical values at V_s = 13.5V, T_j = 25°C; index "x" means "number of channel 1 to 8".**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Powerstages							
NMOS ON Resistance	R_{DSONx}		150	200	mΩ	I_{OUTx}= 0.5A; T_j = 25°C; V_{LS}=V_{INx}= V_S=15V	5.0.1
NMOS ON Resistance	R_{DSONx}		270	320	mΩ	I_{OUTx}= 0.5A; T_j = 125°C; V_{LS}=V_{INx}= V_S=15V	5.0.2
Timings of Power Stages[1)]							
Turn ON Time(to 90% of V_{outx}); L to H transition of V_{INx}	t_{ONx}		50	100	µs	V_S=15V; R_{Lx} = 47Ω	5.0.3
Turn OFF Time (to 10% of V_{outx}); H to L transition of V_{INx}	t_{OFFx}		75	150	µs	V_S=15V; R_{Lx} = 47Ω	5.0.4
ON-Slew Rate (10 to 30% of V_{outx}); L to H transition of V_{INx}	SR_{ONx}		1.0	2.0	V / µs	V_S=15V; R_{Lx} = 47Ω	5.0.5
OFF-Slew Rate (70 to 40% of V_{outx}); H to L transition of V_{INx}	SR_{OFFx}		1.0	2.0	V / µs	V_S=15V; R_{Lx} = 47Ω	5.0.6
Under voltage lockout (charge pump start-stop-restart)							
Supply undervoltage; charge pump stop voltage	V_{SUV}	7.0		10.5	V	V_S decreasing	5.0.7
Supply startup voltage; Charge pump restart voltage	V_{SSU}			11.0	V	V_S increasing	5.0.8
Supply undervoltage hysteresis	V_{SUHY}		0.5		V	V_{SUHY} = V_{SSU} - V_{SUV}	5.0.9
Current consumption							
Operating current	I_{GND}		5	12	mA	V_{INx}= V_{LS}= V_S=30V	5.0.10
Standby current	I_{SSTB}		50	150	µA	V_{INx}= 6.5V; V_{LS}= V_S=15V; V_{OUTx}= 0V	5.0.11
Output leakage current	I_{OUTLKx}		5	10	µA	V_{INx}= 6.5V; V_{LS}=V_S=15V V_{OUTx}= 0V	5.0.12
Protection functions [2)]							
Initial peak short circuit current limit	I_{LSCPx}			1.9	A	T_j = -25°C V_{LS}=V_S =V_{INx}= 30V; t_{mx} = 700µs	5.0.13

Table 4 **V_S = 15V to 30V; Tj = -25°C to 125°C; V_{LS}= 0V; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms". Typical values at V_s = 13.5V, T_j = 25°C; index "x" means "number of channel 1 to 8".**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Initial peak short circuit current limit	I_{LSCPx}		1.4		A	T_j = 25°C V_{LS}=V_S =V_{INx}= 30V; t_{mx} = 700µs	5.0.14
Initial peak short circuit current limit	I_{LSCPx}	0.7			A	T_j = 125°C V_{LS}=V_S =V_{INx}= 30V; t_{mx} = 700µs	5.0.15
Repetitive short circuit current limitT_j = T_{jTrip} ; see timing diagrams	I_{LSCRx}		1.1		A	V_{INx} = 5.0V;	5.0.16
Output clamp at V_{OUTx} = V_S - V_{DSCLx} (inductive load switch off)	V_{DSCLx}	47	53	60	V	I_{OUTx} = 4mA; V_{LS}=30V	5.0.17
Overvoltage protection	V_{SAZ}	47			V	I_S = 4mA V_{LS}=30V	5.0.18
Thermal overload trip temperature	T_{jTrip}	135			°C		5.0.19
Thermal hysteresis	T_{HYS}		10		K		5.0.20
Reverse Battery[3)]							
Continuous reverse battery voltage	V_{SREV}			45	V		5.0.21
Forward voltage of the drain-source reverse diode	V_{FDSx}			1.2	V	I_{FDS} = 1.25A; V_{IN}= 0V	5.0.22
Input interface; pin INx							
Input turn-ON threshold voltage	V_{INONx}	2.2			V	LS = L; CMOS mode	5.0.23
Input turn-OFF threshold voltage	V_{INOFFx}			0.8	V	LS = L; CMOS mode	5.0.24
Input turn-ON threshold voltage	V_{INONx}	V_{ST} / 2 + 1			V	LS = H or open; ratiometric mode	5.0.25
Input turn-OFF threshold voltage	V_{INOFFx}			V_{ST} / 2 - 1	V	LS = H or open; ratiometric mode	5.0.26
Input threshold hysteresis	V_{INHYSx}		0.3		V		5.0.27
Off state input current	I_{INOFFx}	8			µA	LS = L; CMOS mode V_{INx} = 0.8V	5.0.28
On state input current	I_{INONx}			70	µA	LS = L; CMOS mode V_{INx} = 2.2V	5.0.29
Off state input current	I_{INOFFx}	80			µA	LS = H or open; ratiometric mode V_{INx} = V_{ST} / 2 - 1	5.0.30
On state input current	I_{INONx}			260	µA	LS = H or open; ratiometric mode V_{INx} = V_{ST} / 2 + 1	5.0.31
Input switch ON delay time	t_{dON}	150	340		µs		5.0.32

Table 4 **V_S = 15V to 30V; Tj = -25°C to 125°C; V_{LS}= 0V; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms". Typical values at V_s = 13.5V, T_j = 25°C; index "x" means "number of channel 1 to 8".**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input resistance	R_{INx}	2	3	5	kΩ		5.0.33
Input interface; pin LS							
Pull down resistance	R_{LS}	300	800		kΩ	V_{LS}=V_S =15V	5.0.34
Status output (current source); pin ST							
Status output current	I_{ST}	2	3	4	mA	V_{ST} = 5V V_{LS}=V_S =30V	5.0.35
Status leakage current	I_{STLK}	- 2			µA	V_{ST} = 0V; T_j < 135°C; V_{LS}=V_S =30V	5.0.36

1) Timing values only with high slewrate input signal; otherwise slower.

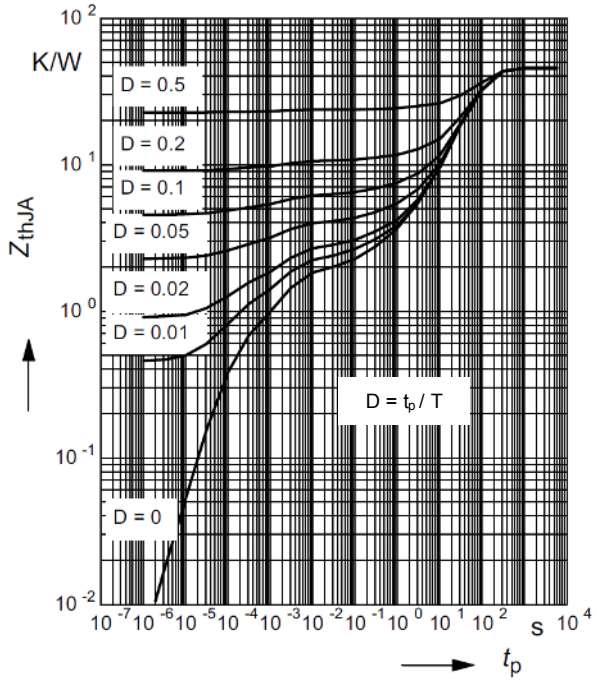
2) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

3) Requires a 150W resistor in GND connection. The reverse load current trough the intrinsic drain-source diode of the power-M

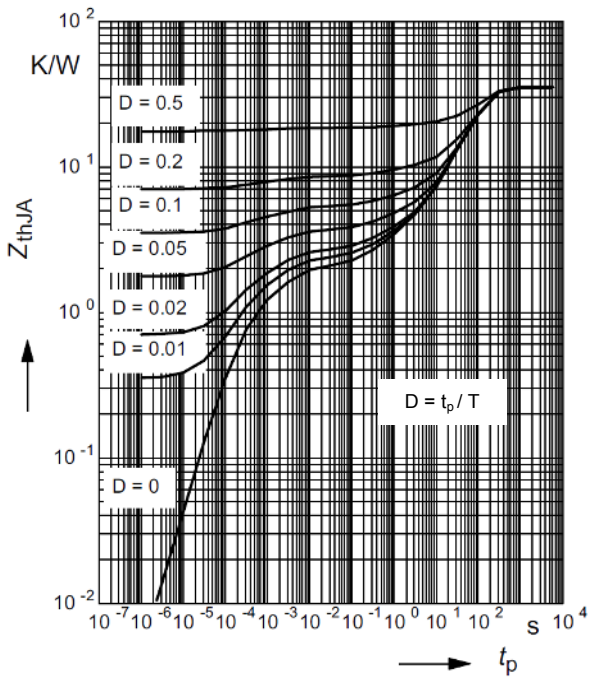
6 Typical Performance Graphs

Typical Characterisitics

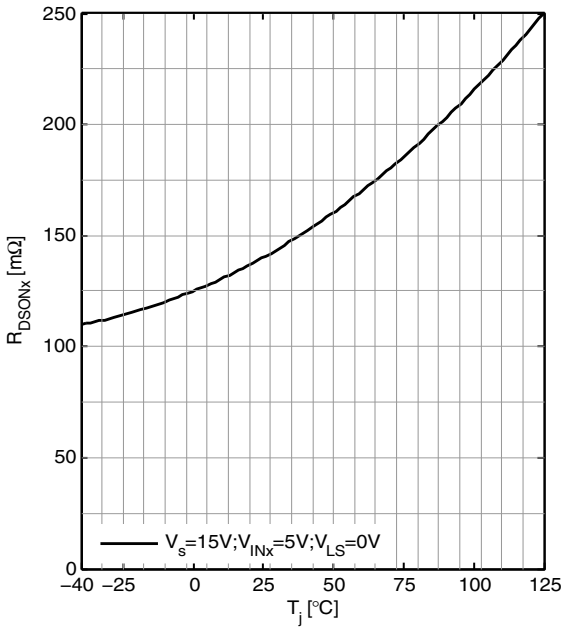
Transient Thermal Impedance Z_{thJA} versus Pulse Time t_p @ 6cm² heatsink area



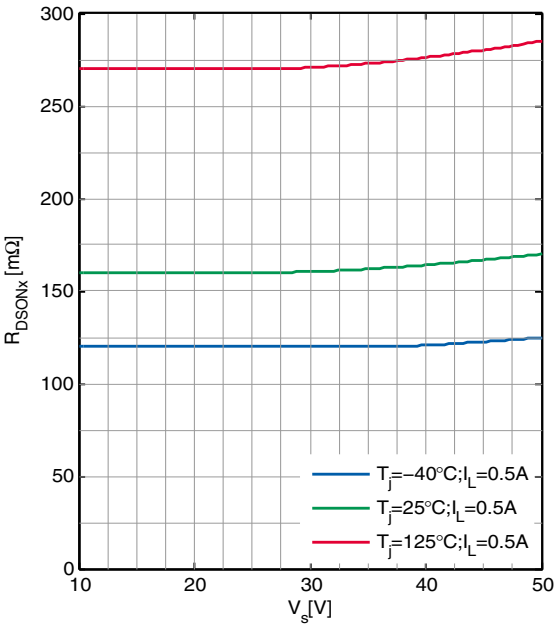
Transient Thermal Impedance Z_{thJA} versus Pulse Time t_p @ min footprint



On-Resistance R_{DSONx} versus Junction Temperature T_j

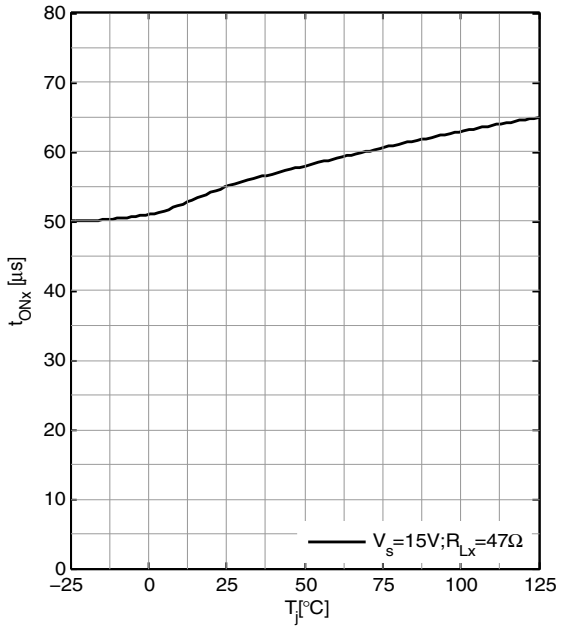


On-Resistance R_{DSONx} versus Supply Voltage V_S

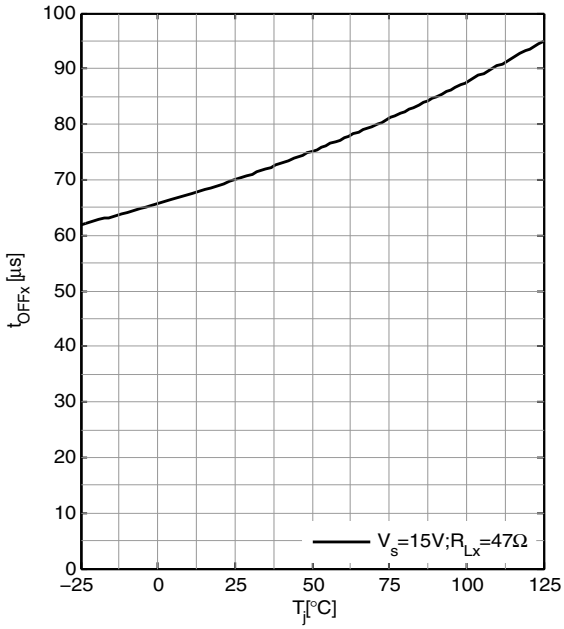


Typical Characterisitics

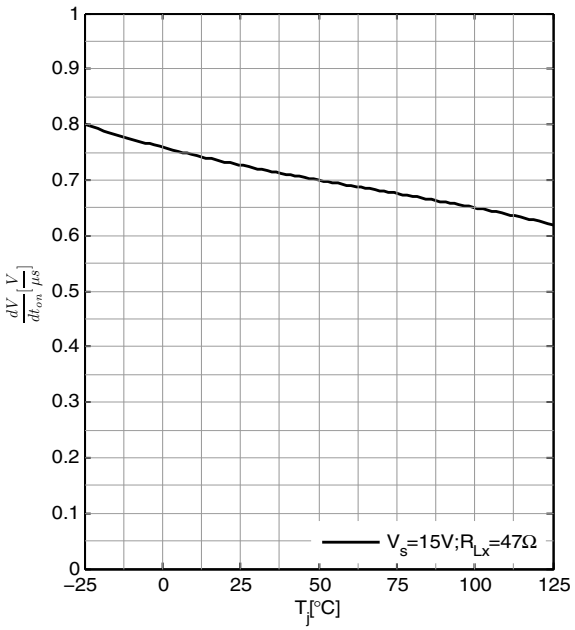
Switch ON Time t_{ONx} versus Junction Temperature T_j



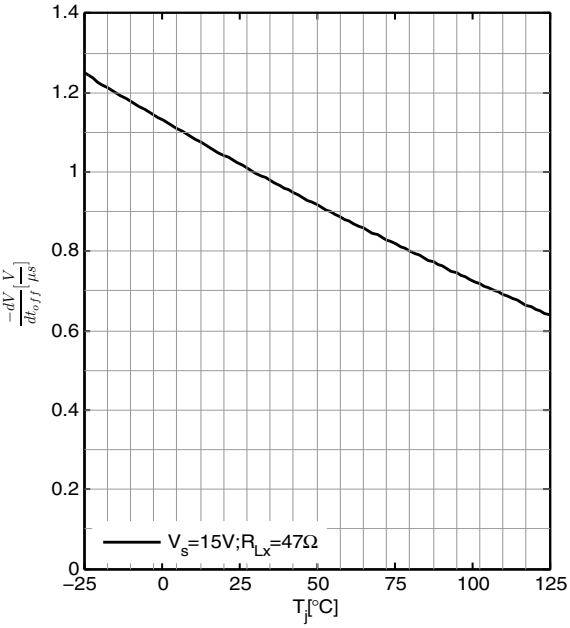
Switch OFF Time t_{OFFx} versus Junction Temperature T_j



ON Slewrate SR_{ONx} versus Junction Temperature T_j

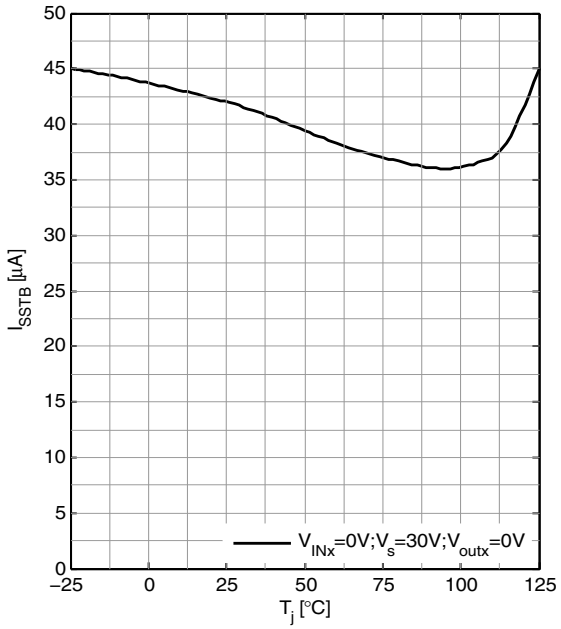


OFF Slewrate SR_{OFFx} versus Junction Temperature T_j

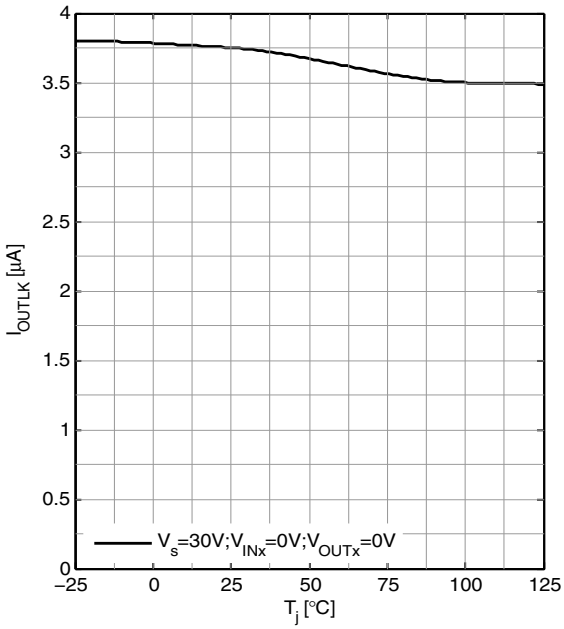


Typical Characterisitics

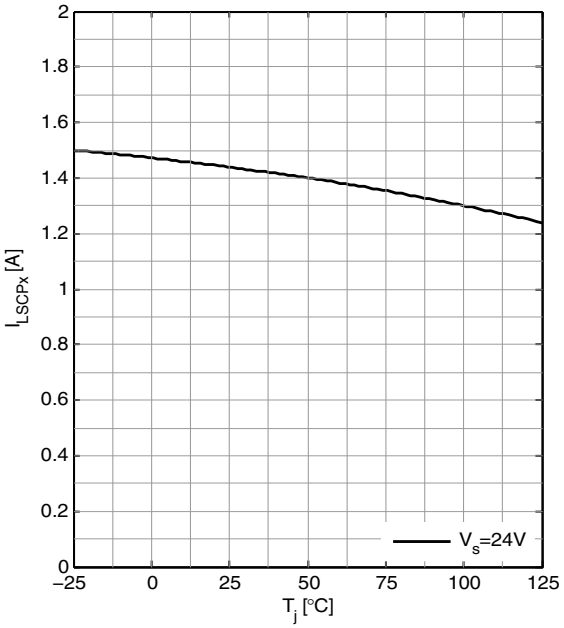
Standby Current I_{SSTB} versus Junction Temperature T_j



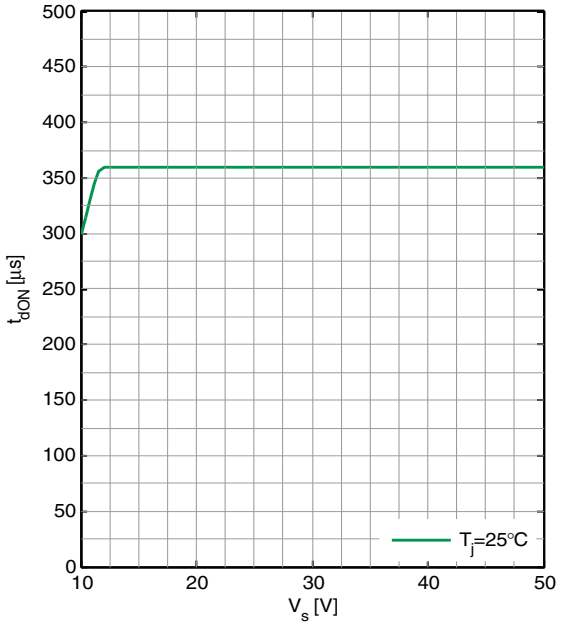
Output Leakage current I_{OUTLKx} versus Junction Temperature T_j



Initial Peak Short Circuit Current Limt I_{LSCPx} versus Junction Temperature T_j

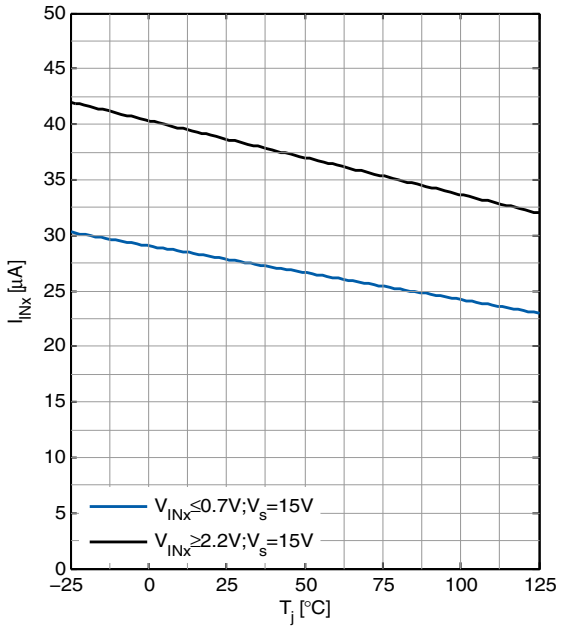


Initial Short Circuit Shutdown time t_{dON} versus Junction Temperature T_j

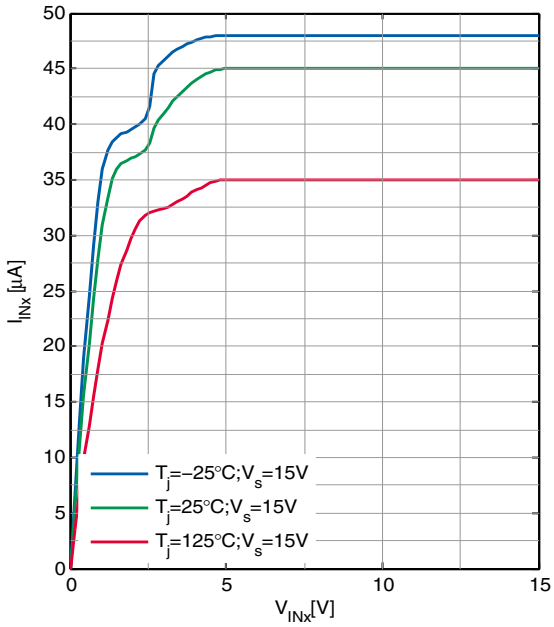


Typical Characterisitics

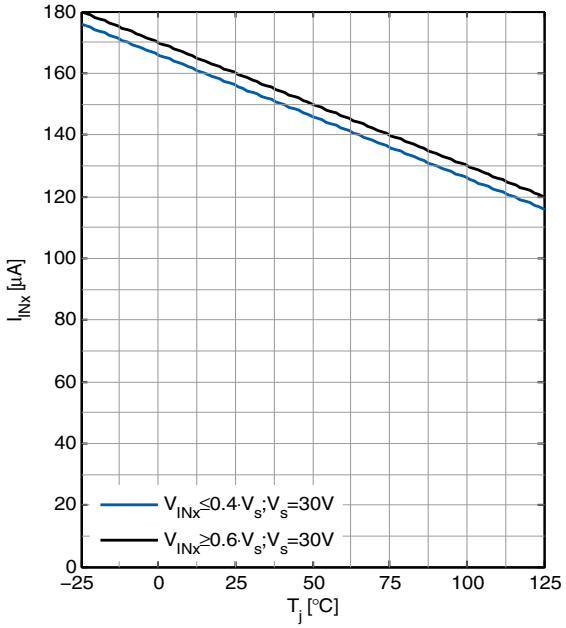
Input Current Consumption I_{INx} versus Junction Temperature T_j



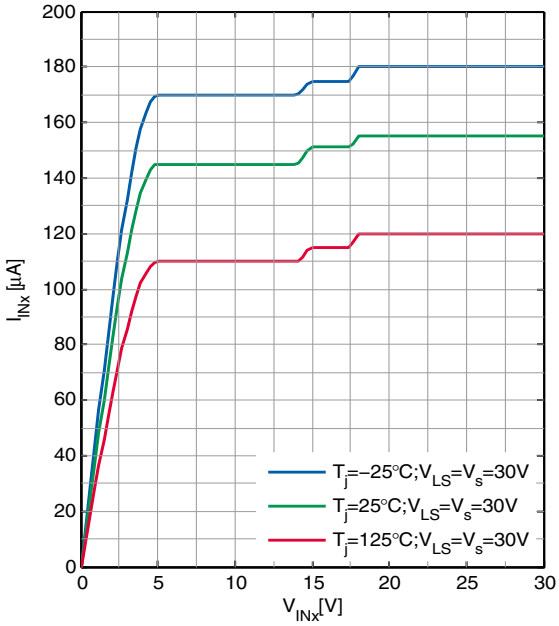
Input Current Consumption I_{INx} versus Input voltage V_{IN}



Input Current Consumption I_{INx} versus Junction Temperature T_j

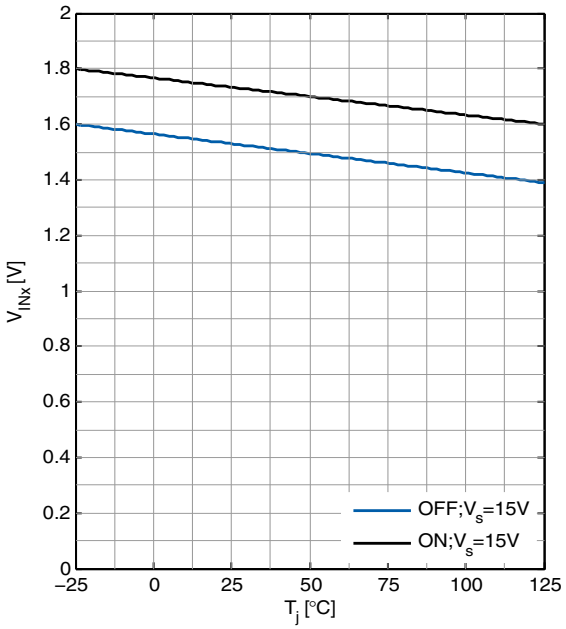


Input Current Consumption I_{INx} versus Input voltage V_{IN}

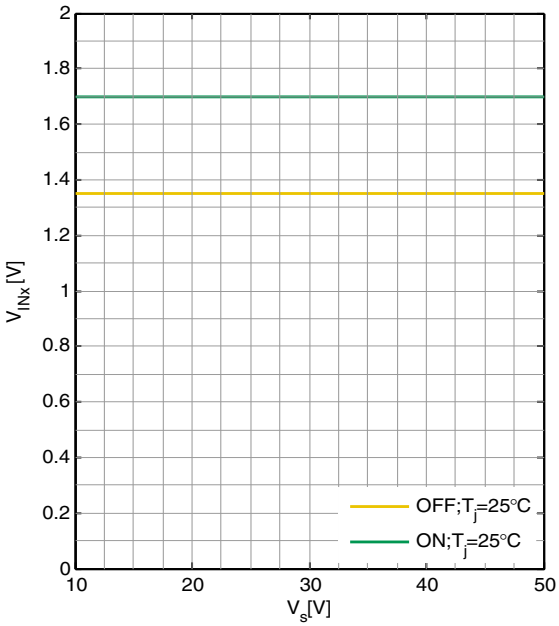


Typical Characterisitics

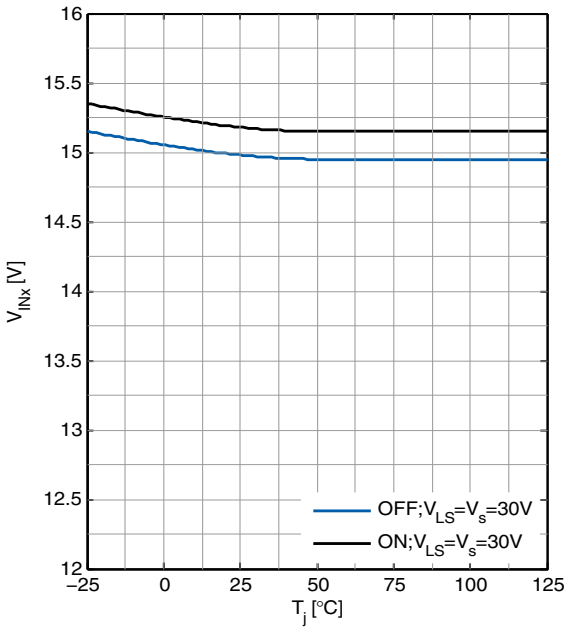
Input Threshold voltage $V_{INH,Lx}$ versus Junction Temperature T_j



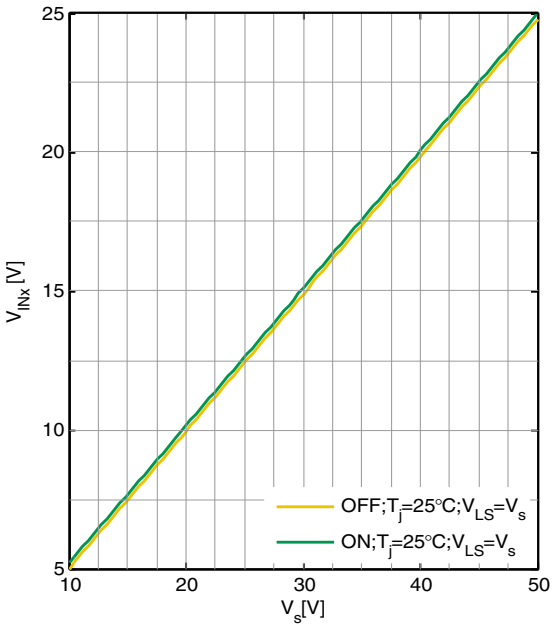
Input Threshold voltage $V_{INH,Lx}$ versusSupply Voltage V_S



Input Threshold voltage $V_{INH,Lx}$ versus Junction Temperature T_j

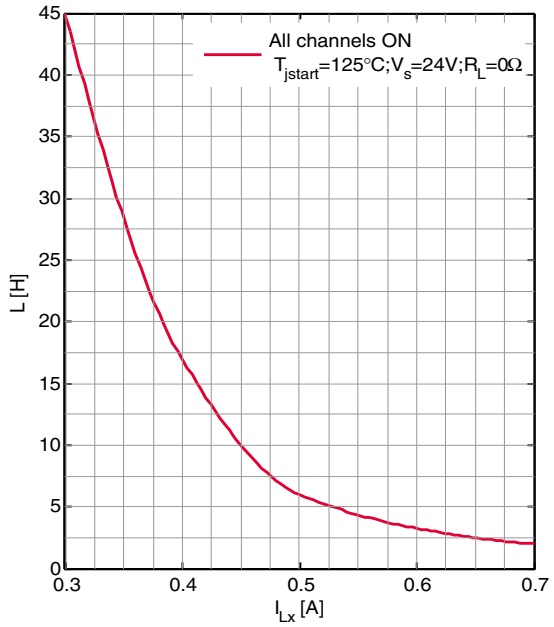


Input Threshold voltage $V_{INH,Lx}$ versusSupply Voltage V_S

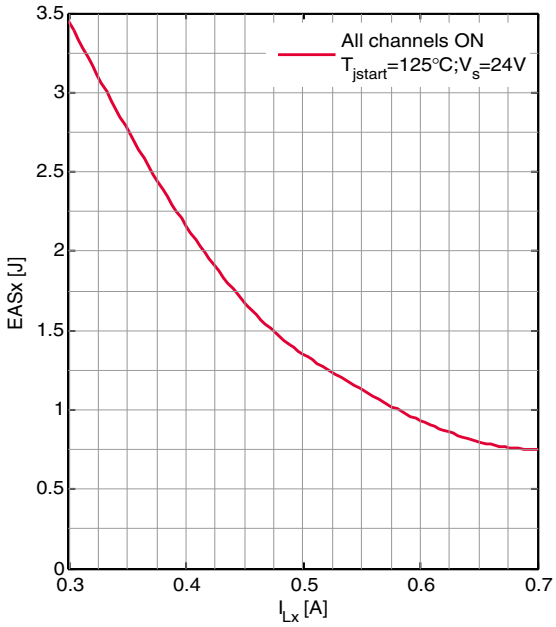


Typical Characterisitics

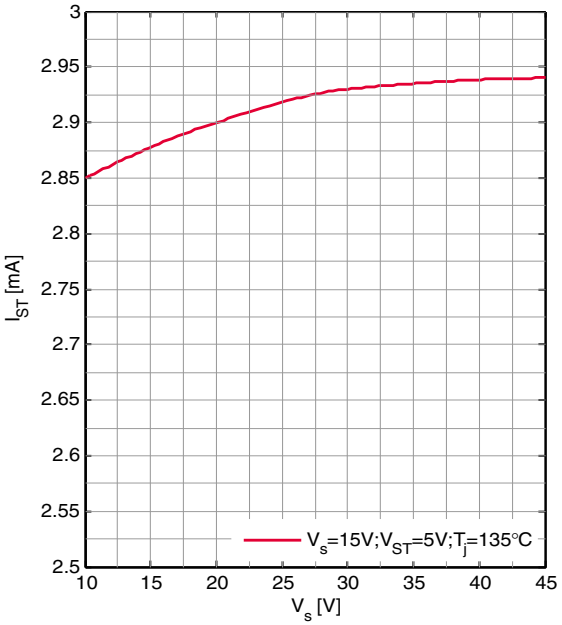
Max. allowable Load Inductance L versus Load current I_{Lx}



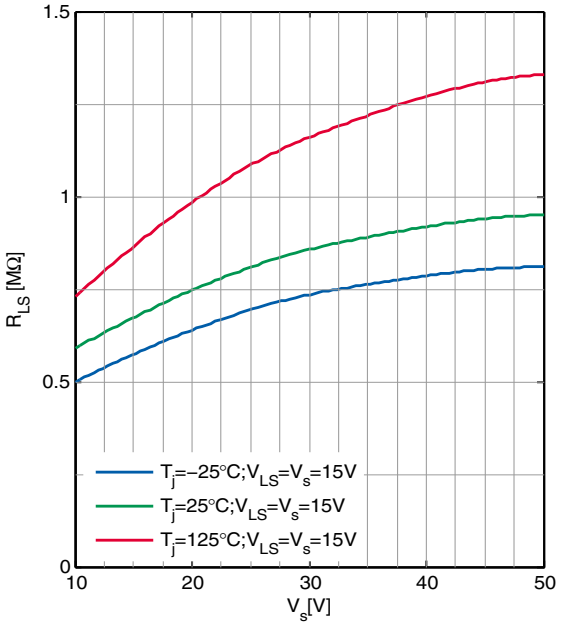
Max. allowable Inductive single pulse Switch-off Energy E_{AS} versus Load current I_{Lx}



Status Output Current I_{ST} versus Supply Voltage V_S



Internal pull down Resistor R_{LS} at pin LS versus Supply Voltage V_S



7 Application Information

7.1 Application Diagram

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty for a certain functionality, condition or quality of the device.

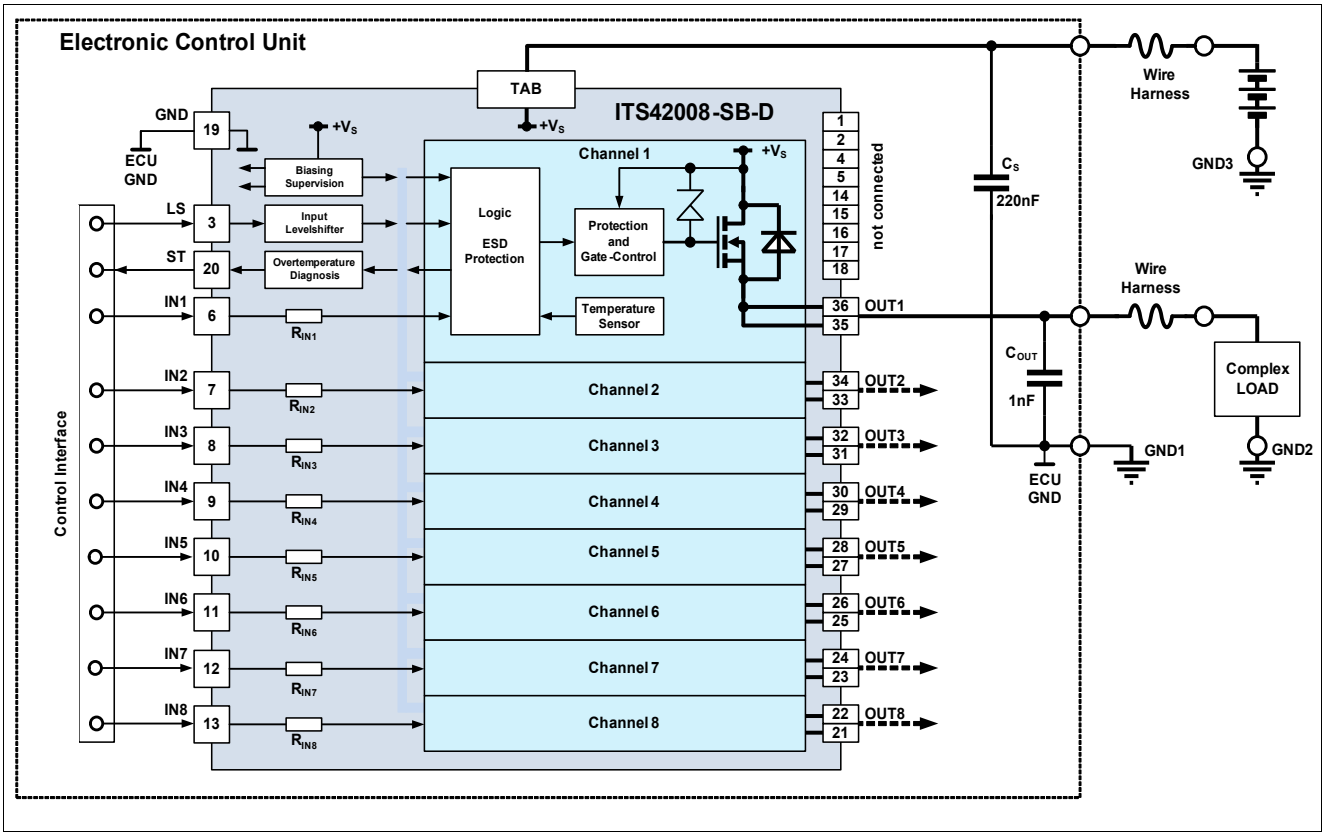


Figure 4 Application Diagram

The ITS42008-SB-D can be connected directly to the battery of a supply network. It is recommended to place a ceramic capacitor (e.g. C_S = 220nF) between supply and GND of the ECU to avoid line disturbances. Wire harness inductors/resistors are sketched in the application circuit above.

The complex load (resistive, capacitive or inductive) must be connected to the output pin OUT.

A built-in current limit protects the device against destruction.

The ITS42008-SB-D can be switched on and off with ground related standard logic signal at pin INx if the level programming pin LS is set to L.

If LS is connected to the supply voltage V_S the input threshold is set to ~ 50% of V_S.

To achieve a higher robustness it is recommended to connect the LS pin to GND or Supply voltage.

If the pin LS is left open the thresholds are automatically set to CMOS level caused by an internal high ohmic pull down resistor to GND.

In standby mode (all inputs INx=L) the ITS42008-SB-D is deactivated with very low current consumption.

The output voltage slope is controlled during on and off transistion to minimize emissions. Only a small ceramic capacitor COUT=1nF is recommended to attenuate RF noise.

In the following chapters the main features, some typical waverforms and the protection behaviour of the ITS42008-SB-D is shown. For further details please refer to application notes on the Infineon homepage.

7.2 Diagnosis Description

For diagnostic purpose the device provides a digital output pin ST in order to indicate fault conditions.

The status output (ST) of the ITS42008-SB-D is a high voltage current source.

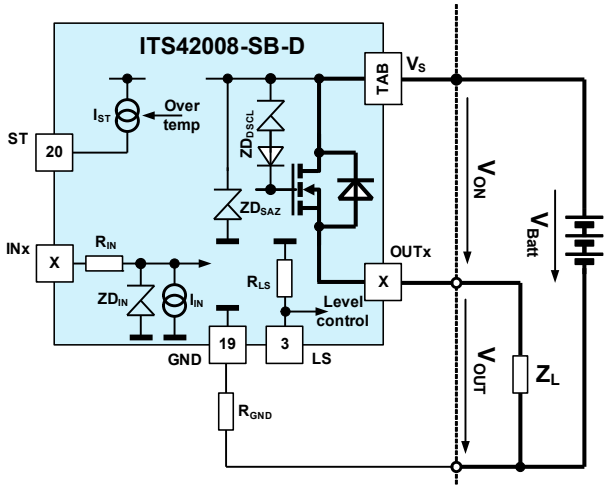
In “normal” operation mode (no overtemperature) the current source is switched OFF. An internal pull down resistor pulls pin ST down to GND. In case of overtemperature the current source is activated. To limit the voltage at pin ST an external zenerdiode to GND must be added.
The following truth table defines the status output.

Table 5 Truth Table of diagnosis feature

Device Operation	INx	OUTx	current source at ST	Comment
Normal Operation	L	L	OFF	
Normal Operation	H	H	OFF	
Short circuit to GND	L	L	OFF	
Short circuit to GND	H	L	OFF	
Undervoltage at V_S	L	L	OFF	
Undervoltage at V_S	H	L	OFF	
Overtemperature	L	L	OFF	
Overtemperature	H	L	ON	toggeling with restart

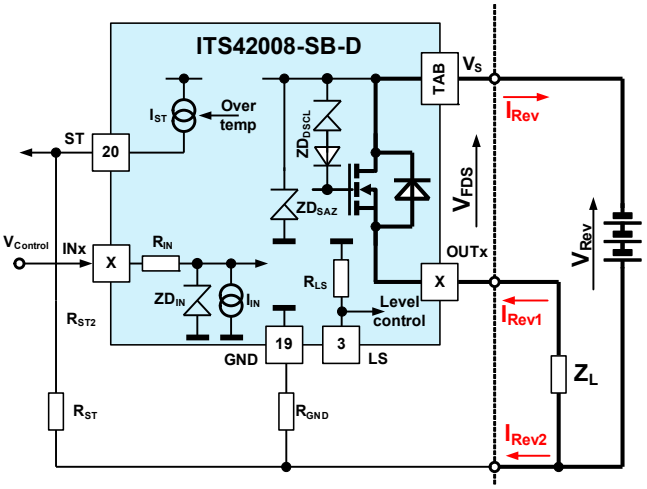
7.3 Special Feature Description

Supply over voltage:



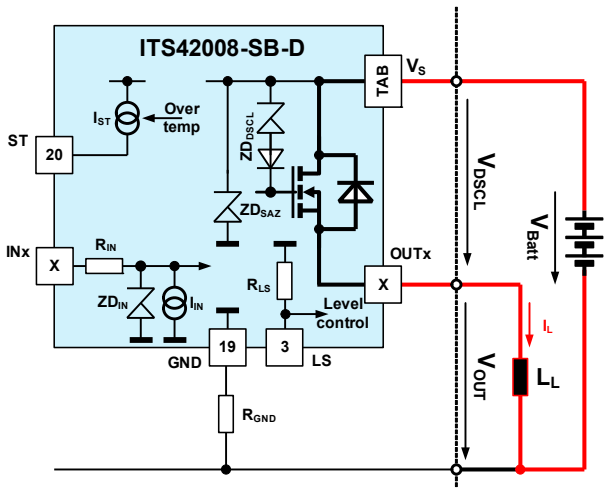
If over-voltage is applied to the V_S-Pin:
Voltage is limited to V_{ZDSAZ}; current can be calculated:
$I_{ZDSAZ} = (V_S - V_{ZDSAZ}) / R_{GND}$
A typical value for RGND is 150Ω.
In case of ESD pulse on the input pin there is in both polarities a peak current $I_{INpeak} \sim V_{ESD} / R_{IN}$

Supply reverse voltage:



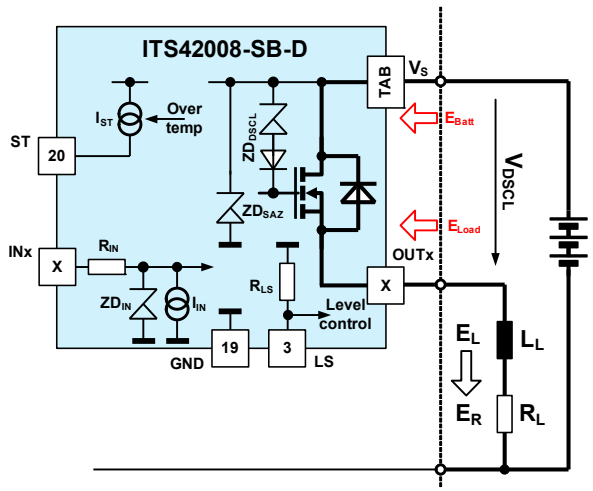
If reverse voltage is applied to the device:
1.) Current via load resistance RL:
$I_{Rev1} = (V_{Rev} - V_{FDS}) / R_L$
2.) Current via Input pin IN and dignostic pin ST:
$I_{Rev2} = I_{ST} + I_{IN}$
To protect the control device the current must be limited with the extrernal series resistors.
Both currents will sum up to:
$I_{Rev} = I_{Rev1} + I_{Rev2}$

Drain-Source power stage clamper V_{DSCL}:



When an inductive load is switched off a current path must be established until the current is sloped down to zero (all energy removed from the inductive load). For that purpose the series combination Z_{DSCL} is connected between Gate and Drain of the power DMOS acting as an active clamp.
When the device is switched off, the voltage at OUT turns negative until V_{DSCL} is reached.
The voltage on the inductive load is the difference between V_{DSCL} and V_S.

Energy calculation:



Energy stored in the load inductance is given by:
$E_L = I_L^2 * L/2$
While demagnetizing the load inductance the energy dissipated by the Power-DMOS is:
$E_{AS} = E_S + E_L - E_R$

With an approximate solution for R_L =0Ω:
$E_{AS} = ½ * L * I_L^2 * \{(1 - V_S / (V_S - V_{DSCL})\}$

Figure 5 Special feature description

7.4 Typical Application Waveforms

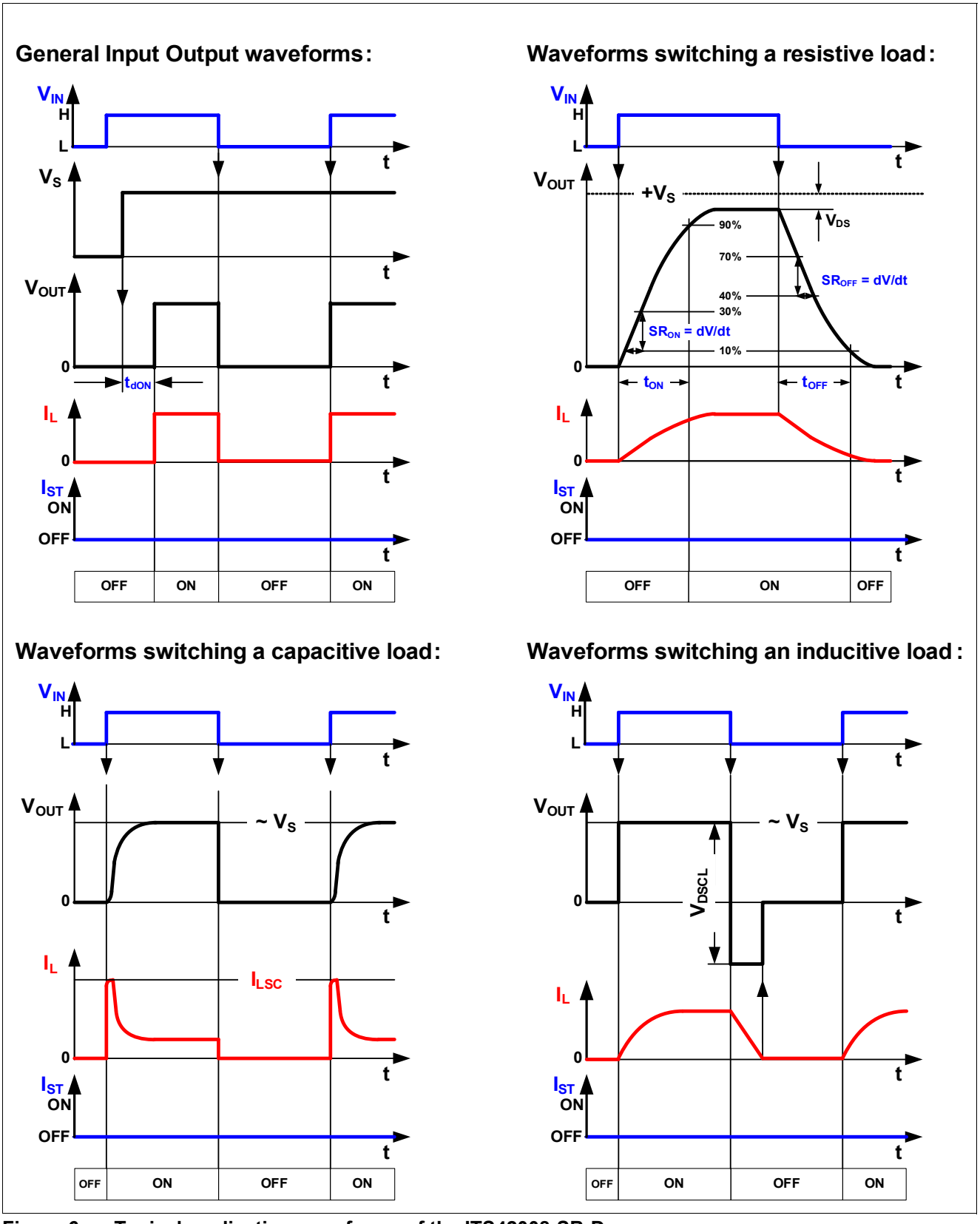


Figure 6 Typical application waveforms of the ITS42008-SB-D

7.5 Protection Behavior

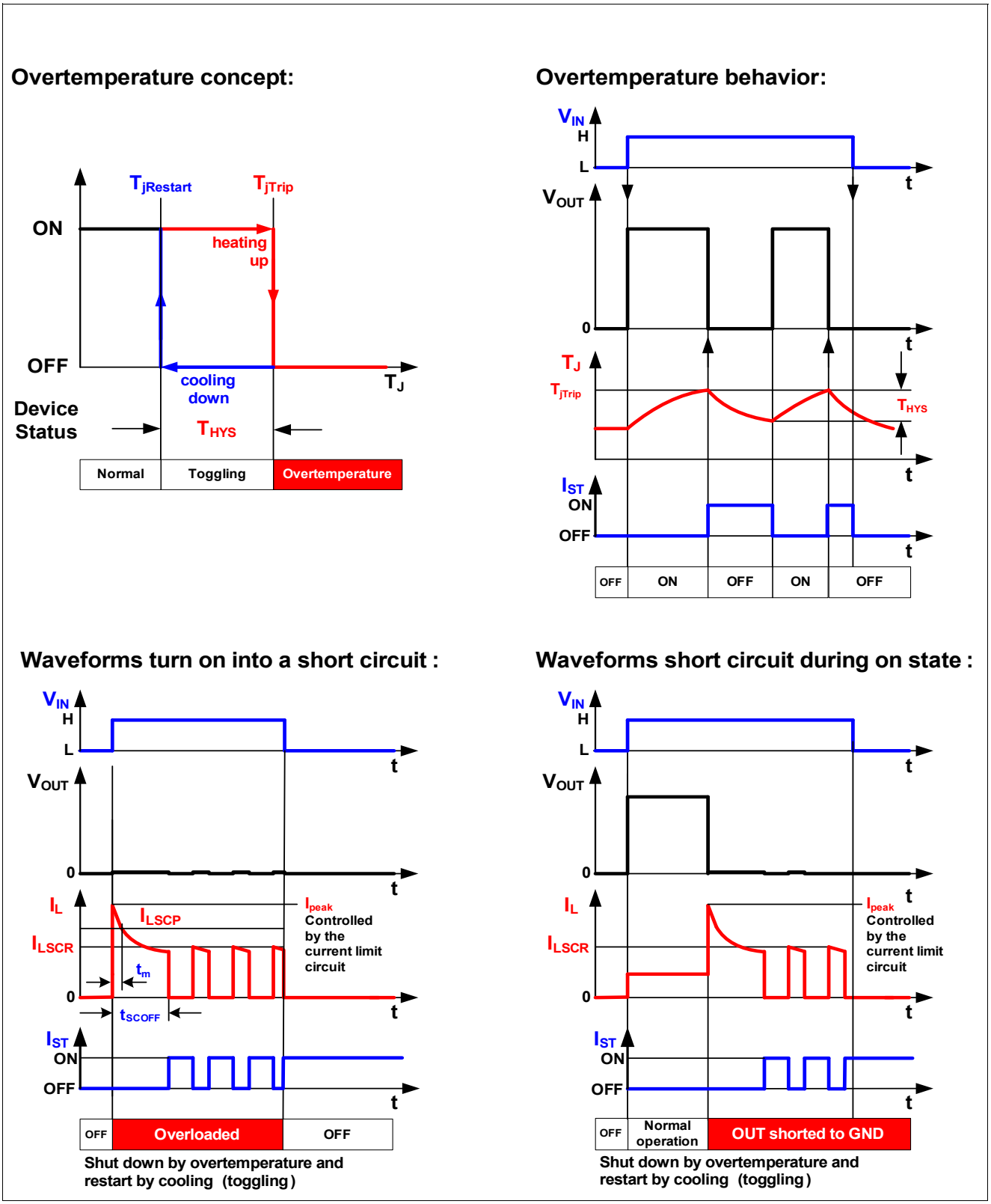


Figure 7 Protective behaviour of the ITS42008-SB-D

8 Package outlines and footprint

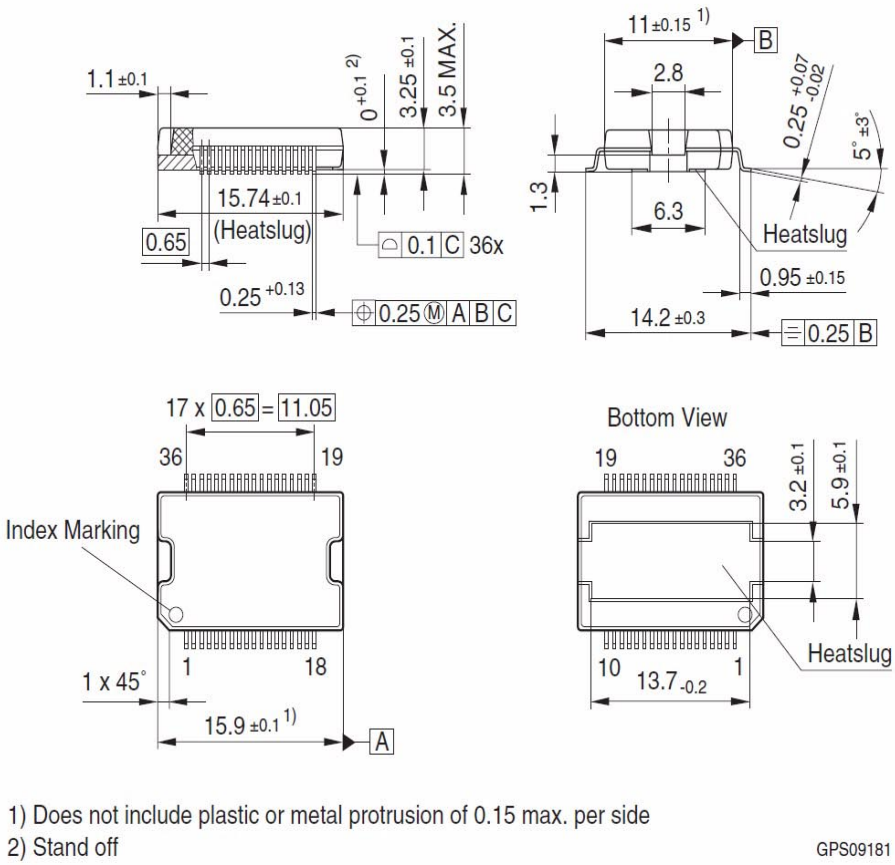


Figure 8 **PG-DSO-36** (Plastic Dual Small Outline Package, RoHS-Compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020

9 Revision History

Revision	Date	Changes
v 1.01	14-05-19	Datasheet release Editorial Change on Page 11 Temperature conditions for lines 5.0.14 and 5.0.15 were corrected to 25°C and 125°C respectively
v 1.0	12-09-01	Datasheet release

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