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FMS6690

Six Channel, 6th Order, SD/PS/HD Video Filter Driver

Features

- Three Selectable Sixth-Order 15/32MHz (PS/HD) Filters
- Three Fixed Sixth-Order 8MHz (SD) Filters with MUXed Input
- Transparent Input Clamping
- Single Video Load Drive (2V_{PP}, 150Ω, A_V= 6dB)
- AC-or DC-Coupled Inputs
- AC-or DC-Coupled Outputs
- DC-Coupled Outputs Eliminate AC-Coupling Capacitors
- Low Power
- 5V Only

Applications

- Cable and Satellite Set-Top Boxes
- DVD Players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)


Description

The FMS6690 Low-Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Six 6th-order Butterworth filters provide improved image quality compared to typical passive solutions. The combination of low-power Standard Definition (SD), Progressive Scan (PS), and High Definition (HD) filters greatly simplifies DVD video output circuitry. Three channels offer fixed SD filters and feature an additional MUXed input, while the other three channels are selectable between PS and HD filters. The FMS6690 offers a fixed gain of 6dB.

The FMS6690 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required (*see Applications section for details*).

The outputs can drive AC-or DC-coupled single (150Ω) video loads. DC-coupling the outputs removes the need for output coupling capacitors. The input DC levels are offset approximately +280mV at the output.

Ordering Information

| Part Number | Operating Temperature Range |  Eco Status | Package | Packing Method |
|---------------|-----------------------------|--|---|-----------------------------|
| FMS6690MTC20X | 0° to 70°C | RoHS | 20-Lead Thin Shrink Outline Package (TSSOP) | 2500 Units in Tape and Reel |

 For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Block Diagram

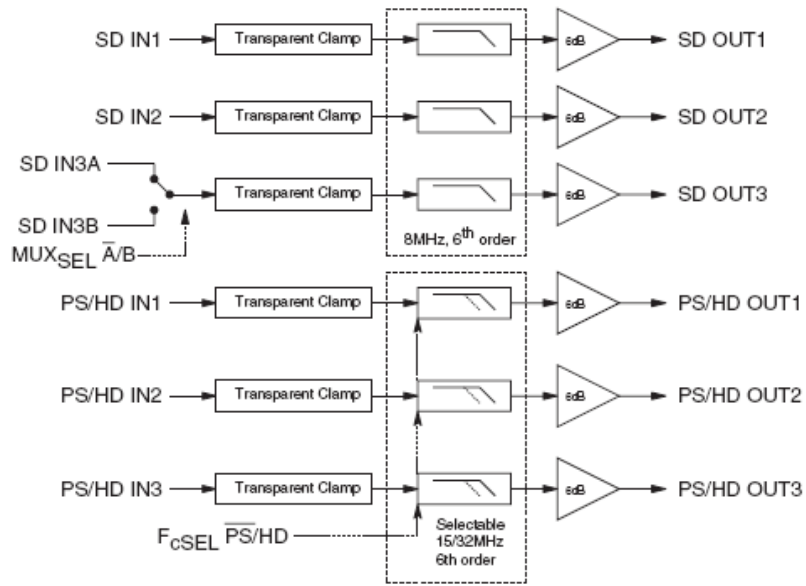


Figure 1. Block Diagram



Pin Configuration

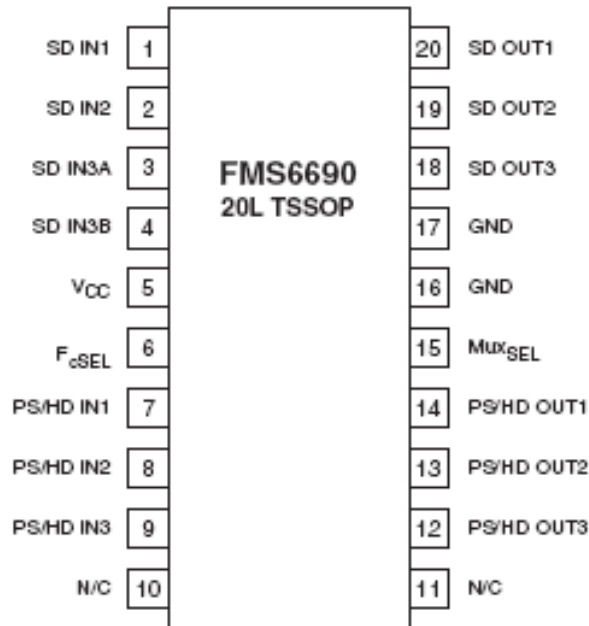


Figure 2. Pin Configuration

Pin Definitions

| Pin # | Name | Type | Description |
|-------|--------------------|--------|--|
| 1 | SD IN1 | Input | SD Video Input, Channel 1 |
| 2 | SD IN2 | Input | SD Video Input, Channel 2 |
| 3 | SD IN3A | Input | SD Video Input, Channel 3A |
| 4 | SD IN3B | Input | SD Video Input, Channel 3B |
| 5 | VCC | Input | +5V Supply |
| 6 | FcSEL | Input | Selects Filter Corner Rrequency for Pins 7, 8, and 9; "0" = PS, "1" = HD |
| 7 | PS/HD IN1 | Input | Selectable PS or HD Video Input, Channel 1 |
| 8 | PS/HD IN2 | Input | Selectable PS or HD Video Input, Channel 2 |
| 9 | PS/HD IN3 | Input | Selectable PS or HD Video Input, Channel 3 |
| 10 | N/C | Input | No Connect |
| 11 | N/C | Input | No Connect |
| 12 | PS/HD OUT3 | Output | Filtered PS or HD Video Output, Channel 3 |
| 13 | PS/HD OUT2 | Output | Filtered PS or HD Video Output, Channel 2 |
| 14 | PS/HD OUT1 | Output | Filtered PS or HD Video Output, Channel 1 |
| 15 | MUX _{SEL} | Input | MUX Selects Between Channel 3A and 3B Inputs; 0 = A, 1 = B |
| 16 | GND | Input | Must Be Tied to Ground |
| 17 | GND | Input | Must Be Tied to Ground |
| 18 | SD OUT3 | Output | Filtered SD Video Output, Channel 3 |
| 19 | SD OUT2 | Output | Filtered SD Video Output, Channel 2 |
| 20 | SD OUT1 | Output | Filtered SD Video Output, Channel 1 |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|------------------|--|-----------------------------------|-----------------------|------|
| V _{CC} | DC Supply Voltage | -0.3 | 6.0 | V |
| V _{IO} | Analog Digital I/O | -0.3 | V _{CC} + 0.3 | V |
| I _{OUT} | Output Current, Any One Channel, Do Not Exceed | | 50 | mA |
| ESD | Electrostatic Discharge Capability | Human Body Model, JESD22-A114 | 9 | kV |
| | | Charged Device Model, JESD22-C101 | 2 | |

Reliability Information

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|---|------|------|------|------|
| T _J | Junction Temperature | | | +150 | °C |
| T _{STG} | Storage Temperature Range | -65 | | +150 | °C |
| T _L | Lead Temperature, Soldering 10 Seconds | | | +300 | °C |
| Θ _{JA} | Thermal Resistance, JEDEC Standard, Multi-Layer Test Board, Still Air | | 74 | | °C/W |

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|-----------------------------|------|------|------|------|
| T _A | Operating Temperature Range | 0 | | +70 | °C |
| V _{CC} | Supply Voltage Range | 4.75 | 5.00 | 5.25 | V |

DC Electrical Characteristics

Unless otherwise noted, T_A=25°C, V_{CC}=5V, AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω loads, referenced to 400kHz.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------------|-----------------------------------|---------------------------------|------|------|-----------------|-----------------|
| I _{CC} | Supply Current ⁽¹⁾ | No Load | | 60 | 80 | mA |
| V _{IN} | Video Input Voltage Range | Referenced to GND if DC Coupled | | 1.4 | | V _{PP} |
| V _{IL} | Digital Input Low ⁽¹⁾ | F _{CSEL} | 0 | | 0.8 | V |
| V _{IH} | Digital Input High ⁽¹⁾ | F _{CSEL} | 2.4 | | V _{CC} | V |

Note:

- 100% tested at 25°C.

Standard-Definition Electrical Characteristics

Unless otherwise noted, $T_A=25^{\circ}\text{C}$, $V_{IN}=1V_{PP}$, $V_{CC}=5V$, all inputs AC coupled with $0.1\mu\text{F}$, all outputs AC coupled with $220\mu\text{F}$ into 150Ω loads, referenced to 400kHz .

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------|--|---|------|------|------|-------|
| AV_{SD} | Channel Gain ⁽²⁾ | All SD Channels | 5.6 | 6.0 | 6.4 | dB |
| f_{1dBSD} | -1dB Flatness ⁽²⁾ | All SD Channels | 5.20 | 7.15 | | MHz |
| f_{cSD} | -3dB Bandwidth ⁽²⁾ | All SD Channels | 6.5 | 8.0 | | MHz |
| f_{SBSD} | Attenuation (Stopband Reject) ⁽²⁾ | All SD Channels at $f=27\text{MHz}$ | 43 | 50 | | dB |
| DG | Differential Gain | All SD Channels | | 0.7 | | % |
| DP | Differential Phase | All SD Channels | | 1.0 | | ° |
| THD | Distortion, Output | $V_{OUT}=1.4V_{PP}$, 3.58MHz | | 0.35 | | % |
| X_{TALKSD} | Crosstalk (Ch-to-Ch) | at 1MHz | | -54 | | dB |
| SNR | Signal-to-Noise Ratio ⁽³⁾ | NTC-7 Weighting, 100kHz to 4.2MHz | | 72 | | dB |
| t_{pdSD} | Propagation Delay | Delay from Input to Output, 4.5MHz | | 90 | | ns |

Notes:

- 100% tested at 25°C .
- SNR=20 • log (714mV / rms noise).

Progressive Scan Electrical Characteristics

Unless otherwise noted, $T_A=25^{\circ}\text{C}$, $V_{IN}=1V_{PP}$, $V_{CC}=3.3V$, $R_{SOURCE}=37.5\Omega$, all inputs AC coupled with $0.1\mu\text{F}$, all outputs AC coupled with $220\mu\text{F}$ into 150Ω loads, referenced to 400kHz .

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------|---|---|------|------|------|-------|
| AV_{PS} | Channel Gain ⁽⁴⁾ | All PS Channels | 5.6 | 6.0 | 6.4 | dB |
| f_{1dBSD} | -1dB Flatness ⁽⁴⁾ | All PS Channels | 12 | 14 | | MHz |
| f_{cPS} | -3dB Bandwidth ⁽⁴⁾ | All PS Channels | 13 | 16 | | MHz |
| f_{SBSD} | Attenuation (Stopband Reject) ⁽⁴⁾ | All PS Channels at $f=54\text{MHz}$ | 37 | 45 | | dB |
| THD | Total Harmonic Distortion, Output (All PS Channels) | $V_{OUT}=1.4V_{PP}$, 7MHz | | 0.35 | | % |
| X_{TALKPS} | Crosstalk (Ch-to-Ch) | at 1MHz | | -53 | | dB |
| SNR | Signal-to-Noise Ratio ⁽⁵⁾ | Unweighted, 100kHz to 15MHz | | 66 | | dB |
| t_{pdSD} | Propagation Delay | Delay from Input to Output | | 47 | | ns |

Notes:

- 100% tested at 25°C .
- SNR=20 • log (714mV / rms noise).

High-Definition Electrical Characteristics

Unless otherwise noted, $T_A=25^{\circ}\text{C}$, $V_{IN}=1V_{PP}$, $V_{CC}=5V$, $R_{SOURCE}=37.5\Omega$, all inputs AC coupled with $0.1\mu\text{F}$, all outputs AC coupled with $220\mu\text{F}$ into 150Ω loads, referenced to 400kHz .

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------|--|---|------|------|------|-------|
| AV_{HD} | Channel Gain ⁽⁶⁾ | All HD Channels | 5.6 | 6.0 | 6.4 | dB |
| f_{1dBHD} | -1dB Flatness ⁽⁶⁾ | All HD Channels | 28 | 31 | | MHz |
| f_{cHD} | -3dB Bandwidth ⁽⁶⁾ | All HD Channels | 30 | 34 | | MHz |
| f_{SBHD} | Attenuation (Stopband Reject) ⁽⁶⁾ | All HD Channels at $f=74.25\text{MHz}$ | 30 | 41 | | dB |
| THD | Output Distortion,(All PS Channels) | $V_{OUT}=1.4V_{PP}$, 22MHz | | 0.9 | | % |
| X_{TALKHD} | Crosstalk (Ch-to-Ch) | at 1MHz | | -54 | | dB |
| SNR | Signal-to-Noise Ratio ⁽⁷⁾ | Unweighted, 100kHz to 30MHz | | 60 | | dB |
| t_{pdHD} | Propagation Delay | Delay from Input to Output | | 25 | | ns |

Notes:

- 100% tested at 25°C .
- SNR=20 • log (714mV / rms noise).

Typical Performance Characteristics

Unless otherwise noted $T_C=25^\circ\text{C}$, $V_{IN}=1V_{PP}$, $V_{CC}=5V$, $R_{SOURCE}=37.5\Omega$, inputs AC coupled with $0.1\mu\text{F}$, all outputs AC coupled with $220\mu\text{F}$ into 150Ω loads.

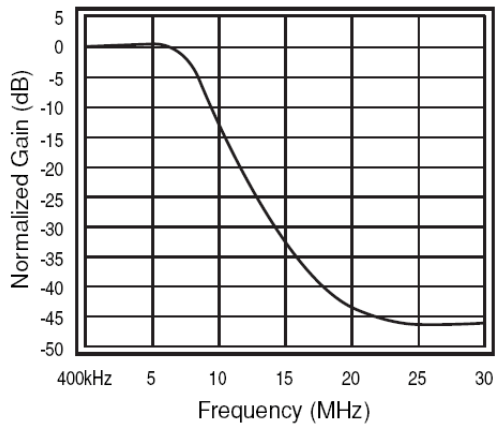


Figure 3. SD Gain vs. Frequency

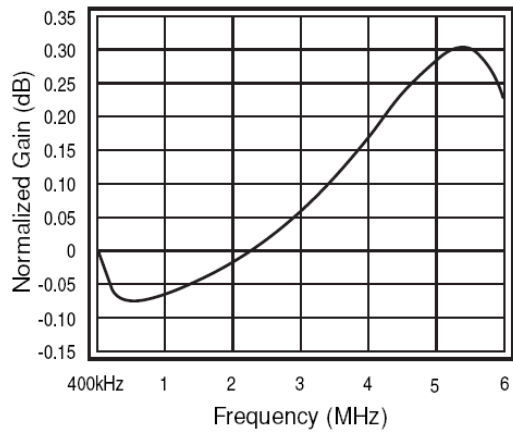


Figure 4. SD Flatness vs. Frequency

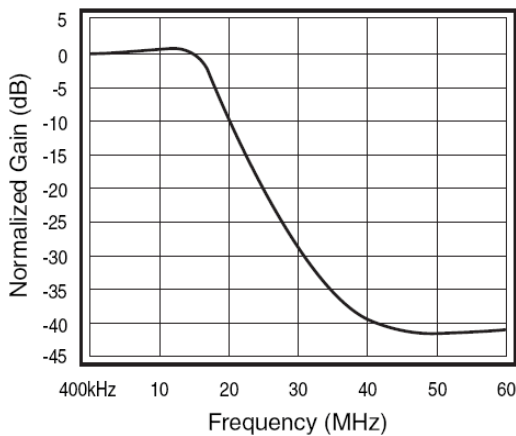


Figure 5. PS Gain vs. Frequency

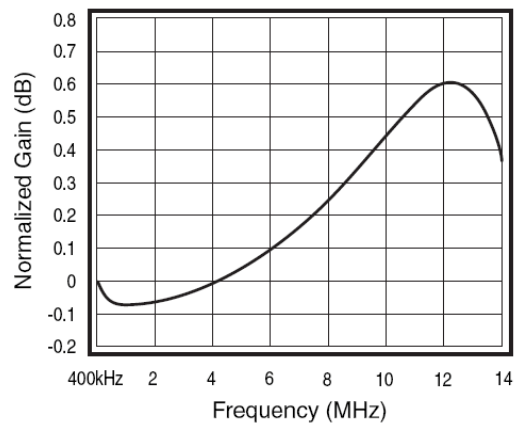


Figure 6. PS Flatness vs. Frequency

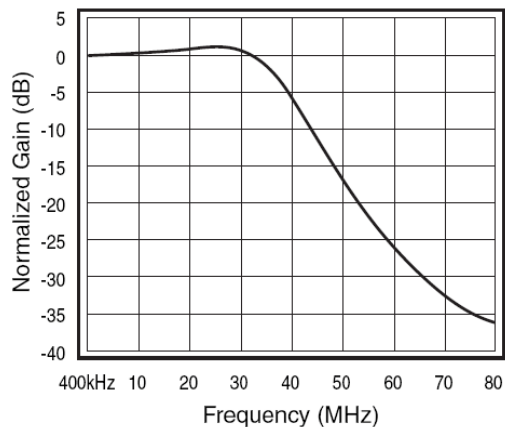


Figure 7. HD Gain vs. Frequency

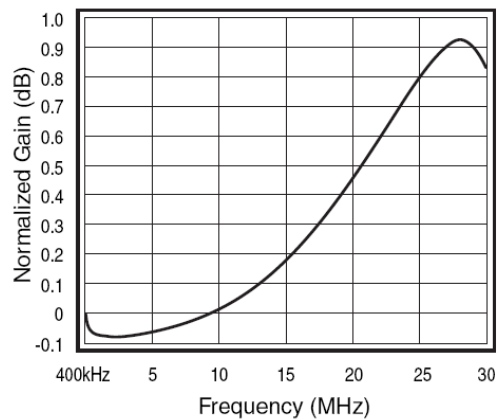


Figure 8. HD Flatness vs. Frequency

Typical Performance Characteristics

Unless otherwise noted $T_C=25^\circ\text{C}$, $V_{IN}=1V_{PP}$, $V_{CC}=5V$, $R_{SOURCE}=37.5\Omega$, inputs AC coupled with $0.1\mu\text{F}$, all outputs AC coupled with $220\mu\text{F}$ into 150Ω loads.

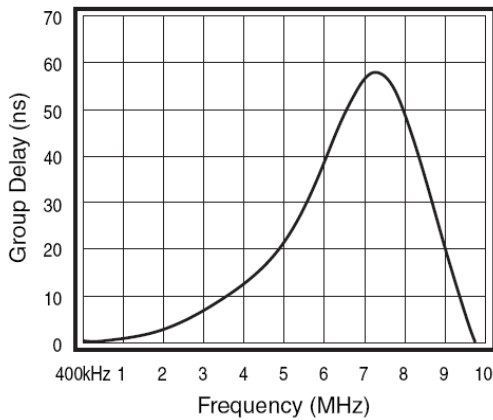


Figure 9. SD Group Delay vs. Frequency

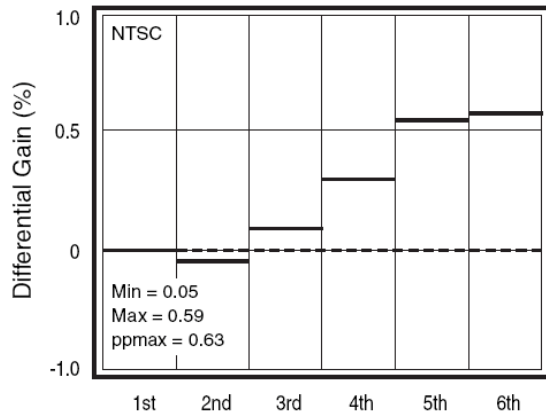


Figure 10. Noise vs. Frequency

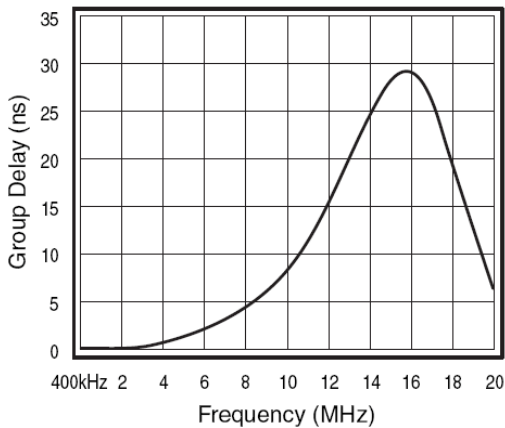


Figure 11. PS Group Delay vs. Frequency

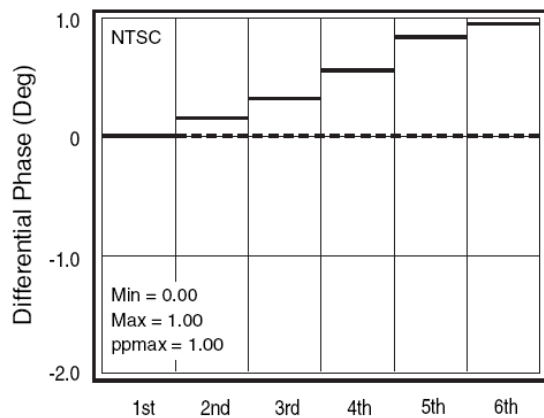


Figure 12. SD Differential Gain

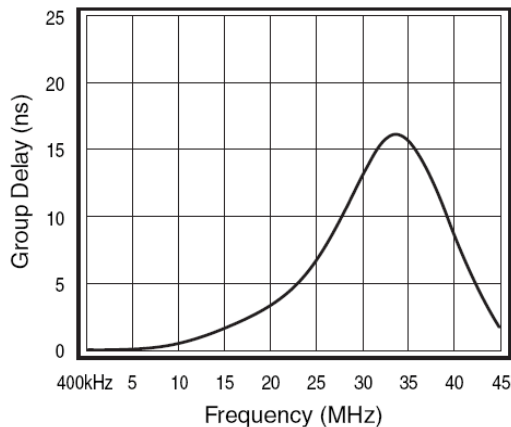
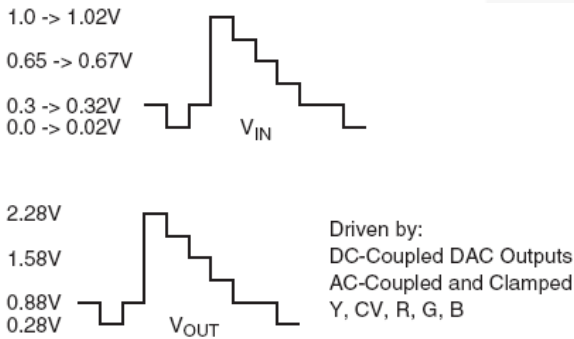


Figure 13. HD Group Delay vs. Frequency

Applications Information

Functional Description

The FMS6690 Low-Cost Video Filter (LCVF) provides 6dB gain (9dB optional, contact factory for further information) from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in Figure 14.



There will be a 280mV offset from the DC input level to the DC output level. $V_{OUT} = 2 * V_{IN} + 280mV$

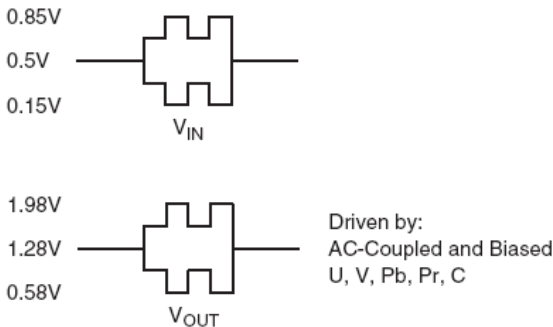


Figure 14. Typical Voltage Levels

The FMS6690 provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the FMS6690 without an AC coupling capacitor. The worst-case sync tip compression, due to the clamp, does not exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within acceptable range. When the input is AC-coupled, the diode clamp sets the sync tip (or lowest voltage) just below ground.

For symmetric signals like C, U, V, Cb, Cr, Pb, and Pr; the average DC bias is fairly constant and the inputs can be AC-coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 15.

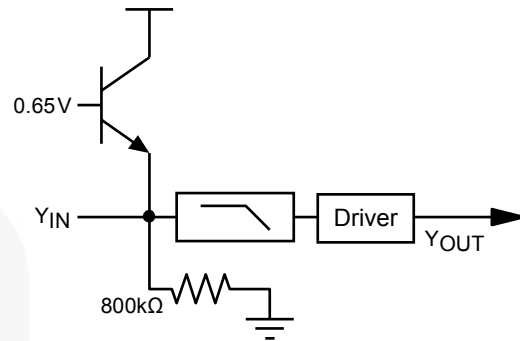


Figure 15. Input Clamp Circuit

I/O Configurations

For DC-coupled DAC drive with DC-coupled outputs, use the configuration in Figure 16.

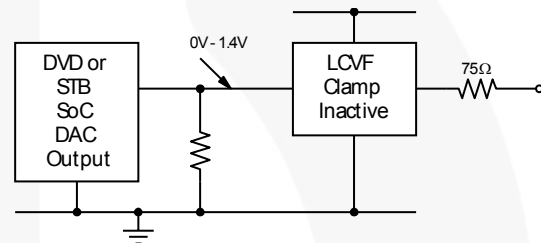


Figure 16. DC-Coupled Inputs and Outputs

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC-coupled, as shown in Figure 17.

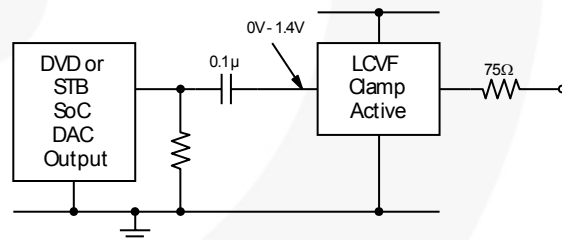


Figure 17. AC-Coupled Inputs, DC-coupled Outputs

When the FMS6690 is driven by an unknown external source or a SCART with its own clamping circuitry, the inputs should be AC-coupled, shown in Figure 18.

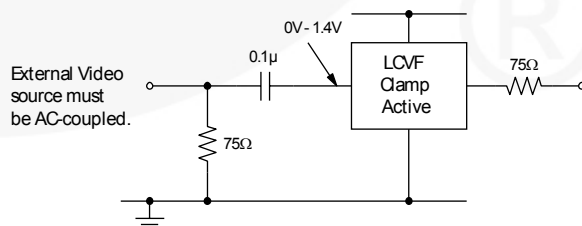


Figure 18. SCART with DC-Coupled Outputs

The same method can be used for biased signals with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is $800k\Omega \pm 20\%$, so the external resistance should be $7.5M\Omega$ to set the DC level to 500mV. If a pull-up resistance of less than $7.5M\Omega$ desired, add an external pull-down such that the DC input level is set to 500mV.

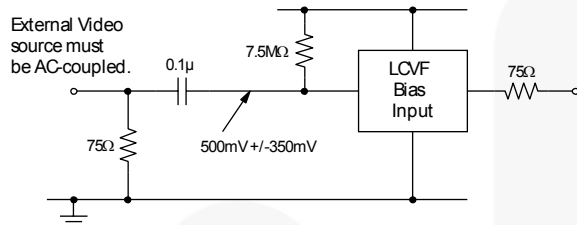


Figure 19. Biased SCART with DC-Coupled Outputs

The same circuits can be used with AC-coupled outputs if desired.

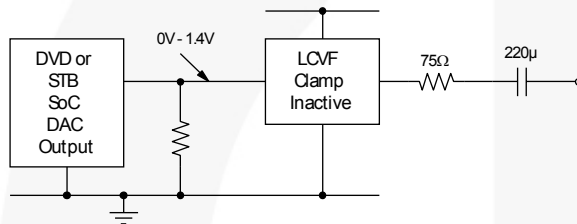


Figure 20. DC-Coupled Inputs, AC-coupled Outputs

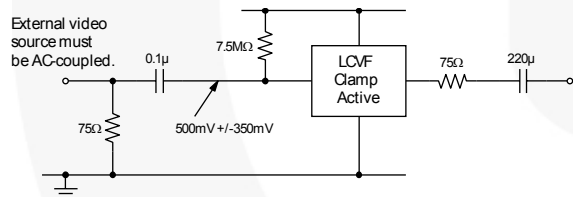


Figure 21. Biased SCART with AC-Coupled Outputs

Note:

- 8. The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond $220\mu F$ to obtain satisfactory operation in some applications.

Power Dissipation

The FMS6690 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the FMS6690's power dissipation and internal temperature rise.

$$T_J = T_A + P_d \cdot \Theta_{JA} \tag{1}$$

where $P_d = P_{CH1} + P_{CH2} + P_{CHx}$,

$$\text{and } P_{CHx} = V_S \cdot I_{CH-} \cdot (V_O^2 / R_L) \tag{2}$$

where:

$$V_O = 2V_{IN} + 0.280V;$$

$$I_{CH} = (I_{CC} / 6) + (V_O / R_L);$$

V_{IN} = RMS value of input signal;

$I_{CC} = 60mA$;

$V_S = 5V$; and

R_L = channel load resistance.

Board layout affects thermal characteristics. Refer to the Layout Considerations section for more information.

Output Considerations

The FMS6690 outputs are DC offset from the input by 150mV therefore, $V_{OUT} = 2 \cdot V_{IN} \text{ DC} + 150\text{mv}$. This offset is required to obtain optimal performance from the output driver and is held at the minimum value to decrease the standing DC current into the load. Since the FMS6690 has a 2x (6dB) gain, the output is typically connected via a 75Ω-series back-matching resistor followed by the 75Ω video cable. Because of the inherent divide by two of this configuration, the blanking level at the load of the video signal is always less than 1V. When AC-coupling the output, ensure that the coupling capacitor of choice passes the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit impedance and the leakage current of the input being driven. To obtain the highest-quality output video signal, the series termination resistor must be placed as close to the device output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the FMS6690 output driver. The distance from device pin to place series termination resistor should be no greater than 0.1 inches.

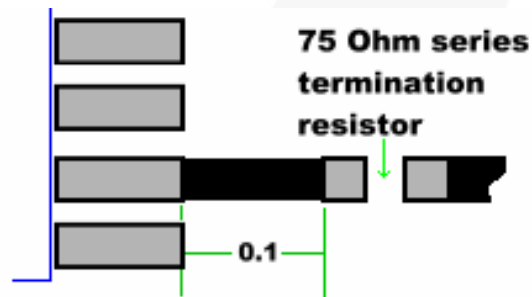


Figure 22. Distance from Device Pin to Series Termination Resistor

Layout Considerations

Layout and supply bypassing play major roles in high-frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6690DEMO, to use as a guide for layout and to aid in device testing and characterization. The FMS6690DEMO is a four-layer board with a full power and ground plane. Following this layout configuration provides the optimum performance and thermal characteristics. For optimum results, follow these steps as a basis for high-frequency layout:

- Include 10 μ F and 0.1 μ F ceramic bypass capacitors.
- Place the 10 μ F capacitor within 0.75 inches of the power pin.
- Place the 0.1 μ F capacitor within 0.1 inches of the power pin.
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For 2 layer boards, use a ground plane that extends beyond the device by at least 0.5.
- Minimize all trace lengths to reduce series inductances.

Typical Application

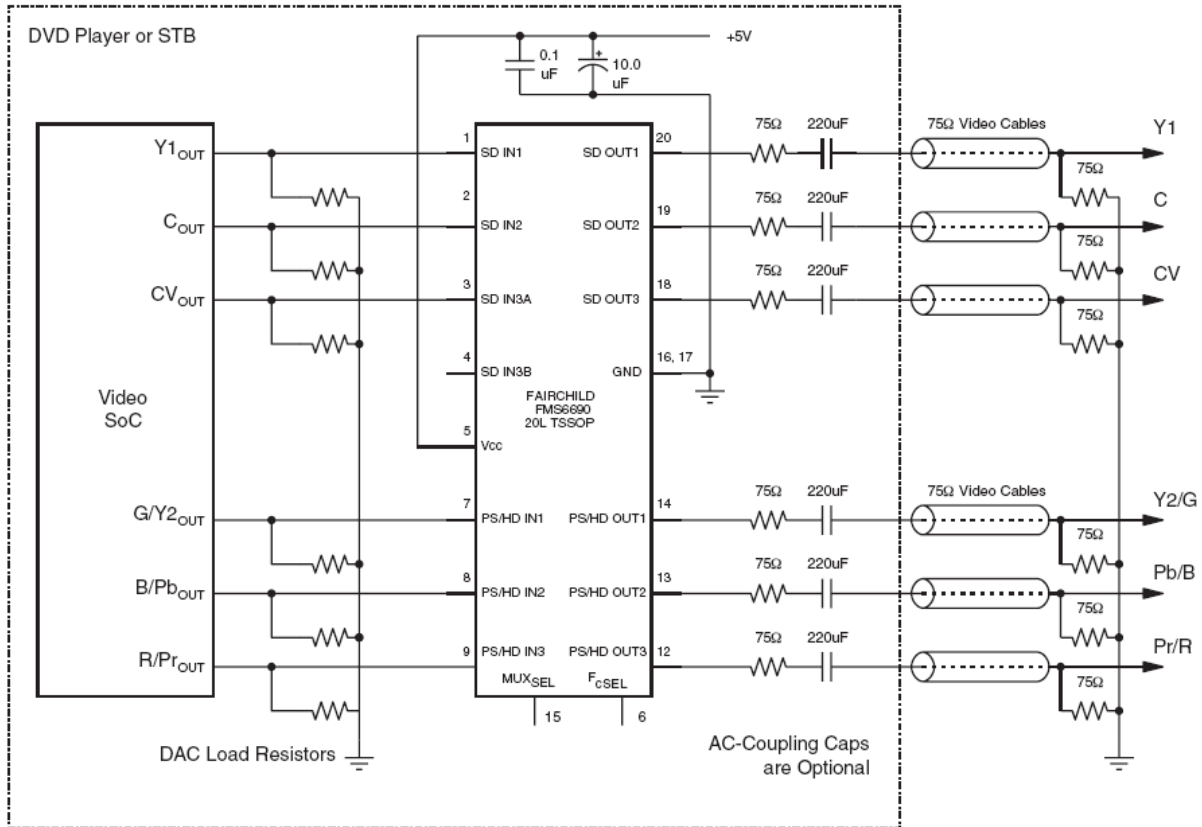
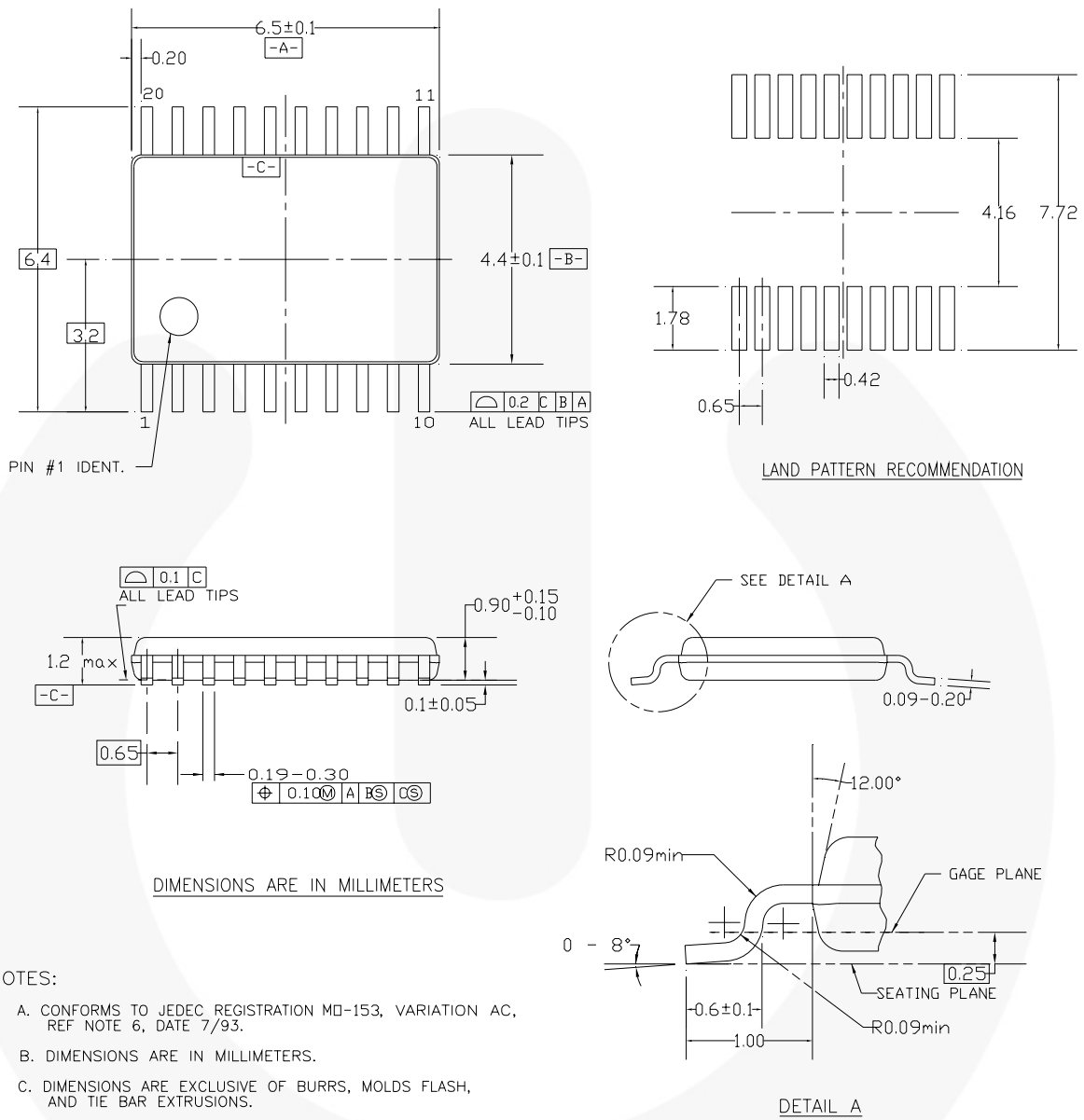


Figure 23. Typical Application Diagram

Physical Dimensions



MTC20REV D1

Figure 24. 20-Lead Thin Shrink Outline Package (TSSOP)






Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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| CROSSVOLT™ | Green FPS™ e-Series™ | Quiet Series™ | TinyLogic® |
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