

SNx4AHC273 Octal D-Type Flip-Flops With Clear

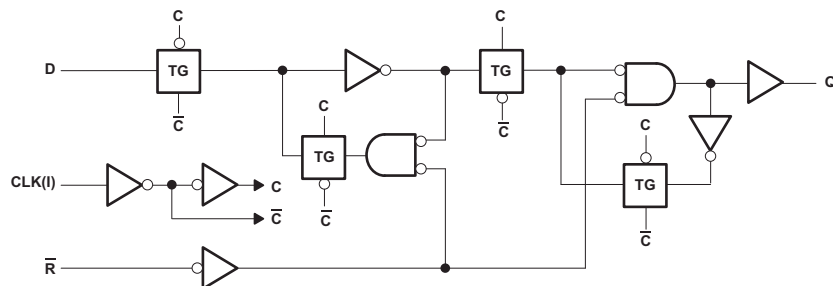
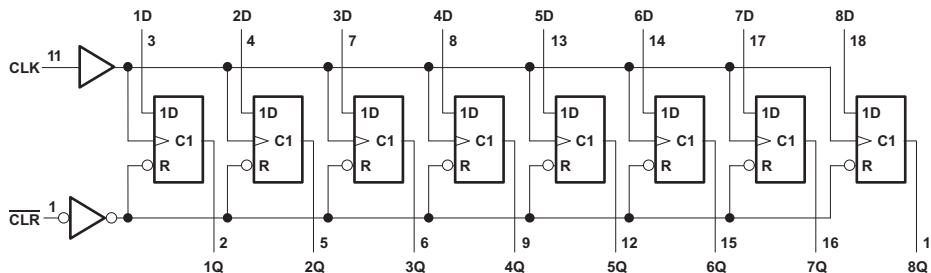
1 Features

- Operating Range 2-V to 5.5-V V_{CC}
- Contain Eight Flip-Flops With Single-Rail Outputs
- Direct Clear Input
- Individual Data Input to Each Flip-Flop
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Buffers and Storage Registers
- Shift Registers
- Pattern Generators
- Servers
- PCs and Notebooks
- Network Switches
- Memory Systems
- Databases

4 Simplified Schematics



3 Description

These devices are positive-edge-triggered D-type flip-flops with a direct clear (CLR) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHC273	PDIP (20)	24.33 mm × 6.35 mm
	SSOP (20)	7.20 mm × 5.30 mm
	TSSOP (20)	6.50 mm × 4.40 mm
	TVSOP (20)	5.00 mm × 4.40 mm
	SOIC (20)	12.80 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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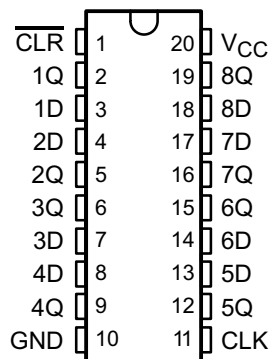
5 Revision History

Changes from Revision H (July 2014) to Revision I	Page
• Changed I_{OH} test conditions for V_{OH} from mA to μA to fix typographical error.	5

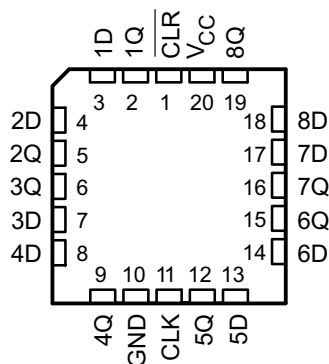
Changes from Revision G (June 1997) to Revision H	Page
• Updated document to new TI data sheet standards.	1
• Deleted Ordering Information table.	1
• Added Military Disclaimer to Features list.	1
• Added Applications.	1
• Added Handling Ratings table.	4
• Changed MAX operating temperature from 85°C to 125°C in Recommended Operating Conditions table.	4
• Added Thermal Information table.	5
• Added Typical Characteristics.	7
• Added Detailed Description section.	9
• Added Application and Implementation section.	11

6 Pin Configuration and Functions

SN54AHC273 . . . J OR W PACKAGE
SN74AHC273 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC273 . . . FK PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{\text{CLR}}$	I	Clear Pin
2	1Q	O	1Q Output
3	1D	I	1D Input
4	2D	I	2D Input
5	2Q	O	2Q Output
6	3Q	O	3Q Output
7	3D	I	3D Input
8	4D	I	4D Input
9	4Q	O	4Q Output
10	GND	—	Ground Pin
11	CLK	I	Clock Pin
12	5Q	O	5Q Output
13	5D	I	5D Input
14	6D	I	6D Input
15	6Q	O	6Q Output
16	7Q	O	7Q Output
17	7D	I	7D Input
18	8D	I	8D Input
19	8Q	O	8Q Output
20	VCC	—	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	−0.5	7	V
V _I	Input voltage range ⁽²⁾	−0.5	7	V
V _O	Output voltage range ⁽²⁾	−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		−20
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}		±20
I _O	Continuous output current	V _O = 0 to V _{CC}		±25
Continuous current through V _{CC} or GND				±75

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	−65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾		
		0	2000	
		0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54AHC273		SN74AHC273		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5		V
		V _{CC} = 3 V		2.1		
		V _{CC} = 5.5 V		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		V
		V _{CC} = 3 V		0.9		
		V _{CC} = 5.5 V		1.65		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		−50		μA
		V _{CC} = 3 V ± 0.3 V		−4		mA
		V _{CC} = 5.5 V ± 0.5 V		−8		−8
I _{OL}	Low-level output current	V _{CC} = 2 V		50		μA
		V _{CC} = 3 V ± 0.3 V		4		mA
		V _{CC} = 5.5 V ± 0.5 V		8		
Δt/Δv	Input transition rise and fall time	V _{CC} = 3 V ± 0.3 V		100		ns/V
		V _{CC} = 5.5 V ± 0.5 V		20		
T _A	Operating free-air temperature	−55	125	−40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC273						UNIT
		N	DW	NS	DB	PW	DGV	
		20 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	53.9	81.8	79.4	98.7	104.7	118.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	38.8	47.8	45.9	60.4	38.8	33.4	
R _{θJB}	Junction-to-board thermal resistance	34.7	49.4	46.9	56.9	55.7	59.6	
ψ _{JT}	Junction-to-top characterization parameter	26.9	20.1	19.1	21.6	2.9	1.1	
ψ _{JB}	Junction-to-board characterization parameter	34.7	49.0	46.5	53.5	55.1	58.9	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the TI application report *IC Package Thermal Metrics* (SPRA953).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC273		SN74AHC273		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9			1.9		1.9	V	
		3 V	2.9			2.9		2.9		
		4.5 V	4.4			4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
		4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	0.1	V	
		3 V			0.1		0.1	0.1		
		4.5 V			0.1		0.1	0.1		
	I _{OL} = 4 mA	3 V			0.36		0.5	0.44		
		4.5 V			0.36		0.5	0.44		
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±0.1		±1 ⁽¹⁾	±1	μA	
I _{CC}	V _I = V _{CC} or GND I _O = 0	5.5 V			4		40	40	μA	
C _i	V _I = V _{CC} or GND	5 V		2.5	10			10	pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

7.6 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

		SN54AHC273				SN74AHC273				UNIT
		T _A = 25°C		MIN	MAX	T _A = 25°C		MIN	MAX	
		MIN	MAX			MIN	MAX			
t _w	Pulse Duration	CLR low	5		6		5		6	ns
		CLK high or low	5		6.5		5		6.5	
t _{su}	Setup time	Data before CLK↑	5.5		6.5		5.5		6.5	ns
		CLR before CLK↑	2.5		2.5		2.5		2.5	
t _h	Hold time, data after CLK↑		1.5		2		1		1	ns

SN54AHC273, SN74AHC273

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7.7 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

		SN54AHC273				SN74AHC273				UNIT
		$T_A = 25^\circ\text{C}$		MIN	MAX	$T_A = 25^\circ\text{C}$		MIN	MAX	
		MIN	MAX			MIN	MAX			
t_w	Pulse Duration	$\overline{\text{CLR}}$ low	5		5		5		5	ns
		CLK high or low	5		5		5		5	
t_{su}	Setup time	Data before CLK \uparrow	4.5		4.5		4.5		4.5	ns
		CLR before CLK \uparrow	2		2		2		2	
t_h	Hold time, data after CLK \uparrow		1.5		2		1		1	ns

7.8 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC273		SN74AHC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	75 ⁽¹⁾	120 ⁽¹⁾		65 ⁽¹⁾		65	MHz	
			$C_L = 50\text{ pF}$	50	75		45		45		
t_{PHL}	$\overline{\text{CLR}}$	Q	$C_L = 15\text{ pF}$		8.9 ⁽¹⁾	13.6 ⁽¹⁾	1 ⁽¹⁾	16 ⁽¹⁾	1	16	ns
t_{PLH}	CKL	Q	$C_L = 15\text{ pF}$		8.7 ⁽¹⁾	13.6 ⁽¹⁾	1 ⁽¹⁾	16 ⁽¹⁾	1	16	
t_{PHL}								8.7 ⁽¹⁾	13.6 ⁽¹⁾	1 ⁽¹⁾	16 ⁽¹⁾
t_{PHL}	$\overline{\text{CLR}}$	Q	$C_L = 50\text{ pF}$		11.4	17.1	1	19.5	1	19.5	ns
t_{PLH}	CLK	Q	$C_L = 50\text{ pF}$		11.2	17.1	1	19.5	1	19.5	
t_{PHL}								11.2	17.1	1	19.5
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1.5 ⁽²⁾				1.5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

7.9 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC273		SN74AHC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	120 ⁽¹⁾	165 ⁽¹⁾		100 ⁽¹⁾		100	MHz	
			$C_L = 50\text{ pF}$	80	110		70		70		
t_{PHL}	$\overline{\text{CLR}}$	Q	$C_L = 15\text{ pF}$		5.2 ⁽¹⁾	8.5 ⁽¹⁾	1 ⁽¹⁾	10 ⁽¹⁾	1	10	ns
t_{PLH}	CKL	Q	$C_L = 15\text{ pF}$		5.8 ⁽¹⁾	9 ⁽¹⁾	1 ⁽¹⁾	10.5 ⁽¹⁾	1	10.5	
t_{PHL}								5.8 ⁽¹⁾	9 ⁽¹⁾	1 ⁽¹⁾	10.5 ⁽¹⁾
t_{PHL}	$\overline{\text{CLR}}$	Q	$C_L = 50\text{ pF}$		6.7	10.5	1	12	1	12	ns
t_{PLH}	CLK	Q	$C_L = 50\text{ pF}$		7.3	11	1	12.5	1	12.5	
t_{PHL}								7.3	11	1	12.5
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1 ⁽²⁾				1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

7.10 Noise Characteristics⁽¹⁾

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		SN74AHC273			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.7		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.7		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

(1) Characteristics are for surface-mount packages only.

7.11 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	No load, $f = 1\text{ MHz}$	31	pF

7.12 Typical Characteristics

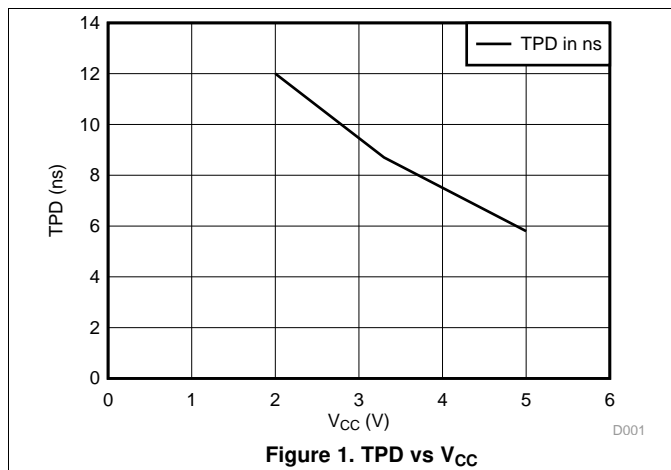


Figure 1. TPD vs VCC

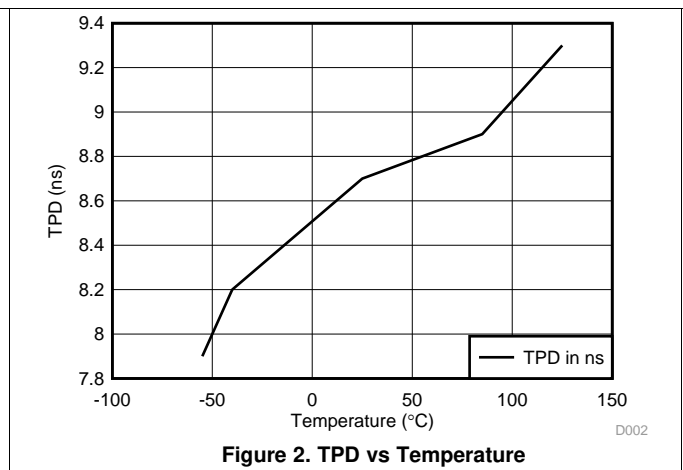
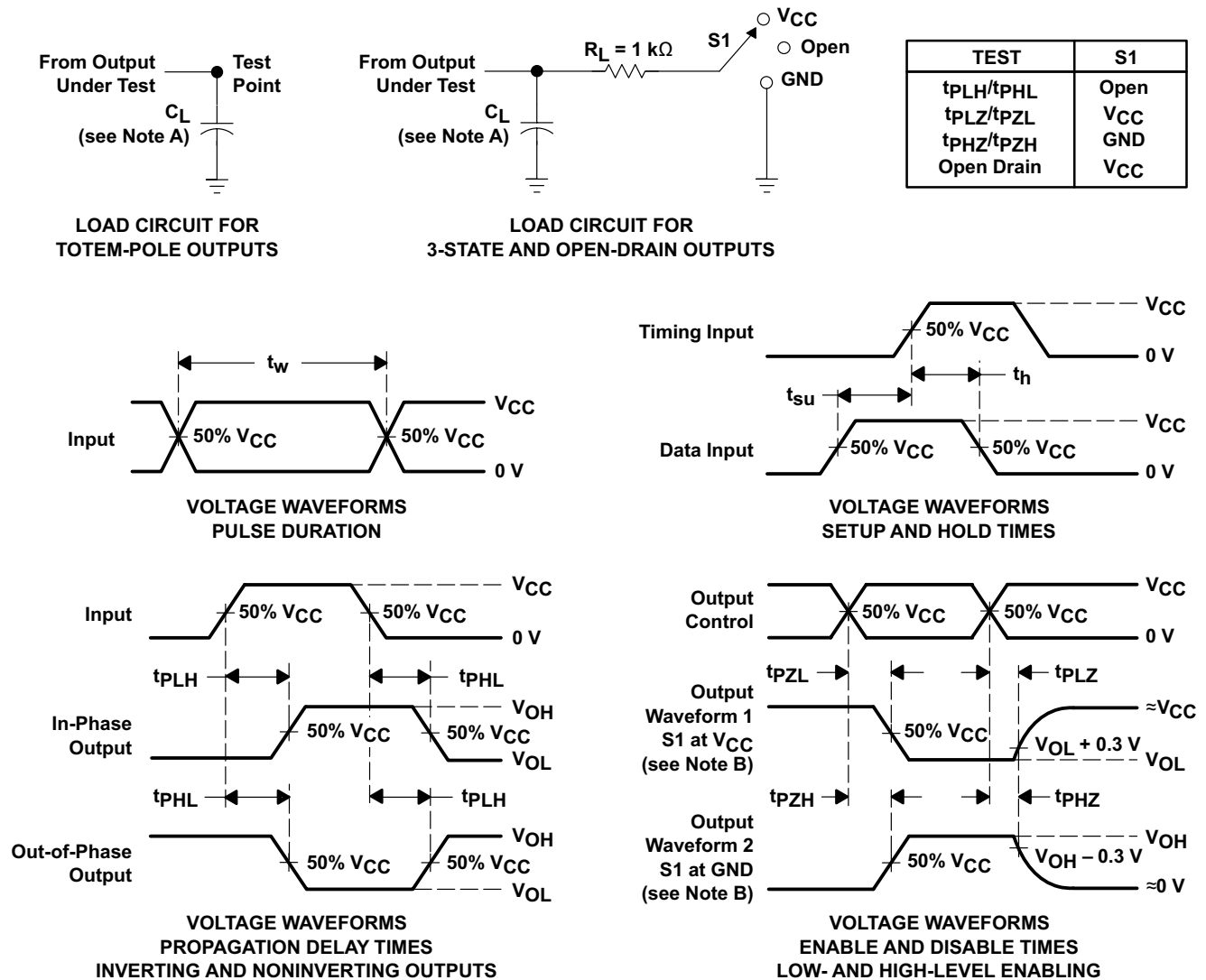


Figure 2. TPD vs Temperature

8 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

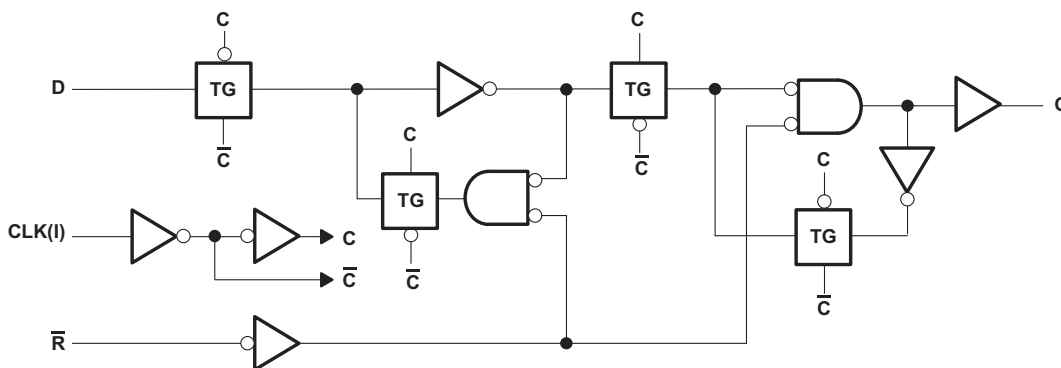
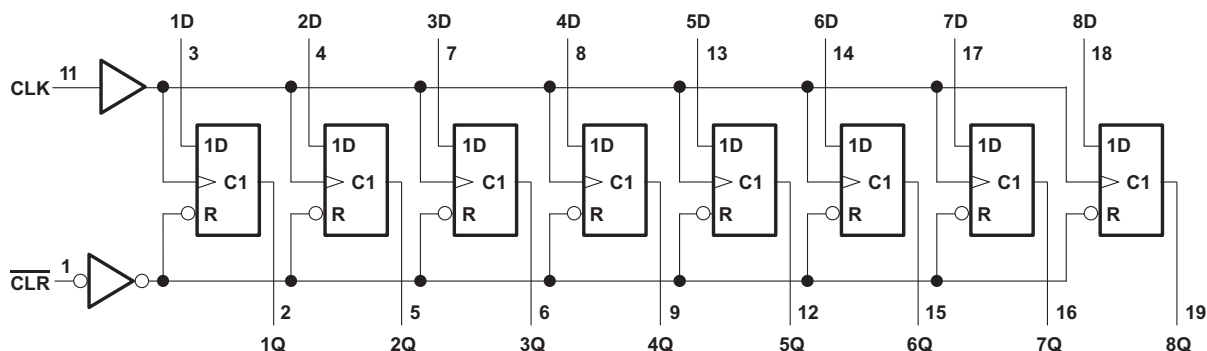
9 Detailed Description

9.1 Overview

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{\text{CLR}}$) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

The inputs are 5 V tolerant and can be driven from 5-V devices. This feature allows the use of these devices as down translators in a mixed 5-V to 3.3-V system environment.

9.2 Functional Block Diagrams



9.3 Feature Description

- Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down voltage translation
 - Inputs accept voltages to 5.5 V
- Slow edge rates minimize output ringing

9.4 Device Functional Modes

Table 1. Function Table

INPUTS			OUTPUT Y
$\overline{\text{CLR}}$	CLK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

10 Application and Implementation

10.1 Application Information

The SNx4AHC273 is a low-drive CMOS device that can be used for a multitude of applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid V_{CC} . This feature makes the device ideal for translating down to the V_{CC} level. Figure 5 shows the reduction in ringing compared to higher drive parts such as AC.

10.2 Typical Application

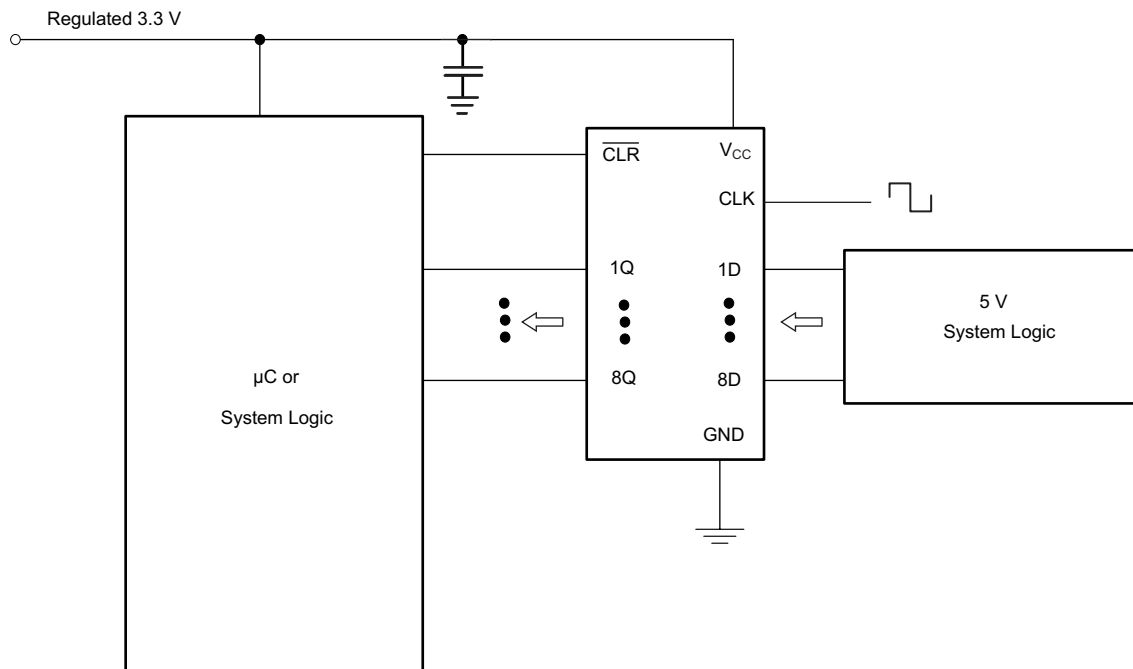


Figure 4. Specific Application Schematic

10.2.1 Design Requirements

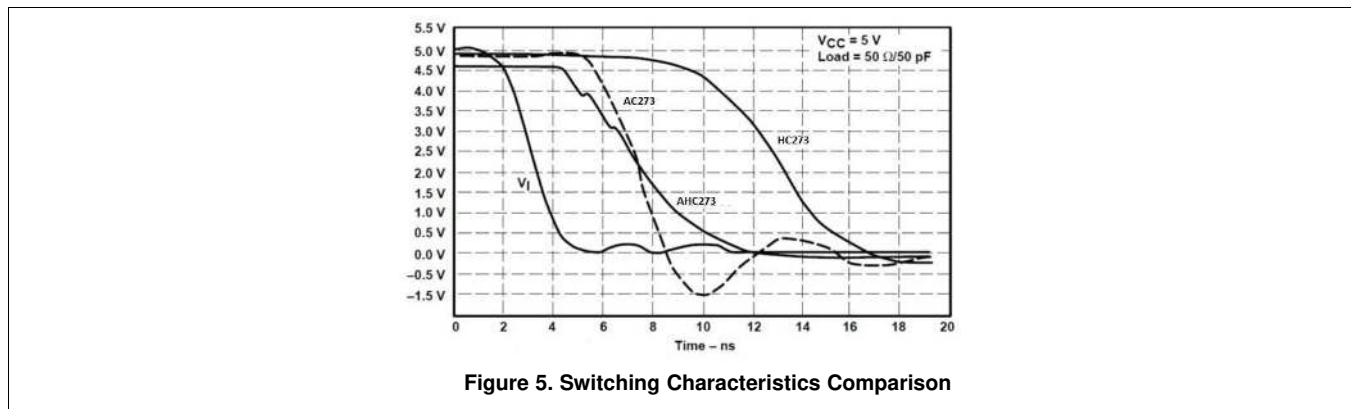
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended input conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - Specified High and low levels: See $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommend output conditions
 - Load currents should not exceed 25 mA per output and 75 mA total for the part
 - Outputs should not be pulled above V_{CC}

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple VCC pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 6](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally inputs will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver.

12.2 Layout Example

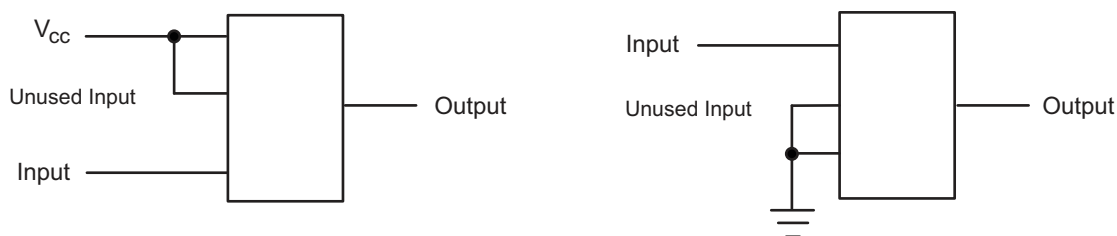


Figure 6. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC273	Click here	Click here	Click here	Click here	Click here
SN74AHC273	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9853001Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9853001Q2A SNJ54AHC 273FK	Samples
5962-9853001QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9853001QR A SNJ54AHC273J	Samples
5962-9853001QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9853001QS A SNJ54AHC273W	Samples
SN74AHC273DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273	Samples
SN74AHC273DGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273	Samples
SN74AHC273DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273	Samples
SN74AHC273DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273	Samples
SN74AHC273N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC273N	Samples
SN74AHC273NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC273	Samples
SN74AHC273PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273	Samples
SN74AHC273PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA273	Samples
SNJ54AHC273FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9853001Q2A SNJ54AHC 273FK	Samples
SNJ54AHC273J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9853001QR A SNJ54AHC273J	Samples
SNJ54AHC273W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9853001QS A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54AHC273W	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC273, SN74AHC273 :

- Catalog: [SN74AHC273](#)

- Military: [SN54AHC273](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC273DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC273DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC273NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC273PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

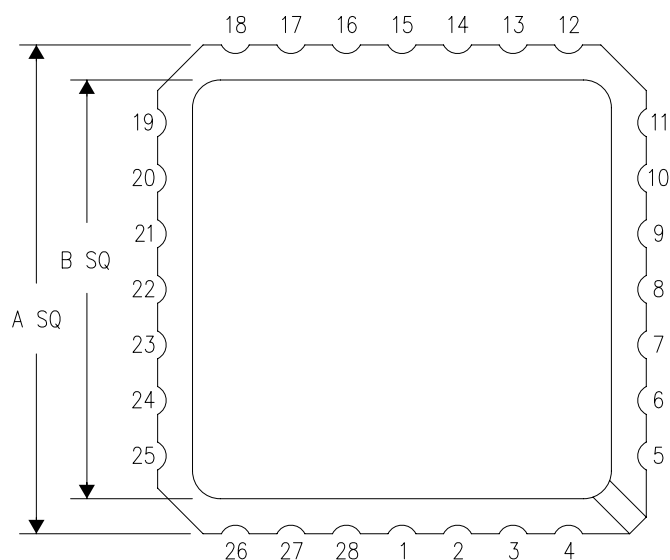

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC273DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74AHC273DGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74AHC273DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC273NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHC273PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

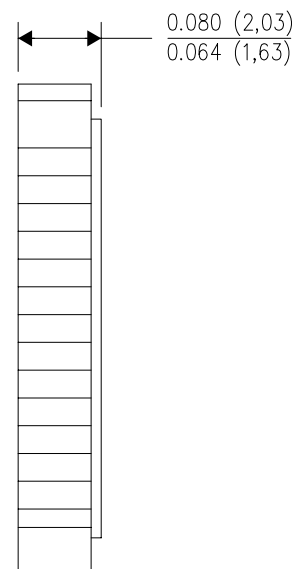
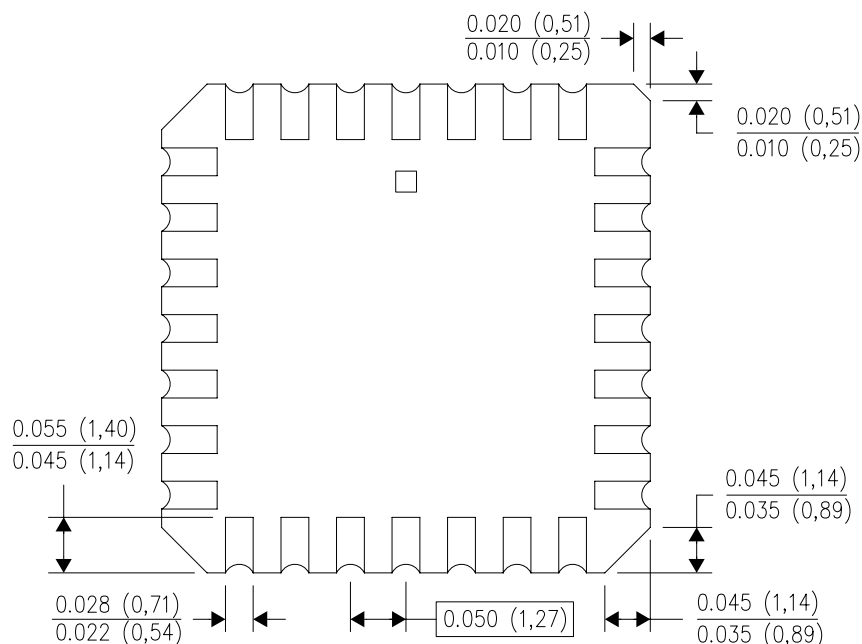
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



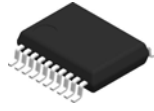
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

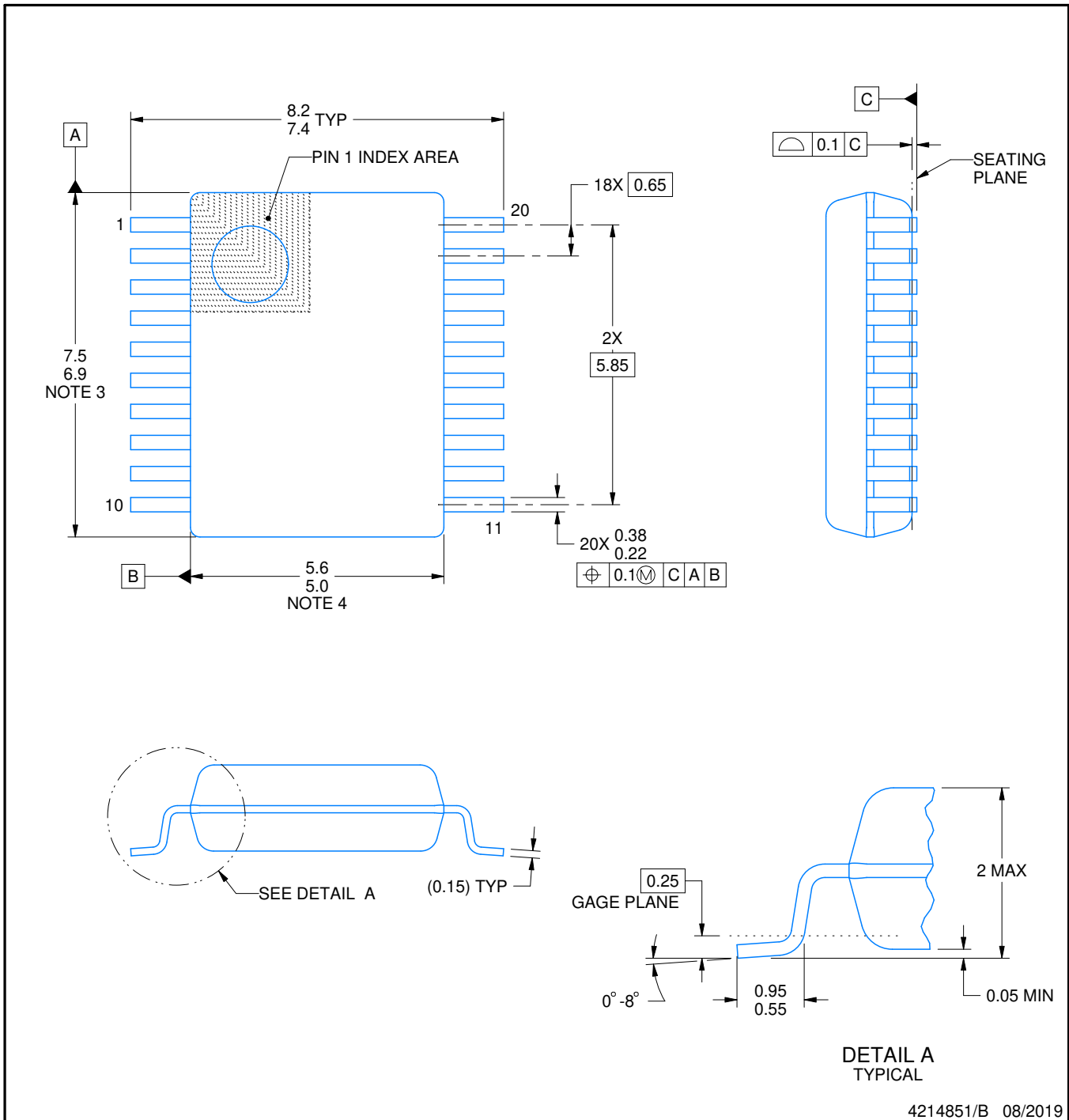
DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

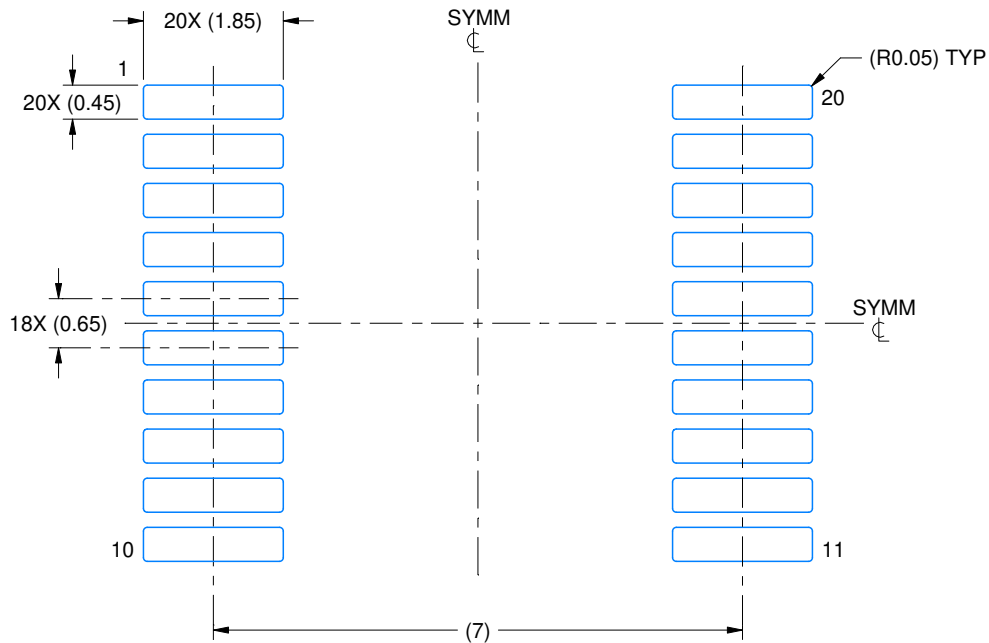
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

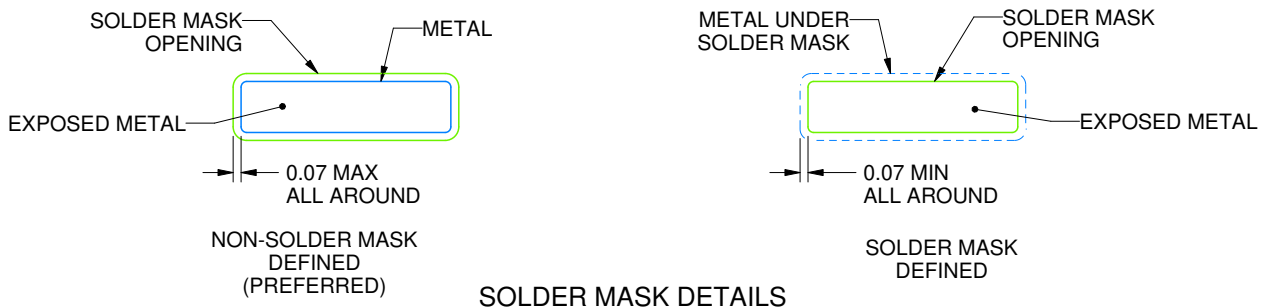
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

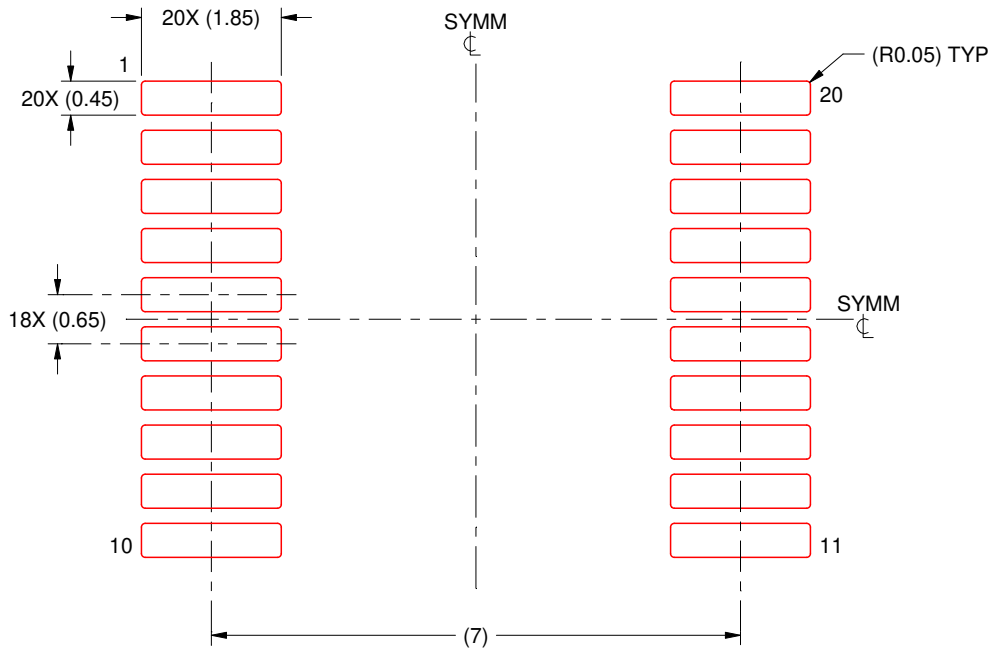
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

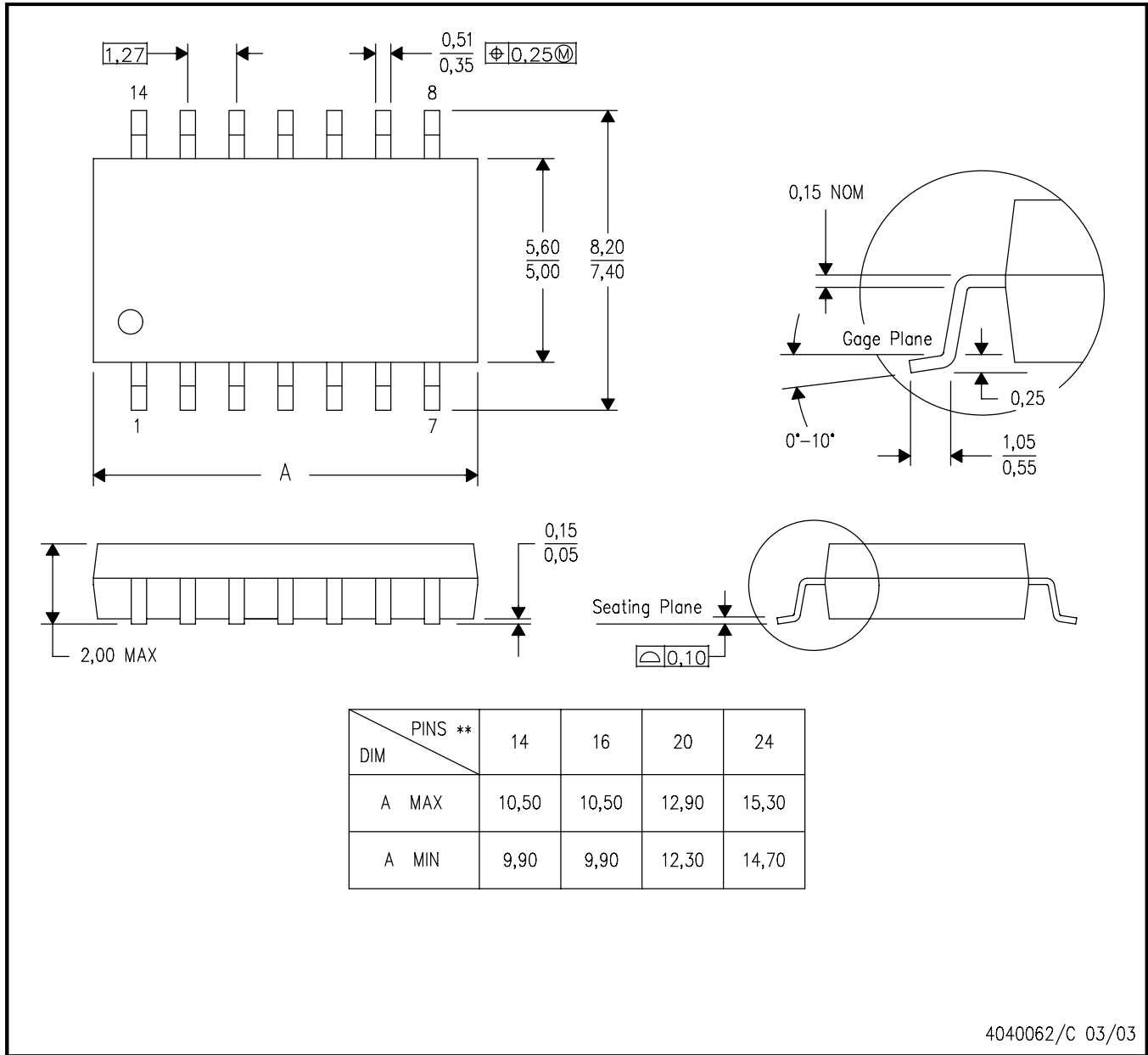
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

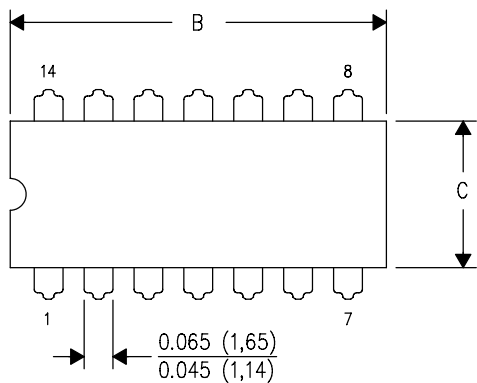


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

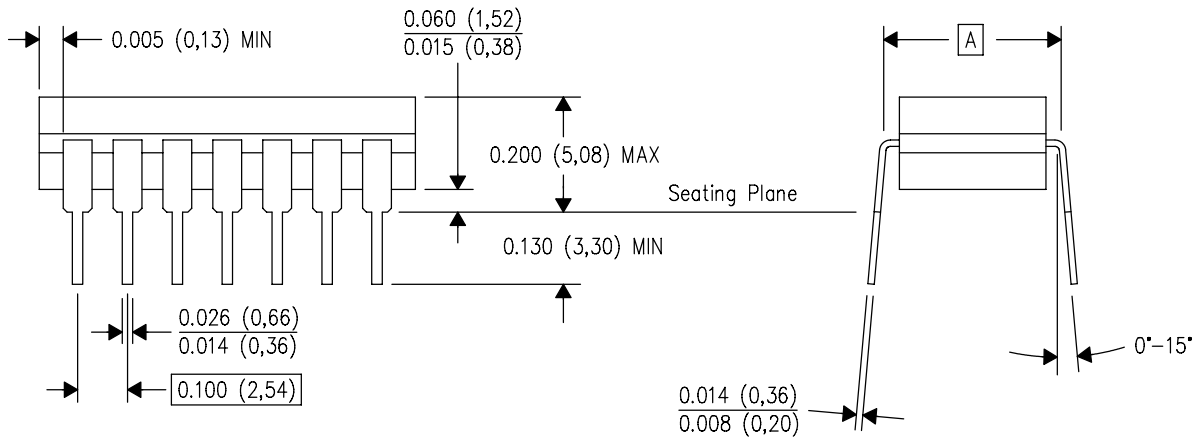
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



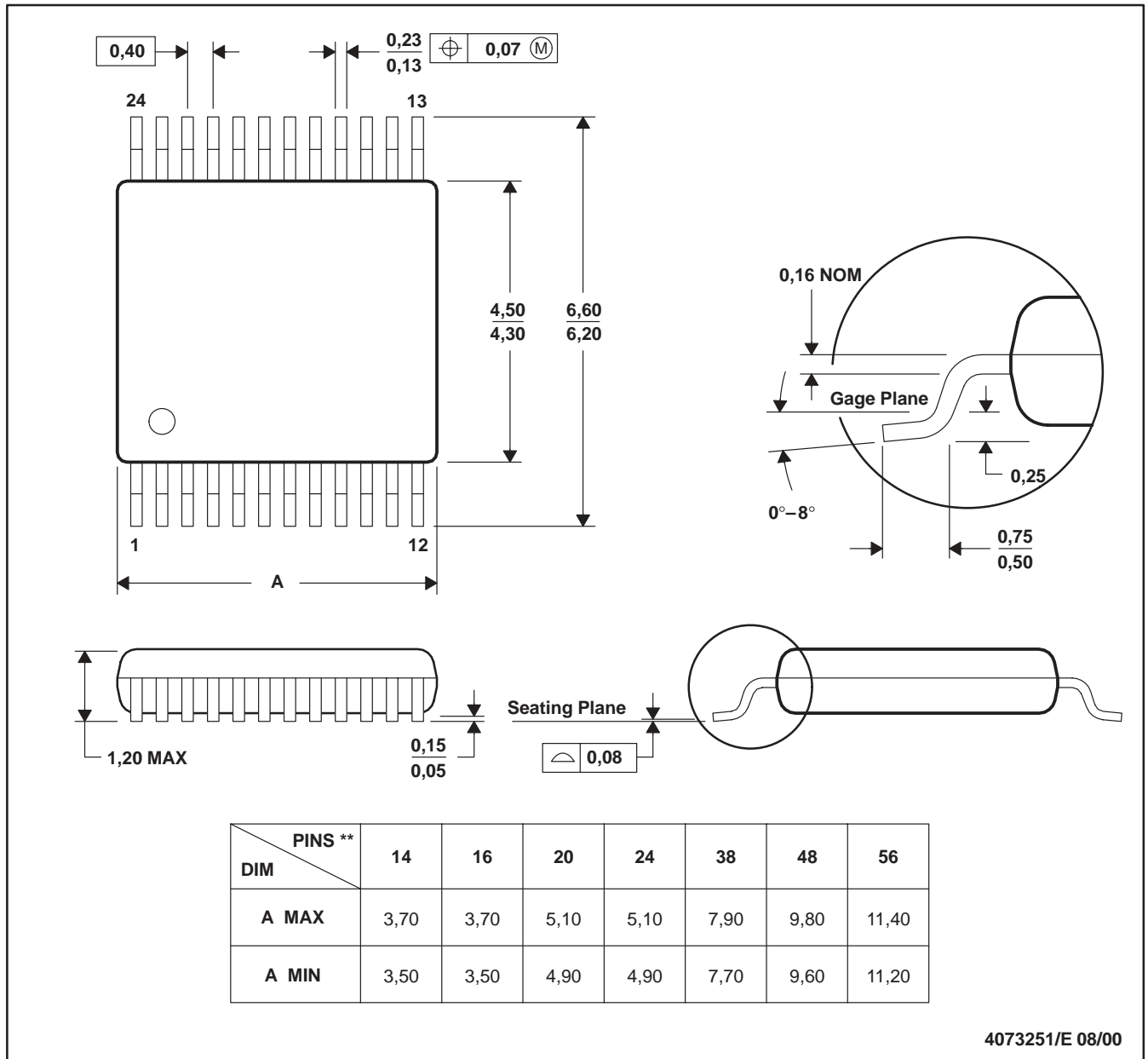
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

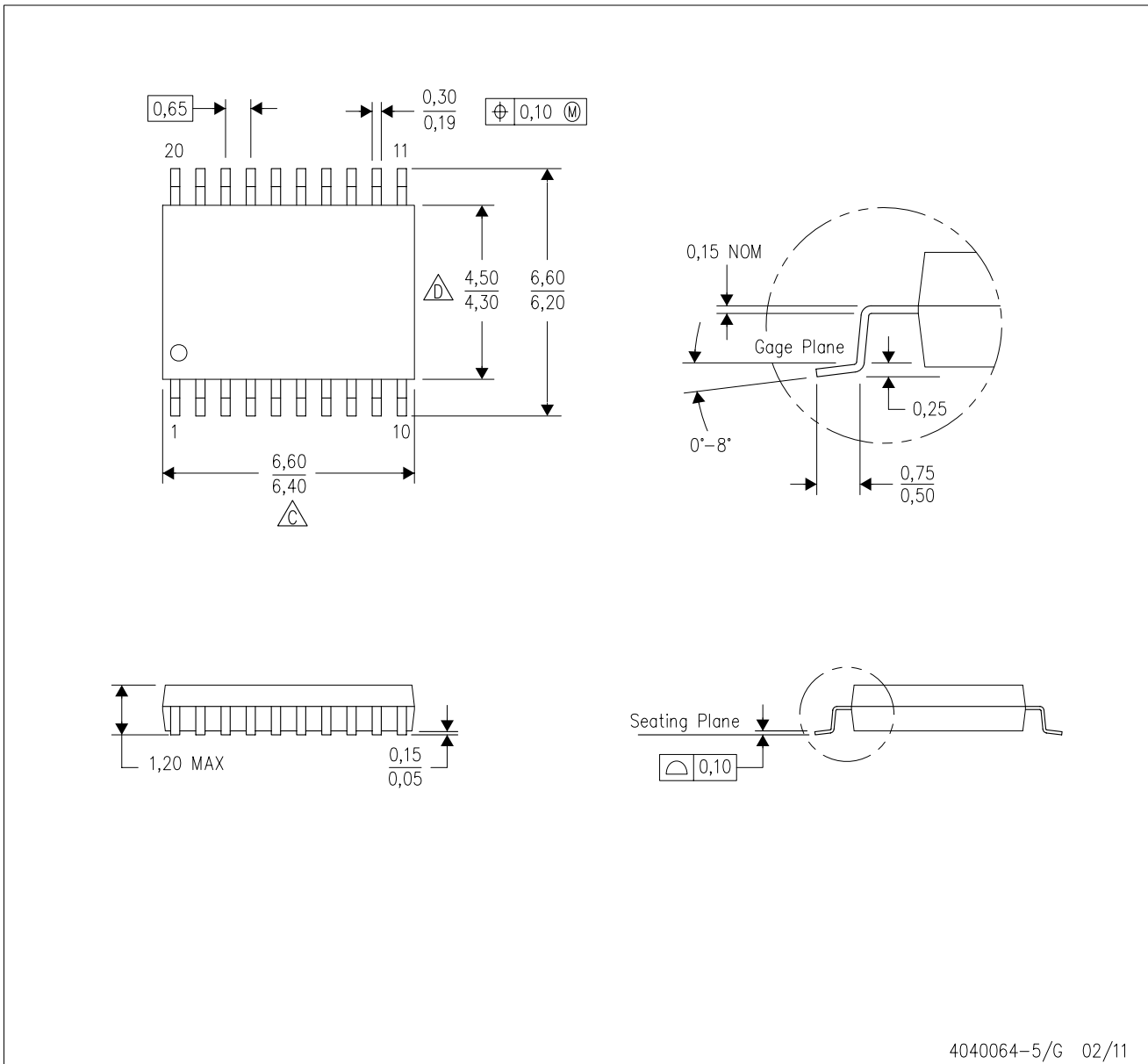


4073251/E 08/00



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

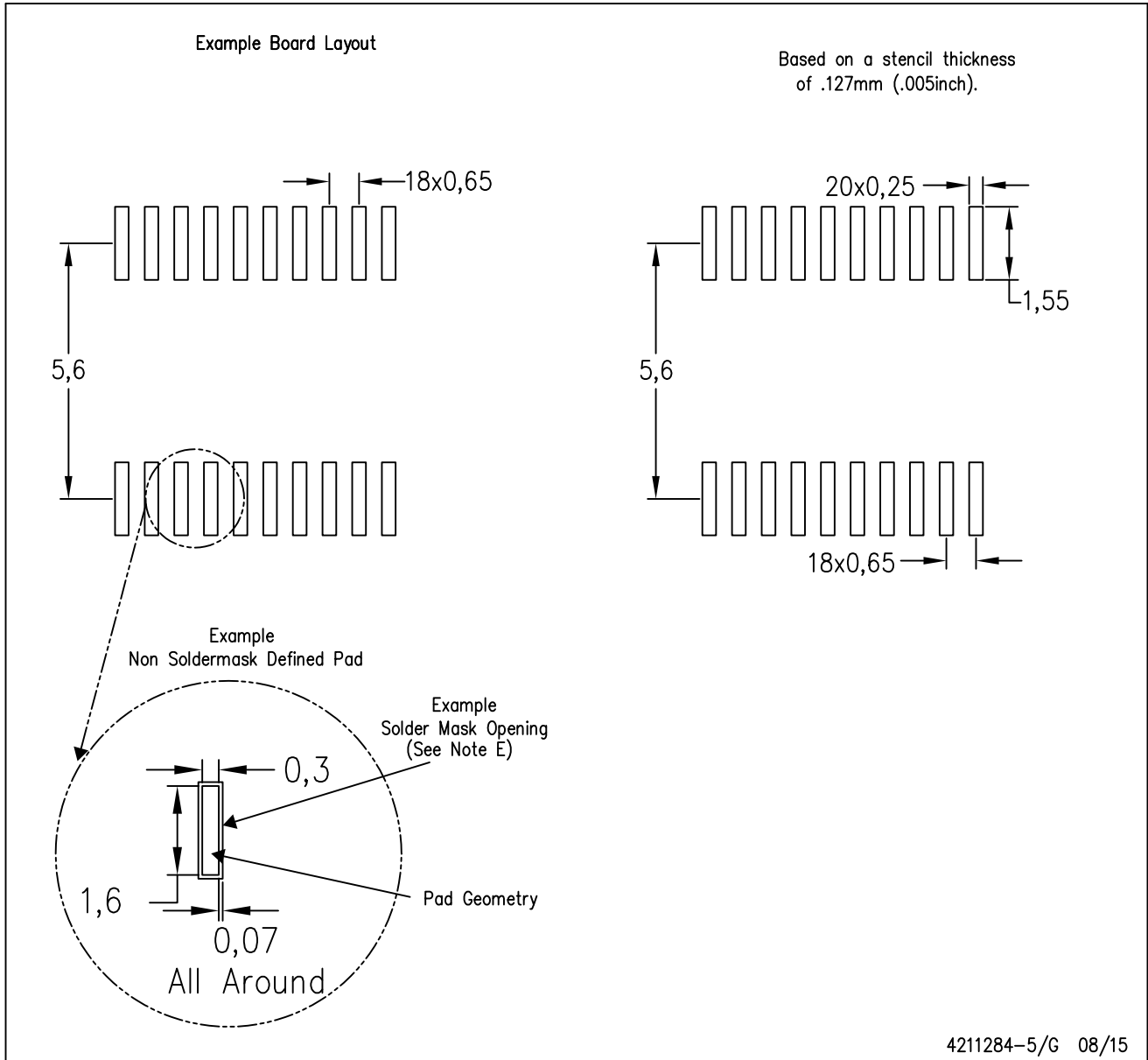


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

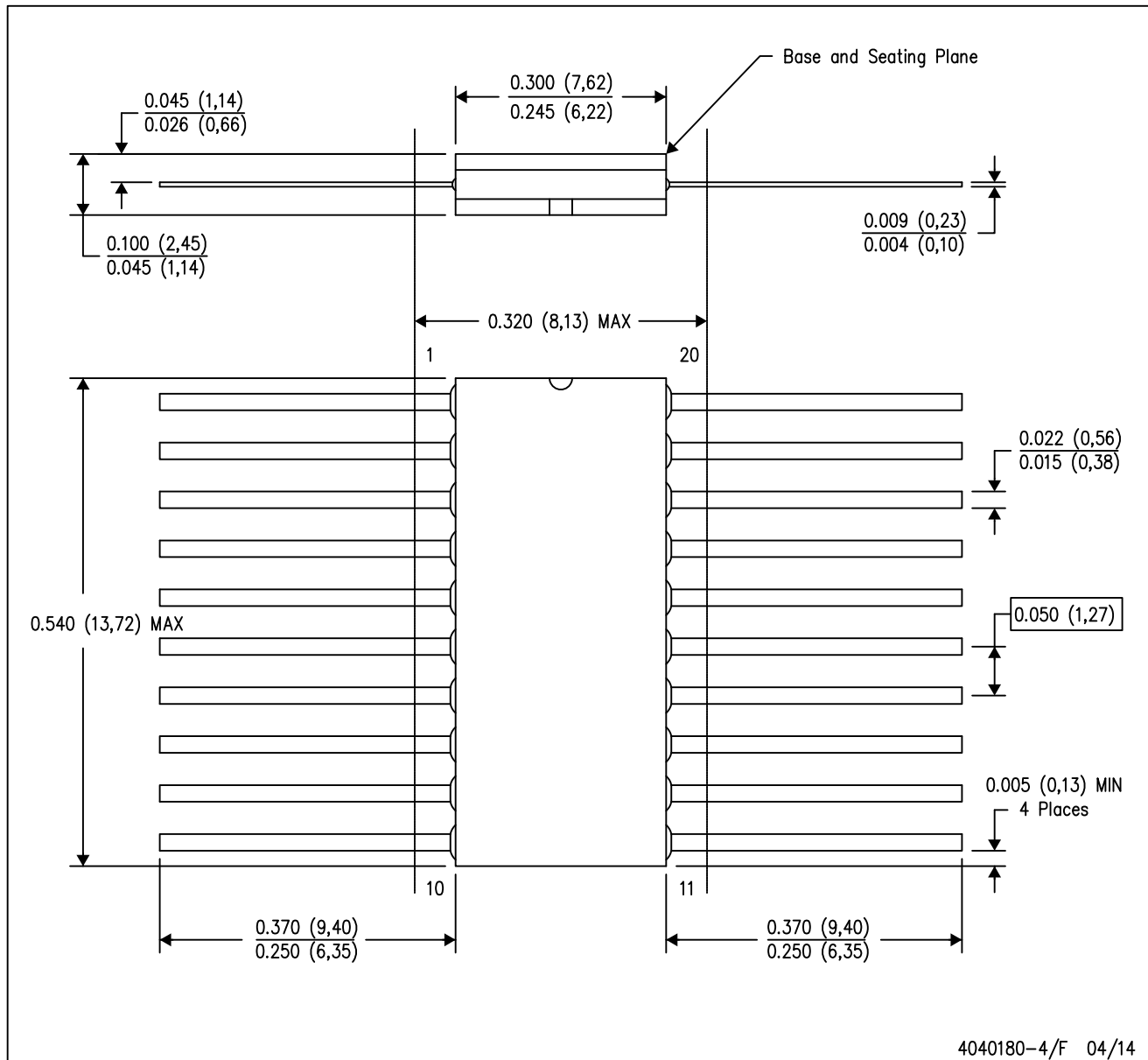
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

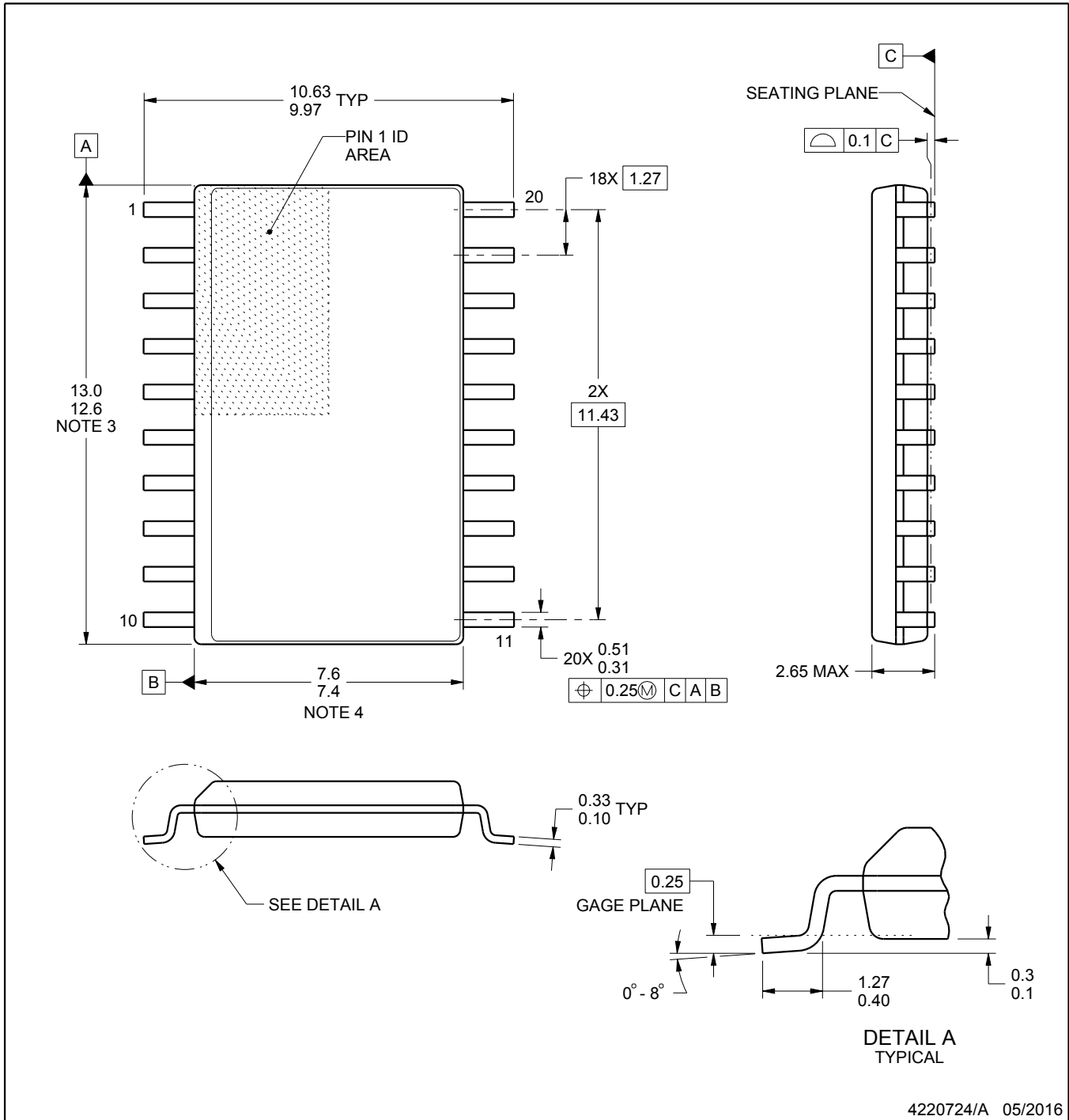
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

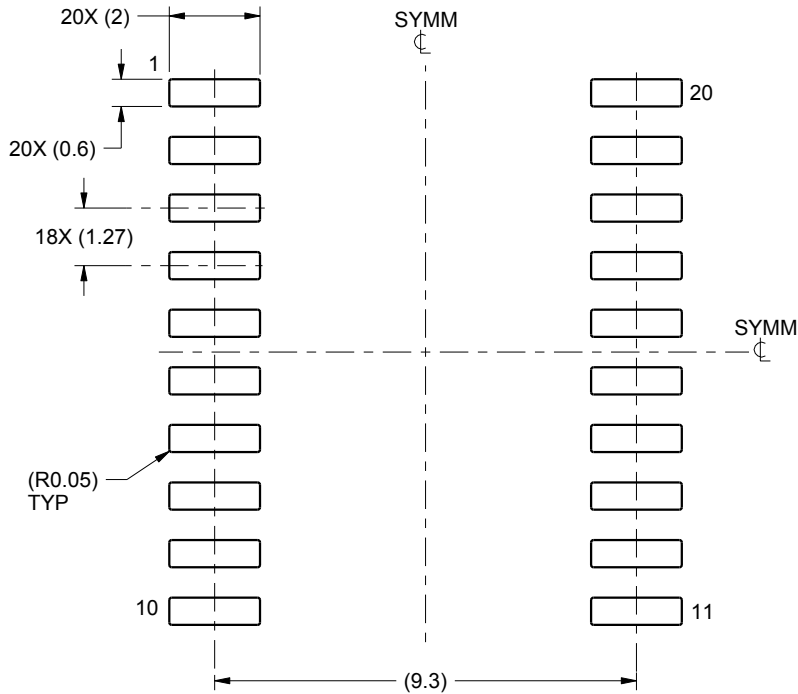
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

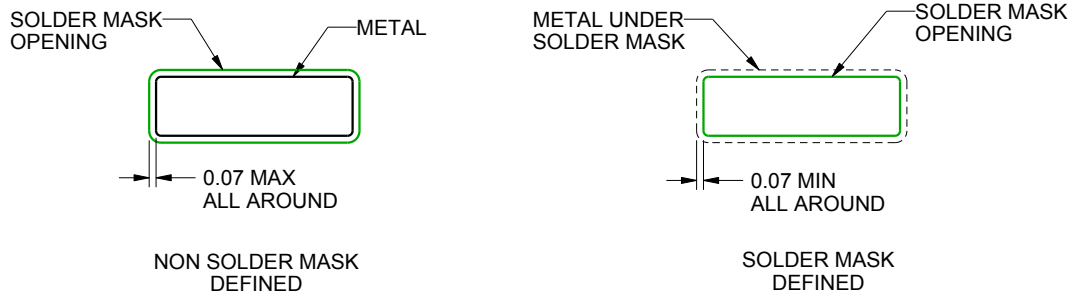
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

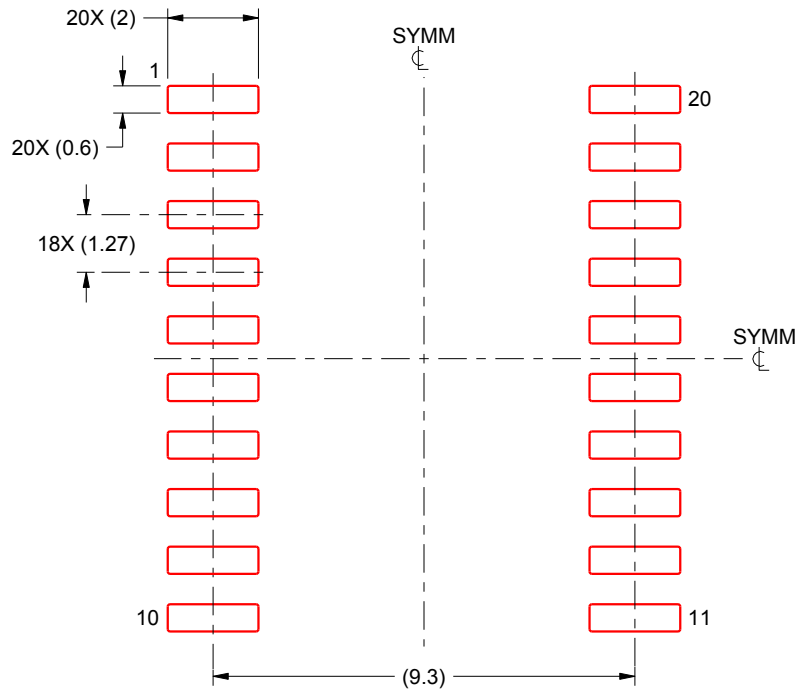
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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