Design Guide: TIDA-050061

Scalable, High-Current, Low-Noise Parallel LDO Reference Design

Description

This parallel LDO reference design showcases the TPS7A57 low-noise, low-dropout linear regulator (LDO) in a parallel configuration using ballast resistors, which is capable of sourcing 13.5 A. A high performance load transient circuit is included to assist the user with high-speed load transient testing. Low inductive current loops are integrative into the board to assist the user with input and output current measurements.

Resources

TIDA-050061	Design Folder
LMG1020	Product Folder
TPS7A57	Product Folder

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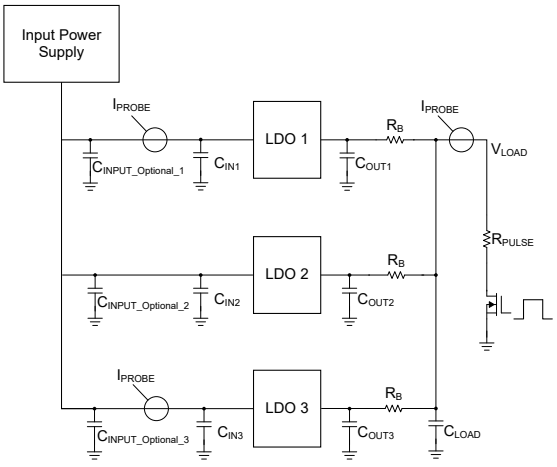
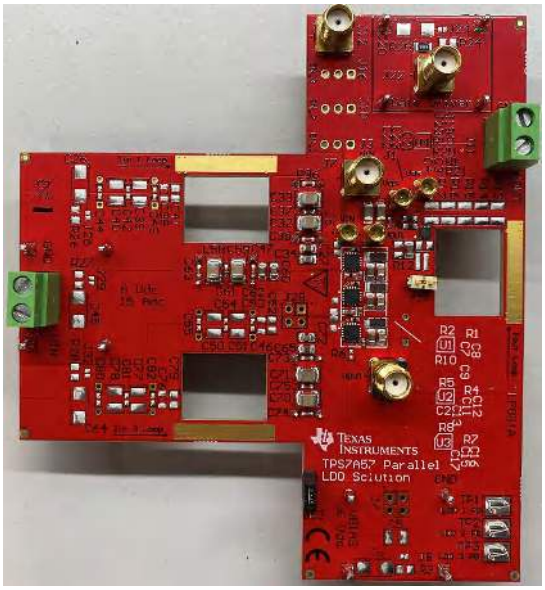
Features

- Small solution size: 174 mm^2 board area, 1.45 mm height
- Output Current: Up to 13.5 A
- Excellent Load Regulation: 1.15 mV / A
- Output voltage noise: 1.45 μV_{RMS}
- Superior load transient response: ±9 mV (10 A/µs ramp rates)
- Low offset voltage (±2 mV worst case) enables very small ballast resistor values

Applications

- Macro Remote Radio Units (RRU)
- Outdoor Backhaul Units
- Active Antenna System mMIMO (AAS)
- Ultrasound Scanners
- Lab and Field Instrumentation
- Sensor, Imaging, and Radar
- Seeker Front End





1 System Description

Low-noise low-dropout regulators (LDO) are required in many applications to ensure that power supply noise does not couple into the signal chain. The requirements for current continue to increase as new high-speed analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and clocking circuitry increase data speed and bandwidth. Transient performance must also improve to meet modern FPGA regulation band requirements. Using a single LDO for the supply is not always possible due to device availability and power dissipation limitations. The TIDA-050061 reference design solves this issue by using multiple LDOs configured to share current in parallel. The current sharing is achieved by using low-value ballast resistors, which can be designed as a discrete resistor or a copper trace on the printed-circuit board (PCB). The topology presented in this reference design can be expanded to include more LDOs if needed, there is no limit to the number of LDOs that can be placed in parallel.

This circuit uses the high-current LDO, TPS7A57, which is a 5-A device. The reference design is populated with three TPS7A57 devices and can provide up to 13.5 A of current using the 2.5 m-ohm ballast resistors. Low inductive current loops and a high speed load transient circuit are included to assist customer evaluation of the reference design.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input Power Rail	0.86 V (with Bias) or 1.1 V (without Bias) to 6 V
Bias Power Rail	3 V to 11 V
Maximum Output Current	13.5 A
V_{OUT} Transient Deviation, 0 A to 13.5 A to 0 A, 1 A/µs (Typical) (1)	± 2 mV_{PK}
V_{OUT} Transient Deviation, 0 A to 13.5 A to 0 A, 10 A/µs (Typical) (1)	± 9 mV_{PK}
V_{OUT} Transient Deviation, 0 A to 13.5 A to 0 A, 100 A/µs (Typical) (1)	+28 mV_{PK} / -19 mV_{PK}
V_{OUT} Transient Deviation, 0 A to 13.5 A to 0 A, 100 A/µs (Typical) (2)	+11 mV_{PK} / -8.5 mV_{PK}
Output Voltage Range	0.5 V to 5.2 V
Optimized for Output Voltage, V_{OUT}	0.75 V
Ballast Resistor	2.5 mΩ
Load Regulation	1.15 mV / A

1. Each TPS7A57 LDO has 22 µF // 2.2 µF ceramic capacitors on the OUT pin to GND, before the ballast resistor. There is one additional 22 µF ceramic capacitor after the 2.5 mΩ ballast resistors located near the load.
2. Each TPS7A57 LDO has 22 µF // 2.2 µF ceramic capacitors on the OUT pin to GND, before the ballast resistor. There are two additional 100 µF ceramic capacitors after the 2.5 mΩ ballast resistors located near the load.

2 System Overview

2.1 Block Diagram

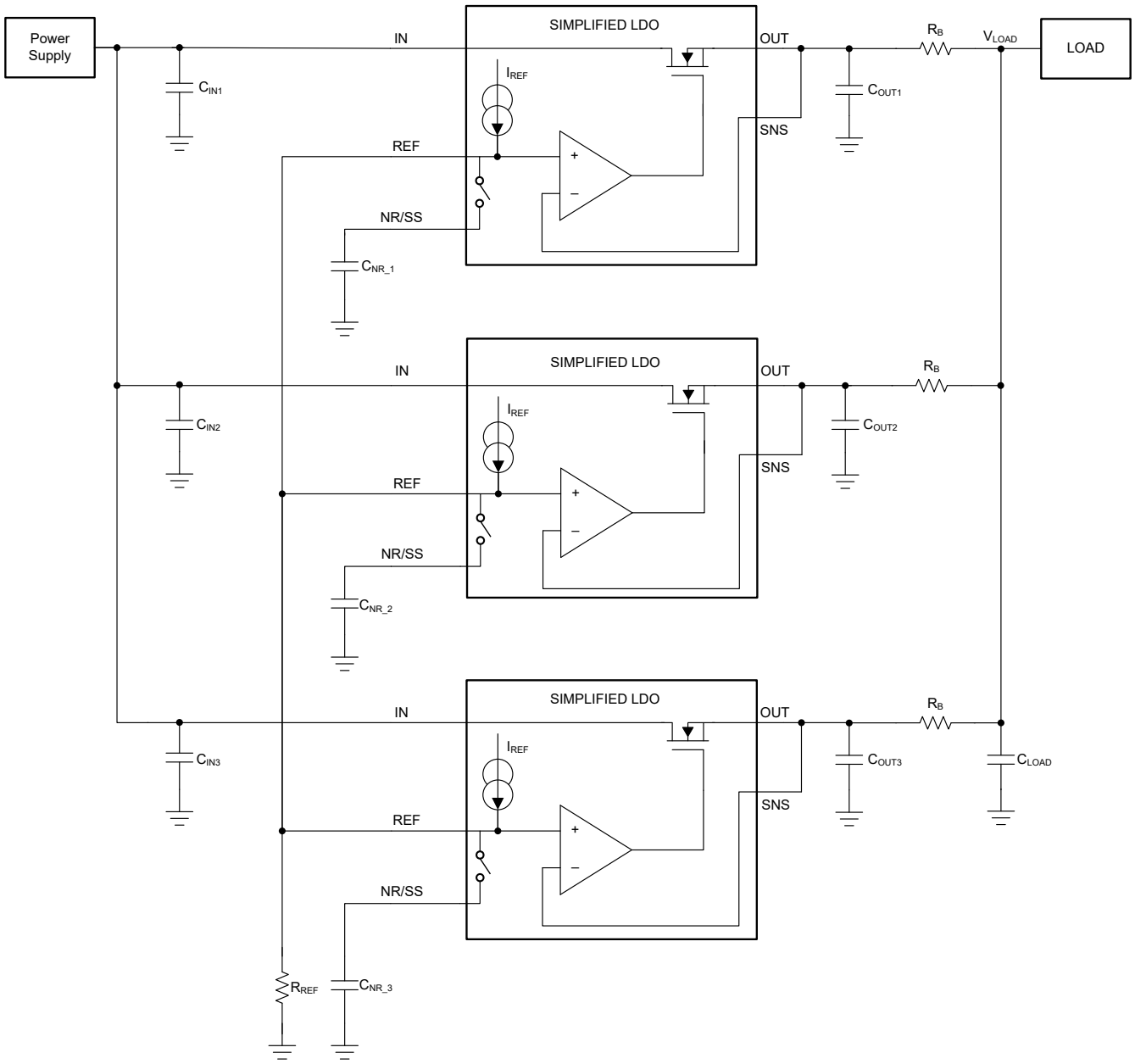


Figure 2-1. Block Diagram

2.2 Design Considerations

This reference design incorporates three high-speed, high-current LDO's. When the reference design output is loaded with a high current, fast ramp rate load step, charge is transferred from the input supply through the LDO to the output. This rapid transfer of charge from V_{IN} to V_{OUT} can cause a significant voltage drop at V_{IN} during the load transient. The LDO can momentarily enter dropout which will negatively affect the load transient performance. There are two common solutions:

1. Power V_{IN} with a high bandwidth power converter, such that V_{IN} is well regulated at all times.
2. Place a capacitor bank on V_{IN} to hold up the voltage during a large load step.

The design engineer needs to carefully evaluate their load transient requirements and design the supply providing V_{IN} accordingly to mitigate these concerns. This reference design has included a large capacitor bank to help with load transient evaluations using bench top power supplies. This capacitor bank might or might not be required in the final system based on the input power supplies performance.

2.3 Theory of Operation

This topology uses ballast resistors. Ballast resistors provide an easy way to connect multiple voltage sources together to supply power to a common load. It is critical to minimize the voltage difference at the output of each individual LDO. As LDO accuracy improves, the designer can reduce the size of the ballast resistor.

Each LDO has its own internal reference, which is slightly different than the other independent references. To achieve the smallest current sharing error between the different LDO's, this solution connects the current source reference's together through the REF pins. The remaining sources of error come from the ballast resistors, the internal output field-effect transistor (FET), and the amplifier. These errors show up as the offset voltage (V_{NR}-V_{OUT}) which itself is also a function of line and load. These sources of error make up the total error V_E of each LDO. In this reference design the ballast resistors are configured to be the same value for simplicity.

Traditionally the ballast resistance was chosen using Equation 1 to set the current imbalance I_{MAX} of the parallel LDO's. This formula does not account for the required load voltage, V_{LOAD}, which is also a requirement for most modern power supplies designed with parallel LDO's. Texas Instruments has modernized the design and analysis of parallel LDO's using ballast resistors (see references [4] and [6]) and a down-loadable software tool has been developed to design R_B for our LDO's and a set of system requirements (see reference [5]).

After R_B has been selected, by using Equation 1, Equation 2 can be used to assess the current out of each LDO. Equation 3 can be used to assess the V_{LOAD} of the system. For additional details on these equations, see reference [4]. Reference [5] can be used to quickly perform the calculations needed to select R_B for a specified load current and load voltage.

$$R_B = \frac{\underset{1<x<n}{max} V_{En} - \underset{1<x<n}{min} V_{En}}{\Delta I_{MAX}} \quad (1)$$

$$I_{OUTn} = \frac{I_{LOAD} - \left(\Sigma_{n=1}^{n} \frac{V_{En}}{R_B}\right)}{n} + \frac{V_{En}}{R_B} \quad (2)$$

$$V_{LOAD} = \frac{\Sigma_{n=1}^{n} \frac{V_{OUTn} + V_{En}}{R_{Bn}} - I_{LOAD}}{\Sigma_{n=1}^{n} \frac{1}{R_{Bn}}} \quad (3)$$

Where:

- V_{OUTn} is the nominal LDO output voltage
- V_{En} is the error of each LDO
- ΔI_{MAX} is the maximum current sharing imbalance between the parallel LDO's
- I_{OUTn} is the LDO output current
- R_B is the ballast resistance
- n is the number of parallel LDO's

In addition to I_{OUTn} and V_{LOAD}, other system requirements can require using a parallel LDO topology such as noise, PSRR, dropout and thermal limitations. In brief, parallel LDO's:

1. Reduce the system noise by the square root of the number of LDO's in parallel
2. Increase the system PSRR when compared with using a single LDO
3. Reduce the dropout requirement by spreading the load current across multiple LDO's
4. Decrease the junction temperature of the linear regulator by spreading the power dissipation across multiple LDO's

For a detailed discussion on all of these system requirements, how parallel LDO's can increase your performance, and how many parallel LDO's are needed for your system requirements, please see the references [4], [5], and [6].

Ballast resistors are typically employed as either a PCB trace or a discrete resistor. In general, PCB trace resistors favor applications which are low cost. PCB trace resistors also favor applications which operate in a narrow temperature range or experience very high temperatures. They are excellent choices where multiple low current devices are paralleled together (such as would be seen in high voltage LDO's which are usually limited in their available output currents). Discrete resistors favor applications which require maximum performance (where output voltage tolerance and transient responses are critical). Discrete resistors also favor applications where high current devices are being paralleled (such as low voltage LDO's where high current devices are readily available). Designing with a discrete ballast resistor becomes challenging when ambient temperatures exceed 125°C, and it is difficult to use discrete ballast resistors above 150°C. For a detailed discussion on ballast resistor analysis and design, see reference [4]

Table 2-1. PCB Trace Resistor vs. Discrete Resistor Summary

Ballast Resistor Option	Cost	Tolerance	Parasitic Inductance	High Temperature Operation
PCB Trace Resistor	*Free* after the PCB trace resistor design is complete.	Large: Resistor value nearly doubles across the operating temperature range.	Increases with PCB trace length	Only limited by the Tg of the FR4
Discrete Resistor	Must be sourced, purchased and installed on each PCB.	Low: discrete resistors come in 100 ppm or lower tolerances	Low	Large package sizes (0805 or 1206) can be required at higher temperatures.

2.4 Highlighted Products

2.4.1 TPS7A57 Low Dropout (LDO) Regulator

The TPS7A57 is a low-noise (2.1 µVRMS), ultra-low-dropout linear regulator (LDO) capable of sourcing 5 A with only 100 mV of maximum dropout. Moreover, the dropout is independent of the output voltage when using the internal charge pump. The device output voltage is adjustable from 0.4 V to 5.1 V using a single external resistor. The combination of low noise (2.1 µVRMS), high PSRR (45 dB at 1 MHz), and high output-current capability makes the TPS7A57 an excellent choice to power noise sensitive components such as those found in radar power, communication and imaging applications. The high performance of this device limits power-supply generated phase noise and clock jitter, making this device ideal for power RF amplifiers, radar sensors, and chipsets. Specifically, RF amplifiers benefit from the high performance and 5.0-V output capability of the device. For digital loads [such as application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs)] requiring low-input voltage, low-output (LILO) voltage operation, the exceptional accuracy (1% over load, line and temperature), remote sensing, excellent transient performance, and soft-start capabilities of the TPS7A57 provides optimal system performance. As an adjustable voltage regulator, there is versatility in design of the TPS7A57 that makes the device a component of choice for analog loads such as voltage-controlled oscillator (VCO), analog-to-digital converter (ADC), digital-to-analog converter (DAC), and imaging sensors and for digital loads such as serializer/deserializer (SerDes), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs).

2.4.2 LMG1020 Low Side Driver

The LMG1020 device is a single, low-side driver designed for driving GaN FETs and logic-level MOSFETs in high-speed applications including LiDAR, time-of-flight, facial recognition, and any power converters involving low side drivers. The design simplicity of the LMG1020 enables extremely fast propagation delays of 2.5 nanoseconds and minimum pulse width of 1 nanosecond. The drive strength is independently adjustable for the pull-up and pull-down edges by connecting external resistors between the gate and OUTH and OUTL, respectively.

The driver features undervoltage lockout (UVLO) and over-temperature protection (OTP) in the event of overload or fault conditions.

0.8-mm × 1.2-mm WCSP package of LMG1020 minimizes gate loop inductance and maximizes power density in high-frequency applications.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

3.2 Test Setup

The TPS7A57EVM-081 reference design contains three parallel TPS7A57 LDO's with input, bias, NR/SS, and output capacitors installed, as well as PG and REF resistors installed. These components provide an implementation example, as illustrated by the white boxes in Figure 3-1. The prepopulated capacitors are sized to ensure the minimum capacitance requirements are maintained under all normal operating conditions. Optional pads are available to test the LDO with additional input, bias, and output capacitors beyond what is already installed on the EVM.

The TPS7A57EVM-081 is assembled for an output voltage of 0.75 V. For other voltage options, resistor R10 can be modified as necessary. See the *Paralleling for Higher Output Current and Lower Noise* section in the TPS7A57 data sheet for guidance on selecting R10 for alternate values of VOUT.

The TPS7A57 LDO can be enabled or disabled by using the J12 SMA connector:

- Tie the center pin of the SMA connector to a voltage source greater than 0.68 V and no greater than 6.5 V to enable the device
- Tie the center pin of the SMA connector to a voltage source less than 0.62 V to disable the device

Alternatively, by connecting an external function generator to TP1 (EN) and a nearby GND post (J17), the user can enable or disable the TPS7A57 LDO. If desired the user can populate the optional 3-pin headers J16, J10 and J3 to enable the parallel LDO's.

If desired, current probes can be inserted in the EVM as shown in Figure 3-1 to measure the input and output current. The slots were sized to fit most current probes, such as the LeCroy™ AP015 or CP031 current probes. The input current of two LDOs (the top and bottom LDOs) and the output current of all three LDOs can be measured directly using the current probes. To measure the current of the third (middle) LDO, subtract the top and bottom LDO current from the output current of all three LDOs:

$$I_{OUT2} = I_{LOAD} - I_{OUT1} - I_{OUT3} \quad (4)$$

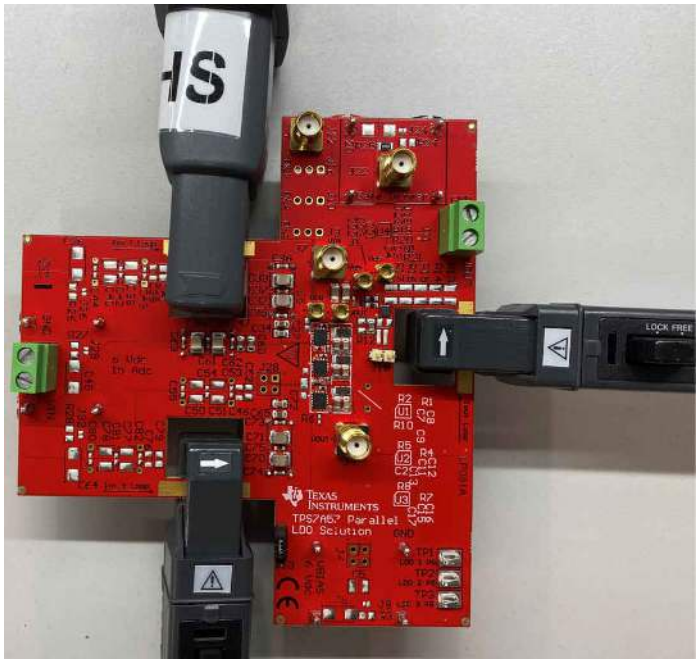


Figure 3-1. TPS7A57EVM-081 With Current Probes Attached

J11 can be used to place a DC load that flows through the current sense path on the output of the LDO. In cases where very fast transient tests are performed, ringing can occur on VIN or VOUT as a result of the PCB parasitic inductance. Placing a strip of wire on the exposed copper in the current path can reduce this ringing. 10 AWG wire can be used as needed. If ringing persists, install damping networks by adding a series resistor and capacitor in parallel with VIN. Locations where damping can be installed include C6 and R3, C20 and R24, C26 and R26, C45 and R27, and C64 and R28.

WARNING

Some current probe sensors can be tied to GND and must not come into contact with energized conductors. See the user manual of your current probe for details. If your current probe has this limitation, use a thin strip of electrical or Kapton® tape to isolate the current sense path from the current probe.

Optional kelvin sense points are provided using the SMA connectors J7 (VIN) and J4 (VOUT) and MMCX connectors J5 (VIN) and J1 (VOUT).

3.2.1 Optional Load Transient Circuit Operation

The TPS7A57EVM-081 reference design contains an optional high-performance load transient circuit to allow efficient testing of the parallel TPS7A57 LDO's load transient performance. To use the optional load transient circuit, install the correct components in accordance with the application. Modify the input and output capacitance connected to the parallel TPS7A57 LDO's to match the expected operating conditions. Determine the desired peak current to test, and modify the parallel resistor combination of R13, R14, R15, R16, and R17 as shown:

$$I_{Peak} = \frac{V_{OUT}}{R_{13}||R_{14}||R_{15}||R_{16}||R_{17}} \quad (5)$$

The slew rate of the load step can be adjusted by C19, R18, R19, and R20. In this section, only R19 and R20 are adjusted to set the slew rate. For a 0-mA to 13.5-A to 0-mA load step, use Table 3-1 to select a value of R19 and R20 that results in the desired rise or fall time.

Table 3-1. Suggested Ramp Rate Resistor Values

R19	R20	Rise, Fall Time
20 kΩ	32.4 kΩ	16.9 µs
15.8 kΩ	25.5 kΩ	13.5 µs
10 kΩ	16.2 kΩ	8.45 µs
4.99 kΩ	8.45 kΩ	4.25 µs
1.5 kΩ	2.61 kΩ	1.35 µs

After the EVM is modified (if needed), connect a power supply to banana connectors J21 (VDD) and J25 (GND) with a 5-V DC supply and a 1-A DC current limit. As illustrated in Section 3.3.3, the parallel TPS7A57 reference design transient response is very fast and the output voltage recovers in well under 1 ms after the initial load transient. Use a pulse-duration limit of 1 ms to prevent excessive heating of the pulsed resistors (R13, R14, R15, R16, and R17). Configure a function generator for the 50-Ω output, in a 0-V DC to 5-V DC square pulse. If necessary, burst mode can be configured in the function generator for repetitive, low duty cycle, load transient testing.

A 20-kΩ resistor is installed on the EVM at R19, and a 20-kΩ resistor is installed on the EVM at R20. These resistors provide approximately 0.75-A/µs slew rate from 0 mA to 13.5 A, and 1.3-A/µs slew rate from 13.5 A to 0 mA.

3.3 Test Results

V_{CP_EN}=GND, V_{IN}=1.25 V, V_{OUT}= 0.75 V, R_B= 2.5 m-ohm, $C_{NR/SS}$ = 1 µF, C_{OUTn} = 22 µF // 2.2 µF, C_{LOAD} = 22 µF, V_{BIAS} = 5 V (unless otherwise noted)

3.3.1 Current Sharing

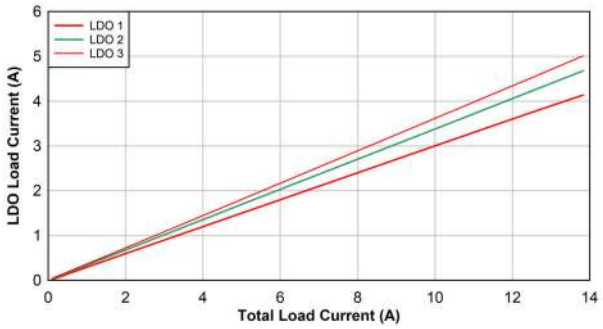


Figure 3-2. Individual LDO Load Current vs. Total Load Current

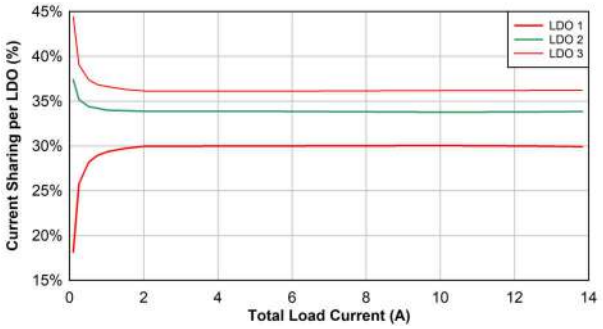


Figure 3-3. Individual LDO Current as a Percentage of the Total Load Current

3.3.2 V_{LOAD} vs I_{LOAD}

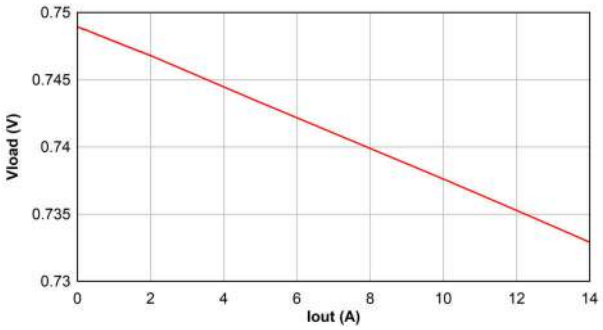
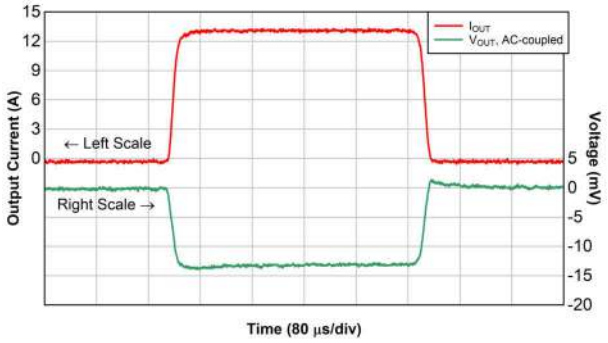


Figure 3-4. Load Voltage vs. Total Load Current

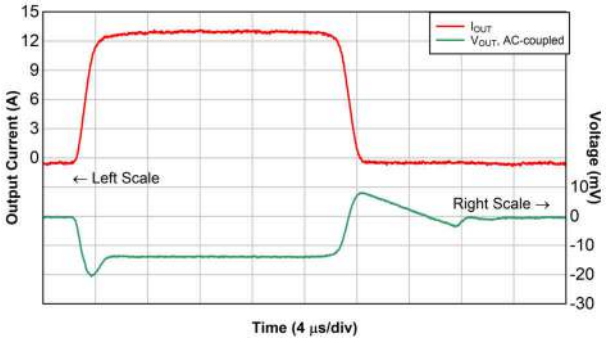
3.3.3 Load Transient Response

All load transient test data is captured from 0 A to 13.5 A and back to 0 A load (unless otherwise noted).



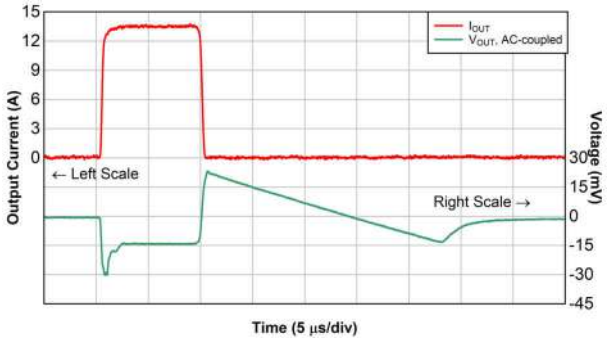
V_{IN}= 1.3 V, SR = 1 A/µs

Figure 3-5. 13.5 A Load Transient, 1 A/µs Slew Rate



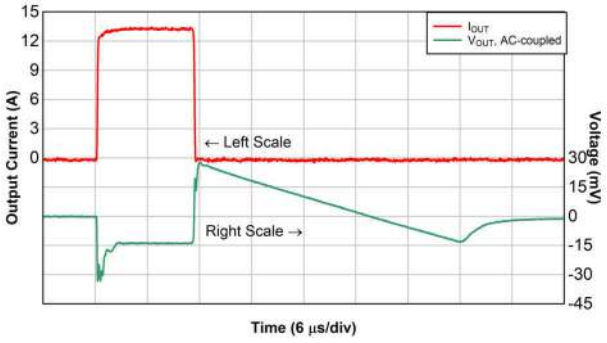
V_{IN}= 1.3 V, SR = 10 A/µs

Figure 3-6. 13.5 A Load Transient, 10 A/µs Slew Rate



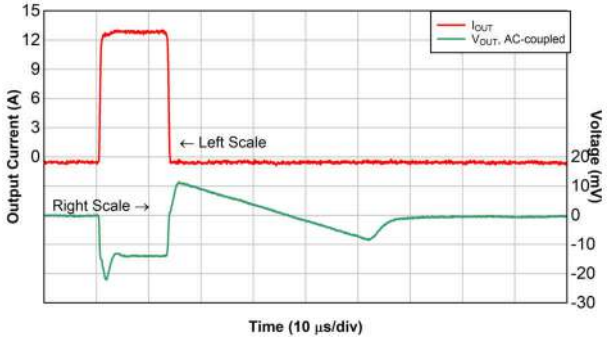
V_{IN}= 1.3 V, SR = 35 A/µs

Figure 3-7. 13.5 A Load Transient, 35 A/µs Slew Rate



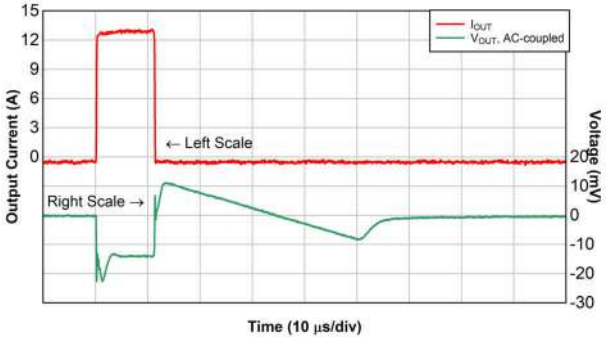
V_{IN}= 1.3 V, SR = 100 A/µs

Figure 3-8. 13.5 A Load Transient, 100 A/µs Slew Rate



C_{LOAD} = 100 µF // 100 µF, V_{IN}= 1.3 V, SR = 35 A/µs

Figure 3-9. 13.5 A Load Transient with 200 µF C_{LOAD}, 35 A/µs Slew Rate



C_{LOAD} = 100 µF // 100 µF, V_{IN}= 1.3 V, SR = 100 A/µs

Figure 3-10. 13.5 A Load Transient with 200 µF C_{LOAD}, 100 A/µs Slew Rate

3.3.4 Current Limit

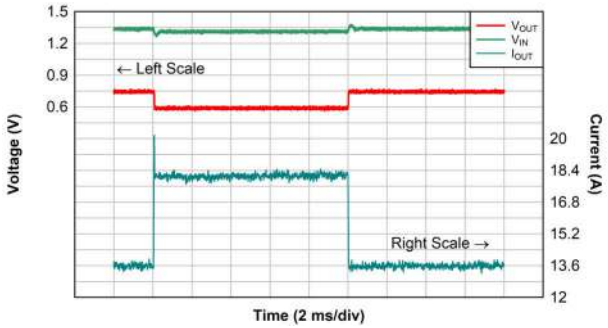


Figure 3-11. Current Limit, 13.5 A to 23.5 A to 13.5 A Step

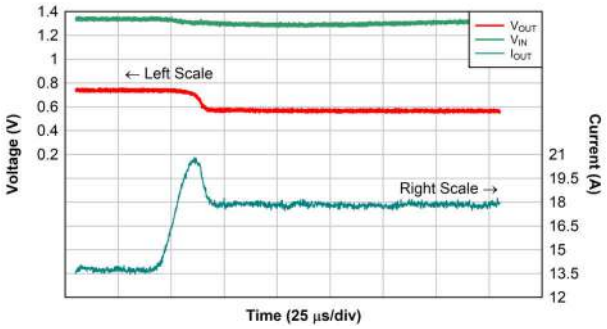
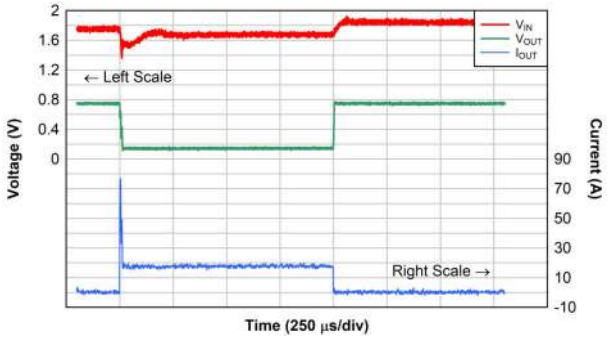
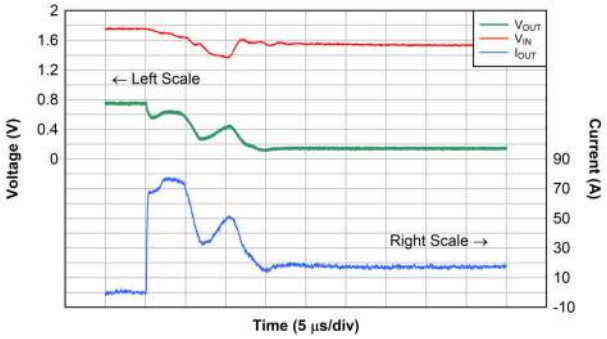


Figure 3-12. Zoomed in Current Limit Response, 13.5 A to 23.5 A Step



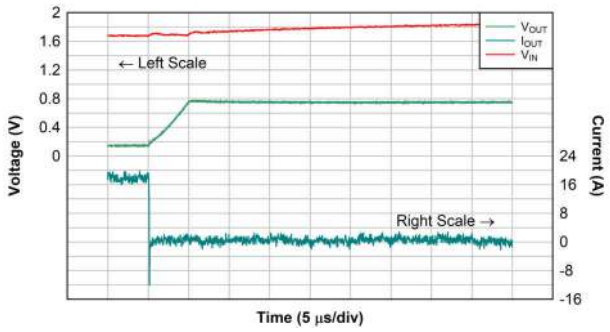
R_{PULSED_LOAD} = 10 m-ohm

Figure 3-13. Short Circuit Current Limit



R_{PULSED_LOAD} = 10 m-ohm

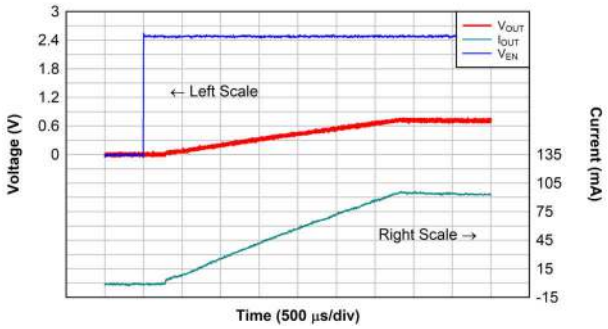
Figure 3-14. Zoomed In Current Limit Response Entering Short Circuit



R_{PULSED_LOAD} = 10 m-ohm

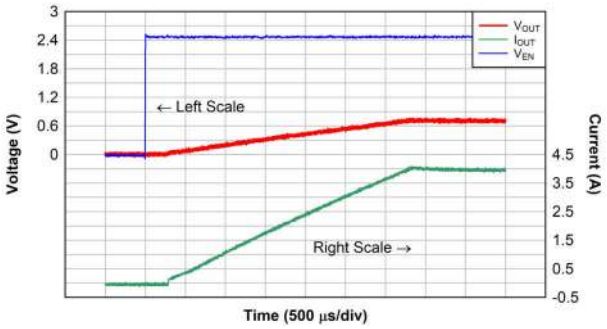
Figure 3-15. Zoomed in Current Limit Response Exiting Short Circuit

3.3.5 Startup



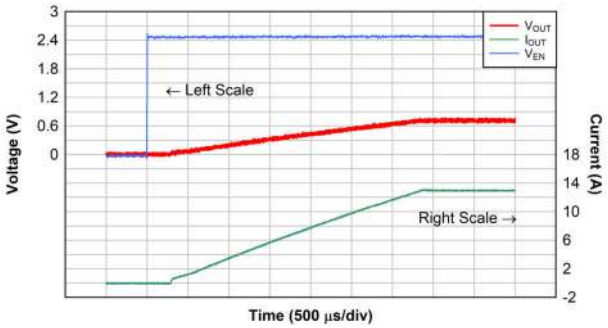
V_{IN}= 1.3 V, I_{OUT} = 100 mA

Figure 3-16. Startup Into a 100 mA Load



V_{IN}= 1.3 V, I_{OUT} = 4 A

Figure 3-17. Startup Into a 4 A Load



V_{IN}= 1.3 V, I_{OUT} = 13.5 A

Figure 3-18. Startup Into a 13.5 A Load

3.3.6 Noise

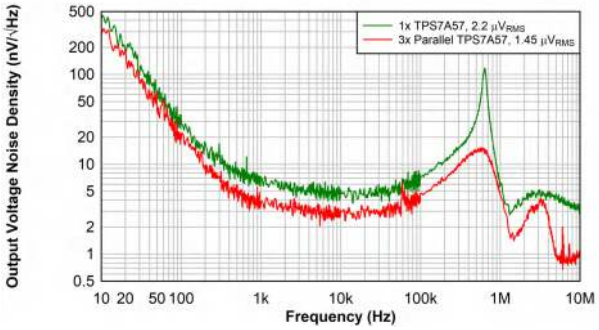
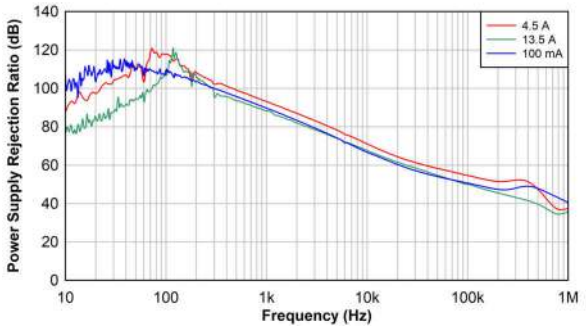


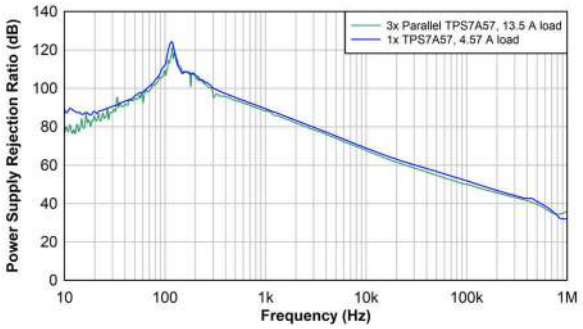
Figure 3-19. Output Voltage Noise Density vs. Frequency

3.3.7 PSRR



V_{IN}= 1.05 V

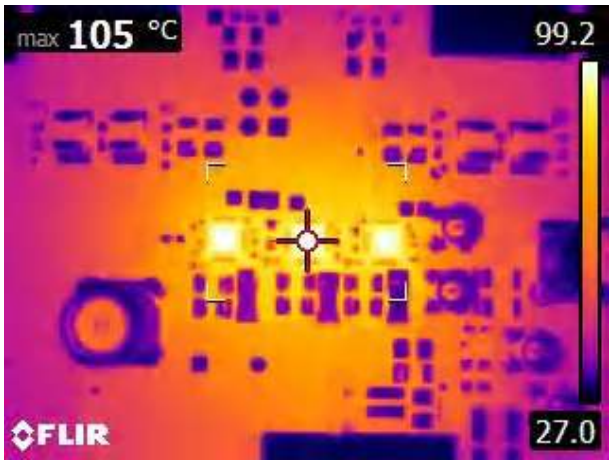
Figure 3-20. 3x LDOs in Parallel: PSRR vs. Frequency and I_{OUT}



V_{IN}= 1.05 V

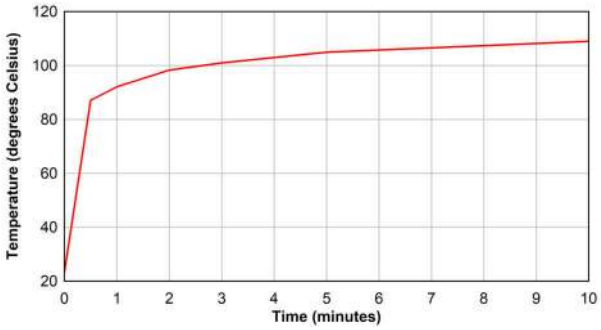
Figure 3-21. PSRR vs. Frequency and I_{OUT} for 3x Parallel TPS7A57 and 1x Single TPS7A57

3.3.8 Thermal



I_{LOAD} = 13.5 A

Figure 3-22. Thermal Image of the Parallel TPS7A57 LDO's (Load Applied for 5 Minutes)

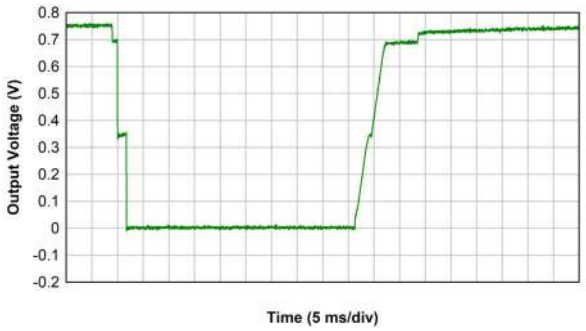


I_{LOAD} = 13.5 A

Figure 3-23. Maximum Hot Spot Measurement across Time

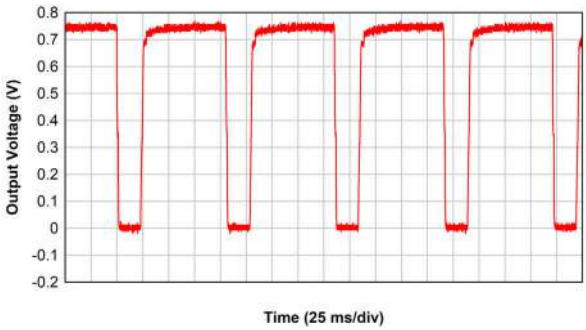
3.3.9 Thermal Limit Protection

The thermal protection performance of the parallel LDOs exhibits a staircase effect on V_{LOAD} during turn off and turn on as each LDO enters and exits thermal shutdown. Thermal protection is repeatedly engaged until the power dissipation from the parallel LDOs is removed. Figure 3-25 demonstrates the desired effect of the thermal protection circuitry in the presence of heavy power dissipation across the LDOs. The parallel LDOs require 12.5 W dissipation in this reference design to enter thermal shutdown when operated from room temperature.



V_{IN}= 1.9 V, I_{LOAD} = 13.5 A

Figure 3-24. Zoomed in Thermal Shutdown Response



V_{IN}= 2 V, I_{LOAD} = 13.5 A

Figure 3-25. Thermal Shutdown Response Protecting the LDOs

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050061.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050061.

4.2 Tools

Tools

Parallel LDOs Using Ballast Resistors Calculator	Easily calculate the minimum number of parallel LDOs required to meet a set of system requirements (temperature, V_{IN}, V_{OUT}, I_{LOAD}, Load Regulation, and noise).

4.3 Documentation Support

1. IPC-2221B, Generic Standard on Printed Board Design.
2. Texas Instruments, *TPS7A57 5-A, Low-VIN (0.7 V), Low-Noise, High-Accuracy, Ultra-Low Dropout (LDO) Voltage Regulator*, data sheet.
3. Texas Instruments, *LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-ns Pulse Width Applications*, data sheet.
4. Texas Instruments, *Comprehensive Analysis and Universal Equations for Parallel LDO's Using Ballast Resistors* white paper.
5. Texas Instruments, *Parallel Low-Dropout (LDO) Calculator*
6. Texas Instruments, *Parallel LDO Architecture Design Using Ballast Resistors* white paper
7. Texas Instruments, *Using New Thermal Metrics*, application note.

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

Stephen Ziel joined Texas Instruments in 2019 as a senior applications engineer in the LDO product line. Previously Stephen was a principal engineer at a large aerospace and defense company where he worked on all aspects of power electronics spanning 1 mW to 1.5 kW. Stephen holds over 15 years experience in power system requirements development and architecture design, power supply design, and engineering management leading large teams of power engineers. Stephen received a BSEE and MSEE from Michigan State University.

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