MSP430F2132-EP Mixed Signal Microcontroller

1 Features

- Low Supply Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Active Mode: 250 µA at 1 MHz, 2.2 V
  - Standby Mode: 0.7 µA
  - Off Mode (RAM Retention): 0.1 µA
- Ultra-Fast Wake-Up From Standby Mode in Less Than 1 µs
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Basic Clock Module Configurations
  - Internal Frequencies up to 16 MHz With Four Calibrated Frequencies to ±1%
  - Internal Very-Low-Power Low-Frequency Oscillator
  - 32-kHz Crystal (1)
  - High-Frequency (HF) Crystal up to 16 MHz
  - Resonator
  - External Digital Clock Source
  - External Resistor
- 16-Bit Timer0_A3 With Three Capture/Compare Registers
- 16-Bit Timer1_A2 With Two Capture/Compare Registers
- On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion
- 10-Bit 200-ksps A/D Converter With Internal Reference, Sample-and-Hold, Autoscan, and Data Transfer Controller
- Universal Serial Communication Interface
  - Enhanced UART Supporting Auto-Baudrate Detection (LIN)
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I^2C™
- Brownout Detector
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- Bootstrap Loader
- On-Chip Emulation Module
- 8KB + 256B Flash Memory
- 512B RAM
- Available in a 32-Pin QFN (RHB) Package
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide*, Literature Number SLAU144

(1) Crystal oscillator cannot be operated beyond 105°C.

2 Applications

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Extended (–40°C to 125°C) Temperature Range (2)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

(2) Custom temperature ranges available

3 Description

The MSP430F2132 is an ultra-low-power microcontroller. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

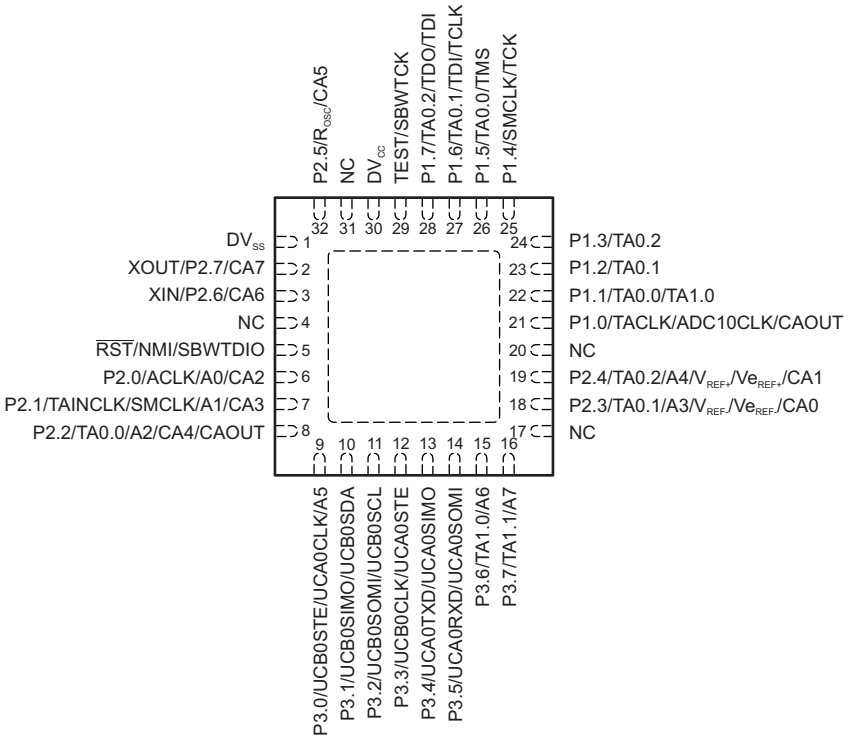
The MSP430F2132 has two built-in 16-bit timers, a fast 10-bit A/D converter with integrated reference and a data transfer controller (DTC), a comparator, built-in communication capability using the universal serial communication interface, and up to 24 I/O pins.

3.1 Development Tool Support

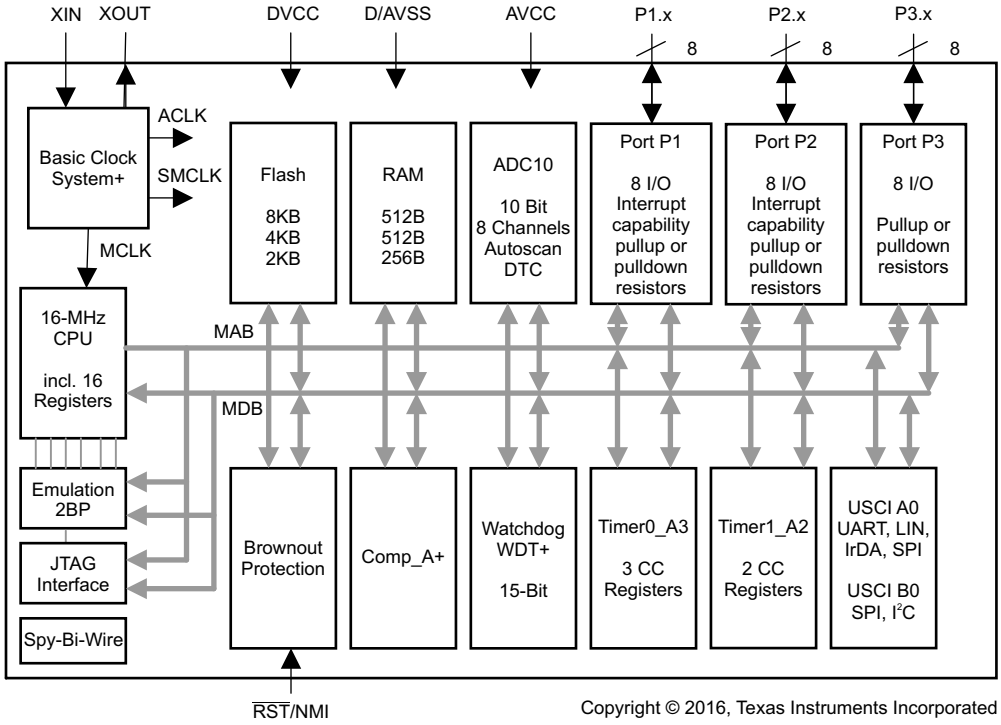
All MSP430 microcontrollers include an Embedded Emulation Module (EEM) that allows advanced debugging and programming through easy-to-use development tools. Recommended hardware options include:

- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP-FET430U28 (PW package)
- Production Programmer
  - MSP-GANG430

3.2 Device Pinout, RHB Package



3.3 Functional Block Diagram



Functional Block Diagram (continued)

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
P1.0/TACLK/ADC10CLK/CAOUT	21	I/O	General-purpose digital I/O pin Timer0_A3, clock signal TACLK input Timer1_A2, clock signal TACLK input ADC10, conversion clock Comparator_A+ output
P1.1/TA0.0/TA1.0	22	I/O	General-purpose digital I/O pin Timer0_A3, capture: CCI0A input, compare: Out0 Output Timer1_A2, capture: CCI0A input
P1.2/TA0.1	23	I/O	General-purpose digital I/O pin Timer0_A3, capture: CCI1A input, compare: Out1 Output
P1.3/TA0.2	24	I/O	General-purpose digital I/O pin Timer0_A3, capture: CCI2A input, compare: Out2 Output
P1.4/SMCLK/TCK	25	I/O	General-purpose digital I/O pin SMCLK signal output Test Clock input for device programming and test
P1.5/TA0.0/TMS	26	I/O	General-purpose digital I/O pin Timer0_A3, compare: Out0 Output JTAG test mode select, input terminal for device programming and test
P1.6/TA0.1/TDI/TCLK	27	I/O	General-purpose digital I/O pin Timer0_A3, compare: Out1 Output JTAG test data input or test clock input in programming an test
P1.7/TA0.2/TDO/TDI	28	I/O	General-purpose digital I/O pin Timer0_A3, compare: Out2 Output JTAG test data output terminal or test data input in programming an test
P2.0/ACLK/A0/CA2	6	I/O	General-purpose digital I/O pin ACLK signal output ADC10 analog input A0 Comparator_A+ input
P2.1/TAINCLK/SMCLK/A1/CA3	7	I/O	General-purpose digital I/O pin SMCLK signal output Timer0_A3, clock signal TACLK input Timer1_A2, clock signal TACLK input ADC10 analog input A1 Comparator_A+ input
P2.2/TA0.0/A2/CA4/CAOUT	8	I/O	General-purpose digital I/O pin Timer0_A3, capture: CCI0B input, compare: Out0 Output ADC10 analog input A2 Comparator_A+ input Comparator_A+ output
P2.3/TA0.1/A3/V_{REF-}/Ve_{REF-}/CA0	18	I/O	General-purpose digital I/O pin Timer0_A3, compare: Out1 Output ADC10 analog input A3 / negative reference Comparator_A+ input

Functional Block Diagram (continued)

Terminal Functions (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
P2.4/TA0.2/A4/V_{REF+}/Ve_{REF+}/CA1	19	I/O	General-purpose digital I/O pin Timer0_A3, compare: Out2 Output ADC10 analog input A4 / positive reference Comparator_A+ input
XIN/P2.6/CA6	3	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Comparator_A+ input
XOUT/P2.7/CA7	2	I/O	Output terminal of crystal oscillator General-purpose digital I/O pin Comparator_A+ input
P3.0/UCB0STE/UCA0CLK/A5	9	I/O	General-purpose digital I/O pin USCI_B0 slave transmit enable/USCI_A0 clock input/output ADC10 analog input A5
P3.1/UCB0SIMO/UCB0SDA	10	I/O	General-purpose digital I/O pin USCI_B0 slave in/master out (SPI mode), SDA I2C data (I2C mode)
P3.2/UCB0SOMI/UCB0SCL	11	I/O	General-purpose digital I/O pin USCI_B0 slave out/master in (SPI mode), SCL I2C clock (I2C mode)
P3.3/UCB0CLK/UCA0STE	12	I/O	General-purpose digital I/O USCI_B0 clock input/output, USCI_A0 slave transmit enable
P3.4/UCA0TXD/UCA0SIMO	13	I/O	General-purpose digital I/O pin USCI_A0 transmit data output in UART mode, slave data in/master out in SPI mode
P3.5/UCA0RXD/UCA0SOMI	14	I/O	General-purpose digital I/O pin USCI_A0 receive data input (UART mode), slave data out/master in (SPI mode)
P3.6/TA1.0/A6	15	I/O	General-purpose digital I/O pin Timer1_A2, capture: CCI0B input, compare: Out0 Output ADC10 analog input A6
P3.7/TA1.1/A7	16	I/O	General-purpose digital I/O pin Timer1_A2, capture: CCI1A input, compare: Out1 Output ADC10 analog input A7
$\overline{RST}$/NMI/SBWTDIO	5	I	Reset or nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/SBWTCK	29	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST.
P2.5/R_{OSC}/CA5	32	I/O	General-purpose digital I/O pin Input for external resistor defining the DCO nominal frequency Comparator_A+ input
DV_{CC}	30		Digital supply voltage
DV_{SS}	1		Digital supply voltage
NC	4, 17, 20, 31		Not connected internally. Connection to V_{SS} is recommended.
QFN Pad	Pad		QFN package pad (RHB, RTV packages). Connection to DV_{SS} is recommended.

4 Short-Form Description

4.1 CPU

The MSP430F2132 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses and can be handled with all instructions.

4.2 Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; Table 2 shows the address modes.

Table 1. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional or conditional	JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S(1)	D(2)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source
(2) D = destination

4.3 Operating Modes

The MSP430F2132 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active.
- Low-power mode 0 (LPM0)
  - CPU is disabled.
  - ACLK and SMCLK remain active. MCLK is disabled.
- Low-power mode 1 (LPM1)
  - CPU is disabled ACLK and SMCLK remain active. MCLK is disabled.
  - DCO dc-generator is disabled if DCO not used in active mode.
- Low-power mode 2 (LPM2)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator remains enabled.
  - ACLK remains active.
- Low-power mode 3 (LPM3)
  - CPU is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator is disabled.
  - ACLK remains active.
- Low-power mode 4 (LPM4)
  - CPU is disabled.
  - ACLK is disabled.
  - MCLK and SMCLK are disabled.
  - DCO dc-generator is disabled.
  - Crystal oscillator is stopped.

4.4 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0xFFFE) contains 0xFFFF (for example, if flash is not programmed), the CPU goes into LPM4 immediately after power up.

Table 3. Interrupt Vector Addresses

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash key violation PC out of range(2)	PORIFG RSTIFG WDTIFG KEYV(1)	Reset	0xFFFE	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(1)(3)	(Non)maskable (Non)maskable (Non)maskable	0xFFFC	30
Timer1_A2	TA1CCR0 CCIFG(4)	Maskable	0xFFFA	29
Timer1_A2	TA1CCR1 CCIFG, TA1CTL TAIFG(1)(4)	Maskable	0xFFF8	28
Comparator_A+	CAIFG	Maskable	0xFFF6	27
Watchdog timer	WDTIFG	Maskable	0xFFF4	26
Timer0_A3	TA0CCR0 CCIFG(4)	Maskable	0xFFF2	25
Timer0_A3	TA0CCR1 CCIFG, TA0CCR2 CCIFG, TA0CTL TAIFG(1)(4)	Maskable	0xFFF0	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(1)(5)	Maskable	0xFFEE	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(1)(6)	Maskable	0xFFEC	22
ADC10	ADC10IFG(4)	Maskable	0xFFEA	21
			0xFFE8	20
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7(1)(4)	Maskable	0xFFE6	19
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7(1)(4)	Maskable	0xFFE4	18
			0xFFE2	17
			0xFFE0	16
See (7)			0xFFDE	15
See (8)			0xFFDC to 0xFFC0	14 to 0, lowest

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0x0000 to 0x01FF) or from within unused address range.
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot. Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG
(6) In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG
(7) This location is used as bootstrap loader security key (BSLSKEY).
A 0xAA55 at this location disables the BSL completely.
A zero (0x0) disables the erasure of the flash if an invalid password is supplied.
(8) The interrupt vectors at addresses 0xFFDC to 0xFFC0 are not used in this device and can be used for regular program code if necessary.

4.5 Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend

rw	Bit can be read and written.
rw-0, 1	Bit can be read and written. It is Reset or Set by PUC.
rw-(0), (1)	Bit can be read and written. It is Reset or Set by POR.
	SFR bit is not present in device.

Table 4. Interrupt Enable 1

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
OFIE	Oscillator fault interrupt enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Table 5. Interrupt Enable 2

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE	USCI_A0 receive-interrupt enable
UCA0TXIE	USCI_A0 transmit-interrupt enable
UCB0RXIE	USCI_B0 receive-interrupt enable
UCB0TXIE	USCI_B0 transmit-interrupt enable

Table 6. Interrupt Flag Register 1

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG	Flag set on oscillator fault
RSTIFG	External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power up.
PORIFG	Power-on reset interrupt flag. Set on V_{CC} power up.
NMIIFG	Set via $\overline{RST}$/NMI pin

Table 7. Interrupt Flag Register 2

Address	7	6	5	4	3	2	1	0
03h					UCB0TXIFG	UCB0RXIFG	UCA0TXIFG	UCA0RXIFG
					rw-1	rw-0	rw-1	rw-0

UCA0RXIFG	USCI_A0 receive-interrupt flag
UCA0TXIFG	USCI_A0 transmit-interrupt flag
UCB0RXIFG	USCI_B0 receive-interrupt flag
UCB0TXIFG	USCI_B0 transmit-interrupt flag

4.6 Memory Organization

Table 8. Memory Organization

		MSP430F2112	MSP430F2122	MSP430F2132
Memory	Size	2 KB	4 KB	8 KB
Main: interrupt vector	Flash	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0
Main: code memory	Flash	0xFFFF to 0xF800	0xFFFF to 0xF000	0xFFFF to 0xE000
Information memory	Size	256 Byte	256 Byte	256 Byte
	Flash	0x10FFh to 0x1000	0x10FFh to 0x1000	0x10FFh to 0x1000
Boot memory	Size	1 KB	1 KB	1 KB
	ROM	0x0FFF to 0x0C00	0x0FFF to 0x0C00	0x0FFF to 0x0C00
RAM	Size	256 B	512 Byte	512 Byte
		0x02FF to 0x0200	0x03FF to 0x0200	0x03FF to 0x0200
Peripherals	16-bit	0x01FF to 0x0100	0x01FF to 0x0100	0x01FF to 0x0100
	8-bit	0x00FF to 0x0010	0x00FF to 0x0010	0x00FF to 0x0010
	8-bit SFR	0x000F to 0x0000	0x000F to 0x0000	0x000F to 0x0000

4.7 Bootstrap Loader (BSL)

The MSP430F2132 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430F2132 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

Table 9. BSL Function Pins

BSL FUNCTION	PW PACKAGE PINS	RHB, RTV PACKAGE PINS
Data transmit	22 - P1.1	22 - P1.1
Data receive	10 - P2.2	8 - P2.2

4.8 Flash Memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset, segment A is protected against programming and erasing. It can be unlocked, but care should be taken not to erase this segment if the device-specific calibration data is required.

4.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

4.10 Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator, an internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, a high-frequency crystal, or the internal very-low-power LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

4.11 Calibration Data Stored in Information Memory Segment A

Calibration data is stored for both the DCO and for ADC10 organized in a tag-length-value (TLV) structure.

Table 10. Tags Used By the ADC Calibration Tags

NAME	ADDRESS	VALUE	DESCRIPTION
TAG_DCO_30	0x10F6	0x01	DCO frequency calibration at V_{CC} = 3 V and T_A = 30°C at calibration
TAG_ADC10_1	0x10DA	0x08	ADC10_1 calibration tag
TAG_EMPTY	-	0xFE	Identifier for empty memory areas

Table 11. Labels Used By the ADC Calibration Tags

LABEL	CONDITION AT CALIBRATION / DESCRIPTION	SIZE	ADDRESS OFFSET
CAL_ADC_25T85	INCHx = 0x1010, REF2_5 = 1, T_A = 85°C	word	0x0010
CAL_ADC_25T30	INCHx = 0x1010, REF2_5 = 1, T_A = 30°C	word	0x000E
CAL_ADC_25VREF_FACTOR	REF2_5 = 1, T_A = 30°C, I_{VREF+} = 1 mA	word	0x000C
CAL_ADC_15T85	INCHx = 0x1010, REF2_5 = 0, T_A = 85°C	word	0x000A
CAL_ADC_15T30	INCHx = 0x1010, REF2_5 = 0, T_A = 30°C	word	0x0008
CAL_ADC_15VREF_FACTOR	REF2_5 = 0, T_A = 30°C, I_{VREF+} = 0.5 mA	word	0x0006
CAL_ADC_OFFSET	External V_{REF} = 1.5 V, $f_{ADC10CLK}$ = 5 MHz	word	0x0004
CAL_ADC_GAIN_FACTOR	External V_{REF} = 1.5 V, $f_{ADC10CLK}$ = 5 MHz	word	0x0002
CAL_BC1_1MHz	-	byte	0x0009
CAL_DCO_1MHz	-	byte	0x0008
CAL_BC1_8MHz	-	byte	0x0007
CAL_DCO_8MHz	-	byte	0x0006
CAL_BC1_12MHz	-	byte	0x0005
CAL_DCO_12MHz	-	byte	0x0004
CAL_BC1_16MHz	-	byte	0x0003
CAL_DCO_16MHz	-	byte	0x0002

4.12 Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

4.13 Digital I/O

There are three 8-bit I/O ports implemented—ports P1, P2, and P3:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup or pulldown resistor.

The MSP430F2132 provides up to 24 total port I/O pins available externally. See the device pinout for more information.

4.14 Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

4.15 ADC10

The ADC10 module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling allowing ADC samples to be converted and stored without any CPU intervention.

4.16 Comparator_A+

The primary function of the Comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

4.17 Timer0_A3

Timer0_A3 is a 16-bit timer/counter with three capture/compare registers. Timer0_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer0_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 12. Timer0_A3 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PW	RHB, RTV					PW	RHB, RTV
21 - P1.0	21 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
9 - P2.1	7 - P2.1	TAINCLK	INCLK				
22 - P1.1	22 - P1.1	TA0	CCI0A	CCR0	TA0	22 - P1.1	22 - P1.1
10 - P2.2	8 - P2.2	TA0	CCI0B			26 - P1.5	26 - P1.5
		DV_{SS}	GND			10 - P2.2	8 - P2.2
		DV_{CC}	V_{CC}			ADC10 (internal)	ADC10 (internal)
23 - P1.2	23 - P1.2	TA1	CCI1A	CCR1	TA1	23 - P1.2	23 - P1.2
		CAOUT (internal)	CCI1B			27 - P1.6	27 - P1.6
		DV_{SS}	GND			19 - P2.3	18 - P2.3
		DV_{CC}	V_{CC}			ADC10 (internal)	ADC10 (internal)
24 - P1.3	24 - P1.3	TA2	CCI2A	CCR2	TA2	24 - P1.3	24 - P1.3
		ACLK (internal)	CCI2B			28 - P1.7	28 - P1.7
		DV_{SS}	GND			20 - P2.4	19 - P2.4
		DV_{CC}	V_{CC}			ADC10 (internal)	ADC10 (internal)

4.18 Timer1_A2

Timer1_A2 is a 16-bit timer/counter with two capture/compare registers. Timer1_A2 can support multiple capture/compares, PWM outputs, and interval timing. Timer1_A2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 13. Timer1_A2 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PW	RHB, RTV					PW	RHB, RTV
21 - P1.0	21 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
9 - P2.1	7 - P2.1	TAINCLK	INCLK				
22 - P1.1	22 - P1.1	TA0	CCI0A	CCR0	TA0	17 - P3.6	15 - P3.6
17 - P3.6	15 - P3.6	TA0	CCI0B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
18 - P3.7	16 - P3.7	TA1	CCI1A	CCR1	TA1	18 - P3.7	16 - P3.7
		CAOUT (internal)	CCI1B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				

4.19 Universal Serial Communications Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols like SPI (3 or 4 pin), I2C and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

USCI_B0 provides support for SPI (3 or 4 pin) and I2C.

4.20 Peripheral File Map

Table 14. Peripherals With Word Access

MODULE	REGISTER NAME	SHORT NAME	ADDRESS OFFSET
ADC10	ADC data transfer start address	ADC10SA	0x01BC
	ADC memory	ADC10MEM	0x01B4
	ADC control register 1	ADC10CTL1	0x01B2
	ADC control register 0	ADC10CTL0	0x01B0
	ADC analog enable 0	ADC10AE0	0x004A
	ADC analog enable 1	ADC10AE1	0x004B
	ADC data transfer control register 1	ADC10DTC1	0x0049
	ADC data transfer control register 0	ADC10DTC0	0x0048
Timer0_A3	Capture/compare register	TA0CCR2	0x0176
	Capture/compare register	TA0CCR1	0x0174
	Capture/compare register	TA0CCR0	0x0172
	Timer0_A3 register	TA0R	0x0170
	Capture/compare control	TA0CCTL2	0x0166
	Capture/compare control	TA0CCTL1	0x0164
	Capture/compare control	TA0CCTL0	0x0162
	Timer0_A3 control	TA0CTL	0x0160
	Timer0_A3 interrupt vector	TA0IV	0x012E
Timer1_A2	Capture/compare register	TA1CCR1	0x0194
	Capture/compare register	TA1CCR0	0x0192
	Timer1_A2 register	TA1R	0x0190
	Capture/compare control	TA1CCTL1	0x0184
	Capture/compare control	TA1CCTL0	0x0182
	Timer1_A2 control	TA1CTL	0x0180
	Timer1_A2 interrupt vector	TA1IV	0x011E
Flash Memory	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Watchdog Timer+	Watchdog/timer control	WDTCTL	0x0120

Table 15. Peripherals With Byte Access

MODULE	REGISTER NAME	SHORT NAME	ADDRESS OFFSET
USCI_B0	USCI_B0 transmit buffer	UCB0TXBUF	0x06F
	USCI_B0 receive buffer	UCB0RXBUF	0x06E
	USCI_B0 status	UCB0STAT	0x06D
	USCI B0 I2C Interrupt enable	UCB0CIE	0x06C
	USCI_B0 bit rate control 1	UCB0BR1	0x06B
	USCI_B0 bit rate control 0	UCB0BR0	0x06A
	USCI_B0 control 1	UCB0CTL1	0x069
	USCI_B0 control 0	UCB0CTL0	0x068
	USCI_B0 I2C slave address	UCB0SA	0x011A
	USCI_B0 I2C own address	UCB0OA	0x0118

Table 15. Peripherals With Byte Access (continued)

MODULE	REGISTER NAME	SHORT NAME	ADDRESS OFFSET
USCI_A0	USCI_A0 transmit buffer	UCA0TXBUF	0x0067
	USCI_A0 receive buffer	UCA0RXBUF	0x0066
	USCI_A0 status	UCA0STAT	0x0065
	USCI_A0 modulation control	UCA0MCTL	0x0064
	USCI_A0 baud rate control 1	UCA0BR1	0x0063
	USCI_A0 baud rate control 0	UCA0BR0	0x0062
	USCI_A0 control 1	UCA0CTL1	0x0061
	USCI_A0 control 0	UCA0CTL0	0x0060
	USCI_A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI_A0 IrDA transmit control	UCA0IRTCTL	0x005E
	USCI_A0 auto baud rate control	UCA0ABCTL	0x005D
Comparator_A+	Comparator_A port disable	CAPD	0x005B
	Comparator_A control 2	CACTL2	0x005A
	Comparator_A control 1	CACTL1	0x0059
Basic Clock System+	Basic clock system control 3	BCSCTL3	0x0053
	Basic clock system control 2	BCSCTL2	0x0058
	Basic clock system control 1	BCSCTL1	0x0057
	DCO clock frequency control	DCOCTL	0x0056
Port P3	Port P3 resistor enable	P3REN	0x0010
	Port P3 selection	P3SEL	0x001B
	Port P3 direction	P3DIR	0x001A
	Port P3 output	P3OUT	0x0019
	Port P3 input	P3IN	0x0018
Port P2	Port P2 selection 2	P2SEL2	0x0042
	Port P2 resistor enable	P2REN	0x002F
	Port P2 selection	P2SEL	0x002E
	Port P2 interrupt enable	P2IE	0x002D
	Port P2 interrupt edge select	P2IES	0x002C
	Port P2 interrupt flag	P2IFG	0x002B
	Port P2 direction	P2DIR	0x002A
	Port P2 output	P2OUT	0x0029
	Port P2 input	P2IN	0x0028
Port P1	Port P1 selection 2 register	P1SEL2	0x0041
	Port P1 resistor enable	P1REN	0x0027
	Port P1 selection	P1SEL	0x0026
	Port P1 interrupt enable	P1IE	0x0025
	Port P1 interrupt edge select	P1IES	0x0024
	Port P1 interrupt flag	P1IFG	0x0023
	Port P1 direction	P1DIR	0x0022
	Port P1 output	P1OUT	0x0021
	Port P1 input	P1IN	0x0020
Special Function	SFR interrupt flag 2	IFG2	0x0003
	SFR interrupt flag 1	IFG1	0x0002
	SFR interrupt enable 2	IE2	0x0001
	SFR interrupt enable 1	IE1	0x0000

5 Specifications

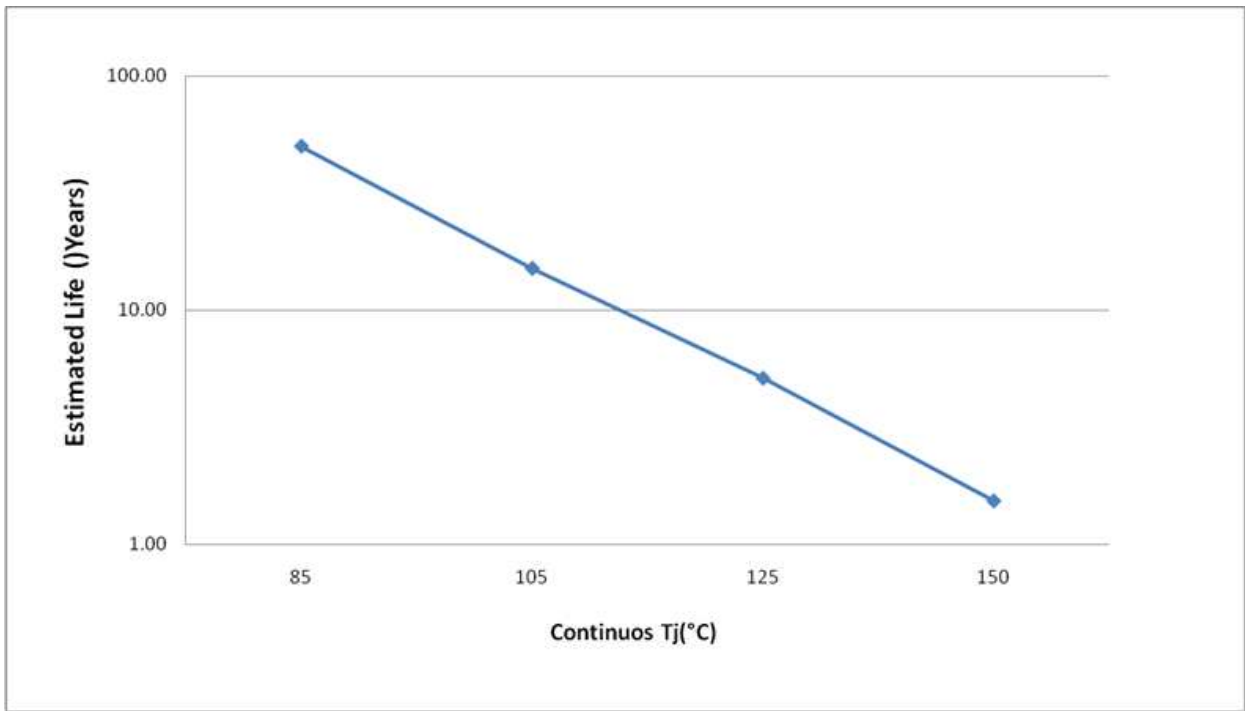
5.1 Absolute Maximum Ratings(1)

Voltage applied at V_{CC} to V_{SS}		-0.3 V to 4.1 V
Voltage applied to any pin (2)		-0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal		±2 mA
Storage temperature, T_{stg} (3)	Unprogrammed device	-55°C to 150°C
	Programmed device	-55°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings*may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions*is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

(3) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.



A. See data sheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 110°C junction temperature (does not include package interconnect life).

C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 1. Operating Life Derating Chart

5.2 THERMAL INFORMATION

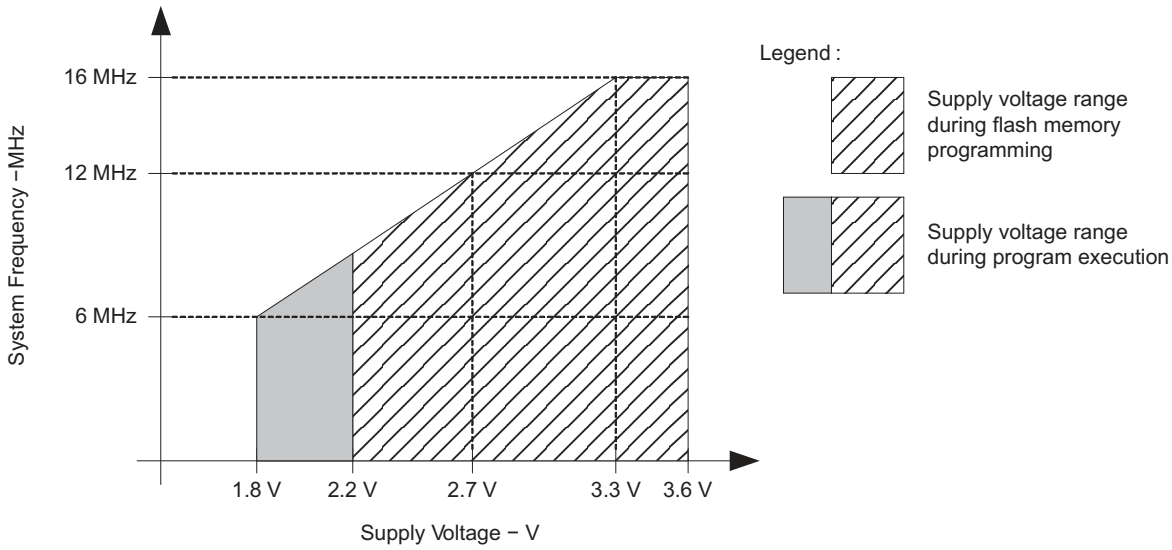
THERMAL METRIC(1)		MSP430F2132-EP RHB 32 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	33.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	24.3	
θ_{JB}	Junction-to-board thermal resistance(4)	7.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.3	
ψ_{JB}	Junction-to-board characterization parameter(6)	7.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.3	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

5.3 Recommended Operating Conditions(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, $AV_{CC} = DV_{CC} = V_{CC}$	During program execution	1.8		3.6	V
		During flash memory programming	2.2		3.6	
V_{SS}	Supply voltage	$AV_{SS} = DV_{SS} = V_{SS}$	0		0	V
T_A	Operating free-air temperature	I version	-40		85	°C
		Q version	-40		125	
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(2)(1) (see Figure 2)	V_{CC} = 1.8 V, Duty cycle = 50% ±10%	dc		6	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ±10%	dc		12	
		V_{CC} ≥ 3.3 V, Duty cycle = 50% ±10%	dc		16	

(1) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(2) The MSP430F2132 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 2. Operating Area

5.4 Active Mode Supply Current (Into DV_{CC} + AV_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1][2]. See Typical Characteristics - Active-Mode Supply Current (Into DV_{CC} + AV_{CC}) for related characterization graphs.

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		250	345	µA
				3 V		350	455	
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		220		µA
				3 V		300		
$I_{AM,4kHz}$	Active mode (AM) current (4 kHz)	$f_{MCLK} = f_{SMCLK} = f_{ACLK}$ = 32768 Hz / 8 = 4096 Hz, f_{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		2	5	µA
			125°C				7	
			-40°C to 85°C	3 V		3	7	
			125°C				10	
$I_{AM,100kHz}$	Active mode (AM) current (100 kHz)	$f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)} \approx$ 100 kHz, f_{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		60	85	µA
			125°C				95	
			-40°C to 85°C	3 V		72	95	
			125°C				105	

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

5.5 Low-Power-Mode Supply Currents (Into V_{CC}) Excluding External Current[1][2]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted). See Typical Characteristics - LPM4 Current for related characterization graphs.

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0, 1MHz}$	Low-power mode 0 (LPM0) current[3]	f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		55	66	µA
			105°C				68	
			-40°C to 85°C	3 V		70	83	
			105°C				90	
$I_{LPM0, 100kHz}$	Low-power mode 0 (LPM0) current[3]	f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO}(0, 0) \approx 100$ kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		33	42	µA
			125°C				46	
			-40°C to 85°C	3 V		37	46	
			125°C				50	
I_{LPM2}	Low-power mode 2 (LPM2) current[4]	$f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40°C to 85°C	2.2 V		20	25	µA
			125°C				29	
			-40°C to 85°C	3 V		22	27	
			125°C				33	
$I_{LPM3, LFXT1}$	Low-power mode 3 (LPM3) current[4]	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C to 25°C	2.2 V		0.7	1.2	µA
			85°C			1.6	2.3	
			105°C			3	6	
			-40°C to 25°C	3 V		0.9	1.9	
			85°C			1.6	2.8	
			105°C			3	7	
$I_{LPM3, VLO}$	Low-power mode 3 current, (LPM3)[4]	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C to 25°C	2.2 V		0.3	0.7	µA
			85°C			1.2	1.9	
			125°C			2	6	
			-40°C to 25°C	3 V		0.7	0.8	
			85°C			1.4	2.1	
			125°C			2.5	6.5	
I_{LPM4}	Low-power mode 4 (LPM4) current[5]	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-40°C	2.2 V, 3 V		0.1	0.5	µA
			25°C			0.1	0.5	
			85°C			0.8	1.5	
			125°C			2	4.5	

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.
(5) Current for brownout included.

5.6 Schmitt-Trigger Inputs (Ports P1, P2, P3, JTAG, $\overline{RST}$/NMI, XIN[1])

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			2.2 V	0.95		1.70	
			3 V	1.30		2.30	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			2.2 V	0.50		1.25	
			3 V	0.70		1.70	
V_{hys}	Input voltage hysteresis (V_{IT+} - V_{IT-})		2.2 V	0.15		1.05	V
			3 V	0.25		1.05	
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$		19	35	52	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

(1) XIN only in bypass mode

5.7 Inputs (Ports P1, P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag[1]	2.2 V, 3 V	20			ns

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set with trigger signals shorter than $t_{(int)}$.

5.8 Leakage Current (Ports P1, P2, P3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	(1) (2)	2.2 V, 3 V			±51	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

5.9 Outputs (Ports P1, P2, P3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = -1.5 mA (1)	2.2 V	V_{CC} - 0.3	V_{CC}	V
		$I_{OH(max)}$ = -6 mA (2)		V_{CC} - 0.65	V_{CC}	
		$I_{OH(max)}$ = -1.5 mA (1)	3 V	V_{CC} - 0.3	V_{CC}	
		$I_{OH(max)}$ = -6 mA (2)		V_{CC} - 0.65	V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA (1)	2.2 V	V_{SS}	V_{SS} + 0.3	V
		$I_{OL(max)}$ = 6 mA (2)		V_{SS}	V_{SS} + 0.65	
		$I_{OL(max)}$ = 1.5 mA (1)	3 V	V_{SS}	V_{SS} + 0.3	
		$I_{OL(max)}$ = 6 mA (2)		V_{SS}	V_{SS} + 0.65	

(1) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

5.10 Output Frequency (Ports P1, P2, P3)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted). See Typical Characteristics - Outputs for related characterization graphs.

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ (2) (3)	2.2 V			7.5	MHz
			3 V			12	
$f_{Port°CLK}$	Clock output frequency	P2.0/ACLK, P1.4/SMCLK, C_L = 20 pF (3)	2.2 V			7.5	MHz
			3 V			16	

(1) Not ensured for T_A > 105°C.
(2) Alternatively, a resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(3) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.11 POR and Brownout Reset (BOR)(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted). See Typical Characteristics - POR/Brownout Reset (BOR) for related characterization graphs.

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 3	$dV_{CC}/dt \le 3$ V/s			0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 3 through Figure 20	$dV_{CC}/dt \le 3$ V/s				1.75	V
$V_{hys(B\_IT-)}$	See Figure 3	$dV_{CC}/dt \le 3$ V/s		65	130	215	mV
$t_{d(BOR)}$	See Figure 3					2000	µs
$t_{(reset)}$	Pulse duration needed at $\overline{RST}$/NMI pin to accepted reset internally		2.2 V, 3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.
(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

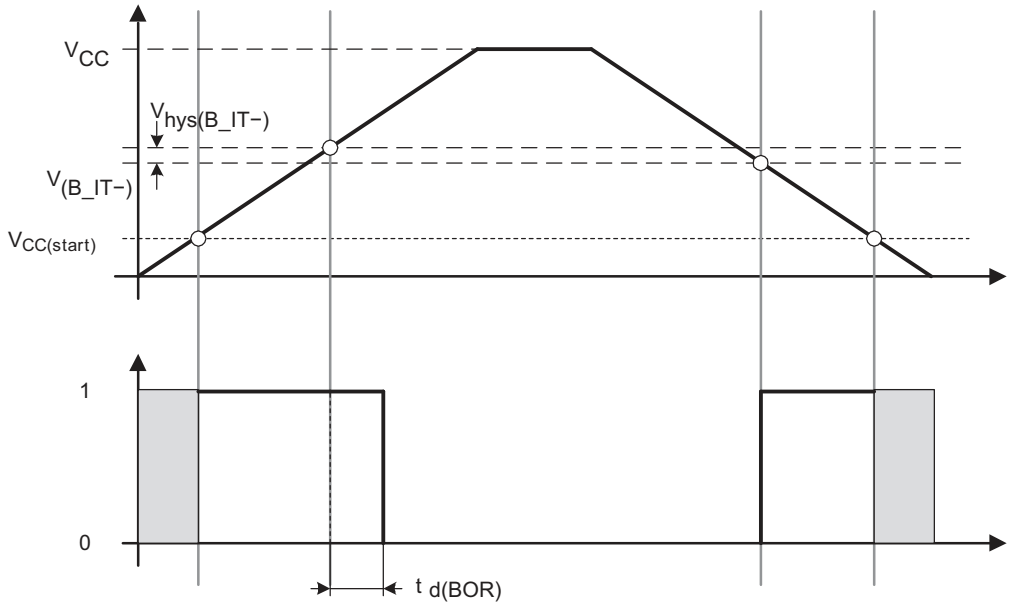


Figure 3. POR and BOR vs Supply Voltage

5.12 Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

5.13 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted). See Typical Characteristics - Calibrated 1-MHz DCO Frequency for related characterization graphs.

DCO Frequency (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted). See Typical Characteristics - Calibrated 1-MHz DCO Frequency for related characterization graphs.

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V, 3 V	0.055		0.145	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V, 3 V	0.065		0.175	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V, 3 V	0.095		0.205	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V, 3 V	0.135		0.285	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V, 3 V	0.195		0.405	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V, 3 V	0.27		0.55	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V, 3 V	0.38		0.78	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V, 3 V	0.53		1.07	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V, 3 V	0.70		1.60	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V, 3 V	1.05		2.20	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V, 3 V	1.50		3.10	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V, 3 V	2.40		4.40	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V, 3 V	2.90		5.60	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V, 3 V	4.20		7.40	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V, 3 V	5.90		9.70	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V, 3 V	8.50		14.0	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	11.5		19	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	15.5		26.5	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)} / f_{DCO(RSEL,DCO)}$	2.2 V, 3 V			1.56	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)} / f_{DCO(RSEL,DCO)}$	2.2 V, 3 V	1.04	1.08	1.13	ratio
	Duty cycle	Measured at P1.4/SMCLK	2.2 V, 3 V	35	50	65	%

5.14 Calibrated DCO Frequencies - Tolerance at Calibration

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	Frequency tolerance at calibration		25°C	3 V	-1	±0.2	+1	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

5.15 Calibrated DCO Frequencies - Tolerance Over Temperature 0°C to 85°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±0.5	+2.5	%
	8-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1	+2.5	%
	12-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1	+2.5	%
	16-MHz tolerance over temperature		0°C to 85°C	3 V	-3	±2	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	0.97	1	1.03	MHz
				3 V	0.975	1	1.025	
				3.6 V	0.97	1	1.03	
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	7.76	8	8.4	MHz
				3 V	7.8	8	8.2	
				3.6 V	7.6	8	8.24	
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	11.64	12	12.36	MHz
				3 V	11.64	12	12.36	
				3.6 V	11.64	12	12.36	
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	0°C to 85°C	3 V	15.52	16	16.48	MHz
				3.6 V	15	16	16.48	

5.16 Calibrated DCO Frequencies - Tolerance Over Supply Voltage V_{CC}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over V_{CC}			25°C	1.8 V to 3.6 V	-3	±2	+3	%
8-MHz tolerance over V_{CC}			25°C	1.8 V to 3.6 V	-3	±2	+3	%
12-MHz tolerance over V_{CC}			25°C	2.2 V to 3.6 V	-3	±2	+3	%
16-MHz tolerance over V_{CC}			25°C	3 V to 3.6 V	-6	±2	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.97	1	1.03	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.76	8	8.24	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V to 3.6 V	15	16	16.48	MHz

5.17 Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance overall			-40°C to 125°C	1.8 V to 3.6 V	-6	±2	+6	%
8-MHz tolerance overall			-40°C to 125°C	1.8 V to 3.6 V	-6	±2	+6	%
12-MHz tolerance overall			-40°C to 125°C	2.2 V to 3.6 V	-6	±2	+6	%
16-MHz tolerance overall			-40°C to 125°C	3 V to 3.6 V	-7	±3	+7	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	-40°C to 125°C	1.8 V to 3.6 V	0.94	1	1.06	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	-40°C to 125°C	1.8 V to 3.6 V	7.5	8	8.5	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	-40°C to 125°C	2.2 V to 3.6 V	11.3	12	12.7	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	-40°C to 125°C	3 V to 3.6 V	14.9	16	17.1	MHz

5.18 Wake-Up From Lower-Power Modes (LPM3/4)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted). See Typical Characteristics - DCO Clock Wake-Up Time From LPM3/4 for related characterization graphs.

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (2)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V, 3 V			2	µs
		BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ				1.5	
		BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ				1	
		BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (3)				$1 / f_{MCLK} + t_{Clock,LPM3/4}$		

(1) Not ensured for $T_A > 105°C$.
(2) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, a port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(3) Parameter applicable only if DCOCLK is used for MCLK.

5.19 DCO With External Resistor R_{OSC}(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted). See Typical Characteristics - DCO With External Resistor R_{OSC} for related characterization graphs.

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO,ROSC}$	DCO output frequency with R_{OSC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, $T_A = 25°C$	2.2 V		1.8		MHz
			3 V		1.95		
D_T	Temperature drift	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V, 3 V		±0.1		%/°C
D_V	Drift with V_{CC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V, 3 V		10		%/V

(1) R_{OSC} = 100 kΩ. Metal film resistor, type 0257, 0.6 W with 1% tolerance and T_K = ±50 ppm/°C.

5.20 Crystal Oscillator LFXT1, Low-Frequency Mode[1][2]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted). See Typical Characteristics - LFXT1 Oscillator in HF Mode (XTS = 1) for related characterization graphs.

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode[3]	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{LFXT1,LF}$ = 32768 Hz	2.2 V, 3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode[4]	XTS = 0, XCAPx = 0, LFXT1Sx = 3[5]	2.2 V, 3 V	10		10000	Hz

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Use of the LFXT1 Crystal Oscillator at T_A > 105°C is not ensured. It is recommended that an external digital clock source or the internal DCO is used to provide clocking.

(3) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the crystal that is used.

(4) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(5) Measured with logic-level input frequency but also applies to operation with crystals.

5.21 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	-40°C to 85°C	2.2 V, 3 V	4	12	20	kHz
		125°C				23	
df_{VLO}/dT	VLO frequency temperature drift[1]		2.2 V, 3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift[2]		1.8 V to 3.6 V		4		%/V

(1) Calculated using the box method:
[MAX(-40...125°C) - MIN(-40...125°C)]/MIN(-40...125°C)/[125°C - (-40°C)]

(2) Calculated using the box method: [MAX(1.8...3.6 V) - MIN(1.8...3.6 V)]/MIN(1.8...3.6 V)/(3.6 V - 1.8 V)

5.22 Crystal Oscillator LFXT1, High-Frequency Mode[1][2]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, XCAPx = 0, LFXT1Sx = 0	1.8 V to 3.6 V	0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, XCAPx = 0, LFXT1Sx = 1	1.8 V to 3.6 V	1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, XCAPx = 0, LFXT1Sx = 2	1.8 V to 3.6 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3 V to 3.6 V	2		16	
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation allowance for HF crystals (see Figure 27 and Figure 28)	XTS = 1, XCAPx = 0, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 1, XCAPx = 0, LFXT1Sx = 1, $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XTS = 1, XCAPx = 0, LFXT1Sx = 2, $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode[3]	XTS = 1, XCAPx = 0[4]			1		pF
	Duty cycle, HF mode	XTS = 1, XCAPx = 0, Measured at P2.0/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V, 3 V	40	50	60	%
		XTS = 1, XCAPx = 0, Measured at P2.0/ACLK, $f_{LFXT1,HF}$ = 16 MHz		40	50	60	
$f_{Fault,HF}$	Oscillator fault frequency [5]	XTS = 1, XCAPx = 0, LFXT1Sx = 3[6]	2.2 V, 3 V	30		300	kHz

(1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Use of the LFXT1 Crystal Oscillator at T_A > 105°C is not ensured. It is recommended that an external digital clock source or the internal DCO is used to provide clocking.

(3) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(4) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(5) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.

(6) Measured with logic-level input frequency, but also applies to operation with crystals.

5.23 Timer0_A3

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer0_A3 clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10%	2.2 V			10	MHz
			3 V			16	
$t_{TA,cap}$	Timer0_A3 capture timing	TA0.0, TA0.1, TA0.2	2.2 V, 3 V	20			ns

5.24 Timer1_A2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer1_A2 clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10%	2.2 V			10	MHz
			3 V			16	
$t_{TB,cap}$	Timer1_A2 capture timing	TA1.0, TA1.1	2.2 V, 3 V	20			ns

5.25 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$f_{max,BITCLK}$	Maximum BITCLK clock frequency (equals baud rate in MBaud)(1)		2.2 V, 3 V	2			MHz
t_τ	UART receive deglitch time(2)		2.2 V	45	150		ns
			3 V	45	100		

(1) The DCO wake-up time must be considered in LPM3 and LPM4 for baud rates above 1 MHz.
(2) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

5.26 USCI (SPI Master Mode)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 4 and Figure 5)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110			ns
			3 V	75			
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0			ns
			3 V	0			
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V			30	ns
			3 V			20	

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Not ensured for $T_A > 105°C$.

5.27 USCI (SPI Slave Mode)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 6 and Figure 7)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock		2.2 V, 3 V		50		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE high		2.2 V, 3 V	10			ns
$t_{STE,ACC}$	STE access time, STE low to SOMI data out		2.2 V, 3 V		50		ns
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance		2.2 V, 3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached slave.
(2) Not ensured for $T_A > 105°C$.

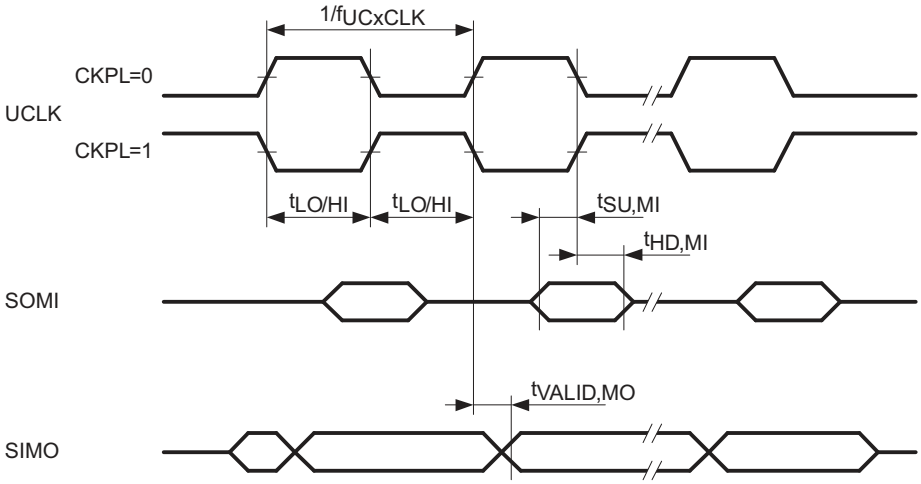


Figure 4. SPI Master Mode, CKPH = 0

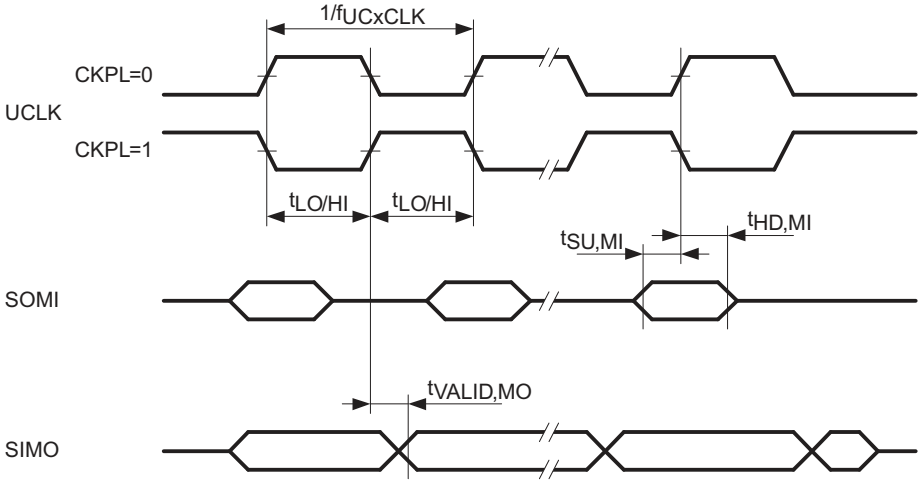


Figure 5. SPI Master Mode, CKPH = 1

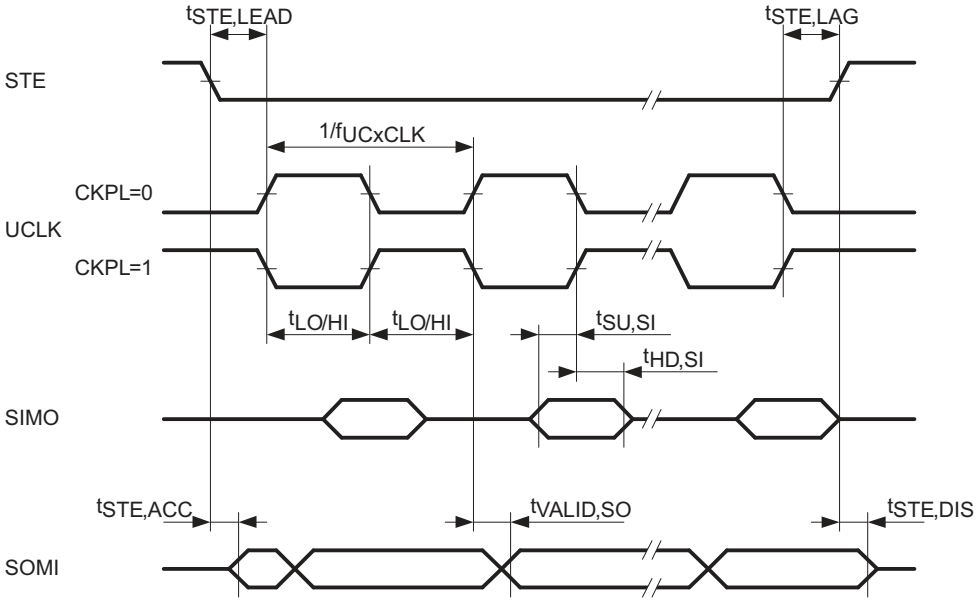


Figure 6. SPI Slave Mode, CKPH = 0

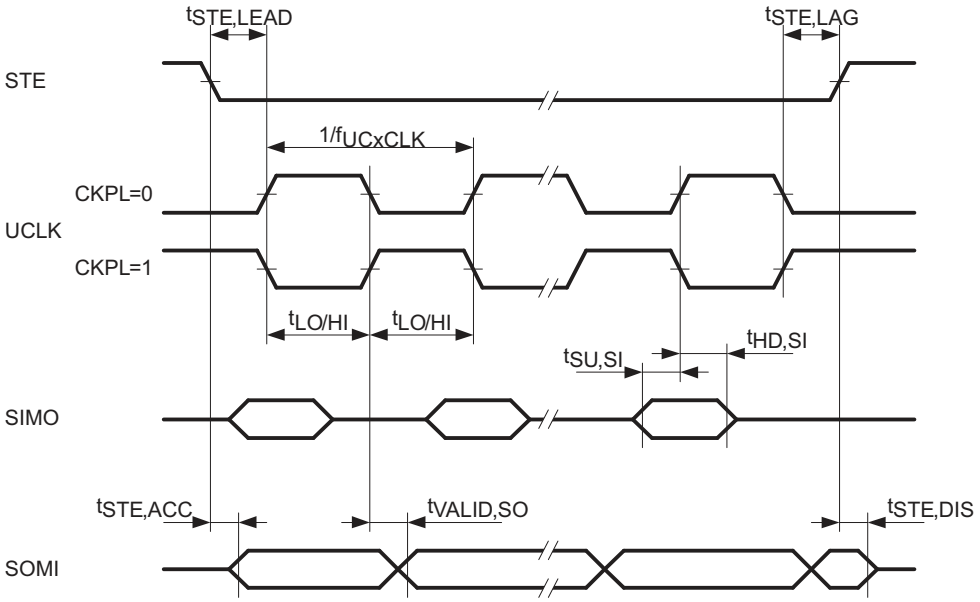


Figure 7. SPI Slave Mode, CKPH = 1

5.28 USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 8)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V, 3 V	4			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	45	150	605	ns
			3 V	45	100	605	

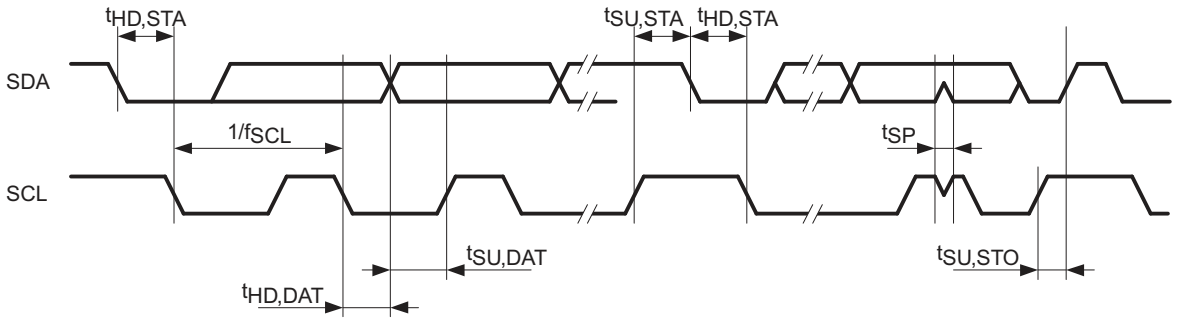


Figure 8. I2C Mode Timing

5.29 Comparator_A+[1]

over recommended operating free-air temperature range (unless otherwise noted). See Typical Characteristics - Comparator_A+ for related characterization graphs.

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		25	45	µA
			3 V		45	65	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at CA0 and CA1	2.2 V		30	55	µA
			3 V		45	85	
V_{IC}	Common-mode input voltage range[2]	CAON = 1	2.2 V, 3 V	0		V_{CC} - 1	V
$V_{(Ref025)}$	Voltage at 0.25 V_{CC} node / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at CA0 and CA1	2.2 V, 3 V	0.225	0.24	0.255	
$V_{(Ref050)}$	Voltage at 0.5 V_{CC} node / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at CA0 and CA1	2.2 V, 3 V	0.465	0.48	0.505	
$V_{(RefVT)}$	See Figure 29 and Figure 30	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at CA0 and CA1, T_A = 85°C	2.2 V	360	480	570	mV
			3 V	370	490	580	
$V_{(offset)}$	Offset voltage[3]		2.2 V, 3 V	-42		42	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V, 3 V		0.7	1.8	mV
$t_{(response)}$	Response time (low-high and high-low)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 0[4] (see Figure 9 and Figure 10)	2.2 V	100	165	320	ns
			3 V	50	120	250	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF = 1[4] (see Figure 9 and Figure 10)	2.2 V	1.3	1.9	3.0	µs
			3 V	0.7	1.5	2.5	

(1) The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.y)}$ specification.
(2) Not ensured for T_A > 105°C.
(3) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
(4) Response time measured at P2.2/TA0.0/A2/CA4/CAOUT. If the Comparator_A+ is enabled a settling time of 60 ns (typical) is added to the response time.

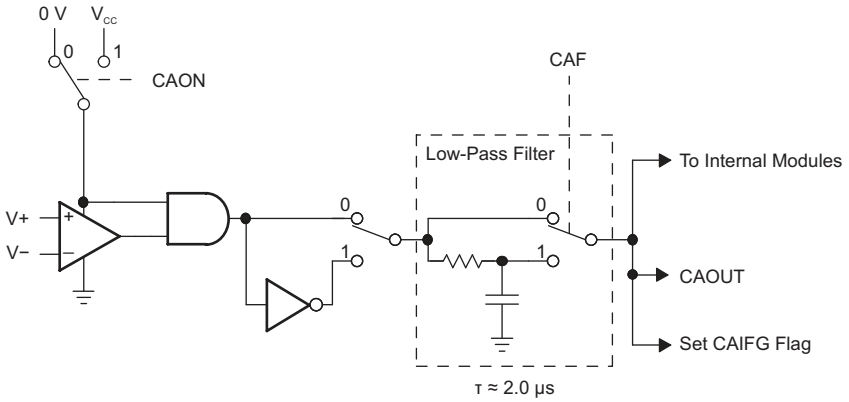


Figure 9. Comparator_A+ Module Block Diagram

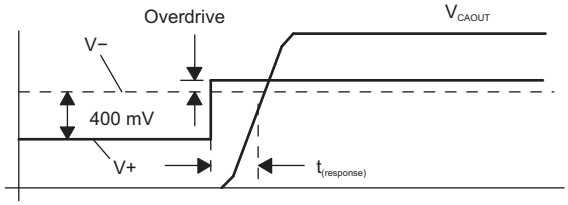


Figure 10. Overdrive Definition

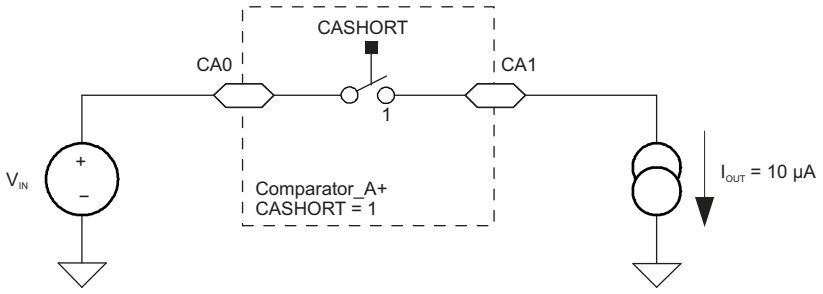


Figure 11. Comparator_A+ Short Resistance Test Condition

5.30 10-Bit ADC, Power Supply and Input Range Conditions(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage	V_{SS} = 0 V			2.2		3.6	V
V_{Ax}	Analog input voltage range(2)	All Ax terminals, Analog inputs selected in ADC10AE register			0		V_{CC}	V
I_{ADC10}	ADC10 supply current(3)	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	I: -40°C to 85°C T: -40°C to 105°C	2.2 V		0.52	1.06	mA
				3 V		0.6	1.25	
I_{REF+}	Reference supply current, reference buffer disabled(4)	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	I: -40°C to 85°C T: -40°C to 105°C	2.2 V, 3 V		0.25	0.45	mA
		$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0		3 V		0.25	0.45	
$I_{REFB,0}$	Reference buffer supply current with ADC10SR = 0(4)	$f_{ADC10CLK}$ = 5 MHz ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0	-40°C to 85°C	2.2 V, 3 V		1.1	1.4	mA
			125°C				1.85	
$I_{REFB,1}$	Reference buffer supply current with ADC10SR = 1(4)	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1	-40°C to 85°C	2.2 V, 3 V		0.5	0.7	mA
			125°C				0.85	
C_I	Input capacitance	Only one terminal Ax selected at a time	I: -40°C to 85°C T: -40°C to 105°C				27	pF
R_I	Input MUX ON resistance	0 V ≤ V_{Ax} ≤ V_{CC}	I: -40°C to 85°C T: -40°C to 105°C	2.2 V, 3 V			2000	Ω

(1) The leakage current is defined in the leakage current table with Px.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC10}.
(4) The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference. The reference voltage must be allowed to settle before an A/D conversion is started.

5.31 10-Bit ADC, Built-In Voltage Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	$I_{VREF+} \le 1$ mA, REF2_5V = 0			2.2			V
		$I_{VREF+} \le 0.5$ mA, REF2_5V = 1			2.8			
		$I_{VREF+} \le 1$ mA, REF2_5V = 1			2.9			
V_{REF+}	Positive built-in reference voltage	$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 0		2.2 V, 3 V	1.40	1.5	1.60	V
		$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 1		3 V	2.30	2.5	2.70	
$I_{LD,VREF+}$	Maximum V_{REF+} load current			2.2 V			±0.5	mA
				3 V			±1	
	V_{REF+} load regulation	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage $V_{Ax} \approx 0.75$ V, REF2_5V = 0		2.2 V, 3 V		±2		LSB
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage $V_{Ax} \approx 1.25$ V, REF2_5V = 1		3 V		±2		
	V_{REF+} load regulation response time(1)	I_{VREF+} = 100 µA to 900 µA, $V_{Ax} \approx 0.5 \times V_{REF+}$, Error of conversion result ≤1 LSB	ADC10SR = 0	3 V			400	ns
			ADC10SR = 1				2000	
C_{VREF+}	Maximum capacitance at pin V_{REF+}(2)	$I_{VREF+} \le$ ±1 mA, REFON = 1, REFOUT = 1		2.2 V, 3 V			100	pF
TC_{REF+}	Temperature coefficient(3)	I_{VREF+} = constant with 0 mA ≤ I_{VREF+} ≤ 1 mA(4)	-40°C to 85°C	2.2 V, 3 V			±100	ppm/°C
			-40°C to 105°C				±110	
t_{REFON}	Settling time of internal reference voltage(1)(5)	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 to 1		3.6 V			30	µs
$t_{REFBURST}$	Settling time of reference buffer(1)(5)	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 1, REFBURST = 1	ADC10SR = 0	2.2 V			1	µs
			ADC10SR = 1				2.5	
		I_{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1	ADC10SR = 0	3 V			2	
			ADC10SR = 1				4.5	

(1) Not ensured for $T_A > 105$°C.
(2) The capacitance applied to the internal buffer operational amplifier, if switched to terminal P2.4/TA2/A4/V_{REF+}/V_{eREF+} (REFOUT = 1), must be limited; otherwise, the reference buffer may become unstable.
(3) Calculated using the box method:
I temperature: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))
T temperature: (MAX(-40 to 105°C) – MIN(-40 to 105°C)) / MIN(-40 to 105°C) / (105°C – (–40°C))
(4) Calculated using the box method: ((MAX(V_{REF}(T)) -- MIN(V_{REF}(T))) / MIN(V_{REF}(T)) / (T_{MAX} - T_{MIN})
(5) The condition is that the error in a conversion started after t_{REFON} or t_{RefBuf} is less than ±0.5 LSB.

5.32 10-Bit ADC, External Reference[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{eREF+}	Positive external reference input voltage range[2]	$V_{eREF+} > V_{eREF-}$, SREF1 = 1, SREF0 = 0		1.4	V_{CC}	V
		$V_{eREF-} \le V_{eREF+} \le (V_{CC} - 0.15\ V)$, SREF1 = 1, SREF0 = 1[3]		1.4	3	
V_{eREF-}	Negative external reference input voltage range[4]	$V_{eREF+} > V_{eREF-}$		0	1.2	V
ΔV_{eREF}	Differential external reference input voltage range $\Delta V_{eREF} = V_{eREF+} - V_{eREF-}$	$V_{eREF+} > V_{eREF-}$[5]		1.4	V_{CC}	V
I_{VeREF+}	Static input current into V_{eREF+}[6]	$0\ V \le V_{eREF+} \le V_{CC}$, SREF1 = 1, SREF0 = 0	2.2 V, 3 V		±1	µA
		$0\ V \le V_{eREF+} \le V_{CC} - 0.15\ V \le 3\ V$, SREF1 = 1, SREF0 = 1[3]			0	
I_{VeREF-}	Static input current into V_{eREF-}[6]	$0\ V \le V_{eREF-} \le V_{CC}$	2.2 V, 3 V		±1	µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) Under this condition, the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
(4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(6) Not ensured for $T_A > 105°C$.

5.33 10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR = 0	2.2 V, 3 V	0.45		6.3	MHz
			ADC10SR = 1		0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V, 3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V, 3 V	2.06		4.00	µs
		$f_{ADC10CLK}$ from ACLK, MCLK or SMCLK, ADC10SSELx ≠ 0			13 × ADC10DIVx × 1 / $f_{ADC10CLK}$			
$t_{ADC10ON}$	Turn on settling time of the ADC[1]	See[2]					100	ns

(1) Not ensured for $T_A > 105°C$.
(2) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

5.34 10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		2.2 V, 3 V			±1.2	LSB
E_D	Differential linearity error		2.2 V, 3 V			±1.2	LSB
E_O	Offset error	Source impedance R_S < 100 Ω	2.2 V, 3 V			±1.2	LSB
E_G	Gain error	SREFx = 010, unbuffered external reference, V_{eREF+} = 1.5 V	2.2 V		±1.1	±2	LSB
		SREFx = 010, unbuffered external reference, V_{eREF+} = 2.5 V	3 V		±1.1	±2	
		SREFx = 011, buffered external reference(1), V_{eREF+} = 1.5 V	2.2 V		±1.1	±4.5	
		SREFx = 011, buffered external reference(1), V_{eREF+} = 2.5 V	3 V		±1.1	±3.5	
E_T	Total unadjusted error	SREFx = 010, unbuffered external reference, V_{eREF+} = 1.5 V	2.2 V		±2	±5	LSB
		SREFx = 010, unbuffered external reference, V_{eREF+} = 2.5 V	3 V		±2	±5	
		SREFx = 011, buffered external reference(1), V_{eREF+} = 1.5 V	2.2 V		±2	±7.5	
		SREFx = 011, buffered external reference(1), V_{eREF+} = 2.5 V	3 V		±2	±6.5	

(1) The reference buffer offset adds to the gain and total unadjusted error.

5.35 10-Bit ADC, Temperature Sensor and Built-In V_{MID}(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Temperature sensor supply current(1)	REFON = 0, INCHx = 0Ah, ADC10ON = 1, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
TC_{SENSOR}		ADC10ON = 1, INCHx = 0Ah(2)	2.2 V, 3 V		3.55		mV/°C
$V_{Offset,Sensor}$	Sensor offset voltage(3)	ADC10ON = 1, INCHx = 0Ah(2)		-100		+100	mV
V_{SENSOR}	Sensor output voltage(4)	Temperature sensor voltage at T_A = 125°C (Q version only)	2.2 V, 3 V	1205	1365	1465	mV
		Temperature sensor voltage at T_A = 85°C		1195	1295	1395	
		Temperature sensor voltage at T_A = 25°C		985	1085	1185	
		Temperature sensor voltage at T_A = 0°C		895	995	1095	
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected(5)	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V, 3 V	31			µs
I_{VMID}	Current into divider at channel 11(5)	ADC10ON = 1, INCHx = 0Bh	2.2 V			N/A(5)	µA
			3 V			N/A(5)	
V_{MID}	V_{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, $V_{MID} \approx 0.5 \times V_{CC}$	2.2 V	1.05	1.1	1.15	V
			3 V	1.45	1.5	1.55	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected(6)	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1600			ns
			3 V	1600			

(1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}.When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
(2) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
$V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A$ = 0°C) [mV]
(3) Not ensured for T_A > 105°C.
(4) Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offset,sensor}$.
(5) No additional current is needed. The V_{MID} is used during sampling.
(6) The on time, $t_{VMID(on)}$, is included in the sampling time, $t_{VMID(sample)}$; no additional on time is needed.

5.36 Flash Memory(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC\ (PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program(2)		2.2 V/3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase(2)		2.2 V/3.6 V		1	7	mA
t_{CPT}	Cumulative program time(2)(3)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time(2)		2.2 V/3.6 V	20			ms
	Program and erase endurance(2)			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	See (4)			30		t_{FTG}
$t_{Block,\ 0}$	Block program time for first byte or word	See (4)			25		t_{FTG}
$t_{Block,\ 1-63}$	Block program time for each additional byte or word	See (4)			18		t_{FTG}
$t_{Block,\ End}$	Block program end-sequence wait time	See (4)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	See (4)			10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	See (4)			4819		t_{FTG}

(1) Additional flash retention documentation located in application report SLAA392.
(2) Not ensured for T_A > 105°C.
(3) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(4) These values are hardwired into the flash controller's state machine (t_{FTG} = 1/f_{FTG}).

5.37 RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage(1)	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

5.38 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	T_A = -40°C to 105°C	2.2 V, 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	T_A = -40°C to 105°C	2.2 V, 3 V	0.025		15	µs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge(1))	T_A = -40°C to 105°C	2.2 V, 3 V			1	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time	T_A = -40°C to 105°C	2.2 V, 3 V	15		100	µs
f_{TCK}	TCK input frequency(2)	T_A = -40°C to 105°C	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pulldown resistance on TEST	T_A = -40°C to 105°C	2.2 V, 3 V	25	60	90	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

5.39 JTAG Fuse(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow	T_A = 25°C	6	7	V
I_{FB}	Supply current into TEST during fuse blow	T_A = 25°C		100	mA
t_{FB}	Time to blow fuse	T_A = 25°C		1	ms

(1) Once the fuse is blown, no further access to the JTAG/Test and emulation features is possible, and the JTAG block is switched to bypass mode.

5.40 Typical Characteristics - Active-Mode Supply Current (Into DV_{CC} + AV_{CC})

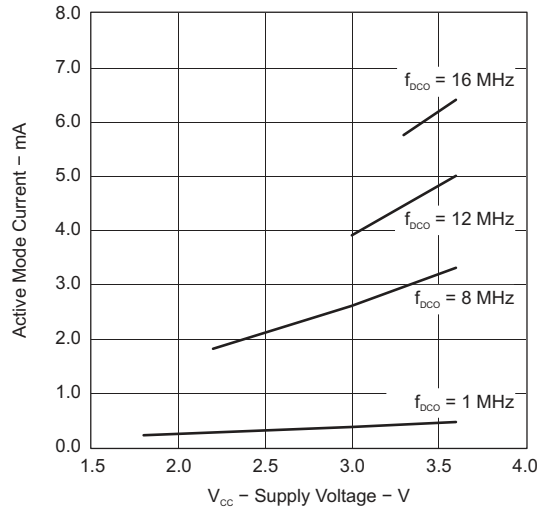


Figure 12. Active-Mode Current vs Supply Voltage T_A = 25°C

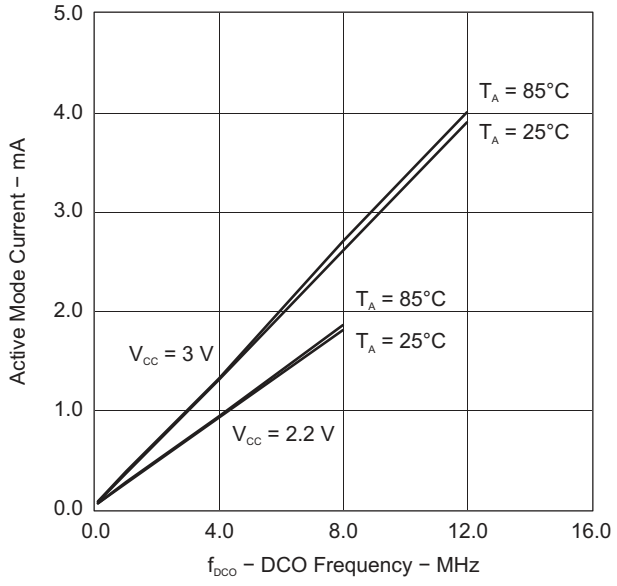


Figure 13. Active-Mode Current vs DCO Frequency

5.41 Typical Characteristics - LPM4 Current

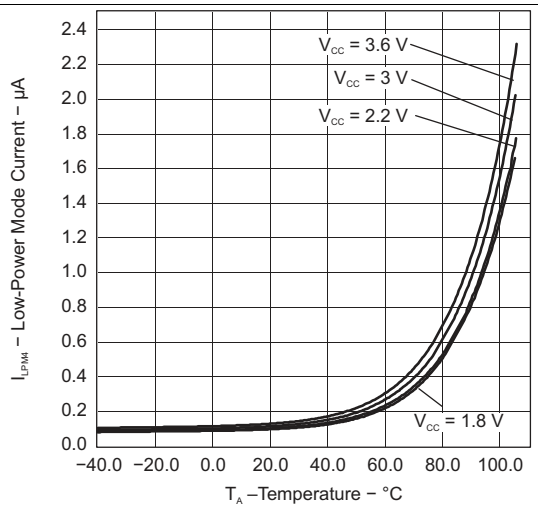


Figure 14. LPM4 Current vs Temperature

5.42 Typical Characteristics - Outputs

One output loaded at a time.

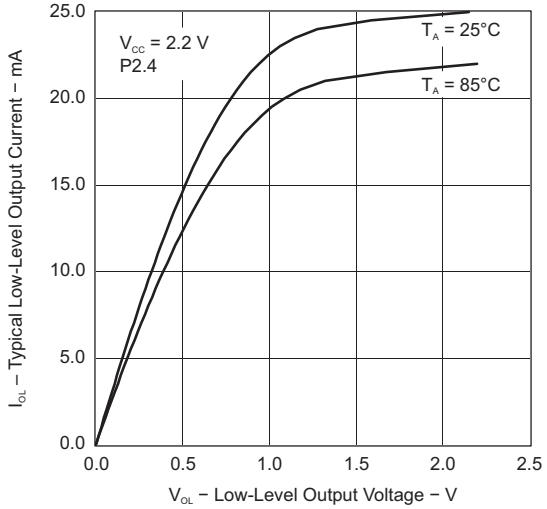


Figure 15. Typical Low-Level Output Current vs Low-Level Output Voltage

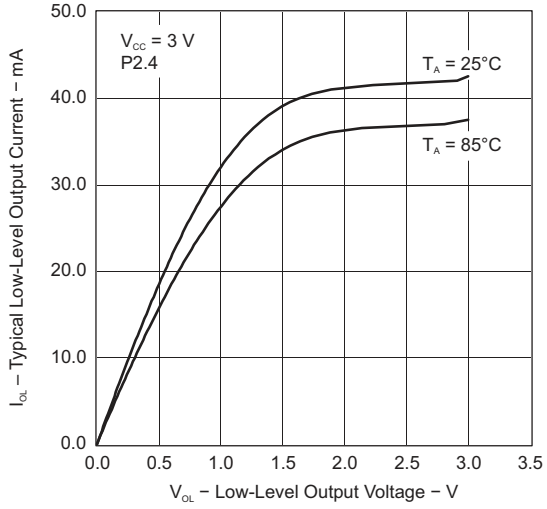


Figure 16. Typical Low-Level Output Current vs Low-Level Output Voltage

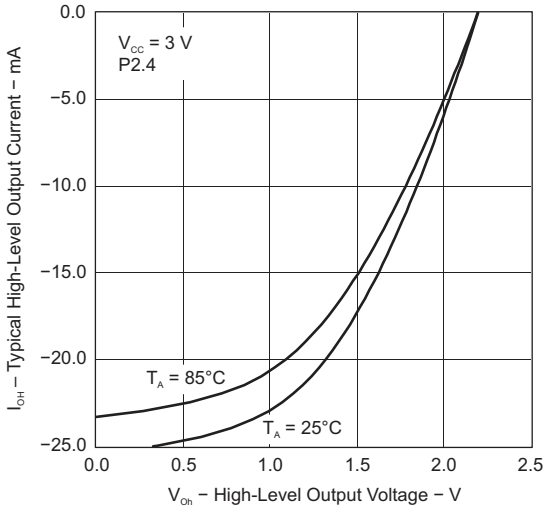


Figure 17. Typical High-Level Output Current vs High-Level Output Voltage

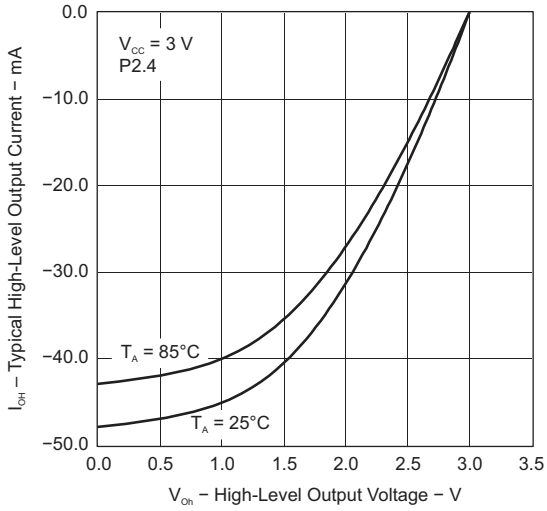


Figure 18. Typical High-Level Output Current vs High-Level Output Voltage

5.43 Typical Characteristics - POR/Brownout Reset (BOR)

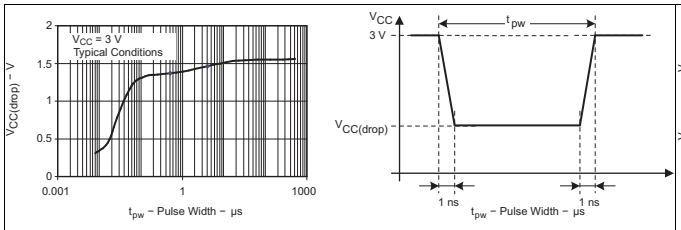


Figure 19. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR or BOR Signal

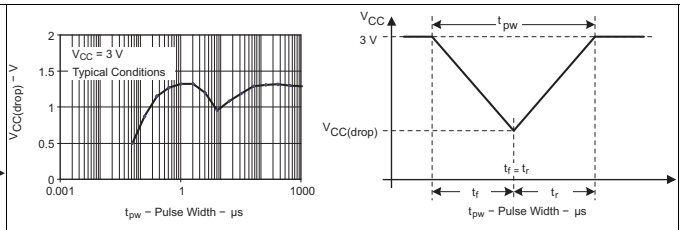


Figure 20. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR or BOR Signal

5.44 Typical Characteristics - Calibrated 1-MHz DCO Frequency

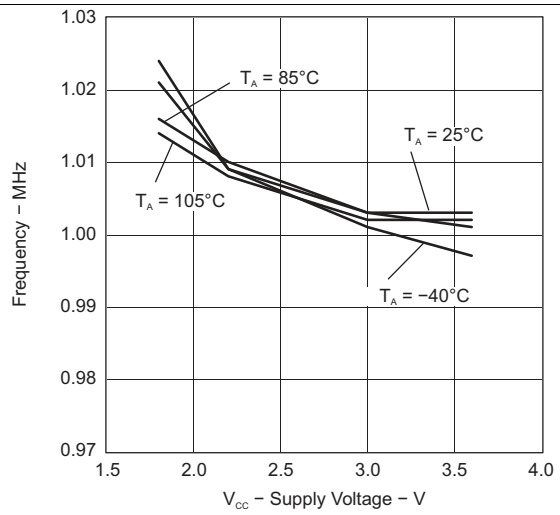


Figure 21. Calibrated 1-MHz Frequency vs Supply Voltage

5.45 Typical Characteristics - DCO Clock Wake-Up Time From LPM3/4

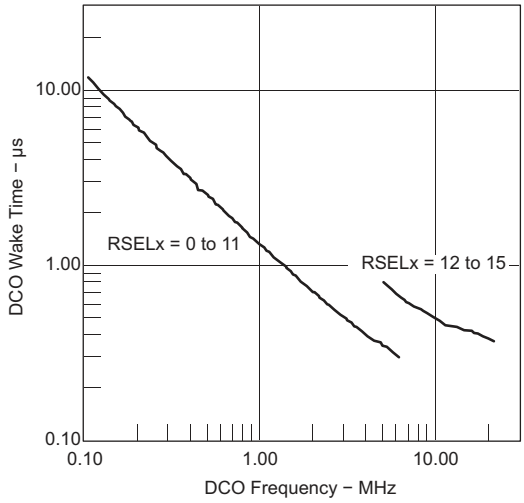


Figure 22. Clock Wake-Up Time From LPM3 vs DCO Frequency

5.46 Typical Characteristics - DCO With External Resistor R_{OSC}

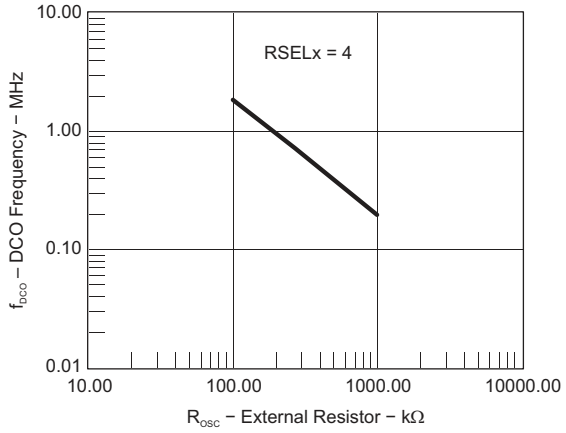


Figure 23. DCO Frequency vs R_{OSC} V_{CC} = 2.2 V, T_A = 25°C

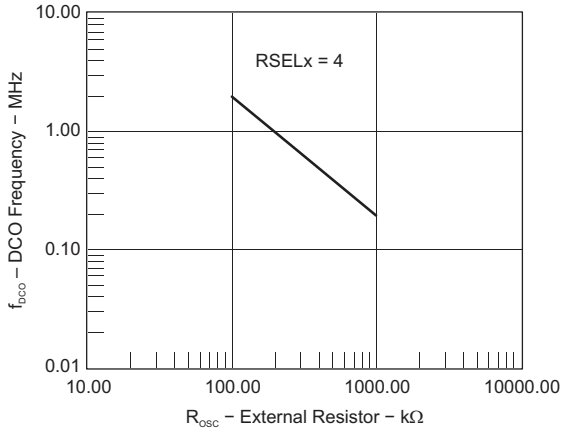


Figure 24. DCO Frequency vs R_{OSC} V_{CC} = 3 V, T_A = 25°C

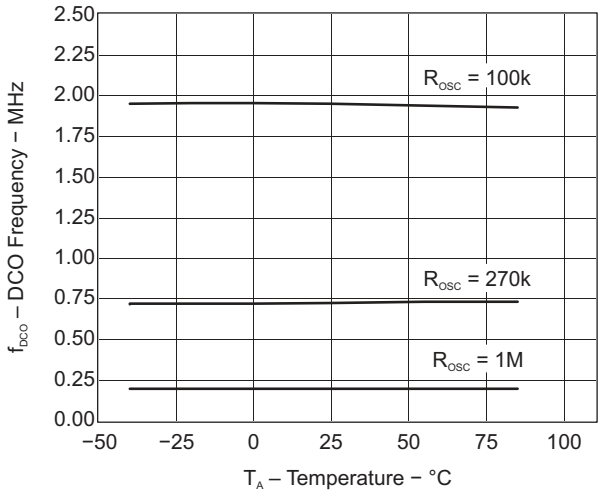


Figure 25. DCO Frequency vs Temperature V_{CC} = 3 V

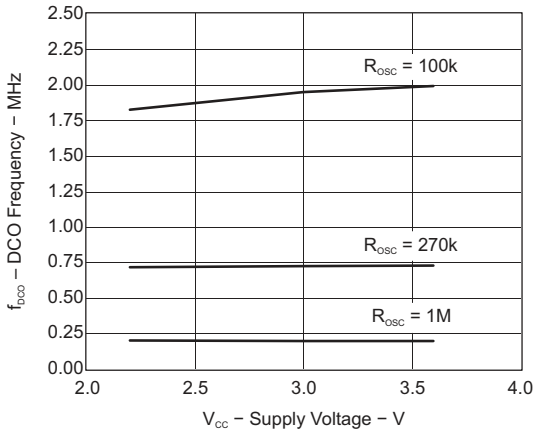


Figure 26. DCO Frequency vs Supply Voltage T_A = 25°C

5.47 Typical Characteristics - LFXT1 Oscillator in HF Mode (XTS = 1)

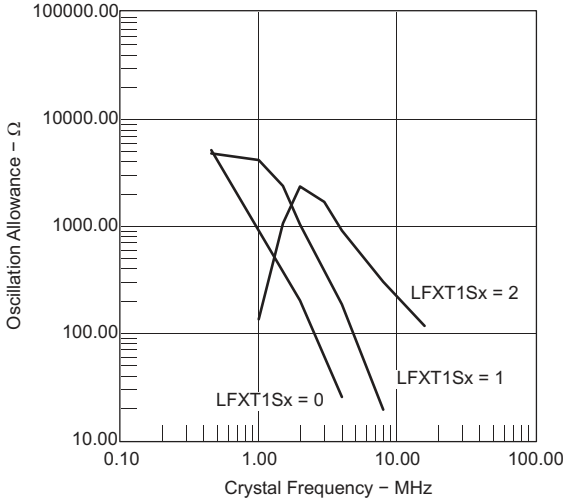


Figure 27. Oscillation Allowance vs Crystal Frequency $C_{L,eff}$ = 15 pF, T_A = 25°C

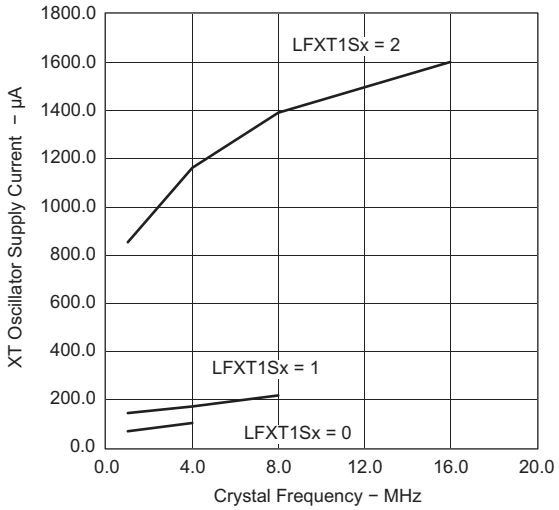


Figure 28. Oscillator Supply Current vs Crystal Frequency $C_{L,eff}$ = 15 pF, T_A = 25°C

5.48 Typical Characteristics - Comparator_A+

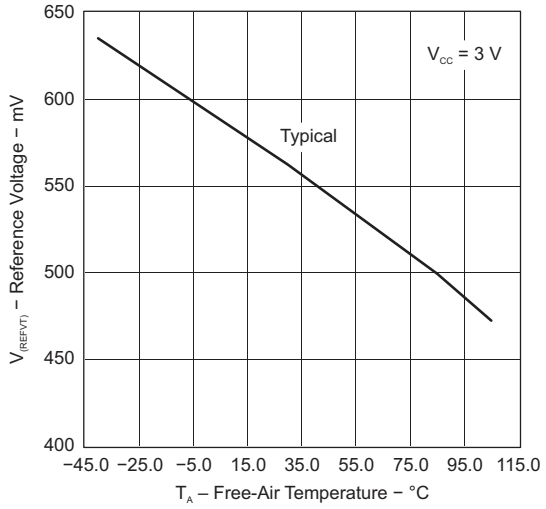


Figure 29. $V_{(RefVT)}$ vs Temperature V_{CC} = 2.2 V

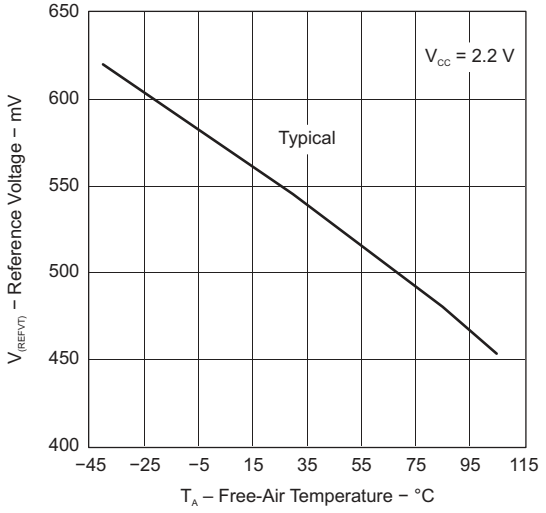


Figure 30. $V_{(RefVT)}$ vs Temperature V_{CC} = 2.2 V

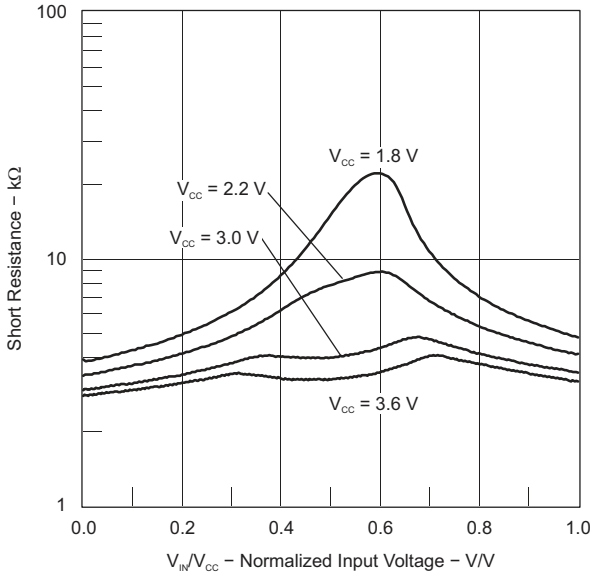


Figure 31. Short Resistance vs V_{IN}/V_{CC}

6 Application Information

6.1 Port P1 Pin Schematic: P1.0, Input/Output With Schmitt Trigger

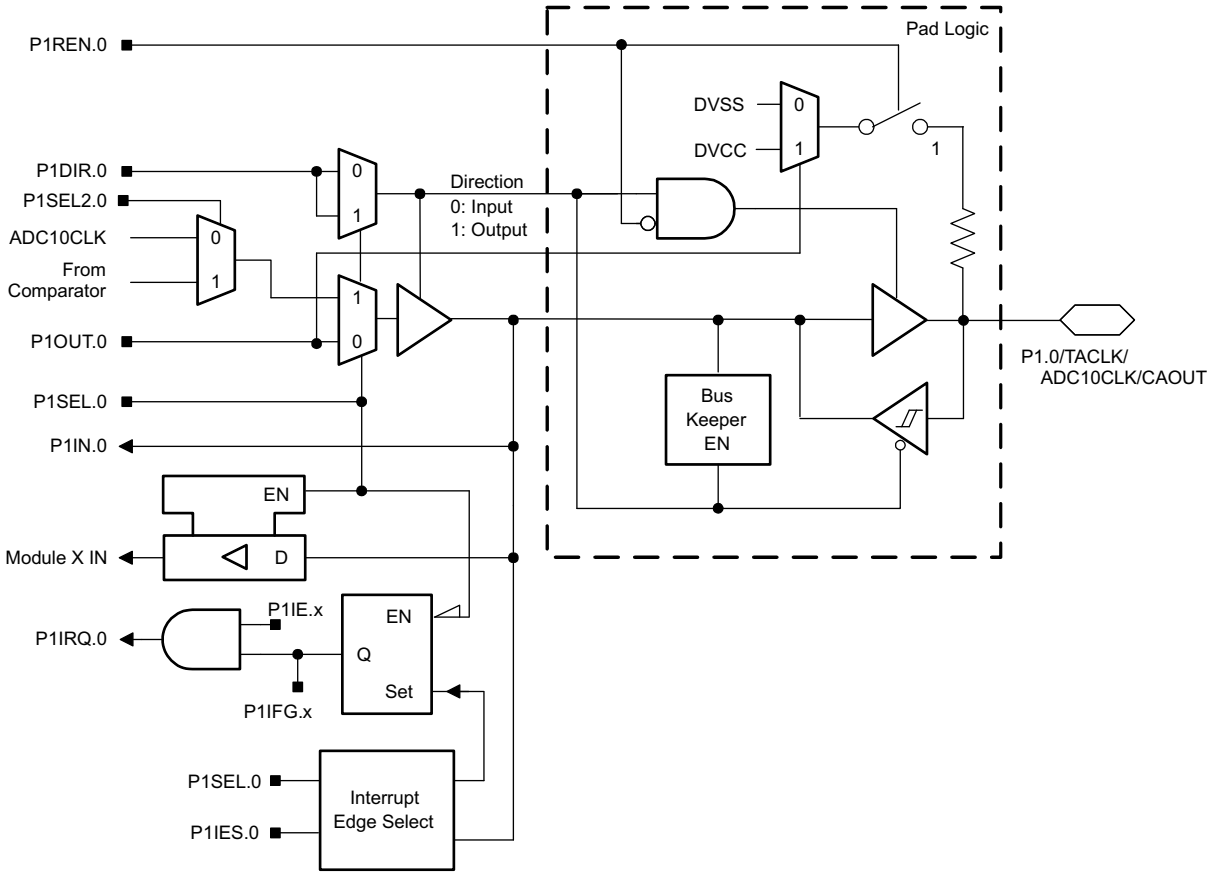


Table 16. Port P1 (P1.0) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS		
			P1DIR.x	P1SEL.x	P1SEL2.x
P1.0/TACLK/ ADC10CLK/CAOUT	0	P1.0 (I/O)	I: 0, O: 1	0	0
		Timer0_A3.TACLK, Timer1_A2.TACLK	0	1	0
		ADC10CLK	1	1	0
		CAOUT	1	1	1

6.2 Port P1 Pin Schematic: P1.1 to P1.3, Input/Output With Schmitt Trigger

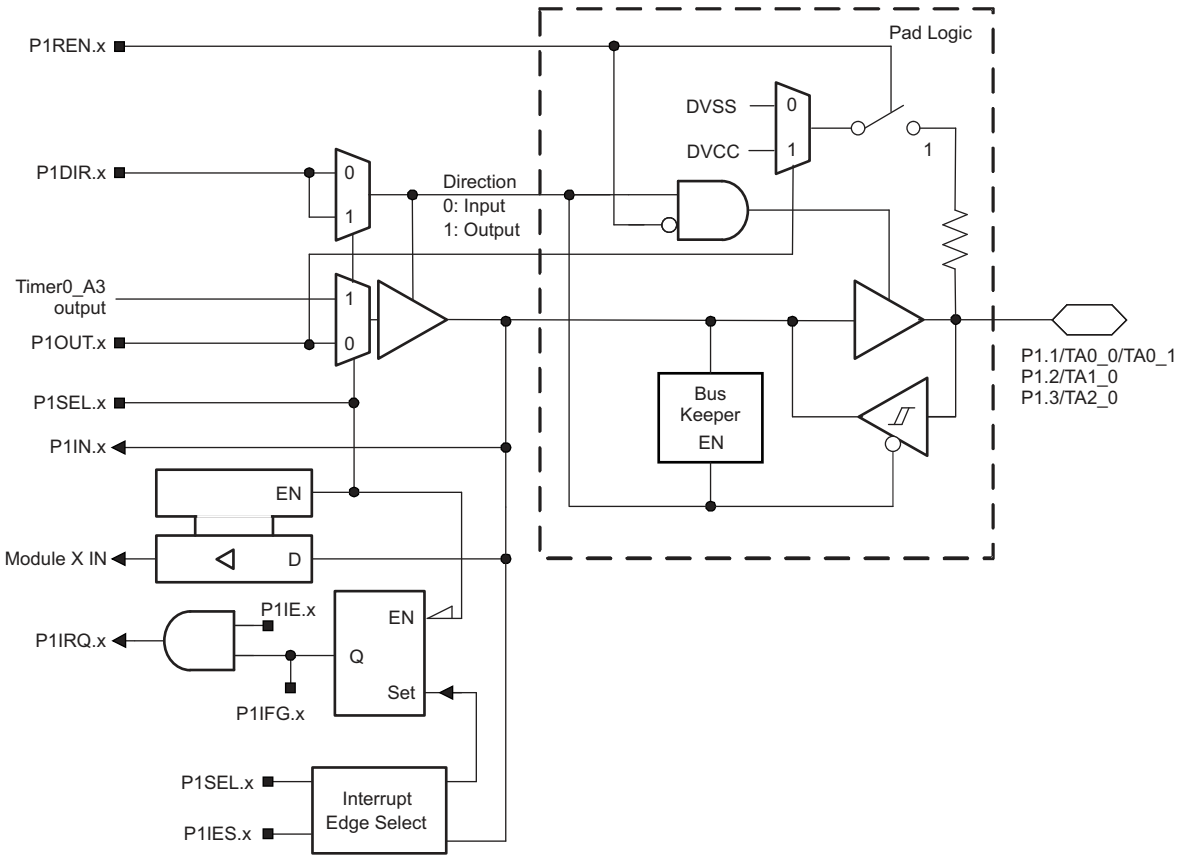


Table 17. Port P1 (P1.1 to P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS		
			P1DIR.x	P1SEL.x	P1SEL2.x
P1.1/TA0.0/TA1.0	1	P1.1 (I/O)	I: 0; O: 1	0	0
		Timer0_A3.CCI0A, Timer1_A2.CCI0A	0	1	0
		Timer0_A3.TA0	1	1	0
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0	0
		Timer0_A3.CCI1A	0	1	0
		Timer0_A3.TA1	1	1	0
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0	0
		Timer0_A3.CCI2A	0	1	0
		Timer0_A3.TA2	1	1	0

6.3 Port P1 Pin Schematic: P1.4

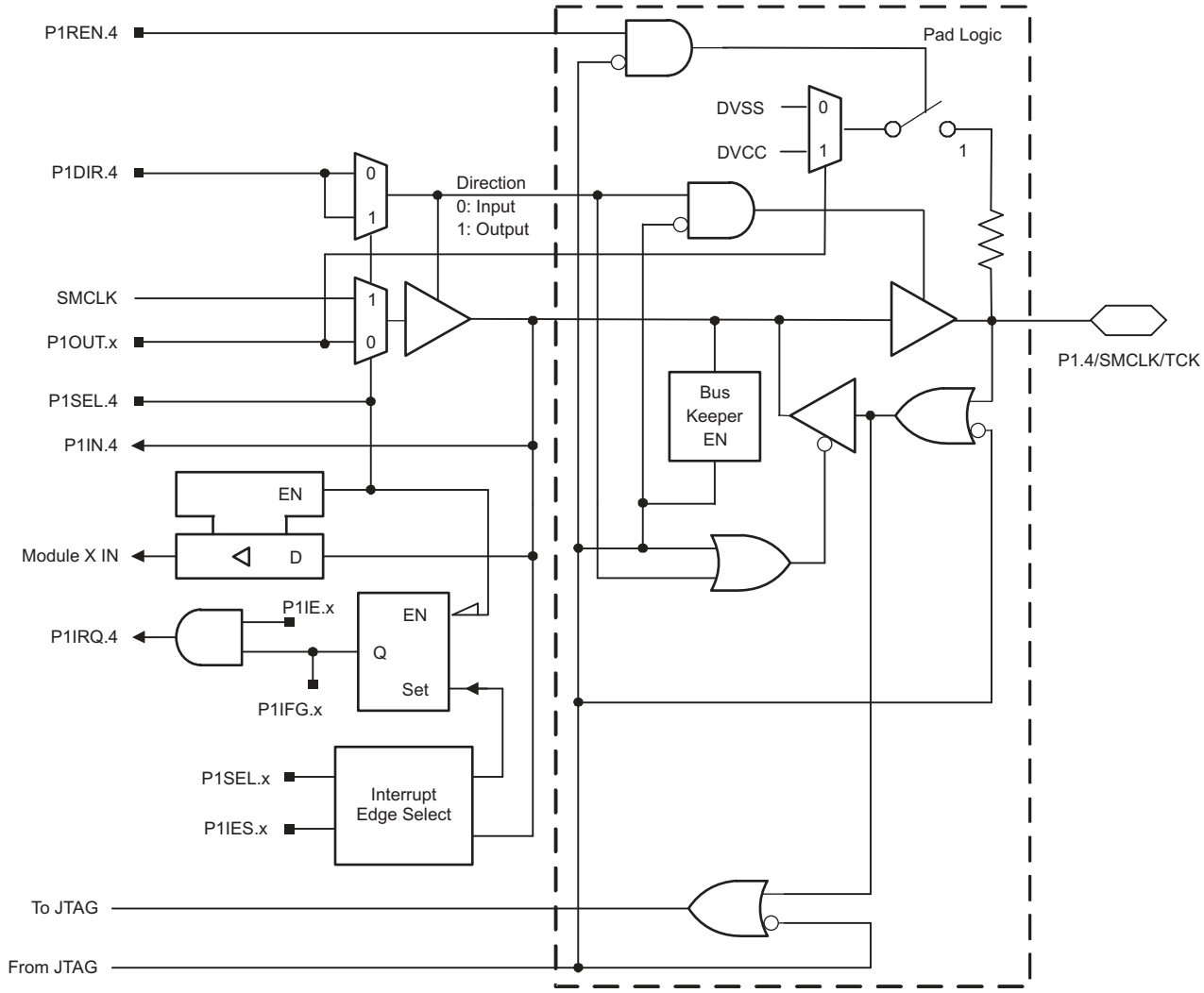


Table 18. Port P1 (P1.4) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P1DIR.x	P1SEL.x P1SEL2.x=0	JTAG Mode
P1.4/SMCLK/TCK	4	P1.4 (I/O)	I: 0; O: 1	0	0
		SMCLK	1	1	0
		TCK[2]	X	X	1

(1) X = Don't care
(2) In JTAG mode, the internal pullup or pulldown resistors are disabled.

6.4 Port P1 Pin Schematic: P1.5 to P1.7

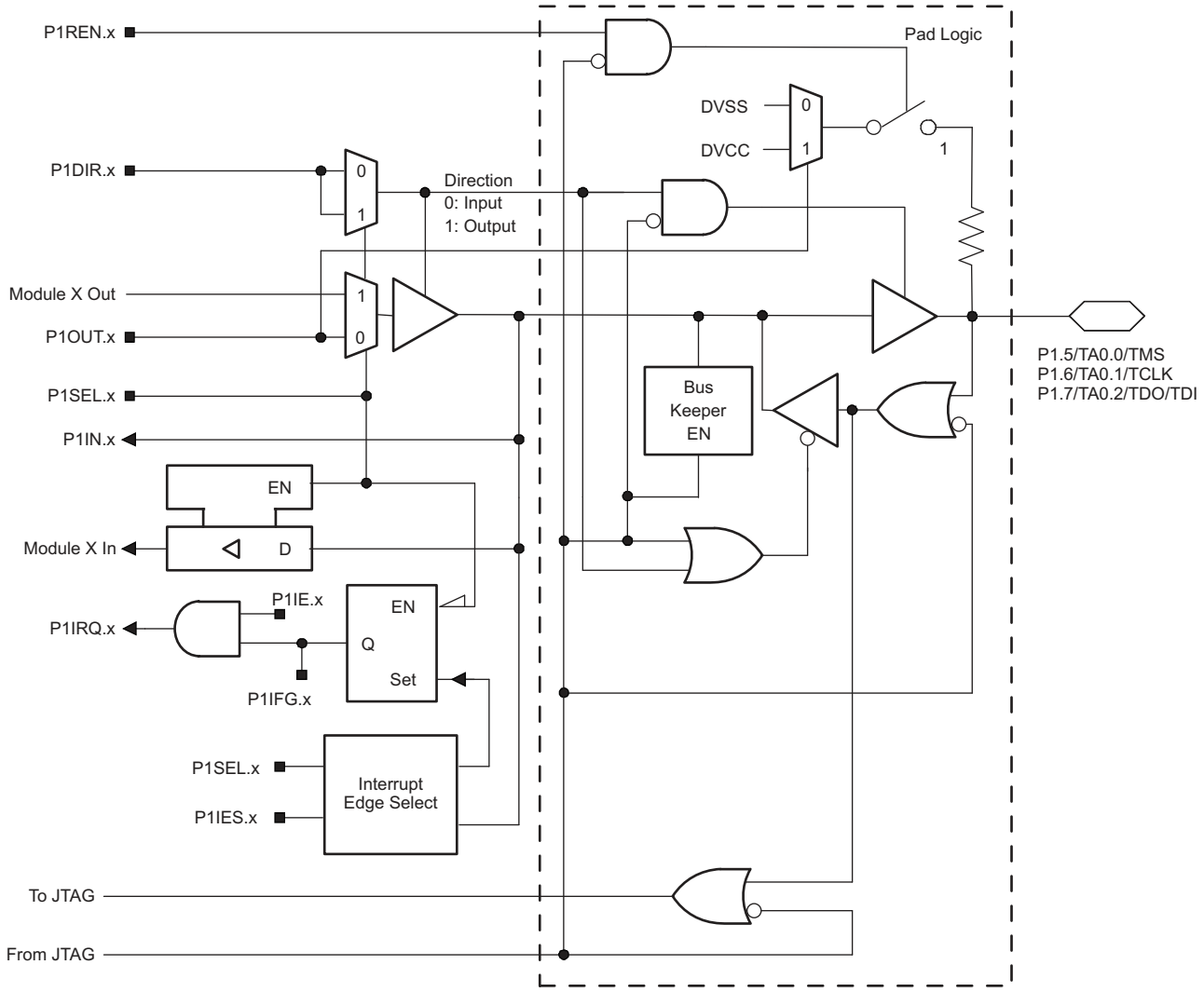


Table 19. Port P1 (P1.5 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P1DIR.x	P1SEL.x P1SEL2.x=0	JTAG Mode
P1.5/TA0.0/TMS	5	P1.5 (I/O)	I: 0; O: 1	0	0
		Timer0_A3.TA0	1	1	0
		TMS[2]	X	X	1
P1.6/TA0.1/TDI/TCLK	6	P1.6 (I/O)	I: 0; O: 1	0	0
		Timer0_A3.TA1	1	1	0
		TDI/TCLK[2]	X	X	1
P1.7/TA0.2/TDO/TDI	7	P1.6 (I/O)	I: 0; O: 1	0	0
		Timer0_A3.TA2	1	1	0
		TDO/TDI[2]	X	X	1

(1) X = Don't care
(2) In JTAG mode, the internal pullup or pulldown resistors are disabled.

6.5 Port P2 Pin Schematic: P2.0 and P2.1, Input/Output With Schmitt Trigger

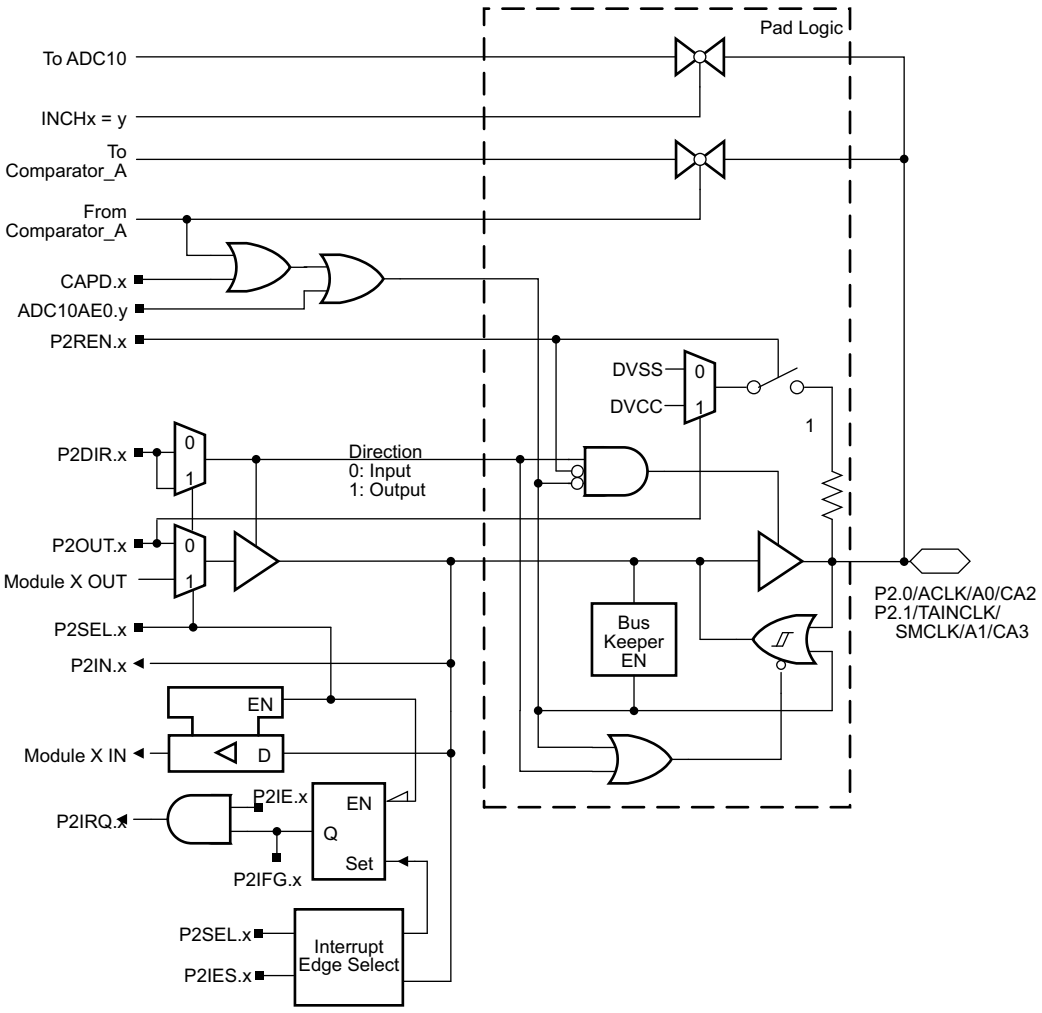


Table 20. Port P2 (P2.0 and P2.1) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)			
			ADC10AE0.y	CAPD.x	P2DIR.x	P2SEL.x P2SEL2.x = 0
P2.0/ACLK/A0/CA2	0	P2.0 (I/O)	0	0	I: 0; O: 1	0
		ACLK	0	0	1	1
		A0	1	0	X	X
		CA2	0	1	X	X
P2.1/TAINCLK/ SMCLK/A1/CA3	1	P2.1 (I/O)	0	0	I: 0; O: 1	0
		Timer0_A3.TAINCLK, Timer1_A2.TAINCLK	0	0	0	1
		SMCLK	0	0	1	1
		A1	1	0	X	X
		CA3	0	1	X	X

(1) X = Don't care

6.6 Port P2 Pin Schematic: P2.2, Input/Output With Schmitt Trigger

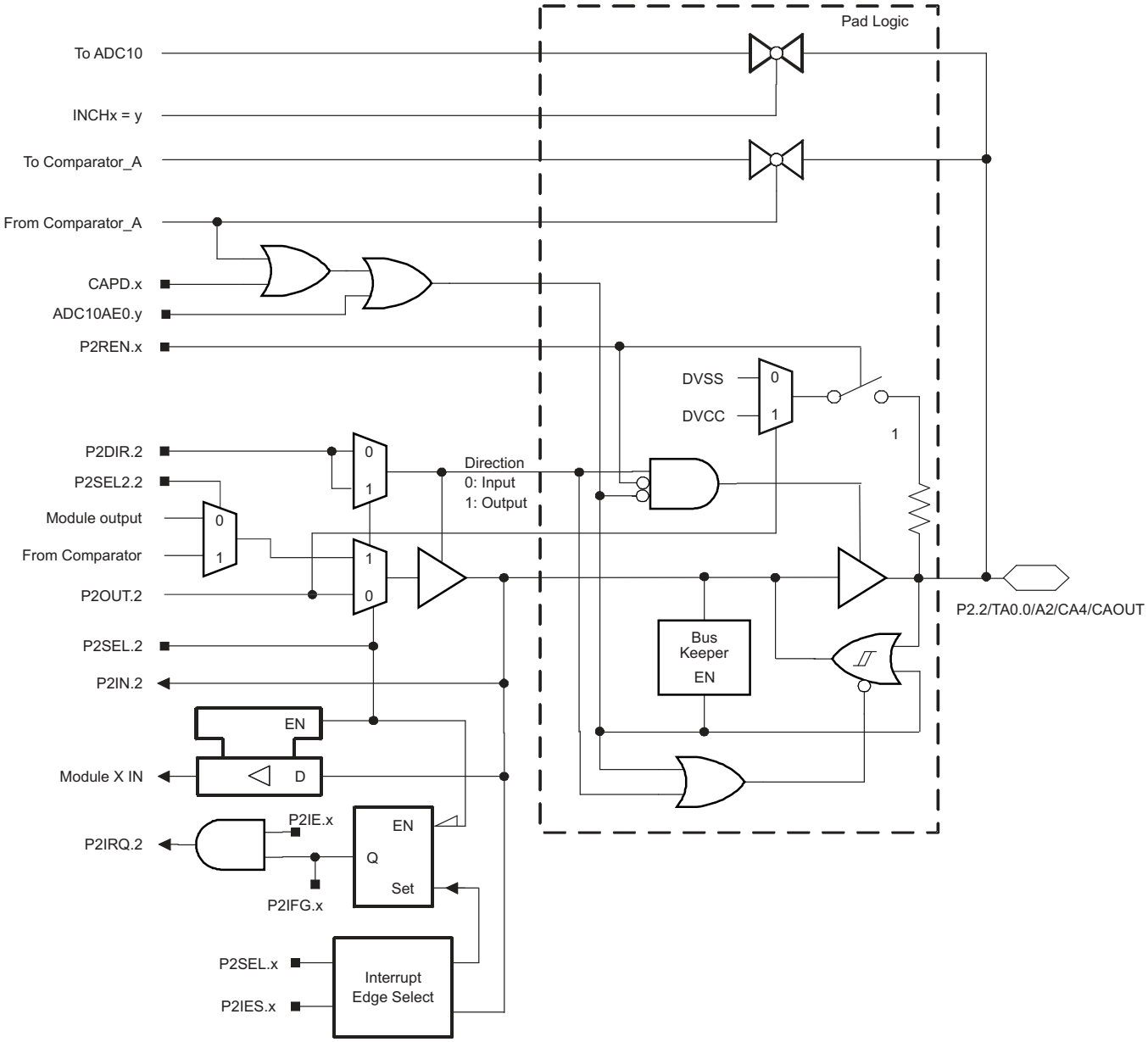


Table 21. Port P2 (P2.2) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]				
			ADC10AE0.x	CAPD.x	P2DIR.x	P2SEL.x	P2SEL2.x
P2.2/TA0.0/A2/CA4/CAOUT	2	P2.0 (I/O)	0	0	I: 0; O: 1	0	0
		Timer0_A3.TA0	0	0	1	1	0
		Timer0_A3.CCI0B	0	0	0	1	0
		A2	1	0	X	X	X
		CA4	0	1	X	X	X
		CAOUT	0	0	1	1	1

(1) X = Don't care

6.7 Port P2 Pin Schematic: P2.3 and P2.4, Input/Output With Schmitt Trigger

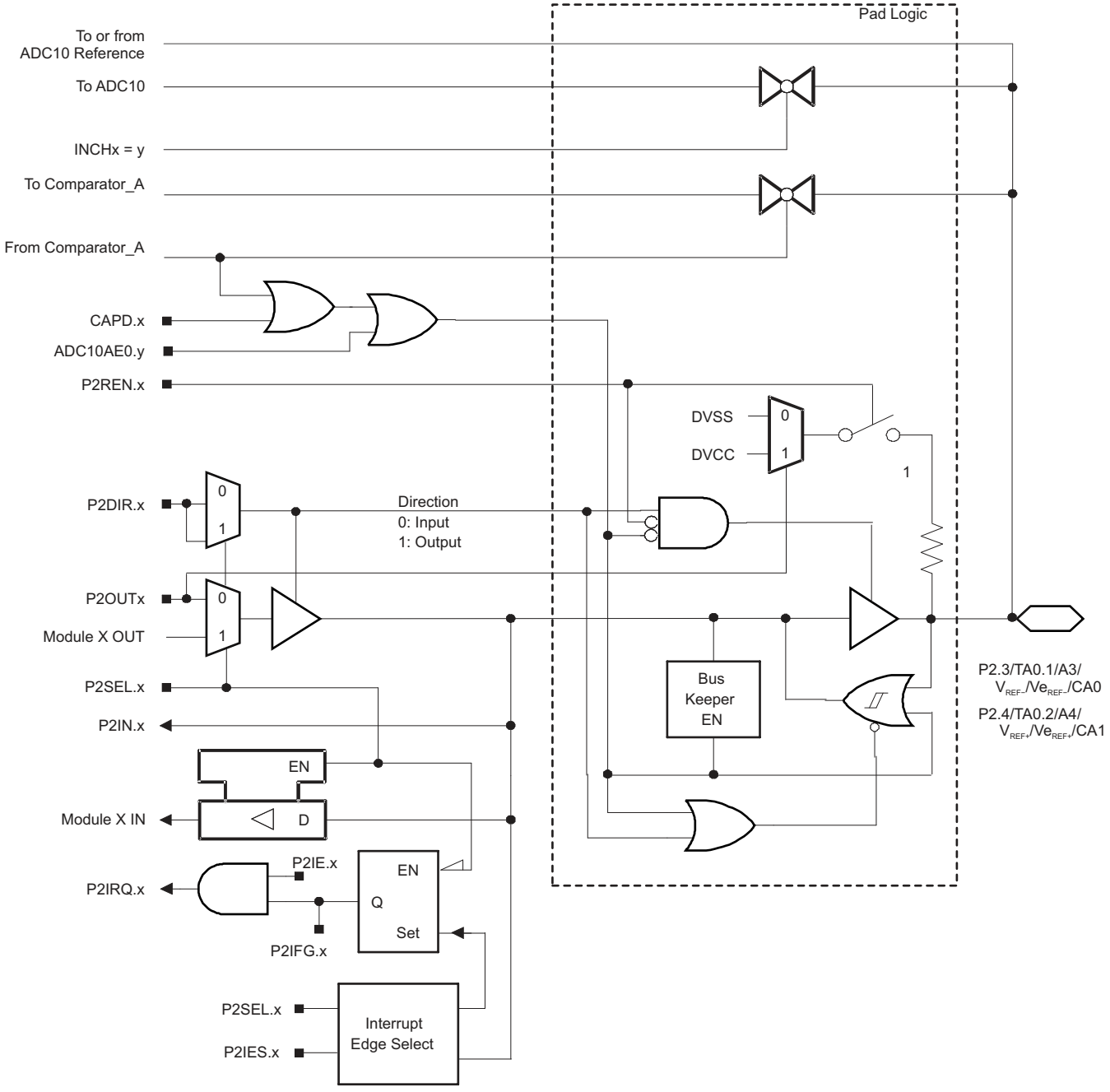


Table 22. Port P2 (P2.3 and P2.4) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]			
			ADC10AE0.y	CAPD.x	P2DIR.x	P2SEL.x P2SEL2.x = 0
P2.3/TA0.1/A3/ V_{REF-}/Ve_{REF-} /CA0	3	P2.3 (I/O)	0	0	I: 0; O: 1	0
		Timer0_A3.TA1	0	0	1	1
		A3/V_{REF-}/Ve_{REF-}	1	0	X	X
		CA0	0	1	X	X

(1) X = Don't care

Port P2 Pin Schematic: P2.3 and P2.4, Input/Output With Schmitt Trigger (continued)

Table 22. Port P2 (P2.3 and P2.4) Pin Functions (continued)

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]			
			ADC10AE0.y	CAPD.x	P2DIR.x	P2SEL.x P2SEL2.x = 0
P2.4/TA0.2/A4/ V_{REF+}/Ve_{REF+}/CA1	4	P2.4 (I/O)	0	0	I: 0; O: 1	0
		Timer0_A3.TA2	0	0	1	1
		A4/V_{REF+}/Ve_{REF+}	1	0	X	X
		CA1	0	1	X	X

6.8 Port P2 Pin Schematic: P2.5, Input/Output With Schmitt Trigger

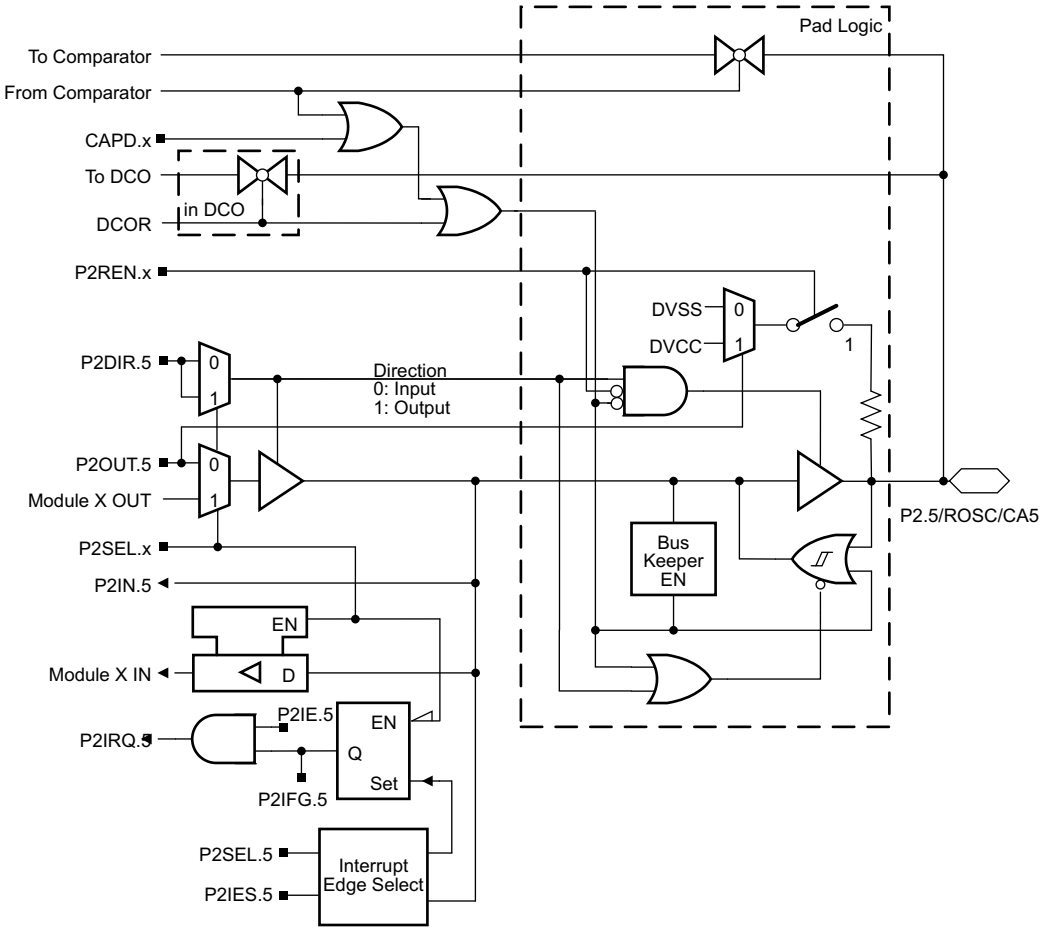


Table 23. Port P2 (P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)			
			CAPD.5	DCOR	P2DIR.5	P2SEL.5 P2SEL2.x = 0
P2.5/R_{OSC}/CA5	5	P2.5 (I/O)	0	0	I: 0, O: 1	0
		R_{OSC}	0	1	X	X
		DVSS	0	0	1	1
		CA5(2)	1	0	X	X

(1) X = Don't care
(2) Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

6.9 Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger

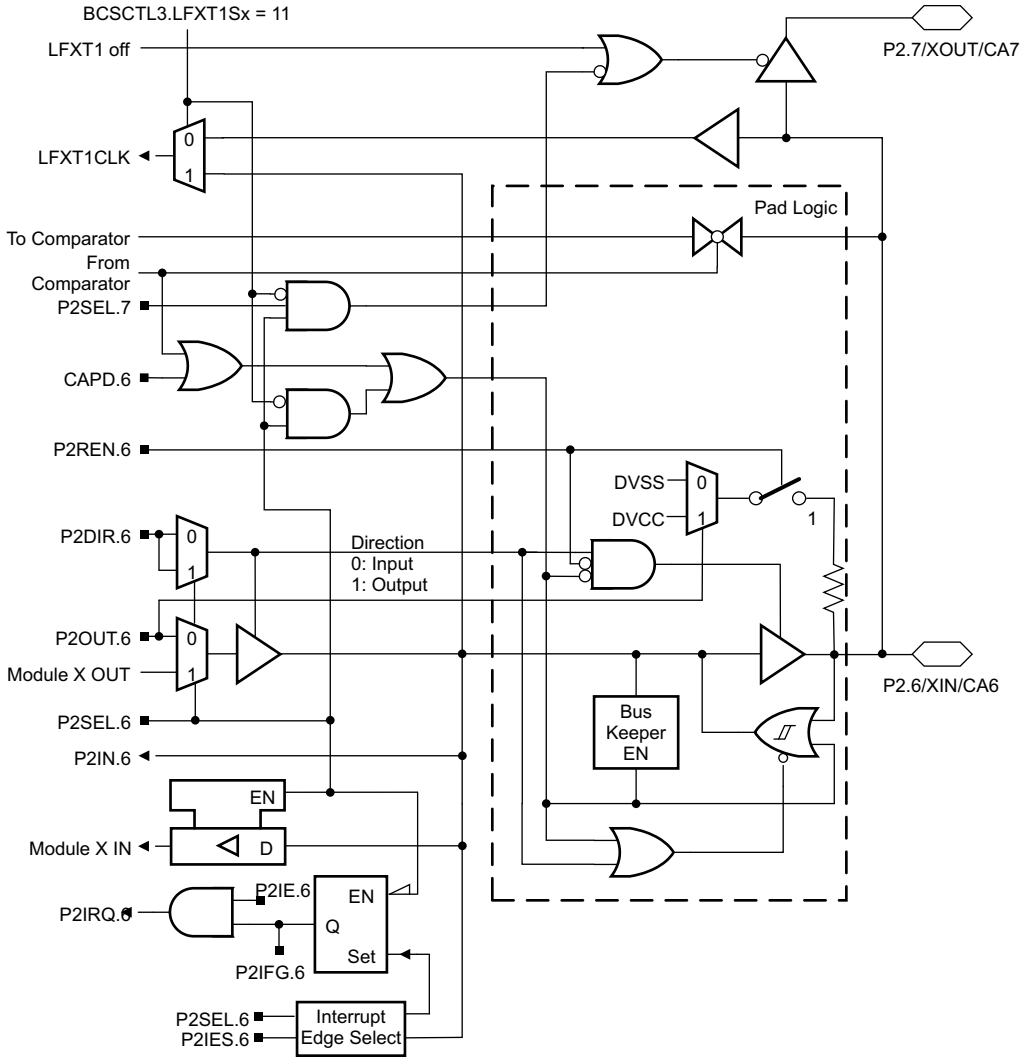


Table 24. Port P2 (P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			CAPD.6	P2DIR.6	P2SEL.6 P2SEL2.x = 0
P2.6/XIN/CA6	6	P2.6 (I/O)	0	I: 0; O: 1	0
		XIN (default)	X	1	1
		CA6[2]	1	X	0

(1) X = Don't care
(2) Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

6.10 Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger

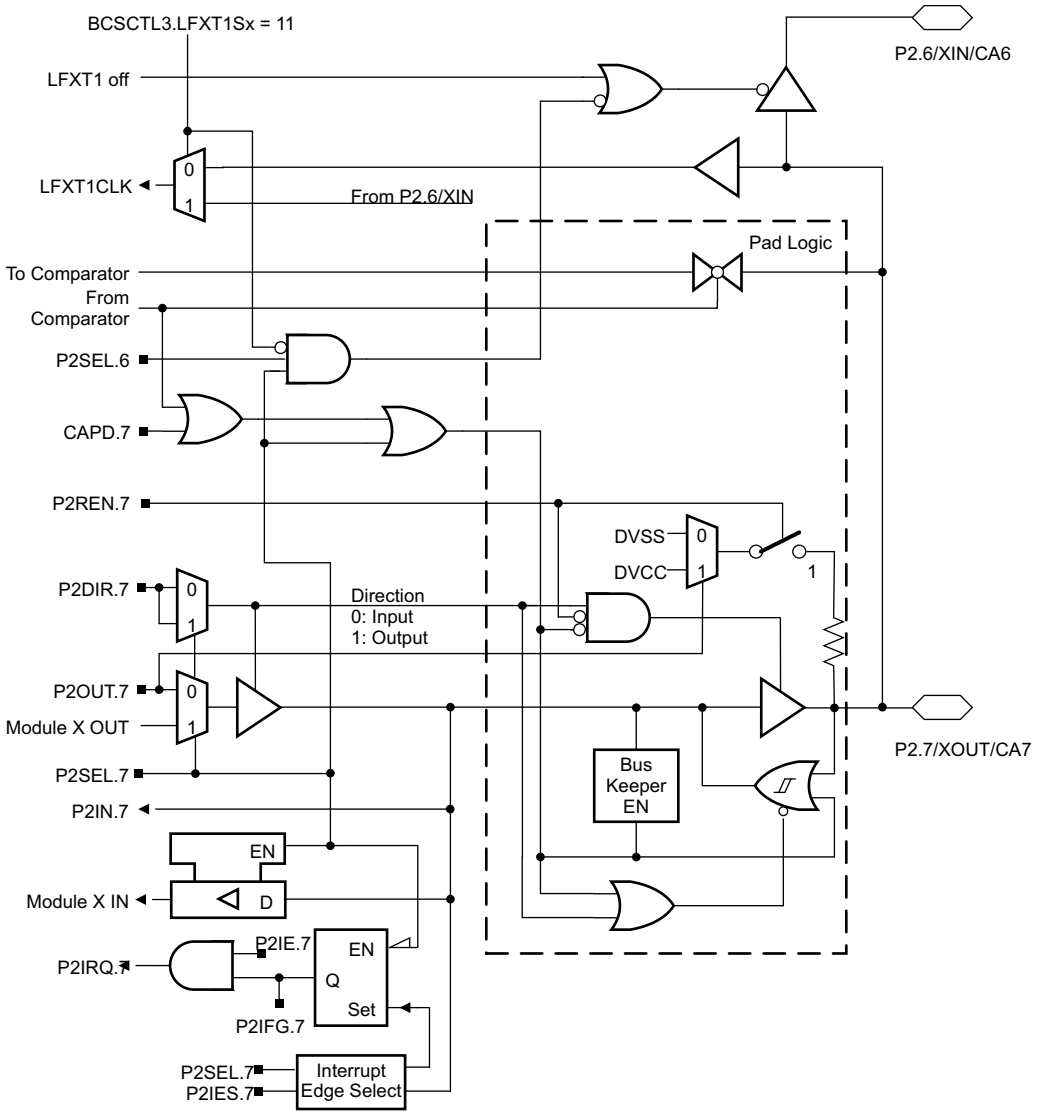


Table 25. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			CAPD.7	P2DIR.7	P2SEL.7 P2SEL2.x = 0
P2.7/XOUT/CA7	7	P2.7 (I/O)	0	I: 0, O: 1	0
		XOUT (default)	X	1	1
		CA7[2]	1	X	0

(1) X = Don't care
(2) Setting the CAPD.x bit disables the output driver as well as the input to prevent parasitic cross currents when applying analog signals. Selecting the CAx input to the comparator multiplexer with the P2CAx bits automatically disables the input buffer for that pin, regardless of the state of the associated CAPD.x bit.

6.11 Port P3 Pin Schematic: P3.0, Input/Output With Schmitt Trigger

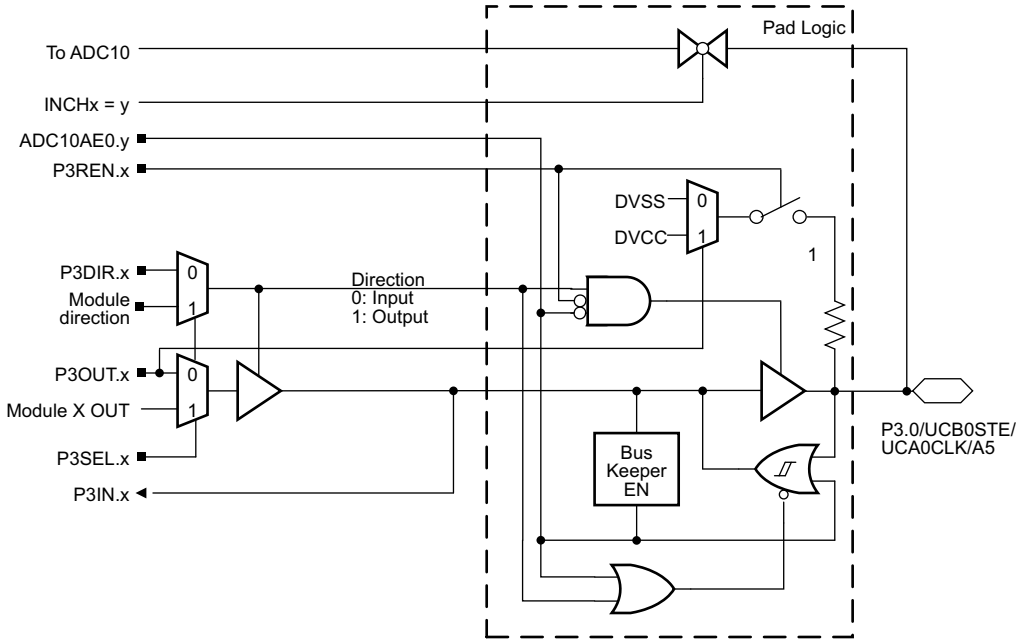


Table 26. Port P3 (P3.0) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			ADC10AE0.y	P3DIR.x	P3SEL.x P3SEL2.x = 0
P3.0/UCB0STE/ UCA0CLK/A5	0	P3.0 (I/O)	0	I: 0; O: 1	0
		UCB0STE/UCA0CLK[2]	0	X	1
		A5[2]	1	X	X

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.

6.12 Port P3 Pin Schematic: P3.1 to P3.5, Input/Output With Schmitt Trigger

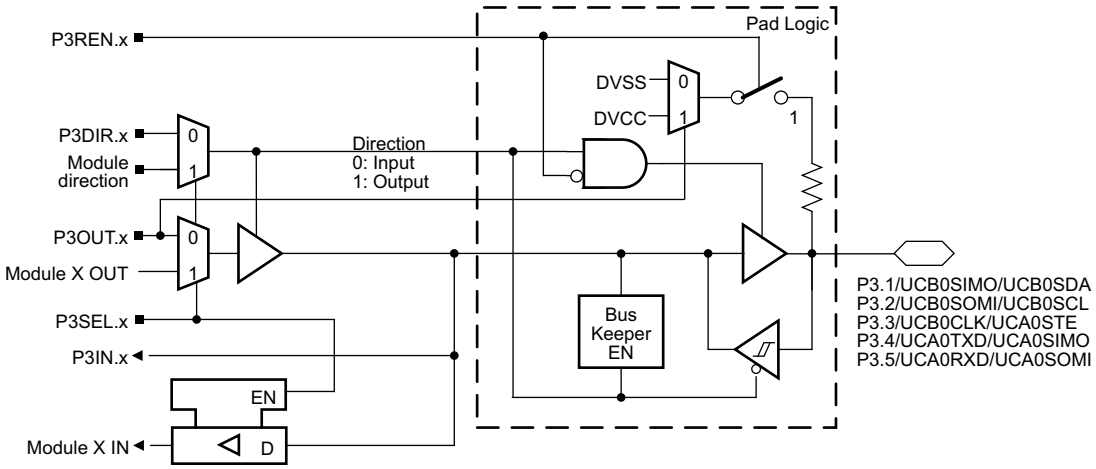


Table 27. Port P3 (P3.1 to P3.5) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]	
			P3DIR.x	P3SEL.x
P3.1/UCB0SIMO/ UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA[2][3]	X	1
P3.2/UCB0SOMI/ UCB0SCL	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL[2][3]	X	1
P3.3/UCB0CLK/ UCA0STE	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE[2]	X	1
P3.4/UCA0TXD/ UCA0SIMO	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO[2]	X	1
P3.5/UCA0RXD/ UCA0SOMI	5	P3.5 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI[2]	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

6.13 Port P3 Pin Schematic: P3.6 and P3.7, Input/Output With Schmitt Trigger

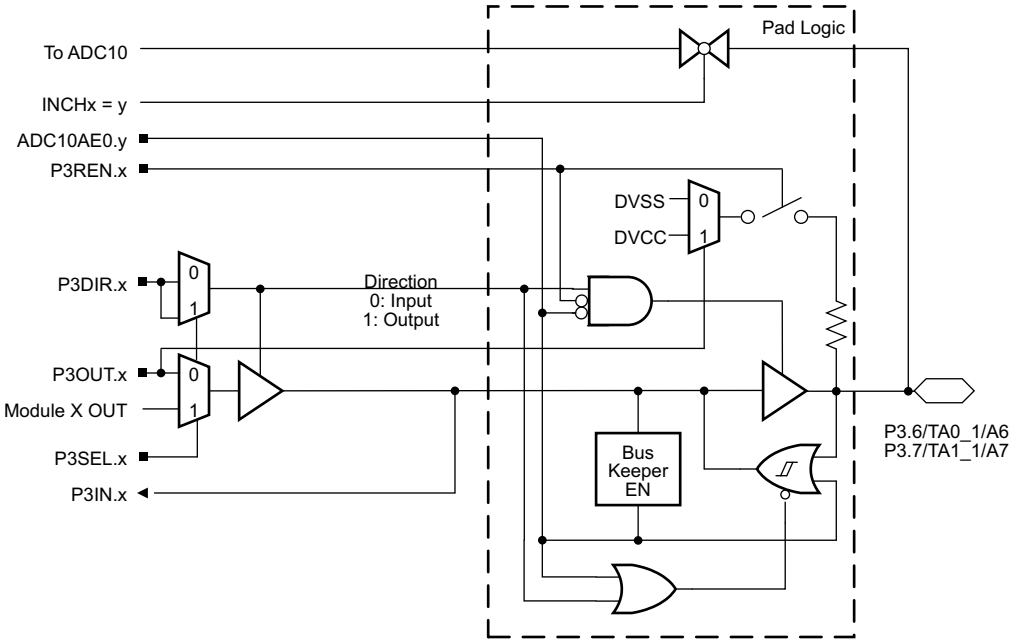


Table 28. Port P3 (P3.6 and P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			ADC10AE0.y	P3DIR.x	P3SEL.x
P3.6/TA1.0/A6	6	P3.6 (I/O)	0	I: 0; O: 1	0
		Timer1_A2.TA0	0	1	1
		Timer1_A2.CCI0B	0	0	1
		A6	1	X	X
P3.7/TA1.1/A7	7	P3.7 (I/O)	0	I: 0; O: 1	0
		Timer1_A2.TA1	0	1	1
		Timer1_A2.CCI1A	0	0	1
		A7	1	X	X

(1) X = Don't care

6.14 JTAG Fuse Check Mode

Devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 32). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

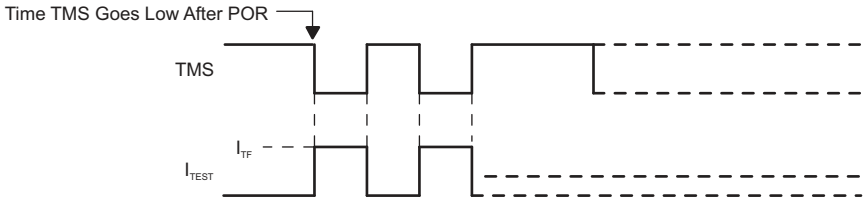


Figure 32. Fuse Check Mode Current

NOTE

The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the Bootstrap Loader section for more information.

7 Device and Documentation Support

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F2132QRHBREP	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F2132Q RHBEP	Samples
MSP430F2132QRHBTEP	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F2132Q RHBEP	Samples
V62/13624-01XE	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F2132Q RHBEP	Samples
V62/13624-01XE-R	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	F2132Q RHBEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSP430F2132-EP :

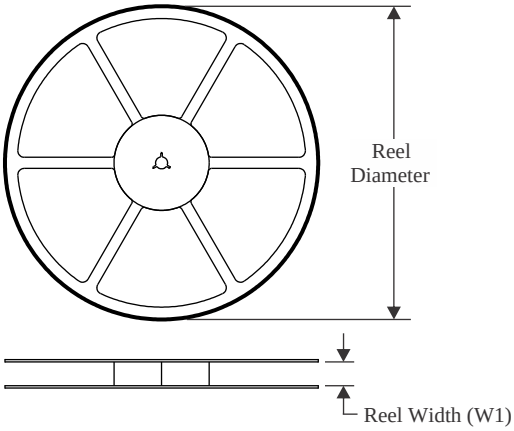
- Catalog: MSP430F2132

NOTE: Qualified Version Definitions:

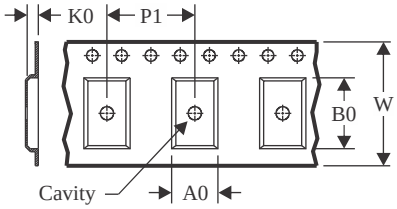
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

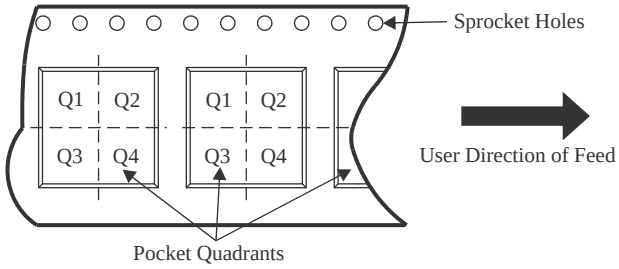


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

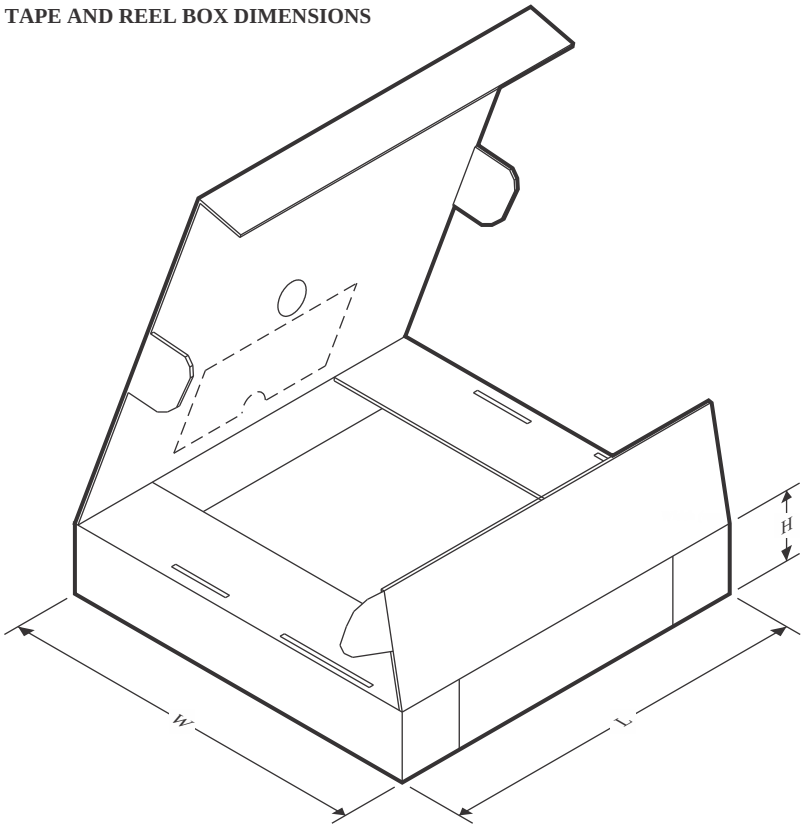
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2132QRHBREP	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
MSP430F2132QRHBTEP	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2132QRHBREP	VQFN	RHB	32	3000	356.0	356.0	35.0
MSP430F2132QRHBTEP	VQFN	RHB	32	250	210.0	185.0	35.0

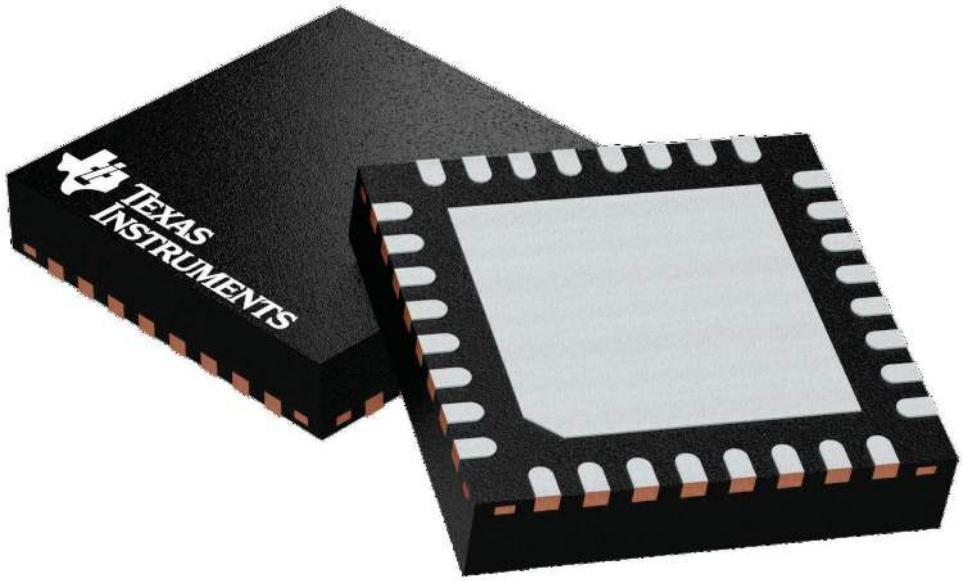
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

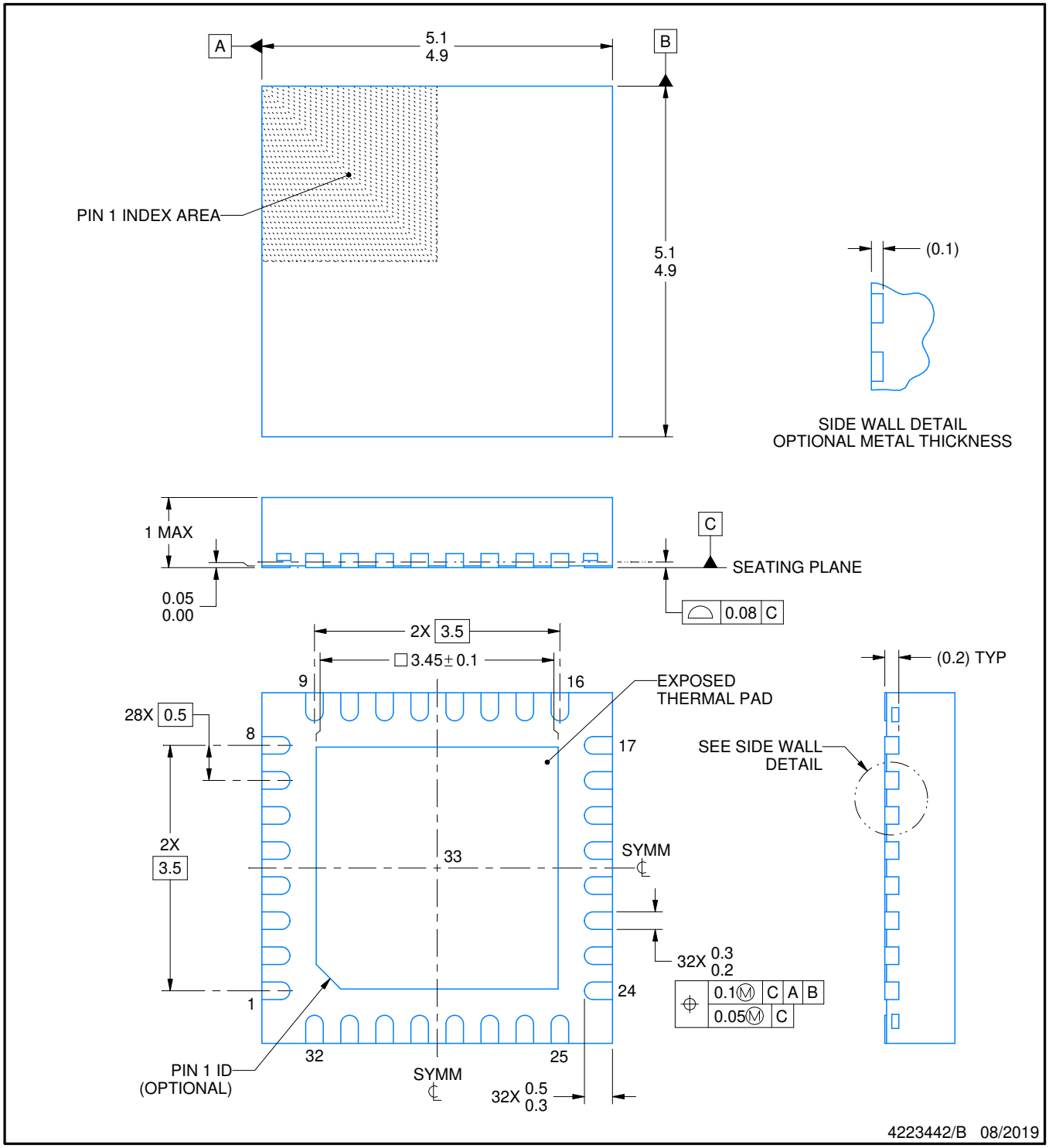
4224745/A

RHB0032E

PACKAGE OUTLINE

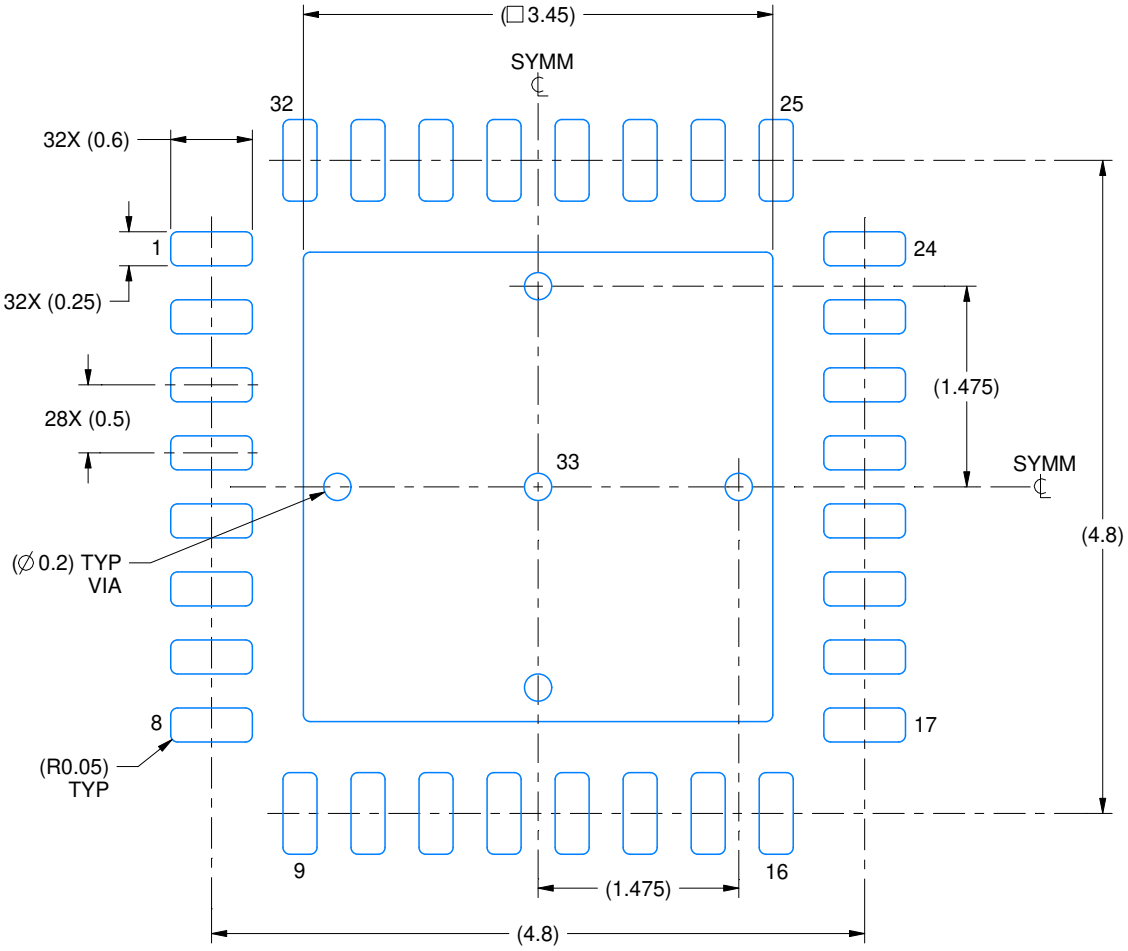
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

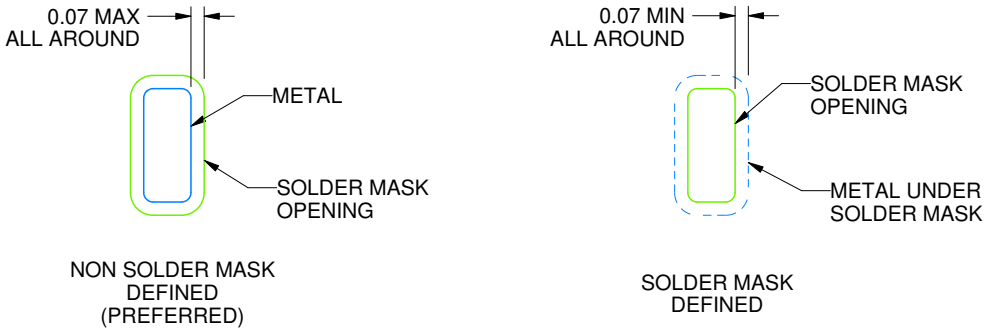


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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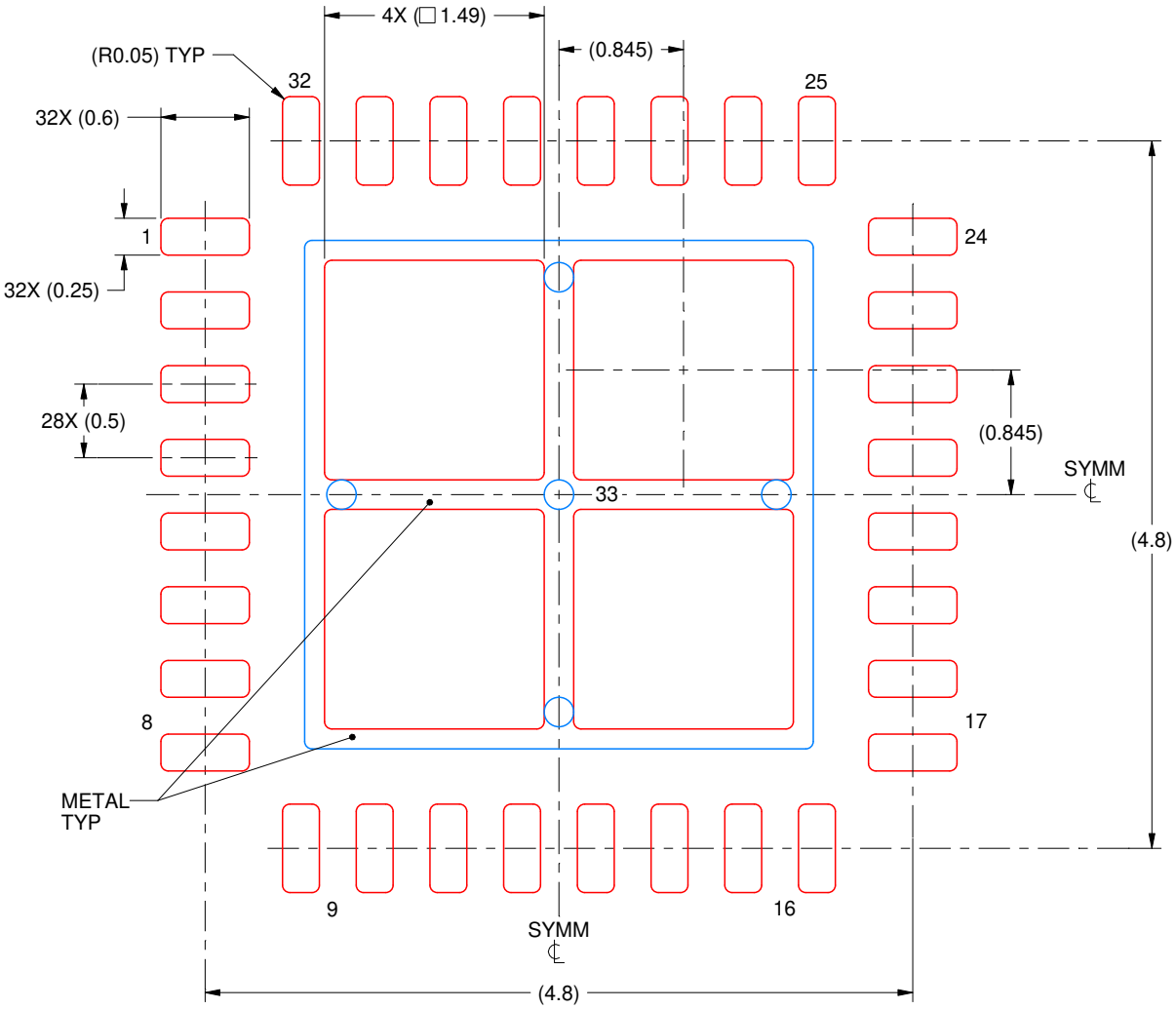
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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