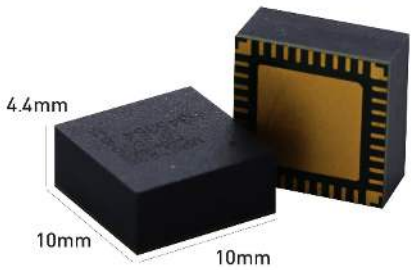
mEZDPD4506AS-84D8

mEZ6A-12Vin-3.3Vout-6A

DESCRIPTION

This device is a dual-phase, high-frequency, synchronous, stepdown power module with a PMBus control interface and configured for single output. It integrates internal high-side and low-side power MOSFETs and inductor with high efficiency, and is available in a LGA45 (10mmx10mmx4.4mm) package. With internal compensation network, this device offers a compact solution with a minimal standard external components.



SPECIFICATION OVERVIEW

I_{OUT}	6A
V_{OUT}	3.3V
Typical V_{IN}	12V
V_{IN} Min	9V
V_{IN} Max	15V

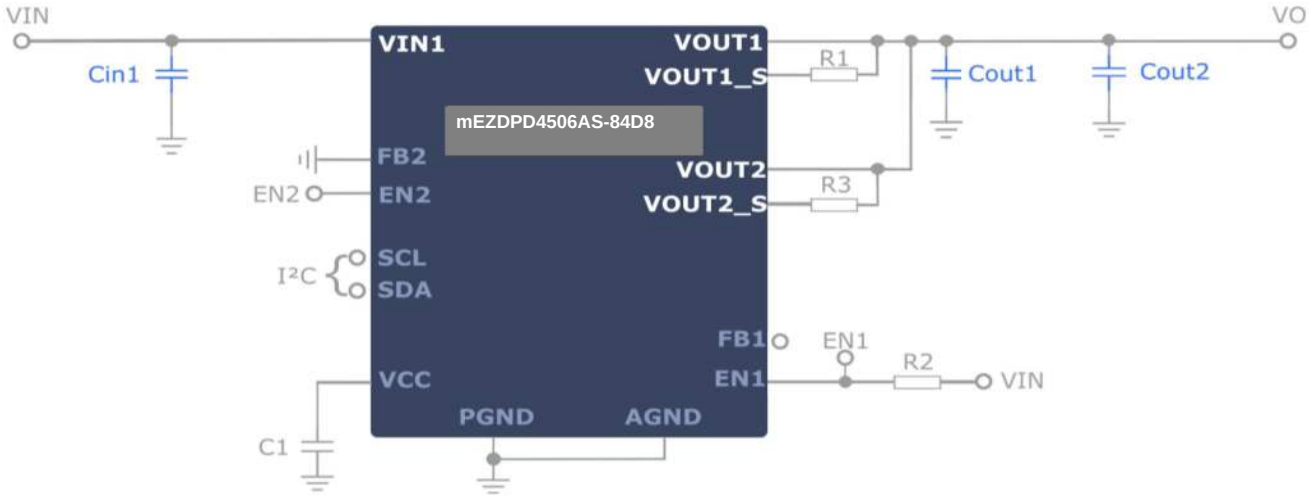
FEATURES

- Telemetry Readback Includes VIN, VOUT, IOUT, Temperature, and Faults
- Noise-Cancelling, Dual-Side Input Capacitors and Frequency Spread Spectrum Option for Low EMI
- Power Good and Fault Indication
- Output Over-Voltage, Under-Voltage, Over-Current, and Over-Temperature Protection
- 1% V_{OUT} Accuracy Over Operation Temperature Range
- Available in an LGA-45 (10mmx10mmx4.4mm) Package

EFFICIENCY

Vin = 12V, Vout = 3.3V, Iout = 6A

TYPICAL APPLICATION



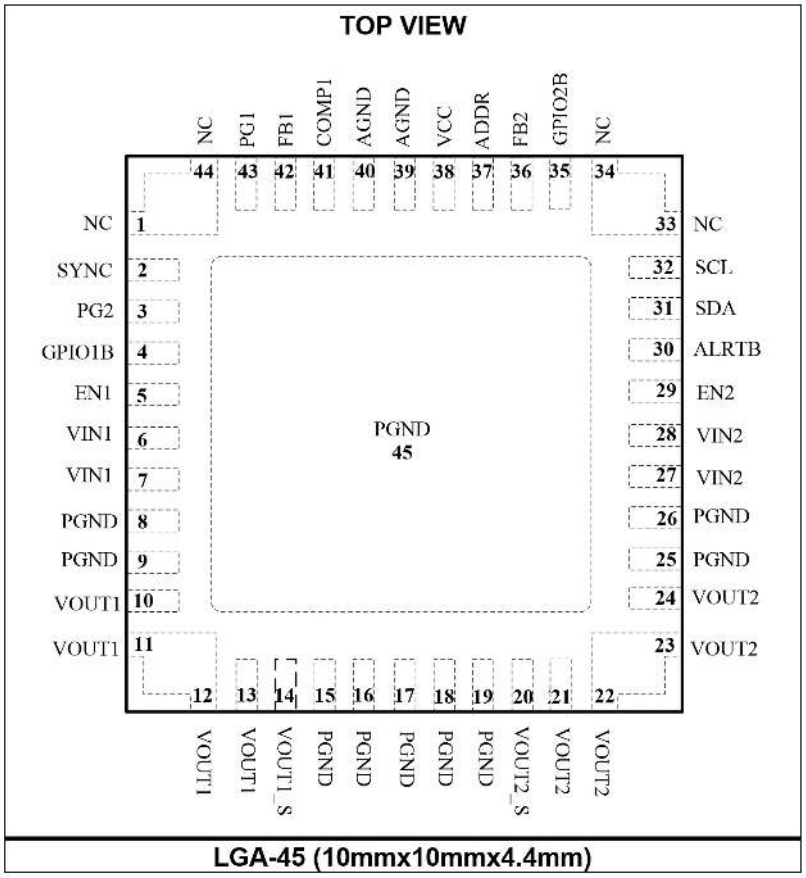
BOM

Reference	Quantity	Value	Description	Package	Manufacturer	Part Number
Cin1	4	4.7uF	Cap,Ceramic,50V,X7R(material)	'1206'	MuRata	GRM31CR71H475K
Cout1	6	22uF	Cap,Ceramic,16V,X5R(material)	'1206'	MuRata	GRM31CR61C226M
Cout2		NS	NS			
R2	1	499kohm	Film Res,1%	'0402'		
R1	1	10ohm	Film Res,1%	'0402'		
R3	1	10ohm	Film Res,1%	'0402'		
C1	1	1uF	Cap, Ceramic,10V,X5R	'0402'		
U1	1	-	Programmable 45V DC/DC Power module supply up to 6A	'LGA (10x10x4.4mm)'	MPS	mEZDPD4506AS

ORDERING INFORMATION

Part Number	Finalize Design to Order
mEZDPD4506AS-84D8	https://www.monolithicpower.com/mezdpd4506as.html

PACKAGE REFERENCE



LGA-45 (10mmx10mmx4.4mm)

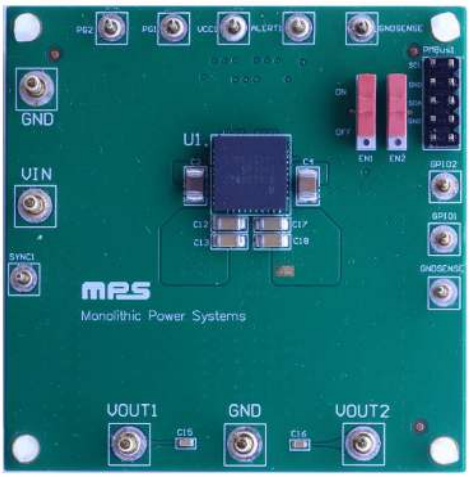
OTHER ORDERING OPTIONS

Evaluation Board for Surface Mount Device

The evaluation board is designed to demonstrate the capabilities of your custom MPS mEZDPD4506AS-84D8.

The EVB device is programmed with custom configuration.

Part Number
EVmEZDPD4506AS-00A



DIP Mount (Pin Out Version)

The mEZDPD4506AS-84D8 is your custom device on a DIP mount for an easy-to-use, plug-and-play form factor.

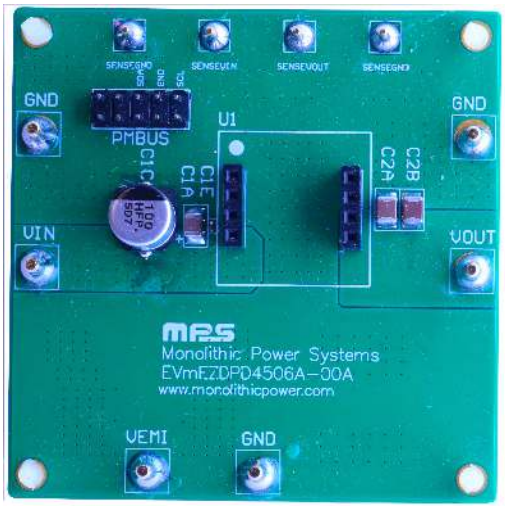
The pin out module device is programmed with custom configuration.

Part Number
mEZDPD4506A

Socket Evaluation Board for DIP Mount

DIP mount socket only. For easy evaluation of pin out module.

Part Number
EVmEZDPD4506A-00A



All EVB schematic and layout files can be found at:
https://www.monolithicpower.com/mezdpd4506as.html

PIN FUNCTIONS

Pin #	Name	Description
1, 33, 34, 44	NC	**No connection.**
2	SYNC	**Synchronized to external clock signal.** Can be programmed by PMBus to sync input or sync output.
3	PG2	**Power good indicator for channel 2.** The output of PG is an open drain. Connect a resistor to a pull-up power source if used.
4	GPIO1B	**General I/O port 1.**
5	EN1	**Enable 1 pin.** Drive EN1 high to turn on channel 1, and drive it low or float it to turn off the device. It has an internal, 1MΩ, pull-down resistor to ground.
6, 7	VIN1	**Channel 1 supply voltage.** This pin supplies all power to the converter. Place a decoupling capacitor to ground as close as possible to the IC to reduce switching spikes. Connect using a wide PCB trace.
8, 9, 15, 16, 17, 18, 19, 25, 26	PGND	**Power ground.** Reference ground of the regulated output voltage. Connect these pins to large copper areas to the negative terminals of the input and output capacitors.
10, 11, 12, 13	VOUT1	**Channel 1 power output.** Connect load to VOUT1. An output capacitor is needed.
14	VOUT1_S	**Channel 1 power output sense input.** Connect directly to VOUT1.
20	VOUT2_S	**Channel 2 power output sense input.** Connect to VOUT2 directly.
21, 22, 23, 24	VOUT2	**Channel 2 power output.** Connect load to VOUT2. An output capacitor is needed.
27, 28	VIN2	**Channel 2 supply voltage.** This pin supplies all power to the converter. Place a decoupling capacitor to ground as close as possible to the IC to reduce switching spikes. Connect using a wide PCB trace.
29	EN2	**Enable 2 pin.** Drive EN2 high to turn on channel 2, and drive it low or float it to turn off the device. It has an internal, 1MΩ, pull-down resistor to ground.
30	/ALERTB	**PMBus alert.**
31	SDA	**PMBus serial data.**
32	SCL	**PMBus serial clock.**
35	GPIO2B	**General I/O port 2.**
36	FB2	**Error amplifier feedback inputs for channel 2.** This pin receives sensed voltage feedback voltage for channel 2 from an external resistive divider across the output. In multi-phase mode, this pin must be pulled up high to disable this channel's error amplifier.
37	ADDR	**Address setting for the PMBus.**
38	VCC	**Internal 5V LDO regulator output.** Decouple with a 0.22μF capacitor.
39, 40	AGND	**Signal ground.** Ground for internal logic and signal circuit. AGND is not internally connected to power ground. Be sure to connect AGND to power ground in PCB layout.
41	COMP1	**Channel 1 error amplifier output.** For multi-chip, multi-phase applications, connect this pin for each chip for current sharing.
42	FB1	**Error amplifier feedback inputs for channel 1.** This pin receives sensed voltage feedback voltage for channel 1 from an external resistive divider across the output.
43	PG1	**Power good indicator for channel 1.** The output of PG is an open drain. If used, connect a resistor to a pull-up power source.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +48V
V_{EN} .....-0.3V to +45V
All other pins.....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
LGA-45 (10mmx10mmx4.4mm) .....TBD
Junction temperature.....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

Recommended Operating Conditions

Supply voltage (V_{IN})..... 3.5V to 45V
Output voltage (V_{OUT})..... 0.6V to 24V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance (3)	θ_{JA}	θ_{JC}
LAG-45 (10mmx10mmx4.4mm)	TBD	TBD °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

PROGRAMMABLE ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Description	Min	Typ	Max	Units
Under-Voltage Lockout (UVLO)						
V_{IN} UVLO rising threshold	$VINUV_{VTH\ RISE}$	Programmed value, device powered on voltage assuming that EN is active		3.456		V
V_{IN} UVLO falling threshold	$VINUV_{VTH\ FALL}$	Programmed value, device powered off voltage assuming that EN is active		3.348		V
V_{IN} UVLO hysteresis	$VINUV_{HYS}$	Programmed value, $VINUV_{VTH\ RISE}$ - $VINUV_{VTH\ FALL}$		0.108		V
EN voltage hysteresis	$V_{EN\ HYS}$	Programmed value		200		mV
Input Over-Voltage Protection						
Input OVP threshold	$VIN_{OVP\ TH}$	Programmed value, threshold for input over-voltage fault detection		50.76		V
Input OVP hysteresis	$VIN_{OVP\ HYS}$	Programmed value		1080		mV
Input OVP retry interval		Programmed value, restart interval time after triggering input over-voltage fault		100		ms
Output Voltage						
Operation V_{OUT}	V_{OUT}	Programmed value, set value of output voltage		3.3		V
Voltage feedback divider range		Programmed value, sets the internal voltage divider ratio		Range3(0-6.24)		
Output voltage margin high	$V_{OUT\ MARGIN\ HIGH}$	Programmed value, output voltage high margin		3.564		V
Output voltage margin low	$V_{OUT\ MARGIN\ LOW}$	Programmed value, output voltage low margin		3.036		V
Output voltage max	$V_{OUT\ MAX}$	Programmed value, upper limit on the output voltage the converter can command regardless of any other commands or combinations		6.138		V
Output voltage transition rates		Programmed value, V_{OUT} changing slew-rate control bits, this control only works after SS finishes and during the SS period, the V_{OUT} slew rate is controlled by the SS pin		2		V/ms
Switching						
Switching frequency	f_{SW}	Programmed value, the set value of the switching frequency		800		kHz
Switching on slew rate (5)		Programmed value, switching rising slew rate		1		V/ns
Switching off slew rate (5)		Programmed value, switching falling slew rate		1		V/ns
Dithering cycle		Programmed value, frequency of dithering		2		kHz

Dithering range		Programmed value	Fsw+2 - Fsw+9			kHz
Soft Start						
Soft-start time	t_{SS}	Programmed value, time from the moment when the output starts to rise to when the output voltage reaches the regulation point		1		ms
t_{ON} delay	t_{ON_DELAY}	Programmed value, the time from the moment EN turns on to when the output voltage starts rising		0		ms
t_{OFF} fall	t_{OFF_FALL}	Programmed value, the time from when the output starts to fall until the voltage reaches the zero point		1		ms
t_{OFF} delay	t_{OFF_DELAY}	Programmed value, the time from the moment EN turns off to when the output starts to fall		0		ms
Light-Load Mode						
AAM threshold for extending frequency		Programmed value, extending frequency if the inductor peak current is below this threshold		350		mA
AAM threshold for blanking clock		Programmed value, blanking the internal clock if the inductor peak current is below this threshold		200		mA
Compensation						
Compensation RTH	R_{TH}	Programmed value, compensation resistor R_{TH}		1000		kΩ
Compensation CTH	C_{TH}	Programmed value, compensation capacitor C_{TH}		60		pF
Compensation CTHP	C_{THP}	Programmed value, compensation capacitor C_{THP}		0.2		pF
Compensation Slope		Programmed value, slope compensation amplitude		1.83		A
Compensation GM	GM	Programmed value, transconductance of the error amplifier		12.5		μA/V
Over-Current Protection						
Peak current limit	$I_{PEAK-LIMIT}$	Programmed value, threshold of the inductor peak current limit		6		A
Valley current limit	$I_{VALLEY-LIMIT}$	Programmed value, threshold of the inductor valley current limit		5		A
Over-current retry interval		Programmed value, restart interval time after triggering over-current fault and shutdown		150		ms
Over-current delay time		Programmed value, device response delay time when output over-current fault is triggered		50		μs

Output Over-Voltage and Under-Voltage Protection						
Output OVP threshold	V_{OVP_TH}	Programmed value, threshold for output over-voltage fault detection, as percentage of V_{OUT} set		120		%
Output OVP hysteresis	V_{OVP_HYS}	Programmed value, as percentage of V_{OUT} set		5		%
Output OVP retry interval		Programmed value, restart interval time after triggering output over-voltage fault and shutdown		20		ms
Output OVP delay time		Programmed value, device response delay time when output over-voltage fault is triggered		10		µs
Output UVP threshold	V_{UVP_TH}	Programmed value, threshold for output under-voltage fault detection, as percentage of VOUT set		90		%
Output UVP hysteresis	V_{UVP_HYS}	Programmed value, as percentage of V_{OUT} set		5		%
Output UVP retry interval		Programmed value, restart interval time after triggering output under-voltage fault and shutdown		150		ms
Output UVP delay time		Programmed value, device response delay time when output under-voltage fault is triggered		50		µs
Thermal Protection						
Thermal shutdown (5)	T_{SD}	Programmed value, threshold for thermal over-temperature fault detection		150		°C
Thermal shutdown hysteresis (5)	T_{SD_HYS}	Programmed value		25		°C

Note:

5) Not tested in production. Guaranteed by design and characterization.

PROGRAM OPERATION SETTINGS

Name	Selected Mode	Description	Note
Output Voltage			
Output voltage set mode	1	0: Use external voltage divider 1: I²C programmable mode	
Output voltage bias enable	1	0: Disable 1: Enable	
Switching			
Switching dithering Enable/Disable	0	Frequency dither function enable bit. 0: Disable 1: Enable	
Light-Load Mode			
Light-load mode	0	0: AAM 1: CCM	
Input Over-Voltage Protection			
Input OVP mode	10	00: Ignore. The device will operate without interruption. 01: Not supported. 10: Immediate off. The device will shut down immediately, and responds according to the Input OVP Retry Settings	
Input OVP retry settings	0	0: No restart 1: Restart continuously	
Over-Current Protection			
Over-current response	10	00: Current limit only 01: Deglitched off 10: Immediate off	
Over-current retry settings	1	0: Latch off 1: Restart continuously	
Output Over-Voltage and Under-Voltage Protection			
Output OVP mode	11	00: Ignore 01: Deglitched off 10: Immediate off 11: Discharge mode	
Output OV retry settings	0	0: Latch off 1: Restart continuously	
Output UVP mode	10	00: Ignore 01: Deglitched off 10: Immediate off	
Output UVP retry settings	1	0: Latch off 1: Hiccup mode	
SYNC IN/OUT	0	0: SYNC OUT 1: SYNC IN	
Power Stage Set			
Power stage select	0	0: Set from ADC sense 1: Set from MTP	
Power stage	000	000: Single-phase 6A operation 001: Dual-phase single output operation	

		010: Two-chip, 4-phase, 12A operation (master1) 101: Two-chip, 4-phase, 12A operation (master2) 011: Two-chip, 4-phase, 12A operation (slave1) 111: Dual-output buck operation	
Rail Address			
Enable rail address	0	0: Disable 1: Enable	
Address	0	Rail Address	
GPIO			
Input over-voltage	1	Input over-voltage indication setting 0: Disable 1: Enable	
Over-temperature	1	Over-temperature indication setting 0: Disable 1: Enable	
Output under-voltage	1	Output under-voltage indication setting 0: Disable 1: Enable	
Over-voltage	1	Over-voltage indication setting 0: Disable 1: Enable	
Over-current	1	Over-current indication setting 0: Disable 1: Enable	
GPIO mode	0	GPIO mode set 0: Analog input 1: Digital output	
Operation			
Operation	80	80: ON 40: Soft off 00: Immediate off 94: Margin low A8: Margin high	

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_A= -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} quiescent current	I_Q	V_{OUT} = 3.3V, with BIAS power, no load		12		μA
	I_Q	V_{FB} > V_{REF}, no load		TBD		μA
V_{IN} shutdown current	I_{SD}	V_{EN} = 0V, T_J =25°C			1	μA
Sync frequency range	f_{SYNC}	Sync clock set range	150		2200	kHz
Sync voltage high threshold	V_{SYNC_HIGH}			1.4	1.8	V
Sync voltage low threshold	V_{SYNC_LOW}		0.4	0.8		V
Minimum on time (5)	t_{ON_MIN}	With peak current mode		100		ns
Minimum off time (5)	t_{OFF_MIN}			130		ns
HS switch on resistance	R_{DSON_H}	V_{BST} - V_{SW} = 5V		62		mΩ
LS switch on resistance	R_{DSON_L}			34		mΩ
Integrated inductor inductance	L_1			3.3		μH
	L_2			3.3		μH
Inductor DC resistance	L_{1_DCR}			26		mΩ
	L_{2_DCR}			26		mΩ
Switch leakage current	I_{SW_LKG}	T_J = 25°C			1	μA
Default EN voltage threshold	V_{EN}	PMBus default set	1	1.2	1.4	V
PG upper trip threshold		Programmed value, as percentage of V_{OUT} set, equal to V_{OVP_TH}				%
PG upper trip hysteresis		As percentage of V_{OUT} set, equal to V_{OVP_HYS}				%
PG lower trip threshold		As percentage of V_{OUT} set, equal to V_{UVP_TH}				%
PG lower trip hysteresis		As percentage of V_{OUT} set, equal to V_{UVP_HYS}				%
PG output voltage low	V_{PG_SINK}	I_{SINK} = 1mA		0.1	0.3	V
PG deglitch timer	t_{PG_DELAY}			20		μs
VCC regulator	V_{CC}	I_{CC} = 0mA	4.7	4.9	5.1	V
Input OVP threshold accuracy		PMBus set 36V	34	36	38	V

Note:

5) Not tested in production. Guaranteed by design and characterization.

PMBUS PORT SIGNAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_A = -40°C to +125°C, typical values tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
PMBus Interface Specifications						
Input logic low	V_{IL}		0		0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data set-up time	$t_{SU,DAT}$		100			ns
Data hold time	$t_{HD,DAT}$		0		0.9	µs
Set-up time for repeated start	$t_{SU,STA}$		0.6			µs
Hold time for start	$t_{HD,STA}$		0.6			µs
Bus free time between a start and a stop condition	t_{BUF}		1.3			µs
Set-up time for stop condition	$t_{SU,STO}$		0.6			µs
Rise time of SCL and SDA	t_R		20 + 0.1 × C_B		120	ns
Fall time of SCL and SDA	t_F		20 + 0.1 × C_B		120	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

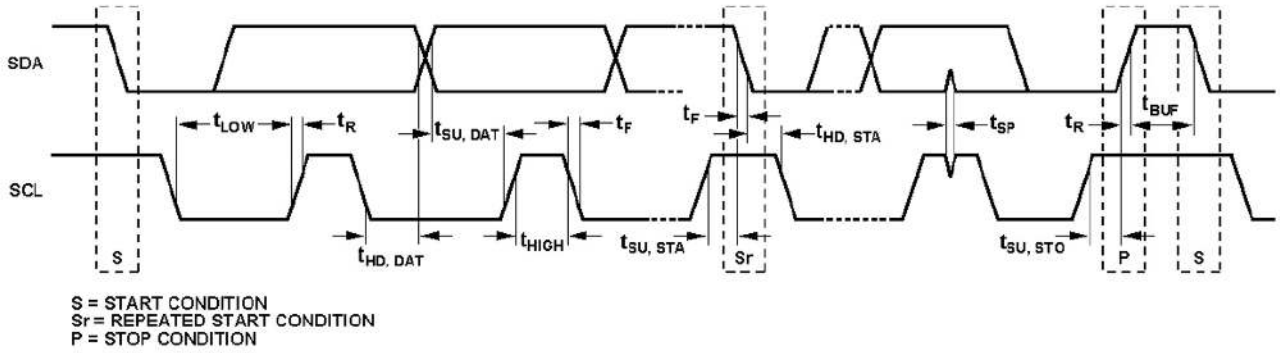


Figure 1: PMBus-Compatible Interface Timing Diagram

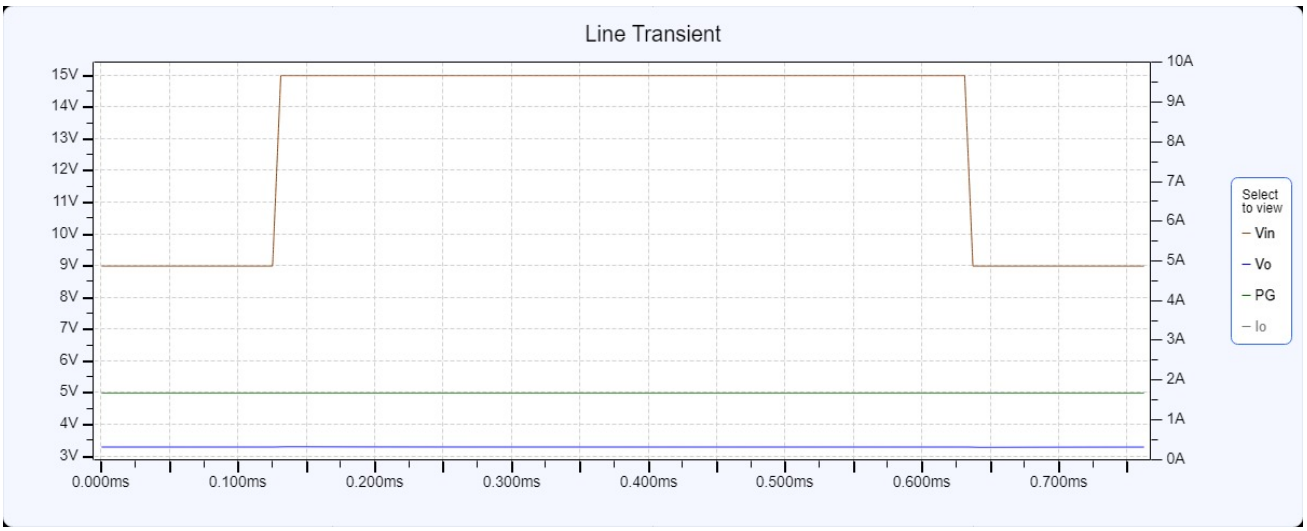
TYPICAL PERFORMANCE CHARACTERISTICS

All waveforms simulated.

EFFICIENCY

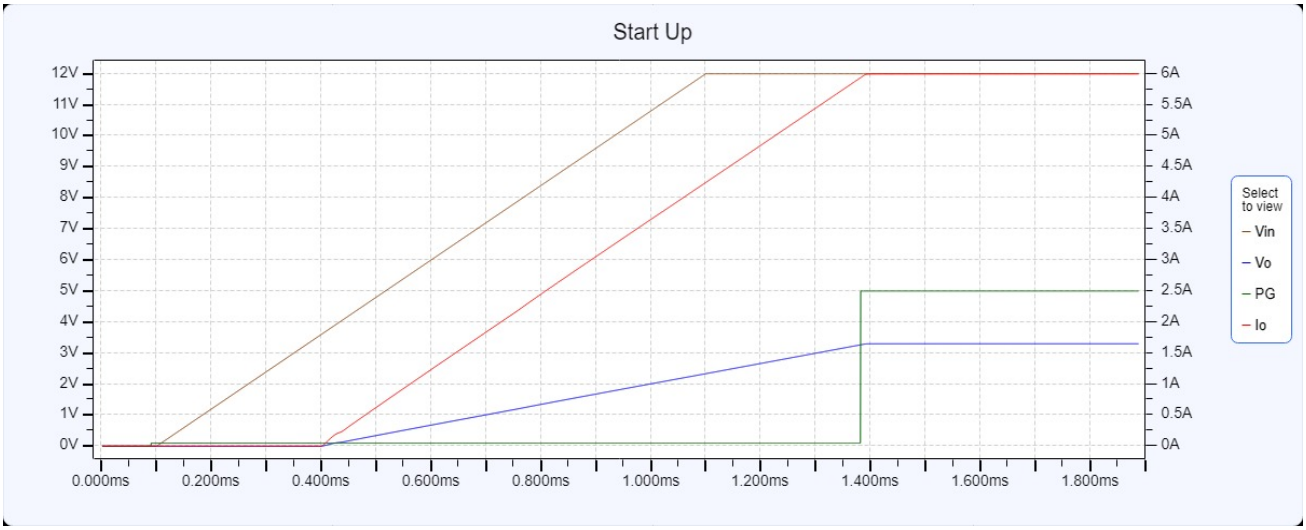
Vin = 12V, Vout = 3.3V, Iout = 6A

LINE TRANSIENT



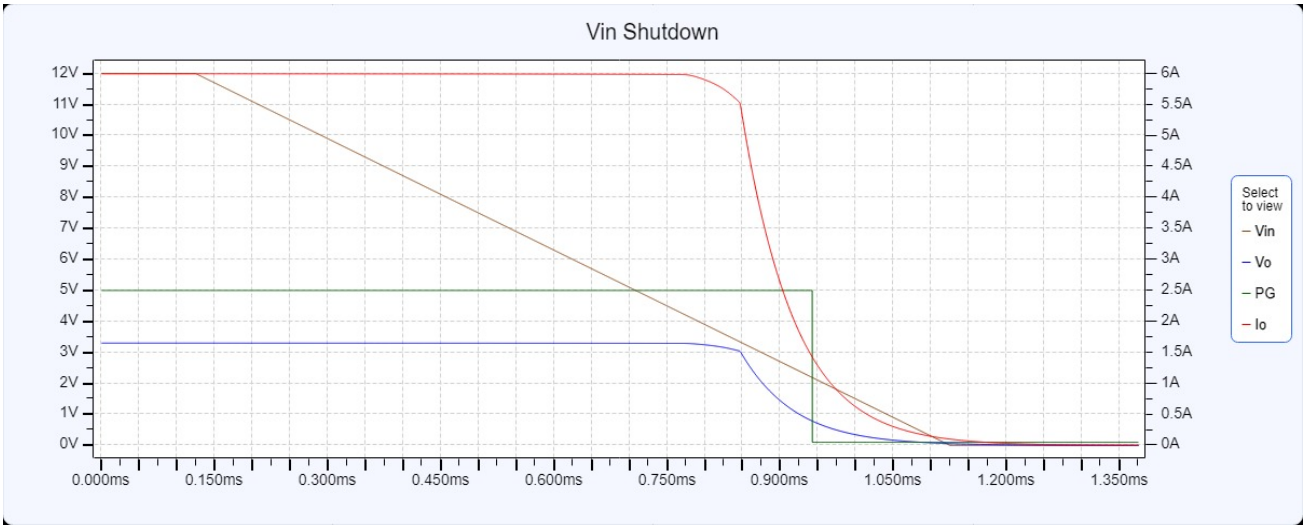
Vlow= 9A, Vhigh= 15A, Iout= 6A, Slew rate= 1V/µs

START UP



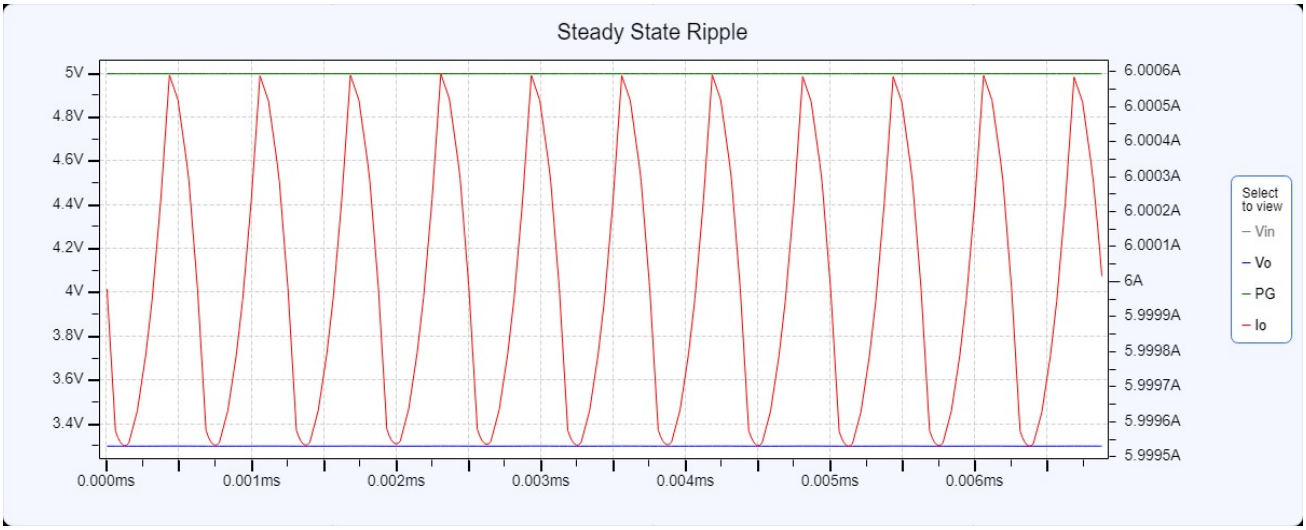
Vin = 12V, Iout = 6A

VIN SHUTDOWN



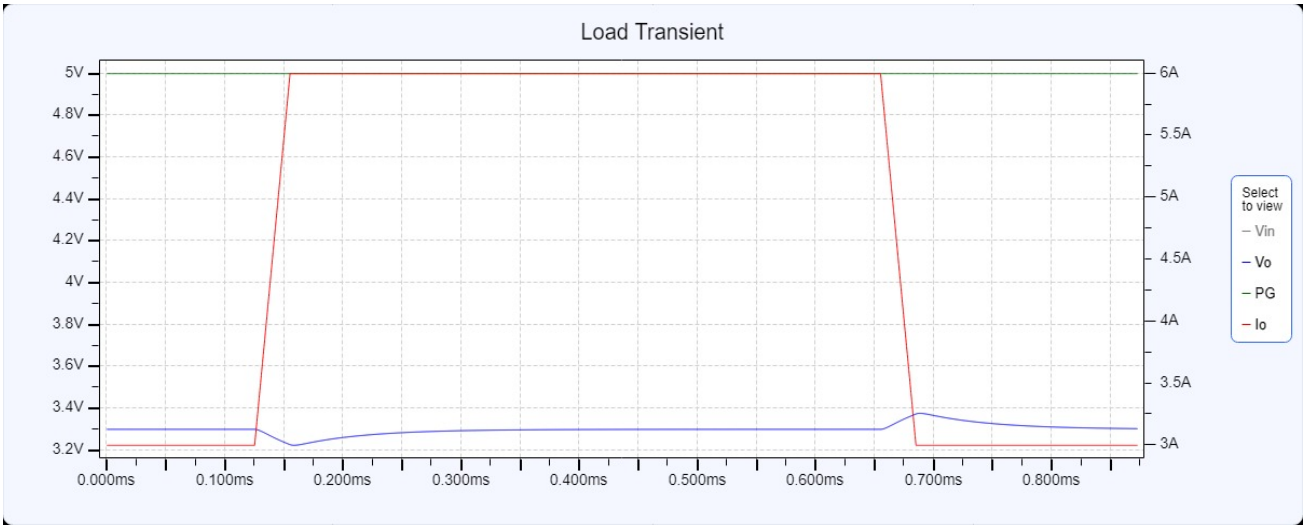
Vin = 12V, Iout = 6A

STEADY STATE RIPPLE



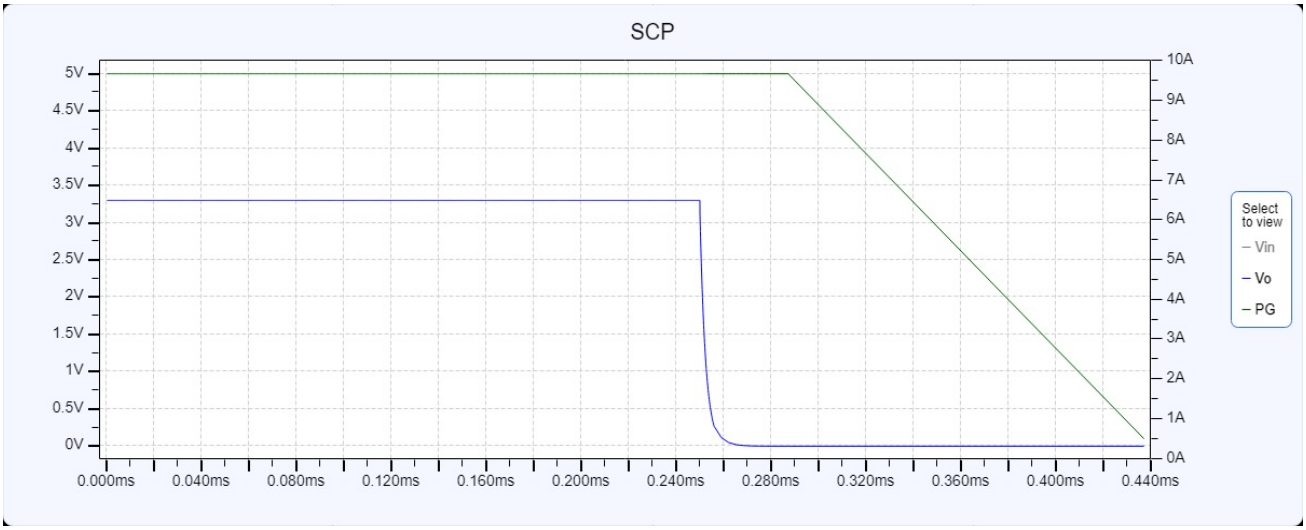
Vin = 12V, Iout = 6A

LOAD TRANSIENT



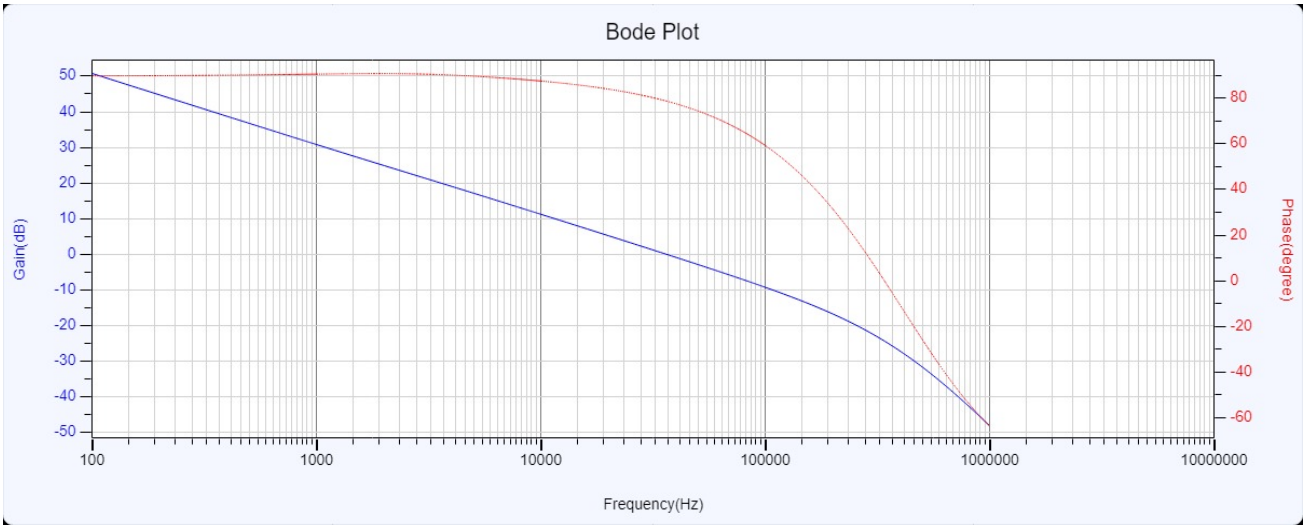
Vin = 12V, Ihigh = 6A, Ilow =3A, Slew rate = 0.1A/µs

SCP



Vin = 12V

BODE PLOT



Bandwidth = 36kHz, Phase Margin = 79.06degree, Gain Margin = -23.75dB

FUNCTIONAL BLOCK DIAGRAM

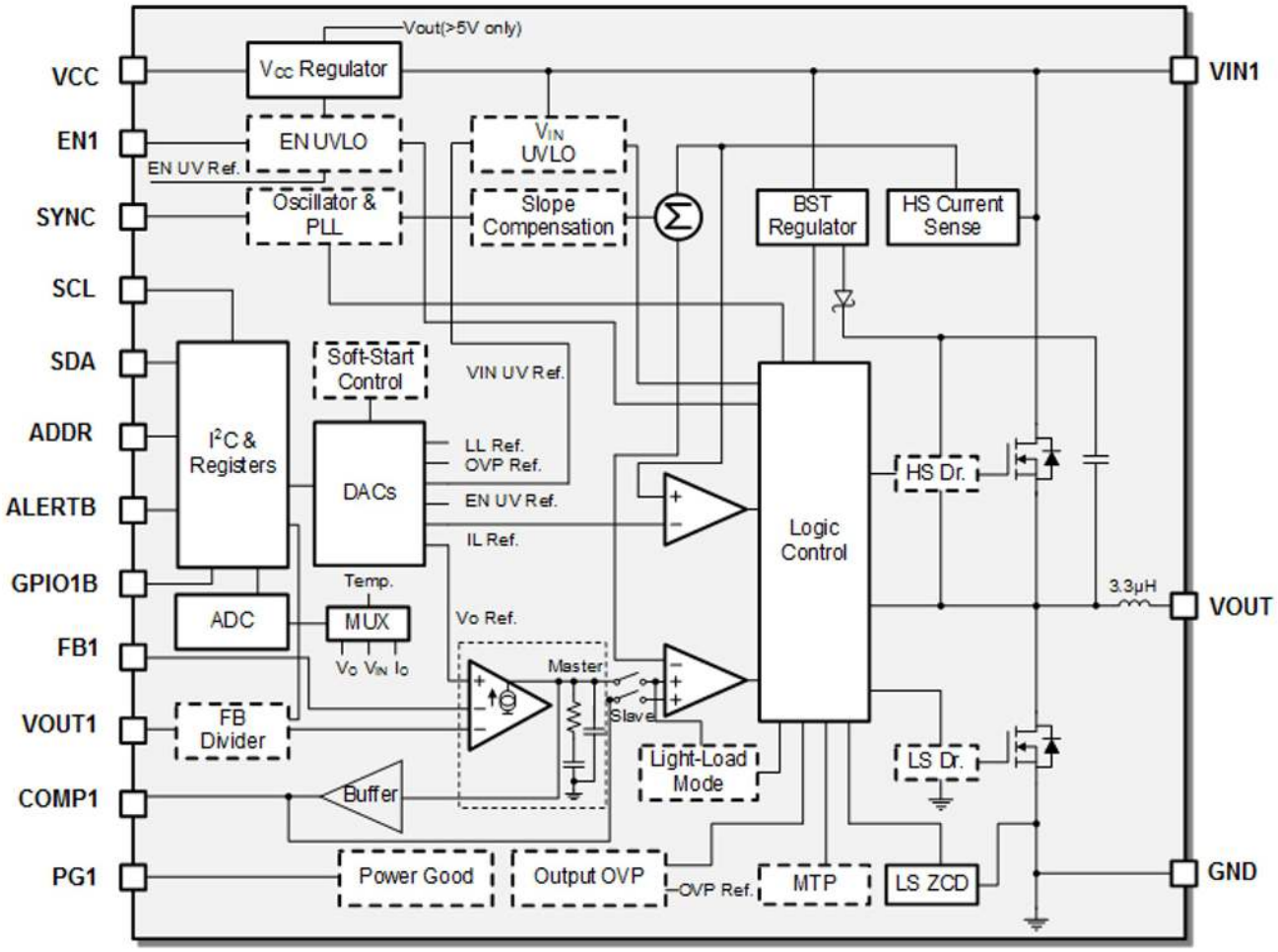


Figure 2: Functional Block Diagram

(Only one channel is shown, blocks in dashed line are programmable via the PMBus)

OPERATION

This device is a high-frequency, synchronous, step-down converter with built-in power MOSFETs. Figure 2 shows a block diagram of the part. It is available with a wide 4V to 45V input supply range, and can achieve up to 3A continuous output current per phase, or parallel for 6A total output current. It can also be paralleled for 4-phase and 6-phase operation. The device offers excellent load and line regulation over an ambient temperature range of -40°C to +125°C.

PWM Control

At moderate to high output current, the device operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a PWM cycle. At the rise edge of the clock, the high-side switch (HS-FET) turns on, and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current hits the COMP voltage, which is the output of the internal error amplifier. The output voltage of error amplifier depends on the difference of output feedback voltage and the internal high-precision reference, which decides how much energy should be transferred to the load. The higher load current, the higher the COMP voltage will be. Both the feedback divider ratio and reference can be adjusted by PMBus, which makes it easy to adjust different output voltages.

When the HS-FET is off, the low-side switch (LS-FET) turns on immediately and remains on until the next clock cycle starts. During this time, the inductor current flows through the LS-FET. In order to avoid shoot-through, a dead time is inserted to avoid the HS-FET and LS-FET being turned on at the same time.

If the current in the HS-FET does not reach COMP set current value in one PWM period, the HS-FET remains on, saving a turn-off operation.

Mode Selection (AAM and Forced CCM)

This device can work in light-load AAM or forced CCM mode by PMBus. AAM (Advanced asynchronous modulation) mode is employed to optimize the efficiency during light-load or no-load conditions, while forced CCM can maintain a constant switch frequency and smaller output ripple, but it has low efficiency at light load.

If AAM mode is enabled with load decreasing, the device first enters discontinuous conduction operation (DCM) and maintains a fixed frequency as long as the inductor current approaches zero. If the load is further decreased, or there is no load that makes the inductor peak current lower than the AAM peak current threshold set by the PMBus, the device enters sleep mode and consumes low quiescent current to further improve light-load efficiency. In sleep mode, the internal clock is blocked, and the device skips some pulses. Then feedback voltage will be less than the reference, so V_{COMP} ramps up until the inductor peak current exceeds the AAM threshold. Then the internal clock resets, and the crossover time is taken as benchmark of the next clock cycle. This control scheme helps achieve high efficiency by scaling down the frequency to reduce switching and gate driver losses (see Figure 3).

As the output current increases from light-load condition, V_{COMP} and the switching frequency increase. If the output current exceeds the critical level set by V_{COMP}, the device resumes fixed-frequency PWM control.

When forced CCM is enabled, the device operates in a fixed-frequency peak current control mode to regulate the output voltage, regardless of the output current.

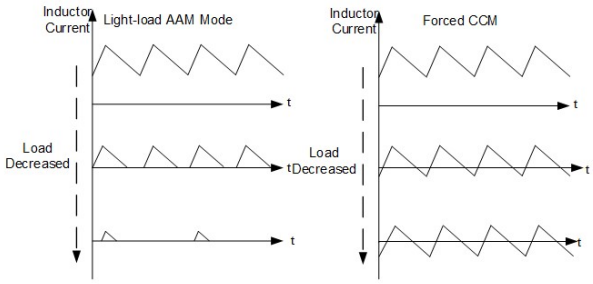


Figure 3: AAM and Forced CCM

Internal Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5.0V, the output of the regulator is in full regulation. Lower values of V_{IN} result in lower output voltages. The regulator is enabled when V_{IN} exceeds its UVLO threshold and EN is high. In EN shutdown mode, the internal VCC

regulator is disabled to reduce power dissipation.

For better thermal performance, BIAS mode can be selected by the PMBus. If V_{OUT} is above 5V, VCC and the internal circuit are powered by V_{OUT}.

Enable Control

EN is a digital control pin that turns the regulator, including the PMBus block, on and off. Drive EN high to turn on the regulator; drive it low to turn it off. The threshold of EN can be programmed by the PMBus. An internal 5MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

Oscillator Frequency

The default frequency of this device is 600kHz, and it can be programmed from 150kHz to 2.2MHz by the PMBus The frequency can also be set by a logic-level synchronous signal.

SYNC IN and SYNC OUT

The SYNC pin can be programmed by the PMBus to SYNC IN or SYNC OUT. When operating as SYNC IN, the internal oscillator frequency can be synchronized by an external clock via this pin. At start-up, the device first operates at the internal set frequency, and quickly synchronizes to the external clock once soft start is ready. Ensure the high amplitude of the SYNC clock is greater than 1.8V and that the low amplitude is below 0.4V to drive the internal logic. The recommended external SYNC frequency is in the range of 250kHz to 2.2MHz.

The device operates in forced CCM mode with fixed frequency when there is a SYNC clock, regardless of output current. A pulse longer than 200ns is recommended in application.

When the SYNC pin is set to SYNC OUT, the device outputs the internal clock with 0° or 180° phase shift. By this function, two devices can operate in same frequency, but 180° out of phase, to reduce the total input current ripple so that a smaller input bypass capacitor can be used.

Under-Voltage Lockout (UVLO)

The device has input under-voltage lockout protection (UVLO) to ensure reliable output power. If EN is active, the device is powered on when the input voltage is higher than the UVLO rising threshold, and is powered off when the input voltage drops below the UVLO falling threshold. The UVLO threshold can be set between 3.3V and 5.7V by the PMBus. This function prevents the device from operating at an insufficient voltage. It is a non-latch protection.

Soft Start

The device has built-in soft start (SS), which ramps up the output voltage in a controlled slew rate when EN goes high, avoiding overshoot during start-up. When the chip starts, the internal circuitry generates a soft-start voltage that ramps up slowly. When the SS voltage (V_{SS}) is lower than the internal reference (V_{REF}), V_{SS} overrides V_{REF} as the error amplifier reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference. At this point, soft start finishes and the device enters steady-state operation.

The SS time is internally set to 1ms as a default, and can also be set to 0.5ms, 2ms or 4ms by the PMBus. When the output voltage shorts to GND, the feedback voltage is pulled low, and V_{SS} is discharged. The part soft starts again when it returns to normal conditions.

Pre-Bias Start-Up

For this device, at start-up, if the output feedback voltage is greater than V_{SS} (which means output has pre-bias voltage), neither the HS-FET or LS-FET turn on until V_{SS} is higher than the feedback voltage.

Power Good Indicator

The device has power good (PG) indication. The PG pin is the open drain of a MOSFET. It should be connected to a voltage source through a resistor (e.g. 100kΩ). In the presence of an input voltage, the MOSFET turns on so that the PG pin is pulled to GND before soft start is ready. When output voltage is within the default ±10% window of rated voltage, PG is pulled high after a delay (typically 30μs). If V_{OUT} moves outside the default ±10% range with a hysteresis, the device pulls PG low to indicate a failure output status. Both the PG threshold and hysteresis can be programmed by the PMBus.

FAULT Indicator

The /FT pin is also an open drain of a MOSFET. It should be connected to a voltage source through a resistor (e.g. 100kΩ). /FT is pulled high at normal operation, and any fault or

warning pulls down this pin to indicate a fault status, including input OVP, output OVP, SCP, and thermal shutdown.

Over-Current Protection (OCP)

The device has cycle-by-cycle, over-current limit control. The inductor current is monitored during the HS-FET on state. Once the inductor peak current exceeds the set current limit threshold, the HS-FET immediately turns off. Then the LS-FET turns on to discharge the energy, and the inductor current decreases. The HS-FET does not turn on again until the inductor current falls below the valley current limit. This function helps prevent the inductor current from running away and possibly damaging the components. Both the peak current and valley current threshold can be programmed by the PMBus.

When the peak current limit is triggered, the OCP timer starts immediately. The OCP timer can be set to 32, 64, 128, or 256 cycles by the PMBus. Hitting the current limit in each cycle of this OCP timer triggers SCP operation (hiccup as default) which is explained in detail below.

Short-Circuit Protection (SCP)

When a short circuit occurs, the device immediately hits its current limit. Meanwhile, the output voltage quickly drops to the under-voltage threshold (default 50% of setting output). Then the device considers this an output dead short, and directly triggers SCP operation. There are three modes that can be selected by the PMBus for SCP operation: hiccup as default, switching with non-hiccup, and latch off.

In default hiccup mode, the device first disables its output power stage and resets the soft-start voltage, then initiates a soft start procedure. The off time is decided by soft-start time and hiccup duty, which can both be set by the PMBus. If the short-circuit condition remains after soft start ends, the device repeats this operation until the short circuit disappears and the output returns to the regulation level. This protection mode greatly reduces the average short circuit current by periodically restarting the part to alleviate thermal issues and protect the regulator.

Over-Voltage Protection (OVP)

The device monitors the output voltage through the VOUT pin to detect output over-voltage conditions. When the output voltage exceeds the OVP threshold (default is 120% of setting voltage), OVP mode is triggered. There are three modes that can be selected by the PMBus for OVP operation: disable as default, discharge, and latch-off.

The device also has optional input OVP. The threshold can be set to 28V or 34V. If VIN exceeds this threshold, the device stops switching. This is a non-latch protection, and the device returns to normal operation when the input OVP is removed.

Thermal Shutdown

The device employs thermal protection by internally monitoring the IC temperature. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature exceeds the threshold (default 175°C), it shuts down the whole chip. This is a non-latch protection, and there is a default 25°C hysteresis. Once the junction temperature drops to about 150°C, the device resumes normal operation by initiating a soft start. Both the OTP threshold and hysteresis can be set by the PMBus.

Floating Driver and Bootstrap Charging

An internal, built-in bootstrap capacitor powers the floating HS-FET driver. When the voltage difference between BST and SW is less than the internal 5V bootstrap regulator, a PMOS pass transistor M1 connected from V_{IN} to BST turns on to charge the bootstrap capacitor. The current path is through D1, M1, C4, L1, and C2 (see Figure 4). If V_{IN} - V_{SW} exceeds 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4. Meanwhile, the external circuit must have enough voltage headroom to accommodate charging. A 10Ω resistor placed between SW and the BST capacitor is strongly recommended to reduce SW spike voltage.

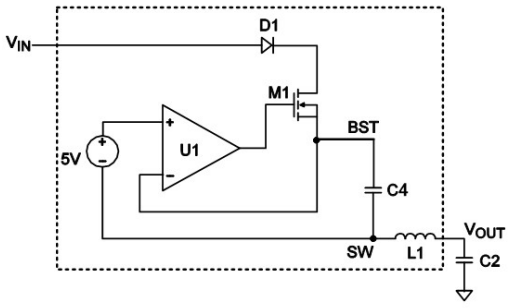


Figure 4: Internal Bootstrap Charging Circuit

As long as V_{IN} is sufficiently higher than V_{SW}, the bootstrap capacitor can be charged. When the HS-FET is on, V_{IN} is about equal to V_{SW} so the bootstrap capacitor cannot charge. The best charging period occurs when the LS_FET is on so that V_{IN} - V_{SW} is at its largest. When there is no current in the inductor, V_{SW} equals V_{OUT}, so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor.

At higher duty cycle operation conditions, the internal charging circuit may not have sufficient voltage and time to charge the bootstrap capacitor, and extra external circuitry can be used to ensure the bootstrap voltage is in the normal operation region.

Low-Dropout Operation (BST Refresh)

To improve dropout, the device is designed to operate at close to 100% duty cycle as long as the BST-to-SW voltage is greater than 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET turns off using an UVLO circuit, which allows the LS-FET to conduct and refresh the charge on the BST capacitor.

In cases where the input voltage drops, the HS-FET remains on and close to 100% duty cycle to maintain output regulation, until the BST-to-SW voltage falls below 2.5V. Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high.

The effective duty cycle during dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and PCB resistance.

PMBus Control and Default Output Voltage

When the device is enabled (EN = high and VIN > UVLO), the chip starts up to a default 5V output voltage. After that, the PMBus can communicate with the master. Once the PMBus receives valid output voltage set instructions, the output voltage will be determined by PMBus control.

The output voltage setting is realized by adjusting the internal reference voltage and output feedback divider ratio. After the device receives a valid data byte of output voltage setting, it searches the corresponding value from the truth table and then sends the command of adjusting reference and divider ratio, and finally outputs the right voltage.

CRC Protection

The integrity of OTP is checked after a power-cycle reset. Each time registers read OTP contents, the device performs the CRC check. If a CRC error occurs, the registers will try to read two more times. If the error still occurs, the register will read the next available OTP page. If there is no available OTP page, then the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the ALERTB pin is pulled low.

PMBUS INTERFACE

PMBus Serial Interface Description

PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The device interface is a PMBus slave that supports both fast mode (400kHz) and high-speed mode (3.4MHz), adding flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be instantaneously controlled via the PMBus interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 5).

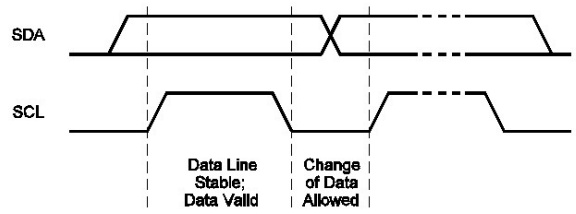


Figure 5: Bit Transfer on the PMBus

Start and Stop Conditions

The start and stop conditions are signaled by the master device, which signifies the beginning and the end of the PMBus transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 6).

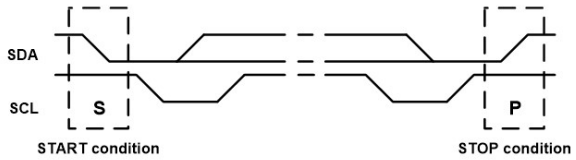


Figure 6: Start and Stop Conditions

Start and stop conditions are generated always by the master. The bus is considered busy after the start condition. The bus is considered free again after a minimum of 4.7μs after the stop condition. The bus stays busy if a repeated start (Sr) is generated instead of a stop condition. The start (S) and repeated start (Sr) conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable low during the high period of the clock pulse.

Figure 7 shows the format that data transfers follow. After the start condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit, which is a data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is terminated always by a stop condition (P), generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

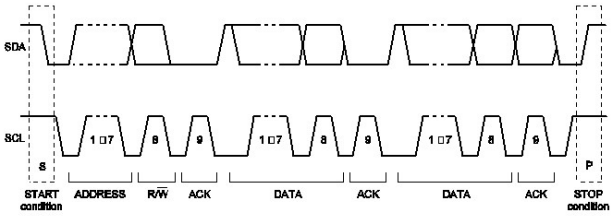


Figure 7: A Complete Data Transfer

PMBus Update Sequence

The device requires a start condition, a valid PMBus address, a register address byte, and a data byte for a single data update. After receipt of each byte, the device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the device. The device performs an update on the falling edge of the LSB byte.

Device PMBus Chip Address

The ADD pin can be used to program the PMBUS address. The device supports 7 addresses for up to 7 voltage rails through configuring the resistor value that connecting between the ADD pin and ground. When the master sends the address as an 8-bit value, the 7-bit address should be followed by “0/1” to indicate write/read operation.

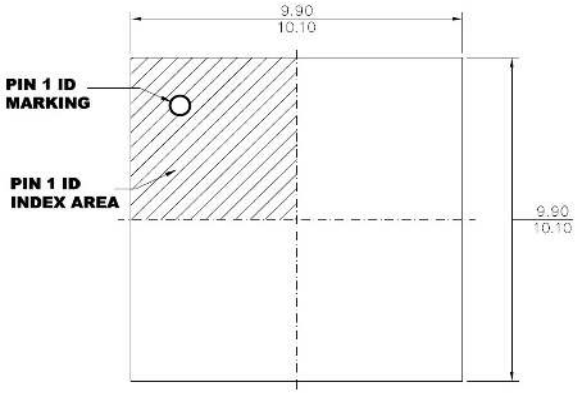
Table 1 shows the resistor values for different PMBus addresses.

Table 1: PMBus Address

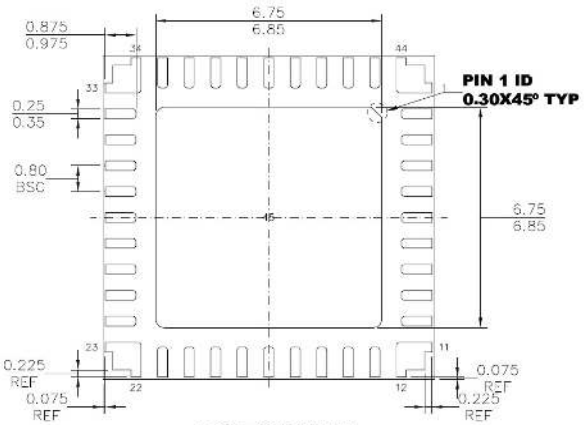
Resistor (kΩ) 1%	Address
0	21h
12.5 + 25	22h
12.5 + 50	23h
12.5 + 75	24h
12.5 + 100	25h
12.5 + 125	26h
12.5 + 150	27h

PACKAGE INFORMATION

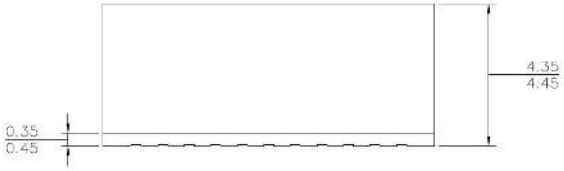
LGA-45 (10mmx10mmx4.4mm)



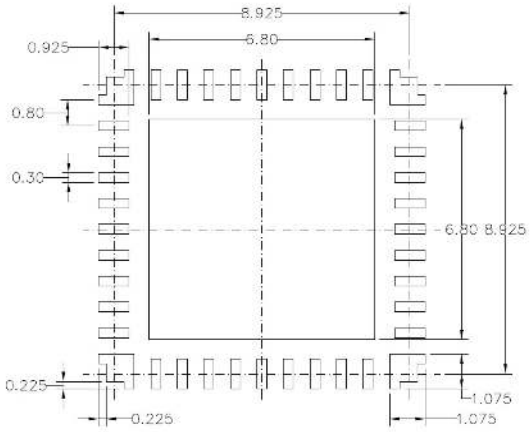
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.