

# **2.5" SATA SSD 840**

# **Datasheet**

**(SQF-S25x-xxx-SCx)**

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**Revision History**

<b>Rev.</b>	<b>Date</b>	<b>History</b>
0.1	2018/5/16	1. Preliminary
0.2	2018/8/22	1. Update PN information
0.3	2018/10/31	1. Update TBW information
0.4	2018/12/14	1. Update Security Features section and TBW
0.5	2019/2/25	1. Update performance information 2. Update power consumption information
0.6	2019/5/10	1. Added performance information
0.7	2019/5/16	1. Update H/W write protect description

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## 1. Overview

Advantech SQFlash 840 series 2.5" SATA-SSD (SQF-S25 840) delivers all the advantages of Flash Disk technology with the Serial ATA III (6.0Gb) interface, fully compliant with standard 2.5-inch form factor. The SATA SSD is based on a standard SATA 7-pin interface for data segment and 15-pin for power segment, designed to operate at a maximum operating frequency of 300MHz with 30MHz external crystal. Its capacity could provide a wide range up to 8TB. Moreover, it can reach up to 550MB/s read and 530MB/s write high performance based on Toshiba 64-layer 3D TLC Flash.

## 2. Features

- **Standard SATA interface**
    - Support SATA 1.5/3.0/6.0 Gbps interface
    - SATA Revision 3.2 compliant
  - **Operating Voltage : 5V**
  - **Support LDPC with RAID ECC**
  - **TRIM 、 AHCI supported**
  - **AES256 and Hardware Quick Erase supported**
  - **Voltage Stabilizer supported (optional)**
  - **Temperature Ranges**
    - Commercial Temperature
      - 0°C to 70°C for operating<sup>1</sup>
      - -40°C to 85°C for storage
    - Industrial Temperature
      - -40°C to 85°C for operating<sup>1</sup>
      - -40°C to 85°C for storage
- \*Note: 1. Based on SMART Attribute C2h, which measured by thermal sensor
- **Mechanical Specification**
    - Shock : 1,500G / 0.5ms
    - Vibration : 20G / 80~2,000Hz
  - **Humidity**
    - Humidity : 5% ~ 95% under 55°C
  - **Data Retention**
    - 10 years
  - **Acquired RoHS 、 WHQL 、 CE 、 FCC Certificate**
  - **Acoustic : 0 dB**
  - **Dimension : 100 mm x 69.85 mm x 7 mm**

### 3. Specification Table

#### ■ Performance

		Sequential Performance (MB/sec)		Random Performance (IOPS @4K)	
		Read	Write	Read	Write
3D TLC (BiCS3)	240 GB	549.8	510.0	74,620	64,382
	480 GB	557.9	511.1	73,811	66,586
	960 GB	560.2	533.5	95,316	69,934
	1920 GB	557.8	532.6	95,733	70,122
	3840 GB	559.6	526.9	79,433	70,817
	7680 GB	559.8	526.3	80,083	70,897

\* All performance above are tested with AHCI mode.

\* Tested by CrystalDiskMark 1GB workload.

## ■ Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a SSD can be written which is a measurement of SSDs' expected lifespan, represents the amount of data written to the device.

$$TBW = [(NAND\ Endurance) \times (SSD\ Capacity)] / WAF$$

- **NAND Endurance:** Program / Erase cycle of a NAND flash.
  - SLC: 100,000 cycles
  - Ultra MLC: 30,000 cycles
  - MLC: 3,000 cycles
  - 3D TLC (BiCS3): 3,000 cycles
- **SSD Capacity:** SSD physical capacity in total of a SSD.
- **WAF:** Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

$$WAF = (Lifetime\ write\ to\ flash) / (Lifetime\ write\ to\ host)$$

Endurance measurement is based on New JEDEC 218/ 219 Client Workload and verified with following workload conditions,

- PreCond%full = 100%
- Trim commands enabled
- Random data pattern.

### ➤ SQFlash 840 2.5" SSD TBW

	WAF	TBW
		3D TLC (BiCS3)
240 GB	1.85	389
480 GB	1.85	778
960 GB	1.85	1556
1920 GB	1.85	3113
3840 GB	1.83	6295
7680 GB	1.81	12729

## 4. General Description

### ■ Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, SQFlash 840 series SSD applies the LDPC with RAID ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

### ■ Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

SQFlash provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

### ■ Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as "Initial Bad Blocks". Bad blocks that are developed during the lifespan of the flash are named "Later Bad Blocks". SQFlash implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

### ■ Power Loss Protection

#### – Flush Manager

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, SQFlash SSD applies the Flush Manager technology, only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

In addition, it is critical for a controller to shorten the time the in-flight data stays in the controller internal cache. Thus, SQFlash applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. With Flush Manager, incoming data would only have a "pit stop" in the cache and then move to NAND flash directly. Also, the onboard DDR will be treated as an "organizer" to consolidate incoming data into groups before written into the flash to improve write amplification.

#### – Voltage Stabilizer (optional)

While the built-in voltage detector detects an unstable power input ( $< 4.75\text{ V}$  or  $> 5.25\text{ V}$ ), the controller will issue a power failure interrupt and force a Flush CMD first. At the same time, the whole internal power supply will be switched to Voltage Stabilizer immediately to ensure stable power is supplied throughout the whole drive. This ensures the Flash IC and DDR IC will not operate with unstable power which could lead to data errors or bad data integrity.

### ■ TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.



**■ SMART**

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

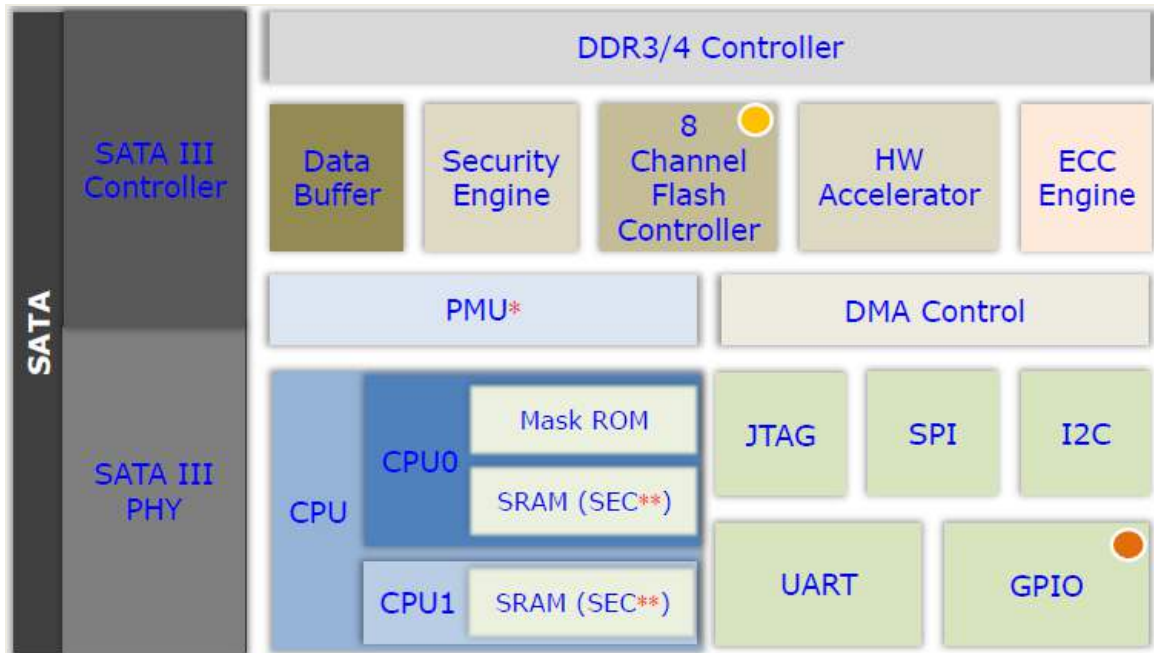
**■ Over-Provision**

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

**■ Thermal Throttling**

Thermal Throttling function is for protecting the drive and reducing the possibility of read / write error due to overheat. The temperature is monitored by the thermal sensor. As the operating temperature continues to increase to threshold temperature, the Thermal Throttling mechanism is activated. At this time, the performance of the drive will be significantly decreased to avoid continuous heating. When the operating temperature falls below threshold temperature, the drive can resume to normal operation.

## ■ Block Diagram



## ■ LBA value

Density	LBA
240 GB	468,862,128
480 GB	937,703,088
960 GB	1,875,385,008
1920 GB	3,750,748,848
3840 GB	7,501,476,528
7680 GB	15,002,931,888

## 5. Security Features

### ■ **Advanced Encryption Standard (AES)**

An AES 256-bit encryption key is generated in the drive's security controller before the data got stored on the NAND flash. When the controller or firmware fails, the data that is securely stored in the encryption key becomes inaccessible through the NAND flash.

### ■ **Secure / Quick Erase**

SQFlash 840 series supports standard SATA command secure erase. Also, with internal AES encryption support, the erase process will start with resetting AES key. By doing so, existing data will be scrambled within 10ms and cannot be recovered anymore. Moreover, erase flag is set when erase function is triggered, which will ensure the whole erase process can be 100% completed. Even there's power interrupt, after power resume, erase operation will be resume right away as well.

### ■ **TCG-OPAL 2.0 Compliance (optional)**

TCG-OPAL compliance SED (Self-encryption Drive) supports a built-in shadow MBR to process user authentication to SSD before booting to normal MBR area and OS. SQFlash 840 series supports such feature with 100% TCG-OPAL compliance. Further, with SQFlash Flash Lock function, the user authentication process in shadow MBR can be done automatically by bonding with motherboard unique ID such as UUID in BIOS / MAC address / TPM unique code. So with Flash Lock enabled, only designated motherboard can have access to the SSD.

### ■ **Write Protect**

SQFlash 840 series supports Write Protect function though firmware setting. Users can perform write protection through SQFlash Smartwp software in DOS interface. The SSD will not execute Write command to perform write protection function by issuing write protection enable command through the DOS interface.

### ■ **Flash Vault**

Flash Vault is to lock Read and Write command by SSD firmware setting and make the SSD need password to verify and only operate with the corresponding platform. User can use Flash Vault to prevent data being stolen by reading the SQFlash SSD with other computers and unauthorized person.

### ■ **Security ID**

Security ID is to encrypt user's specific application software encryption. To enable this function, the application software is required to build Security ID function code and user needs to enable the firmware function by entering Access Code of SQFlash Utility, and then the Security ID can be set. When Security ID sets, the application software is protected by Security ID and SQFlash Utility

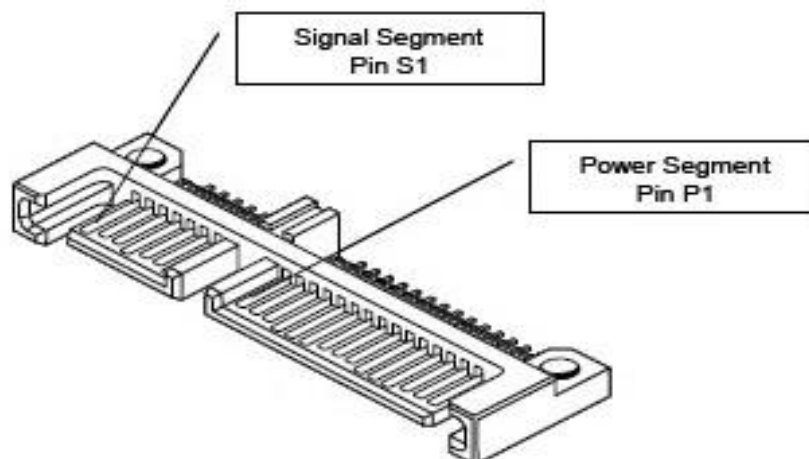
## 6. Pin Assignment and Description

### 6.1 2.5" SATA-SSD Interface Pin Assignments (Signal Segment)

Pin #	Function	Description
S1	GND	2 <sup>nd</sup> mate
S2	A+	Differential signal pair A
S3	A-	
S4	GND	2 <sup>nd</sup> mate
S5	B-	Differential signal pair B
S6	B+	
S7	GND	2 <sup>nd</sup> mate

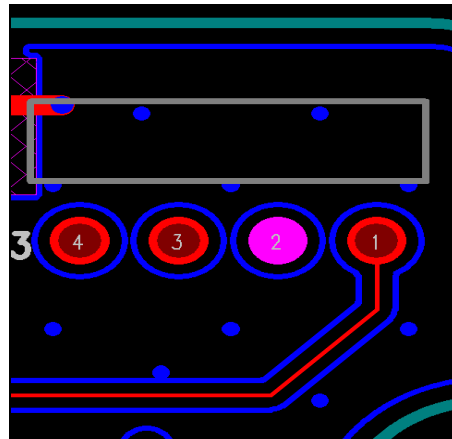
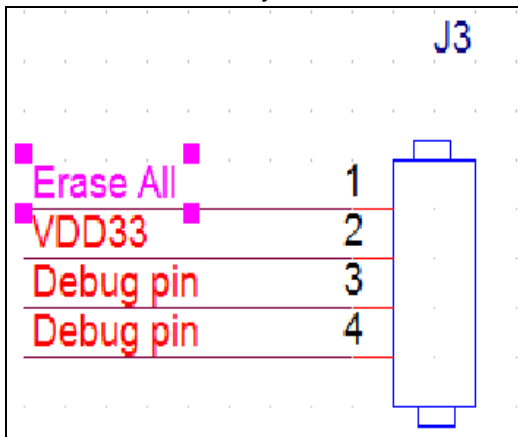
### 6.2 2.5" SATA-SSD Interface Pin Assignments (Power Segment)

Pin #	Function
P1	Not Used (3.3V)
P2	Not Used (3.3V)
P3	Not Used (3.3V Pre-Charge)
P4	GND
P5	GND
P6	GND
P7	5V Pre-Charge
P8	5V
P9	5V
P10	GND
P11	LED pin
P12	GND
P13	Not Used (12V Pre-Charge)
P14	Not Used (12V)
P15	Not Used (12V)

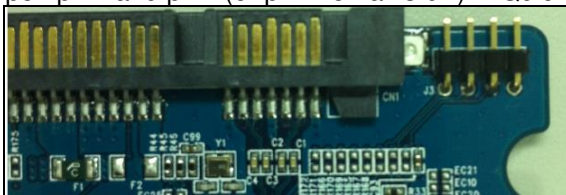


### 6.3 Hardware Quick Erase / Write Protect (Optional, either one support only)

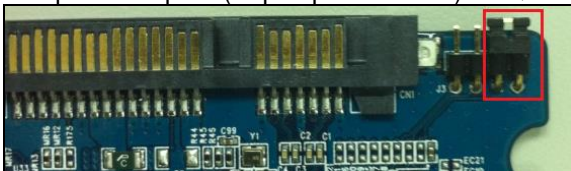
- The Hardware Quick Erase is a function of overall destruction. Once the function is triggered, the SSD controller will set erase flag and reset AES key within 10ms and then all the data in Flash IC will become scrambled data. The SSD will be inaccessible immediately and will be in erase mode before erase process is completed. After that, the new mapping table will be generated. Even there is power failure during the process, erase will be carried on after power resume. Optionally, the function can be set to several different erase protocol, also, can be set to end up with removing firmware and mapping table to make SSD become unusable anymore.
- Write Protect is a function of prohibiting writing data into drive. When the reserved GPIO pins are shorted or pull to 3.3V, all of the write command will be carried to a buffer area without real programming to the Flash IC. So the data won't be saved in this mode and will be totally discarded upon power shutting down.
- GPIO pin is reserved on the PCB without any default function. Optionally the pin can be set to either Quick Erase or Write Protect by loading the specific version firmware. Please contact Advantech sales representative if you would like to enable the function.
- GPIO schematic and layout



- Open pin1 and pin2 (or pin1 remains 0V) → Quick Erase disabled or Write Protect disabled



- Short pin1 and pin2 (or pull pin1 to 3.3V) → Quick Erase enabled or Write Protect enabled



## 7. Identify Device Data

The Identify Device Data enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

Word	ATA Identify Parameter	Value
0	General configuration	0040h
1	Number of cylinders in the default CHS translation	3FFFh
2	Specific configuration	C837h
3	Number of heads in the default CHS translation	0010h
4-5	Retired	0000h
6	Number of sectors per track in the default CHS translation	003Fh
7-8	Reserved for the CFA	0000h
9	Obsolete	0000h
10-19	Serial number	ASCII
20	Retired	0000h
21	Retired	0000h
22	Obsolete	0000h
23-26	Firmware revision	ASCII
27-46	Model number	ASCII
47	READ/WRITE MULTIPLE commands function	8010h
48	Trusted Computing feature set options	4000h
49	Capabilities	2F00h
50	Capabilities	4000h
51-52	Obsolete	0000h
53	field validity	0007h
54	Number of cylinders in the current CHS translation	3FFFh
55	Number of heads in the current CHS translation	0010h
56	Number of sectors per track in the current CHS translation	003Fh
57-58	Current capacity in sectors	00FBFC10h
59	Multiple sector setting	0110h
60-61	Total number of user addressable logical sectors for 28-bit commands	*3
62	Obsolete	0000h
63	Multiword DMA modes	0407h
64	PIO mode supported	0003h
65	Minimum Multiword DMA transfer cycle time per word	0078h
66	Manufacturer's recommended Multiword DMA transfer cycle time	0078h
67	Minimum PIO transfer cycle time without flow control	0078h
68	Minimum PIO transfer cycle time with IORDY flow control	0078h
69	Additional Supported	5F20h
70-73	Reserved	0000h
74	Reserved	0000h
75	Queue depth	001Fh
76	Serial ATA Capabilities	E70Eh
77	Supported Serial ATA Phy speed	0006/0004/0002h
78	Serial ATA features supported	054Ch

79	Serial ATA features enabled	0040h
80	Major version number	03F8h
81	Minor version number	0000h
82	Commands and feature sets supported	746Bh
83	Commands and feature sets supported	7D09h
84	Commands and feature sets supported	4163h
85	Commands and feature sets supported or enabled	7469h
86	Commands and feature sets supported or enabled	BC09h
87	Commands and feature sets supported or enabled	4163h
88	Ultra DMA modes	007Fh
89	Time required for Normal Erase mode SECURITY ERASE UNIT command	0001h
90	Time required for an Enhanced Erase mode SECURITY ERASE UNIT command	0001h
91	Current APM level value	00FEh
92	Master Password Identifier	FFFEh
93	Hardware reset result	0000h
94	Current AAM value	0000h
95	Stream Minimum Request Size	0000h
96	Streaming Transfer Time - DMA	0000h
97	Streaming Access Latency -DMA and PIO	0000h
98-99	Streaming Performance Granularity	0000h
100-103	Total Number of User Addressable Logical Sectors for 48-bit commands	*4
104	Streaming Transfer Time - PIO	0000h
105	Maximum number of 512-byte blocks of LBA Range Entries per DATA SET MANAGEMENT command	0008h
106	Physical sector size / logical sector size	4000h
107	Inter-seek delay for ISO 7999 standard acoustic testing	0000h
108-111	World wide name	Vendor Specific
112-115	Reserved	0000h
116	Reserved for TLC	0000h
117-118	Logical sector size	0000h
119	Commands and feature sets supported	401Ch
120	Commands and feature sets supported or enabled	401Ch
121-124	Reserved for expanded supported and enabled settings	0000h
125-126	Reserved for expanded supported and enabled settings	0000h
127	Obsolete	0000h
128	Security status	0021h
129-159	Vendor specific	0000h
160	CFA power mode	0000h
161-164	Reserved for the CFA	0000h
165-167	Reserved for the CFA	0000h
168	Device Nominal Form Factor	0003h
169	DATA SET MANAGEMENT is supported	0001h
170-173	Additional Product Identifier	0000h
174-175	Reserved	0000h
176-205	Current media serial number	0000h
206	SCT Command Transport	0039h

Specifications subject to change without notice, contact your sales representatives for the most update information.

207-208	Reserved for CE-ATA	0000h
209	Alignment of logical blocks within a physical block	4000h
210-211	Write-Read-Verify Sector Count Mode 3	0000h
212-213	Write-Read-Verify Sector Count Mode 2	0000h
214	NV Cache Capabilities	0000h
215-216	NV Cache Size in Logical Blocks	0000h
217	Nominal media rotation rate	0001h
218	Reserved	0000h
219	NV Cache Options	0000h
220	Current mode of the Write-Read-Verify feature set	0000h
221	Reserved	0000h
222	Transport major version number	107Fh
223	Transport minor version number	0000h
224-227	Reversed for CE-ATA	0000h
228-229	Reversed for CE-ATA	0000h
230-233	Extend Number of User Addressable Sectors	0000h
234	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h	0001h
235	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h	FFFFh
236-239	Reserved	0000h
240-242	Reserved	0000h
243	Security feature 4000 : Self Encrypting Drive	4000h
244-247	Reserved	0000h
248-251	Reserved	0000h
252-254	Reserved	0000h
255	Integrity word	xxA5h

Capacity (GB)	*1 (Word 1/Word 54)	*2 (Word 57 – 58)	*3 (Word 60 – 61)	*4 (Word 100 – 103)
240	3FFFh	FBFC10h	FFFFFFFh	1BF244B0h
480	3FFFh	FBFC10h	FFFFFFFh	37E436B0h
960	3FFFh	FBFC10h	FFFFFFFh	6FC81AB0h
1920	3FFFh	FBFC10h	FFFFFFFh	DF8FE2B0h
3840	3FFFh	FBFC10h	FFFFFFFh	1BF1F72B0h
7680	3FFFh	FBFC10h	FFFFFFFh	37E3E92B0h



## 8. ATA Command Set [Command Set List]

Op-Code		Command Description	Op-Code		Command Description
00h		NOP	60h		Read FPDMA Queued
06h		Data Set Management	61h		Write FPDMA Queued
10h		Recalibrate	70h		Seek
20h		Read Sectors	90h		Execute Device Diagnostic
21h		Read Sectors without Retry	91h		Initialize Device Parameters
24h		Read Sectors EXT	92h		Download Microcode
25h		Read DMA EXT	93h		Download Microcode DMA
27h		Read Native Max Address EXT	B0h		SMART
29h		Read Multiple EXT	B0h	D0h	SMART READ DATA
2Fh		Read Log EXT	B0h	D1h	SMART READ DATA ATTRIBUTE THRESHOLD
30h		Write Sectors	B0h	D2h	SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE
31h		Write Sectors without Retry	B0h	D3h	SMART SAVE ATTRIBUTE VALUES
34h		Write Sectors EXT	B0h	D4h	SMART EXECUTE OFF-LINE IMMEDIATE
35h		Write DMA EXT	B0h	D5h	SMART READ LOG
37h		Set Native Max Address EXT	B0h	D6h	SMART WRITE LOG
39h		Write Multiple EXT	B0h	D8h	SMART ENABLE OPERATIONS
3Dh		Write DMA FUA EXT	B0h	D9h	SMART DISABLE OPERATIONS
3Fh		Write Long EXT	B0h	DAh	SMART RETURN STATUS
40h		Read Verify Sectors	B0h	DBh	SMART ENABLE/DISABLE AUTOMATIC OFF-LINE
41h		Read Verify Sectors without Retry	B1h		DEVICE CONFIGURATION OVERLAY
42h		Read Verify Sectors EXT	B1h	C0h	DEVICE CONFIGURATION RESTORE
45h		Write Uncorrectable EXT	B1h	C1h	DEVICE CONFIGURATION FREEZE LOCK
47h		Read Log DMA EXT	B1h	C2h	DEVICE CONFIGURATION IDENTIFY
57h		Write Log DMA EXT	B1h	C3h	DEVICE CONFIGURATION SET
B1h	C4h	DEVICE CONFIGURATION IDENTIFY DMA	ECh		Identify Device
B1h	C5h	DEVICE CONFIGURATION SET DMA	EFh		Set Features
C4h		Read Multiple	EFh	02h	Enable 8-bit PIO transfer mode

Specifications subject to change without notice, contact your sales representatives for the most update information.

C5h	Write Multiple	EFh	03h		Set transfer mode based on value in Count field
C6h	Set Multiple Mode	EFh	05h		Enable advanced power management
C8h	Read DMA	EFh	10h		Enable use of Serial ATA feature
C9h	Read DMA without Retry	EFh	10h	02h	Enable DMA Setup FIS Auto-Activate optimization
CAh	Write DMA	EFh	10h	03h	Enable Device-initiated interface power state (DIPM) transitions
CBh	Write DMA without Retry	EFh	10h	06h	Enable Software Settings Preservation (SSP)
CEh	Write Multiple FUA EXT	EFh	10h	07h	Enable Device Automatic Partial to Slumber transitions
E0h	Standby Immediate	EFh	10h	09h	Enable Device Sleep
E1h	Idle Immediate	EFh	55h		Disable read look-ahead feature
E2h	Standby	EFh	66h		Disable reverting to power-on defaults
E3h	Idle	EFh	82h		Disable write cache
E4h	Read Buffer	EFh	85h		Disable advanced power management
E5h	Check Power Mode	EFh	90h		Disable use of Serial ATA feature set
E6h	Sleep	EFh	90h	02h	Disable DMA Setup FIS Auto-Activate optimization
E7h	Flush Cache	EFh	90h	03h	Disable Device-initiated interface power state (DIPM) transitions
E8h	Write Buffer	EFh	90h	06h	Disable Software Settings Preservation (SSP)
E9h	Read Buffer DMA	EFh	90h	07h	Disable Device Automatic Partial to Slumber transitions
EAh	Flush Cache EXT	EFh	90h	09h	Disable Device Sleep
EBh	Write Buffer DMA	EFh	AAh		Enable read look-ahead feature
EFh	CCh	Enable reverting to power-on defaults	F4h		Security Erase Unit
F1h	Security Set Password	F5h			Security Freeze Lock
F2h	Security Unlock	F6h			Security Disable Password
F3h	Security Erase Prepare	F8h			Read Native Max Address

Note: ND = Non-Data Command  
 PI = PIO Data-In Command  
 PO = PIO Data-Out Command  
 DM = DMA Command  
 DD = Execute Diagnostic Command

**[Command Set Descriptions]**

**1. CHECK POWER MODE (code: E5h);**

This command allows host to determine the current power mode of the device.

**2. DOWNLOAD MICROCODE (code: 92h);**

This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.

All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the content of the LBA Low register and the Sector Count register.

This allows transfer sizes from 0 bytes to 33,553,920 bytes, in 512bytes increments.

**3. EXECUTE DEVICE DIAGNOSTIC (code: 90h);**

This command performs the internal diagnostic tests implemented by the module.

**4. FLUSH CACHE (code: E7h);**

This command is used by the host to request the device to flush the write cache.

**5. FLUSH CACHE EXT (code: EAh);**

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media.

**6. IDENTIFY DEVICE (code: ECh);**

The IDENTIFY DEVICE command enables the host to receive parameter information from the module.

**7. IDLE (code: 97h or E3h);**

This command allows the host to place the module in the IDLE mode and also set the Standby timer. INTRQ may be asserted even through the module may not have fully transitioned to IDLE mode. If the Sector Count register is non-"0", then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer. If the Sector Count register is "0" then the Standby timer is disabled.

**8. IDLE IMMEDIATE (code: E1h);**

This command causes the module to set BSY, enter the Idle (Read) mode, clear BSY and generate an interrupt.

**9. INITIALIZE DEVICE PARAMETERS (code: 91h);**

This command enables the host to set the number of sectors per track and the number of heads per cylinder.

**10. NOP (code: 00h);**

If this command is issued, the module respond with command aborted.

**11. READ BUFFER (code: E4h);**

This command enables the host to read the current contents of the module's sector buffer.

**12. READ DMA (code: C8h or C9h);**

This command reads from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the

sector specified in the Sector Number register.

**13. READ DMA Ext (code: 25h);**

This command allows the host to read data using the DMA data transfer protocol.

**14. READ MULTIPLE (code: C4h);**

This command performs similarly to the READ SECTORS command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sector per block is defined by the content of word 59 in the IDENTIFY DEVICE response.

**15. READ MULTIPLE EXT (code: 29h);**

This command performs similarly to the READ SECTORS command. The number of sectors per block is defined by a successful SET MULTIPLE command. If no successful SET MULTIPLE command has been issued, the block is defined by the device's default value for number of sectors per block as defined in bits (7:0) in word 47 in the IDENTIFY DEVICE information.

**16. READ NATIVE MAX ADDRESS (code: F8h);**

This command returns the native maximum address. The native maximum address is the highest address accepted by the device in the factory default condition.

**17. READ NATIVE MAX ADDRESS EXT (code: 27h);**

This command returns the native maximum address.

**18. READ SECTOR(S) (code: 20h or 21h);**

This command reads from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

**19. READ SECTOR(S) EXT (code: 24h);**

This command reads from "1" to "65536" sectors as specified in the Sector Count register. A sector count of "0" requests "65536" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

**20. READ VERIFY SECTOR(S) (code: 40h or 41h);**

This command is identical to the READ SECTORS command, except that DRQ is never set and no data is transferred to the host.

**21. READ VERIFY SECTOR(S) EXT (code: 42h);**

This command is identical to the READ SECTORS command, except that DRQ is never set and no data is transferred to the host.

**22. RECALIBRATE (code: 1Xh);**

This command returns value is select address mode by the host request.

**23. SECURITY DISABLE PASSWORD (code: F6h);**

This command transfers 512 bytes of data from the host. Table defines the content of this information. If the password selected by word 0 match the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated when a User password is set.

**24. SECURITY ERASE PREPARE (code: F3h);**

This command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking.

**25. SECURITY ERASE UNIT (code: F4h);**

This command transfers 512 bytes of data from the host. Table## defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command.

**26. SECURITY FREEZE LOCK (code: F5h);**

This command shall set the device to frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen shall be disabled by power-off or hardware reset.

If SECURITY FREEZE LOCK is issued when the drive is in frozen mode, the drive executes the command and remains in frozen mode.

**27. SECURITY SET PASSWORD (code: F1h);**

This command transfers 512 bytes of data from the host. Table defines the content of this information. The data transferred controls the function of this command. Table defines the interaction of the identifier and security level bits.

**28. SECURITY UNLOCK (code: F2h);**

This command transfers 512 bytes of data from the host. Table (as Disable Password) defines the content of this information.

If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the identifier bit is set to user then the device shall compare the supplied password with the stored User password.

If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall be decremented for each password mismatch when SECURITY UNLOCK is issued and the device is locked. When this counter reaches zero then SECURITY UNLOCK and SECURITY ERASE UNIT command shall be aborted until a power-on or hardware reset.

**29. SEEK (code: 7Xh);**

This command performs address range check.

**30. SET MAX ADDRESS (code: F9h);**

After successful command completion, all read and write access attempts to address greater than specified by the successful SET MAX ADDRESS command shall be rejected with an IDNF error.

IDENTIFY DEVICE response words (61:60) shall reflect the maximum address set with this command.

**31. SET MAX ADDRESS EXT (code: 37h);**

After successful command completion, all read and write access attempts to address greater than specified by the successful SET MAX ADDRESS command shall be rejected with an IDNF error.

IDENTIFY DEVICE response words (61:60) shall reflect the maximum address set with this command.

**32. SET FEATURE (code: EFh);**

This command is used by the host to establish parameters that affect the execution of certain device features.

**33. SET MULTIPLE MODE (code: C6h);**

This command enables the device to perform READ and Write Multiple operations and establishes the block count for these commands.

**34. SLEEP (code: 99h or E6h);**

This command causes the module to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

- 35. SMART READ DATA (code: B0h with Feature register value of D0h);**  
This command returns the Device SMART data structure to the host.
- 36. SMART ENABLE/DISABLE AUTO SAVE (code: B0h with Feature register value of D2h);**  
This command enables and disables the optional attribute auto-save feature of the device.
- 37. SMART EXECUTE OFF\_LINE (code: B0h with Feature register value of D4h);**  
This command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory, or execute a self-diagnostic test routine in either captive or off-line mode.
- 38. SMART READ LOG (code: B0h with Feature register value of D5h);**  
This command returns the specified log data to the host.
- 39. SMART ENABLE OPERATION (code: B0h with Feature register value of D8h);**  
This command enables access to all SMART capabilities within the device. Prior to receipt of this command SMART data are neither monitored nor saved by the device.
- 40. SMART DISABLE OPERATION (code: B0h with Feature register value of D9h);**  
This command disables all SMART capabilities within the device including any and all timer and event count functions related exclusively to this feature. After command acceptance the device shall disable all SMART operations.  
After receipt of this command by the device, all other SMART commands including SMART DISABLE OPERATION commands, with exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be command aborted by the device.
- 41. SMART RETURN STATUS (code: B0h with Feature register value of DAh);**  
This command causes the device to communicate the reliability status of the device to the host.
- 42. STANDBY (code: E2h);**  
This command causes the module to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.
- 43. STANDBY IMMEDIATE (code: E0h);**  
This command causes the module to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.
- 44. WRITE BUFFER (code: E8h);**  
This command enables the host to overwrite contents of the module's sector buffer with any data pattern desired.
- 45. WRITR DMA (code: CAh or CBh);**  
This command writes from "1" to "256" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.
- 46. WRITR DMA EXT (code: 35h);**  
This command writes from "1" to "65536" sectors as specified in the Sector Count register using the DMA data transfer protocol. A sector count of "0" requests "65536" sectors transfer. The transfer begins at the sector specified in the Sector Number register.
- 47. WRITE MULTIPLE (code: C5h);**

This command is similar to the WRITE SECTORS command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

**48. WRITE MULTIPLE EXT (code: 39h);**

This command is similar to the WRITE SECTORS command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

**49. WRITE SECTOR(S) (code: 30h);**

This command writes from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

**50. WRITE SECTOR(S) EXT (code: 34h);**

This command writes from "1" to "65536" sectors as specified in the Sector Count register. A sector count of "0" requests "65536" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

**51. WRITE SECTOR(S) W/O ERASE (code: 38h);**

This command writes from "1" to "256" sectors as specified in the Sector Count register. A sector count of "0" requests "256" sectors transfer. The transfer begins at the sector specified in the Sector Number register.

**52. WRITE VERIFY (code: 3Ch);**

This command is similar to the WRITE SECTOR(S) command, except that each sector is verified before the command is completed.

## 9. System Power Consumption

### 9.1 Supply Voltage

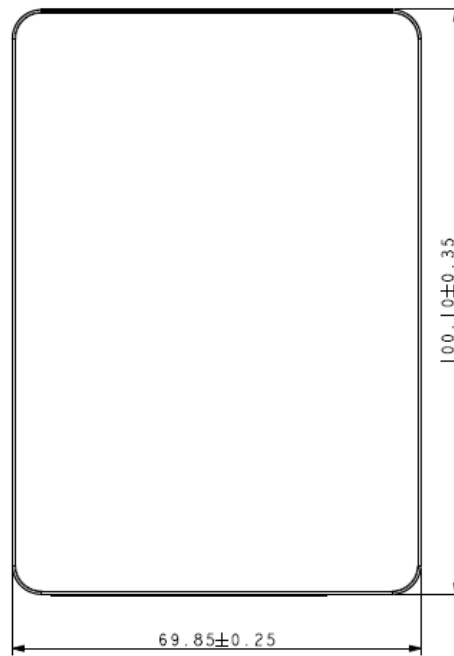
Parameter	Rating
Operating Voltage	5V

### 9.2 Power Consumption

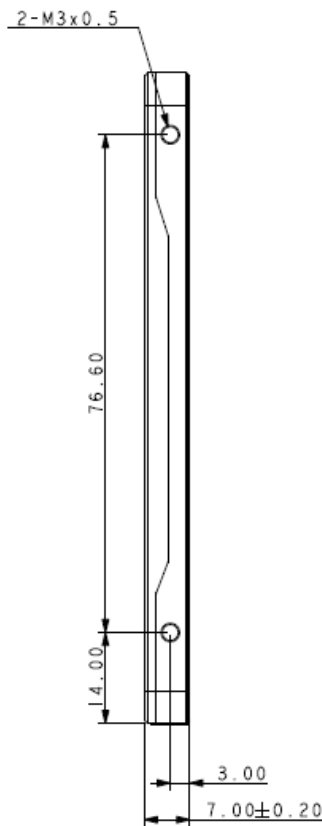
Unit: W		Read	Write	Idle
3D TLC (BiCS3)	240 GB	3.0	2.5	1.5
	480 GB	3.0	2.5	1.5
	960 GB	3.5	3.0	1.5
	1920 GB	3.5	3.2	1.5
	3840 GB	4.0	3.5	1.5
	7680 GB	4.0	4.0	1.5



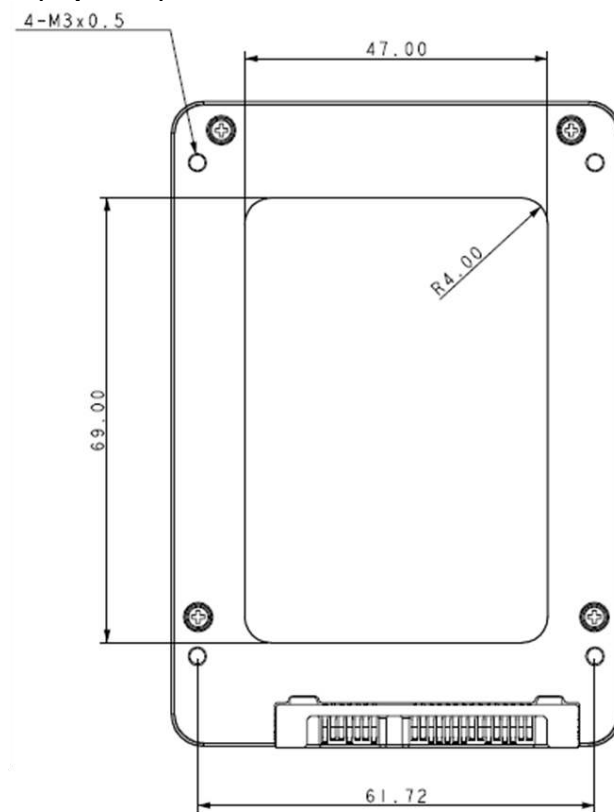
### 10. Physical Dimension 2.5" SATA SSD (Unit: mm)



(Top View)



(Side View)



(Bottom View)

**Appendix: Part Number Table**

Product	Advantech PN
SQF 2.5 SATA SSD 840 240G 3D TLC (0~70°C)	SQF-S25V4-240G-SCC
SQF 2.5 SATA SSD 840 480G 3D TLC (0~70°C)	SQF-S25V8-480G-SCC
SQF 2.5 SATA SSD 840 960G 3D TLC (0~70°C)	SQF-S25V8-960G-SCC
SQF 2.5 SATA SSD 840 1920G 3D TLC (0~70°C)	SQF-S25VF-1K9G-SCC
SQF 2.5 SATA SSD 840 3840G 3D TLC (0~70°C)	SQF-S25VF-3K8G-SCC
SQF 2.5 SATA SSD 840 7680G 3D TLC (0~70°C)	SQF-S25VF-7K6G-SCC
SQF 2.5 SATA SSD 840 240G 3D TLC (-40~85°C)	SQF-S25V4-240G-SCE
SQF 2.5 SATA SSD 840 480G 3D TLC (-40~85°C)	SQF-S25V8-480G-SCE
SQF 2.5 SATA SSD 840 960G 3D TLC (-40~85°C)	SQF-S25V8-960G-SCE
SQF 2.5 SATA SSD 840 1920G 3D TLC (-40~85°C)	SQF-S25VF-1K9G-SCE
SQF 2.5 SATA SSD 840 3840G 3D TLC (-40~85°C)	SQF-S25VF-3K8G-SCE
SQF 2.5 SATA SSD 840 7680G 3D TLC (-40~85°C)	SQF-S25VF-7K6G-SCE