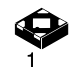
Low Dropout Regulator, Very-Low Quiescent Current, I_Q 25 μA, Low Noise

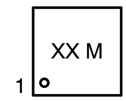
200 mA

NCP707



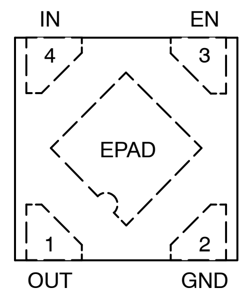
XDFN4
MX SUFFIX
CASE 711AJ

MARKING DIAGRAM



XX = Specific Device Code
M = Date Code

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 18 of this data sheet.

The NCP707 is 200 mA LDO that provides the engineer with a very stable, accurate voltage with very low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP707 employs the dynamic quiescent current adjustment for very low I_Q consumption at no−load.

Features

- Operating Input Voltage Range: 1.8 V to 5.5 V
- Available in Fixed Voltage Options: 1.5 V to 3.3 V
  Contact Factory for Other Voltage Options
- Very Low Quiescent Current of Typ. 25 μA
- Very Low Noise: 22 μV_{RMS} from 100 Hz to 100 kHz
- Very Low Dropout: 100 mV Typical at 200 mA
- ±2% Accuracy Over Load/Line/Temperature
- High Power Supply Ripple Rejection: 70 dB at 1 kHz
- Thermal Shutdown and Current Limit Protections
- Stable with a 1 μF Ceramic Output Capacitor
- Available in XDFN 1.0 x 1.0 mm Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applicaitons

- PDAs, Mobile phones, GPS, Smartphones
- Wireless Handsets, Wireless LAN, Bluetooth®, Zigbee®
- Portable Medical Equipment
- Other Battery Powered Applications

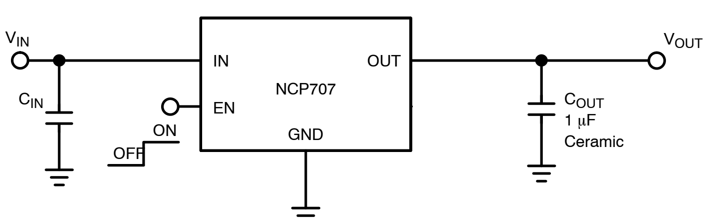
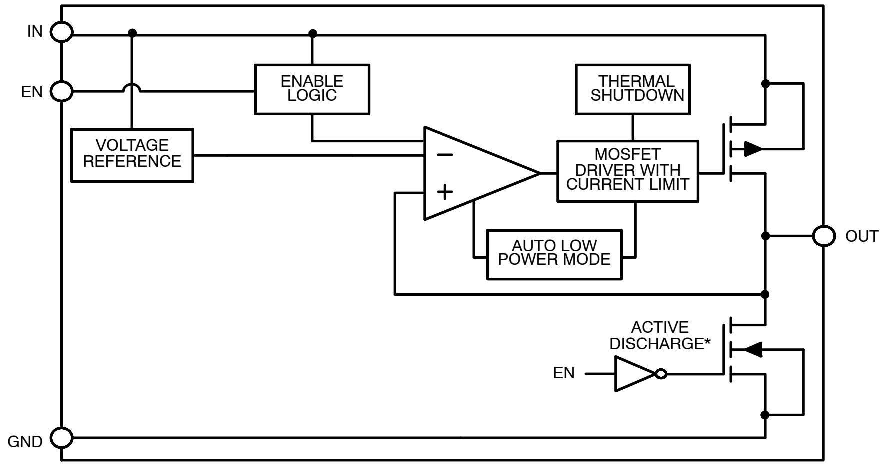


Figure 1. Typical Application Schematic

September, 2022 − Rev. 10

Publication Order Number:
NCP707/D



*Active output discharge function is present only in NCP707AMXyyyTCG and NCP707CMXyyyTCG devices.
yyy denotes the particular V_{OUT} option.

Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OUT	Regulated output voltage pin. A small ceramic capacitor with minimum value of 1 μF is needed from this pin to ground to assure stability.
2	GND	Power supply ground.
3	EN	Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
4	IN	Input pin. A small 1 μF capacitor is needed from this pin to ground to assure stability.
–	EPAD	Exposed pad should be connected directly to the GND pin. Soldered to a large ground copper plane allows for effective heat removal.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6 V	V
Output Voltage	V_{OUT}	−0.3 V to V_{IN} + 0.3 V	V
Enable Input	V_{EN}	−0.3 V to V_{IN} + 0.3 V	V
Output Short Circuit Duration	t_{SC}	∞	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Rating tested per JEDEC standard: JESD78

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN4 1x1 mm Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	250	°C/W

3. Single component mounted on 2 oz, FR4 PCB with 100 mm^2 Cu area.

ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125°C$; $V_{IN} = V_{OUT(NOM)} + 0.5$ V or 1.9 V, whichever is greater; $I_{OUT} = 10$ mA, $C_{IN} = C_{OUT} = 1$ µF, unless otherwise noted. $V_{EN} = 0.9$ V. Typical values are at $T_J = +25°C$. Min./Max. are for $T_J = -40°C$ and $T_J = +125°C$ respectively (Note 4).

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.8		5.5	V
Output Voltage Accuracy	$V_{OUT} + 0.5\ V \le V_{IN} \le 5.5$ V, $I_{OUT} = 0 - 200$ mA		V_{OUT}	−2		+2	%
Line Regulation	$V_{OUT} + 0.5\ V \le V_{IN} \le 5.5$ V, $I_{OUT} = 10$ mA		Reg_{LINE}		400		µV/V
Load Regulation	$I_{OUT} = 0$ mA to 200 mA		Reg_{LOAD}		10		µV/mA
Load Transient	$I_{OUT} = 1$ mA to 200 mA or 200 mA to 1 mA in 1 µs, $C_{OUT} = 1$ µF		$Tran_{LOAD}$		75		mV
Dropout Voltage (Note 5)	$I_{OUT} = 200$ mA	$V_{OUT} = 1.5$ V	V_{DO}		415	490	mV
		$V_{OUT} = 1.8$ V			221	380	
		$V_{OUT} = 1.85$ V			218	370	
		$V_{OUT} = 2.5$ V			135	225	
		$V_{OUT} = 2.8$ V			118	175	
		$V_{OUT} = 2.85$ V			114	170	
		$V_{OUT} = 3.0$ V			111	165	
		$V_{OUT} = 3.1$ V			107	160	
		$V_{OUT} = 3.2$ V			105	155	
		$V_{OUT} = 3.3$ V			100	150	
Output Current Limit	$V_{OUT} = 90\%\ V_{OUT(nom)}$		I_{CL}	250	379	500	mA
Ground Current	$I_{OUT} = 0$ mA		I_Q		25	35	µA
	$I_{OUT} = 2$ mA		I_{GND}		105		µA
	$I_{OUT} = 200$ mA		I_{GND}		240		µA
Shutdown Current	$V_{EN} \le 0.4$ V, $V_{IN} = 5.5$ V		I_{DIS}		0.01	1	µA
EN Pin Threshold Voltage High Threshold Low Threshold	 V_{EN} Voltage increasing V_{EN} Voltage decreasing		 V_{EN_HI} V_{EN_LO}	 0.9 		 0.4	V
EN Pin Input Current	$V_{EN} = 5.5$ V		I_{EN}		180	500	nA
Turn−on Time	$C_{OUT} = 1.0$ µF, From assertion of V_{EN} to 98% $V_{OUT(NOM)}$		t_{ON}		200		µs
Power Supply Rejection Ratio	$V_{IN} = 3.6$ V, $V_{OUT} = 3.1$ V $I_{OUT} = 150$ mA	f = 100 Hz f = 1 kHz f = 10 kHz	PSRR		58 70 55		dB
Output Noise Voltage	$V_{OUT} = 3.1$ V, $V_{IN} = 3.6$ V, $I_{OUT} = 200$ mA f = 100 Hz to 100 kHz		V_N		22		μV_{rms}
Thermal Shutdown Temperature	Temperature increasing from $T_J = +25°C$		T_{SD}		160		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}		T_{SDH}		20		°C
Active Output Discharge Resistance	$V_{EN} < 0.4$ V, Version A only $V_{EN} < 0.4$ V, Version C only		R_{DIS}		1.2 120		kΩ Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_J = T_A = 25°C$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Characterized when V_{OUT} falls 100 mV below the regulated voltage at $V_{IN} = V_{OUT(NOM)} + 0.5$ V.

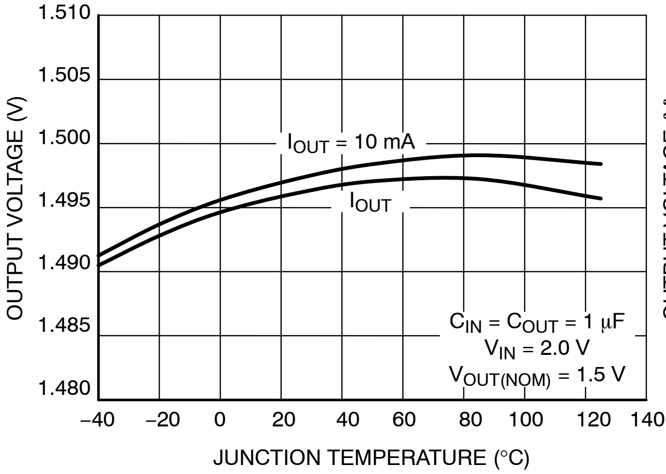


Figure 3. Output Voltage vs. Temperature
V_{OUT} = 1.5 V

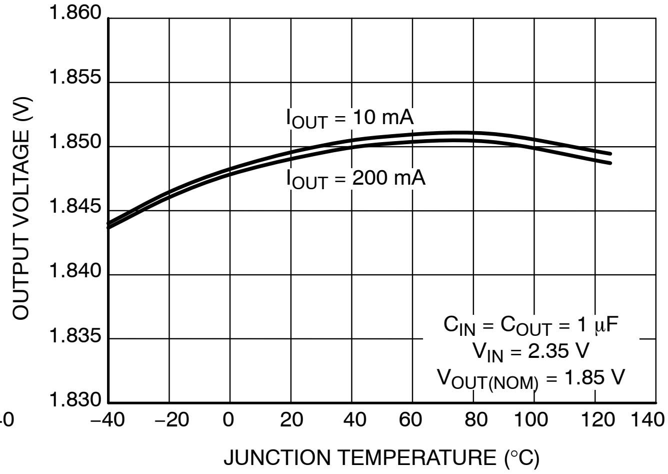


Figure 4. Output Voltage vs. Temperature
V_{OUT} = 1.85 V

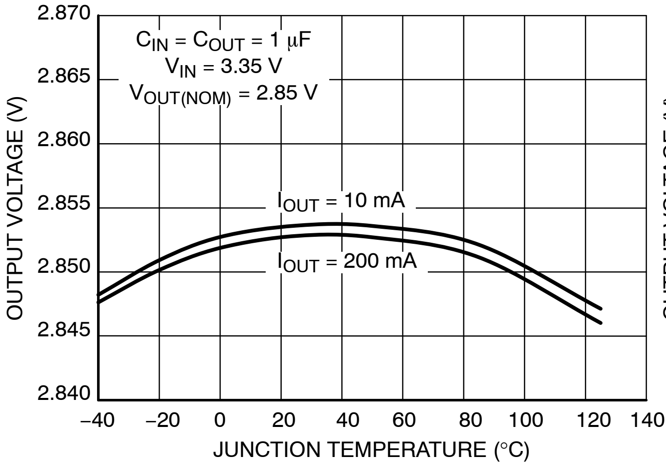


Figure 5. Output Voltage vs. Temperature
V_{OUT} = 2.85 V

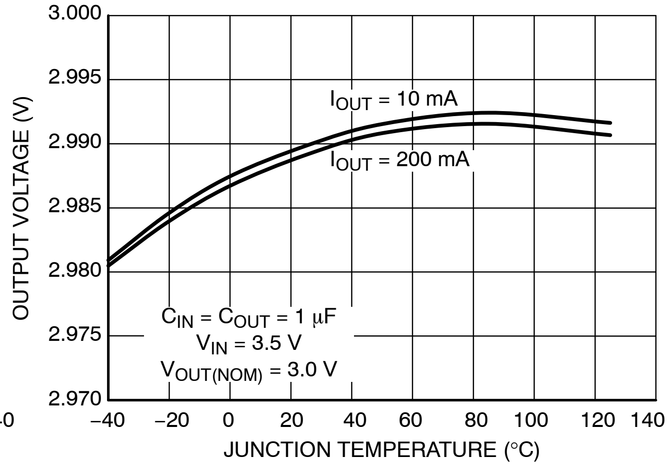


Figure 6. Output Voltage vs. Temperature
V_{OUT} = 3.0 V

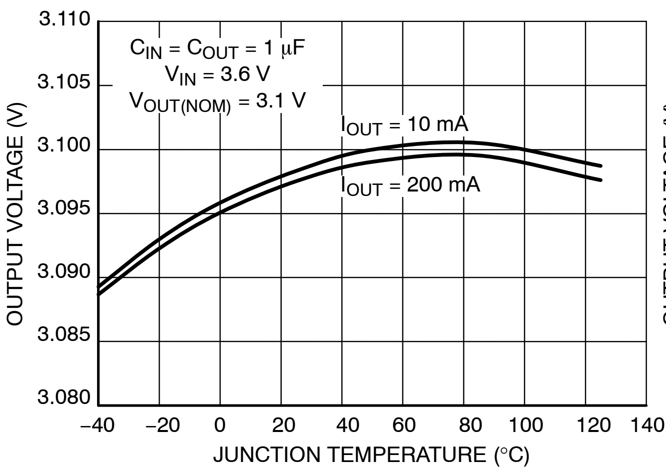


Figure 7. Output Voltage vs. Temperature
V_{OUT} = 3.1 V

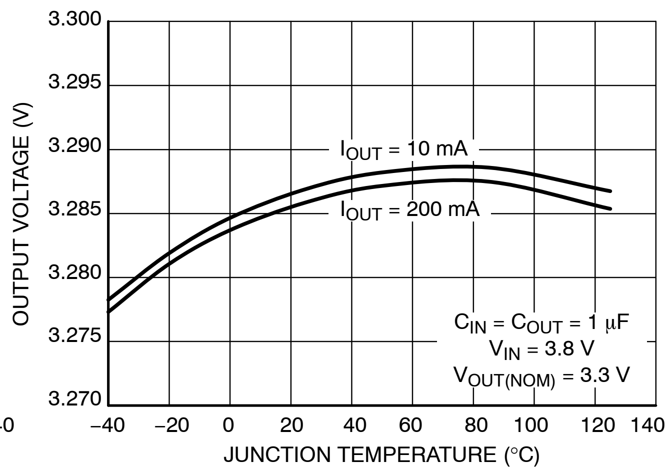


Figure 8. Output Voltage vs. Temperature
V_{OUT} = 3.3 V

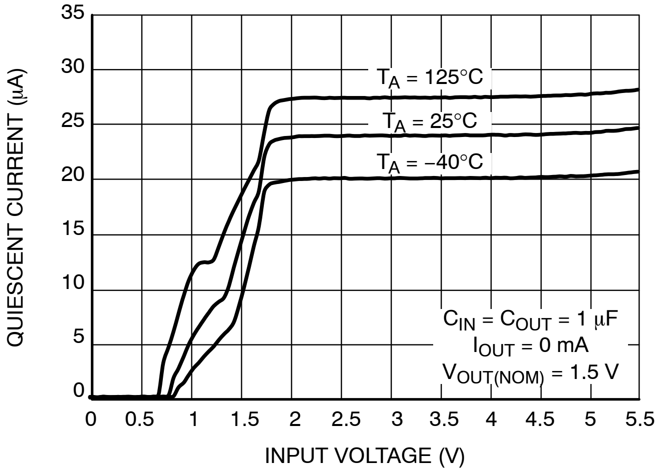


Figure 9. Quiescent Current vs. Input Voltage V_{OUT} = 1.5 V

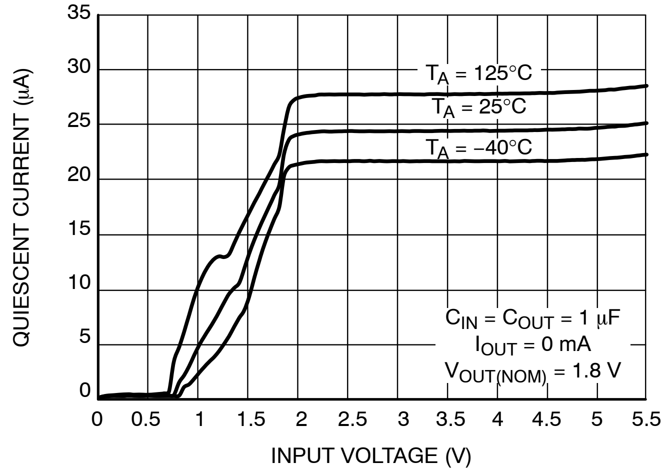


Figure 10. Quiescent Current vs. Input Voltage V_{OUT} = 1.8 V

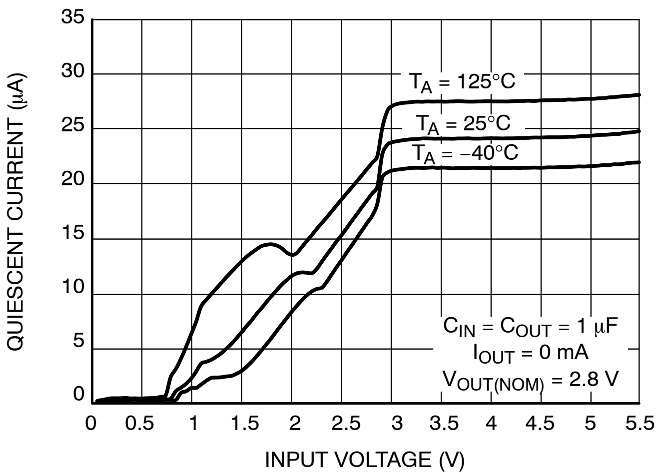


Figure 11. Quiescent Current vs. Input Voltage V_{OUT} = 2.8 V

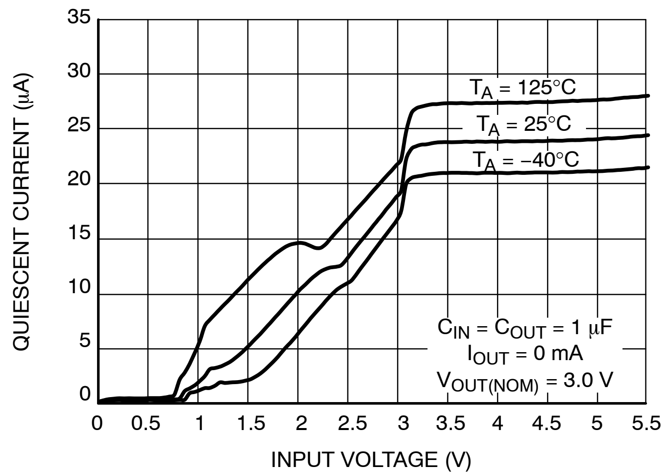


Figure 12. Quiescent Current vs. Input Voltage V_{OUT} = 3.0 V

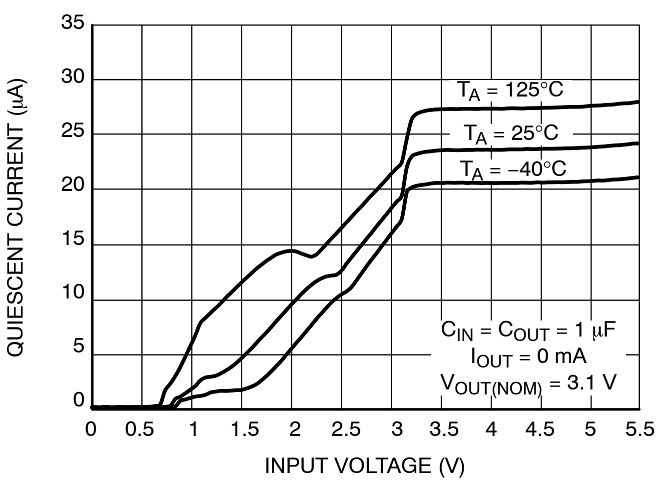


Figure 13. Quiescent Current vs. Input Voltage V_{OUT} = 3.1 V

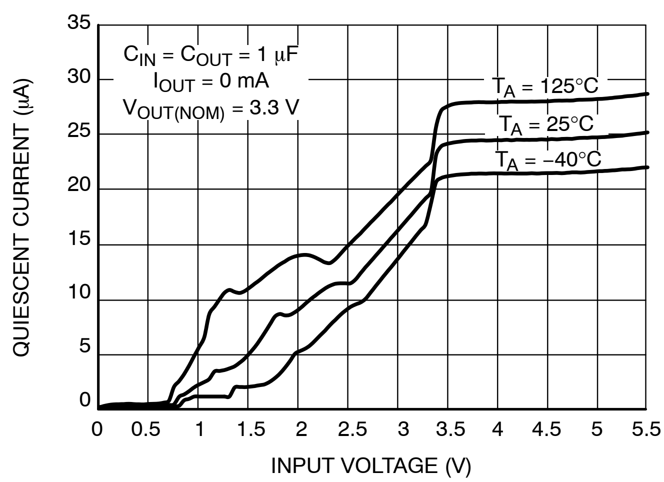


Figure 14. Quiescent Current vs. Input Voltage V_{OUT} = 3.3 V

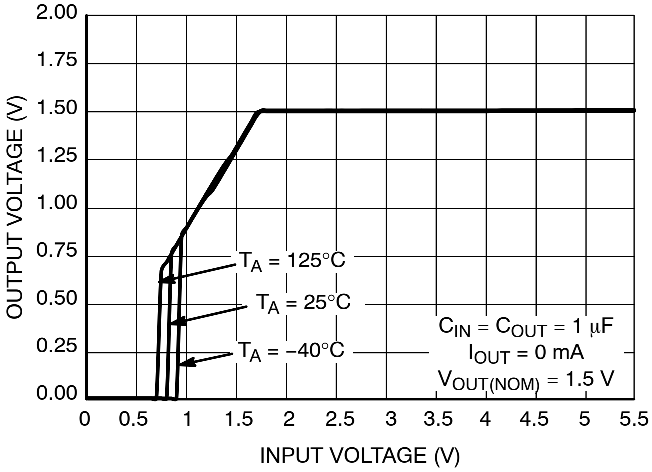


Figure 15. Output Voltage vs. Input Voltage V_{OUT} = 1.5 V

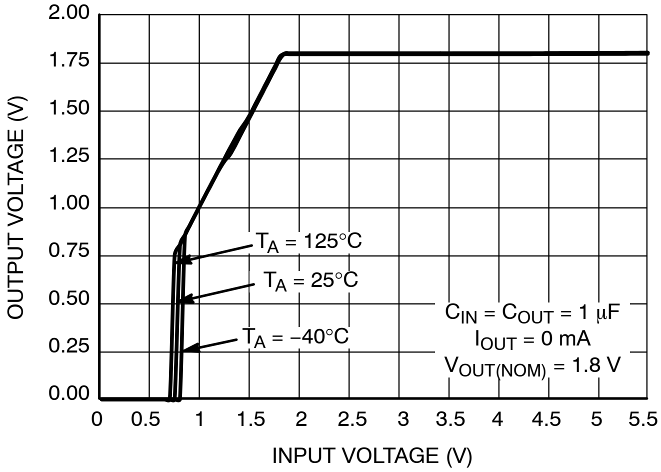


Figure 16. Output Voltage vs. Input Voltage V_{OUT} = 1.8 V

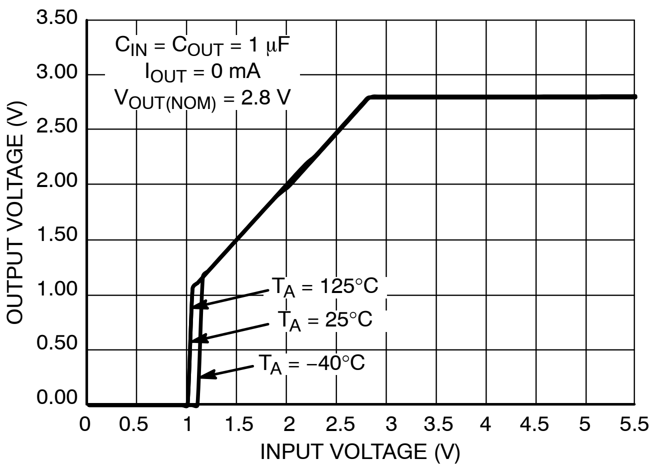


Figure 17. Output Voltage vs. Input Voltage V_{OUT} = 2.8 V

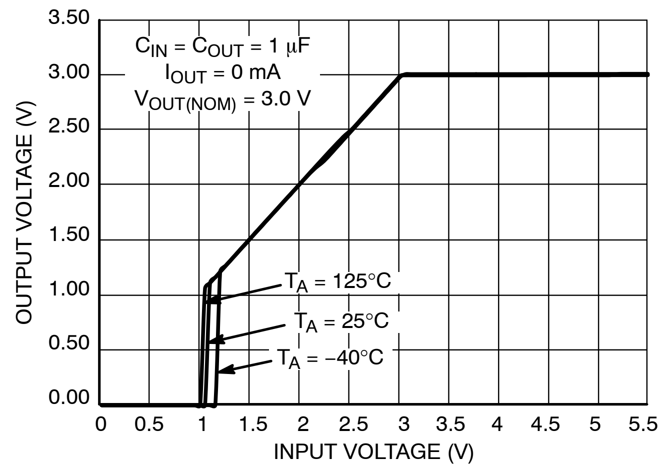


Figure 18. Output Voltage vs. Input Voltage V_{OUT} = 3.0 V

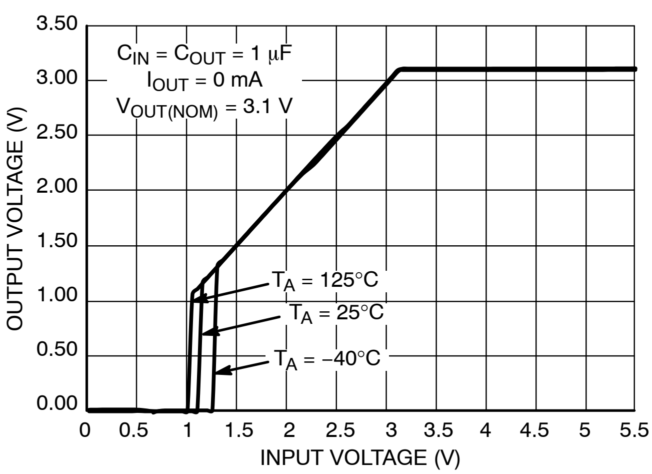


Figure 19. Output Voltage vs. Input Voltage V_{OUT} = 3.1 V

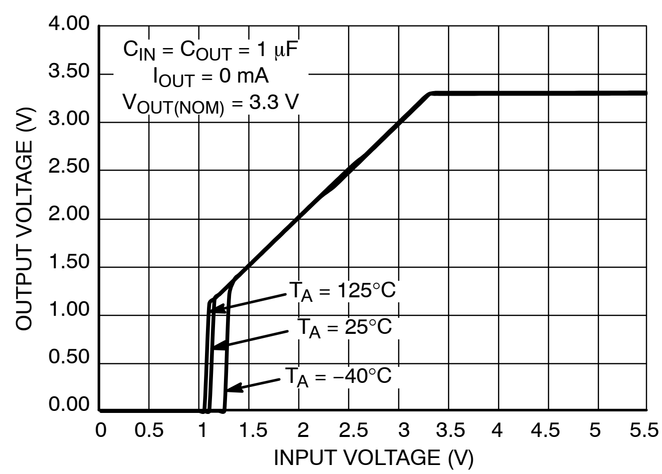


Figure 20. Output Voltage vs. Input Voltage V_{OUT} = 3.3 V

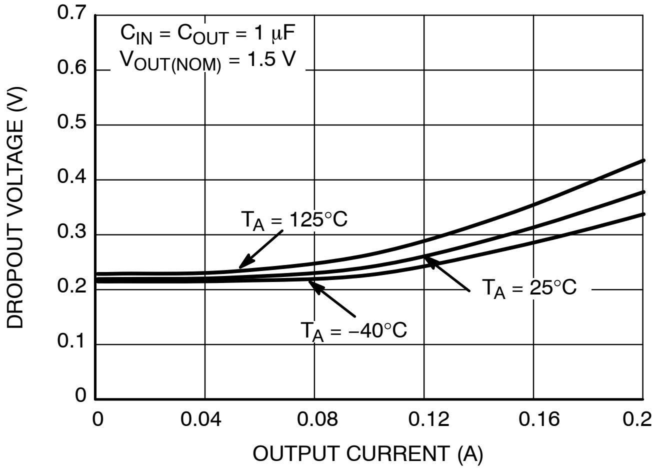


Figure 21. Dropout Voltage vs. Output Current $V_{OUT} = 1.5\ V$

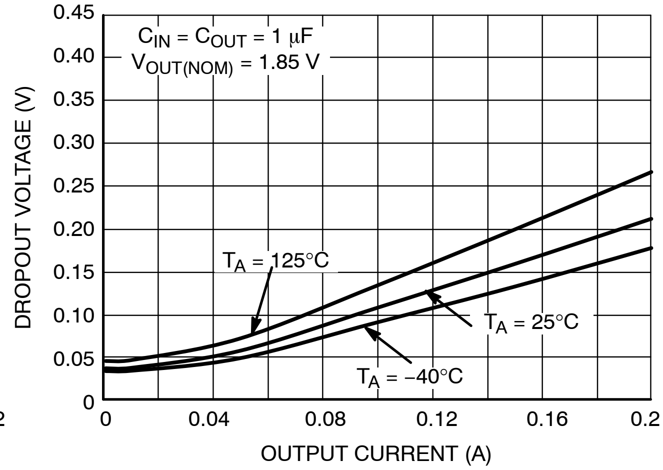


Figure 22. Dropout Voltage vs. Output Current $V_{OUT} = 1.85\ V$

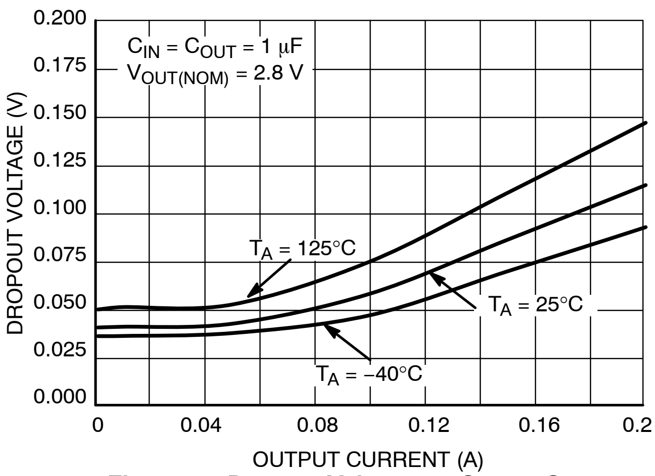


Figure 23. Dropout Voltage vs. Output Current $V_{OUT} = 2.8\ V$

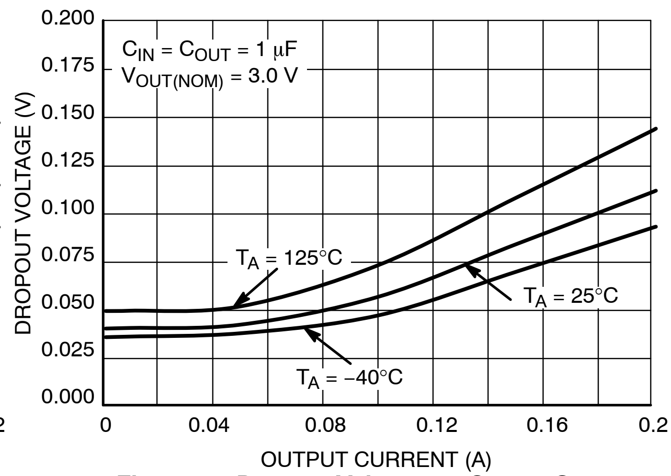


Figure 24. Dropout Voltage vs. Output Current $V_{OUT} = 3.0\ V$

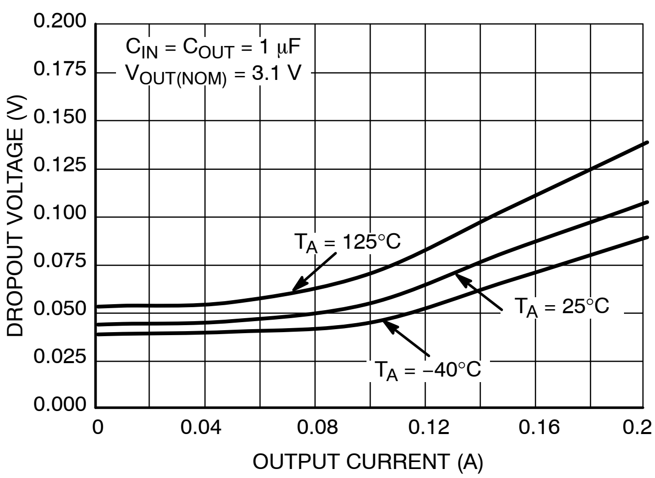


Figure 25. Dropout Voltage vs. Output Current $V_{OUT} = 3.1\ V$

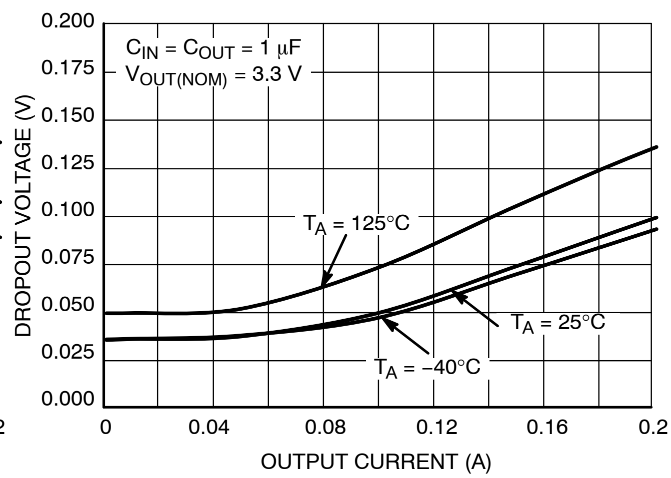


Figure 26. Dropout Voltage vs. Output Current $V_{OUT} = 3.3\ V$

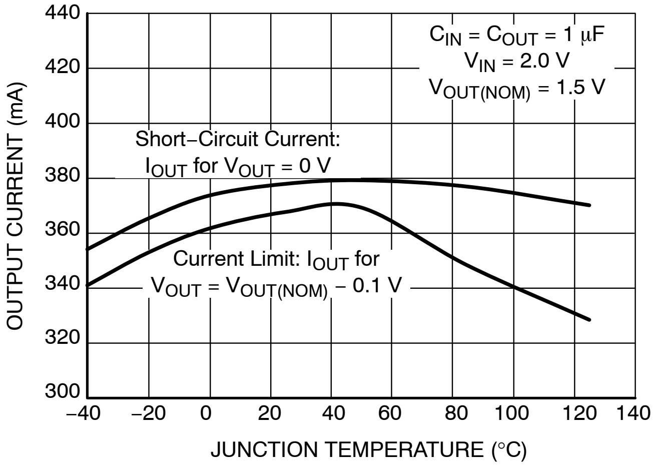


Figure 27. Short−Circuit Limit vs. Temperature V_{OUT} = 1.5 V

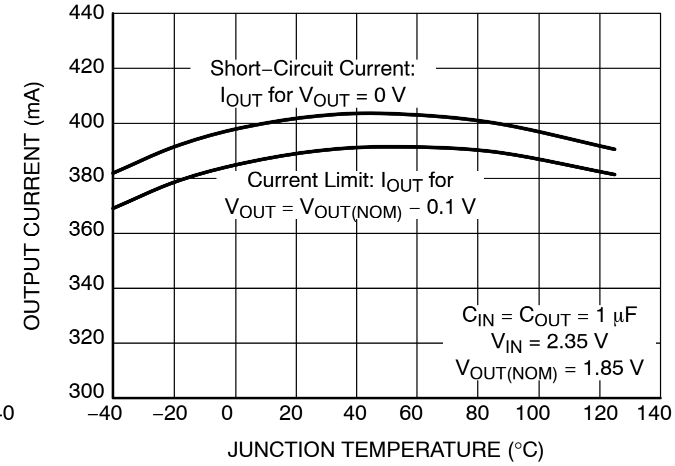


Figure 28. Short−Circuit Limit vs. Temperature V_{OUT} = 1.85 V

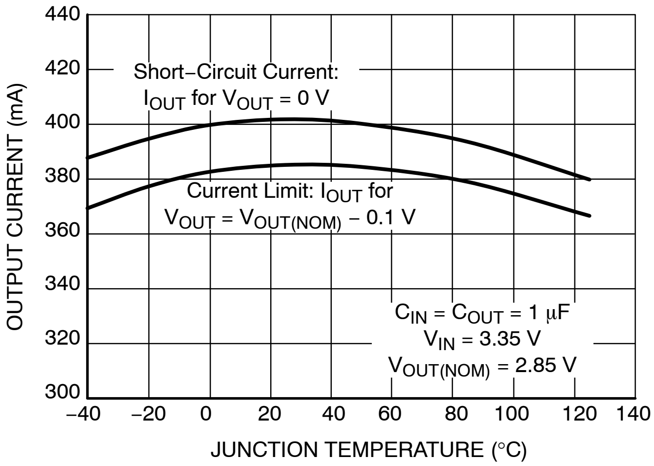


Figure 29. Short−Circuit Limit vs. Temperature V_{OUT} = 2.85 V

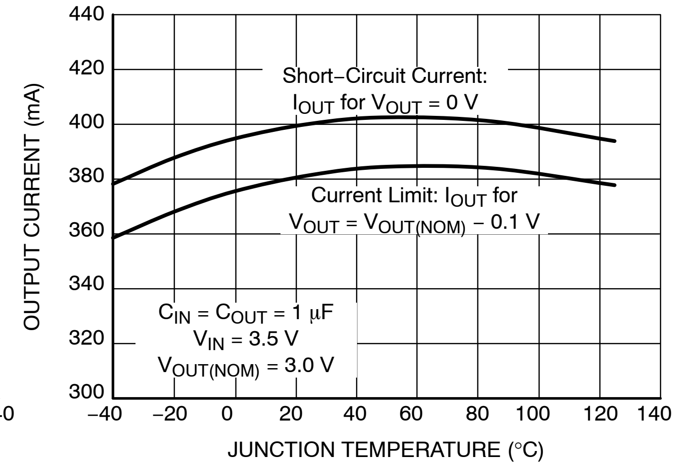


Figure 30. Short−Circuit Limit vs. Temperature V_{OUT} = 3.0 V

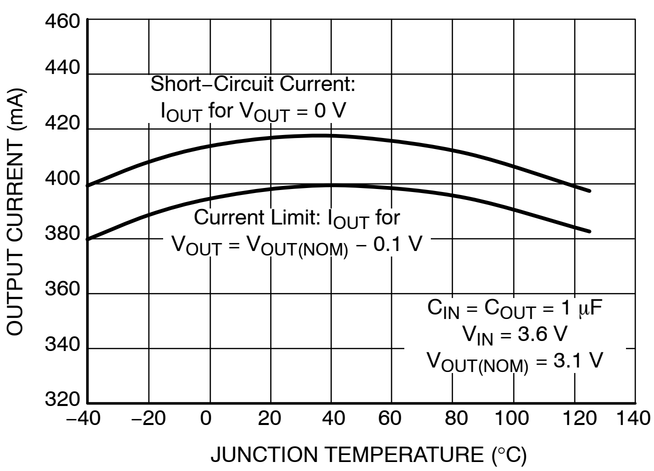


Figure 31. Short−Circuit Limit vs. Temperature V_{OUT} = 3.1 V

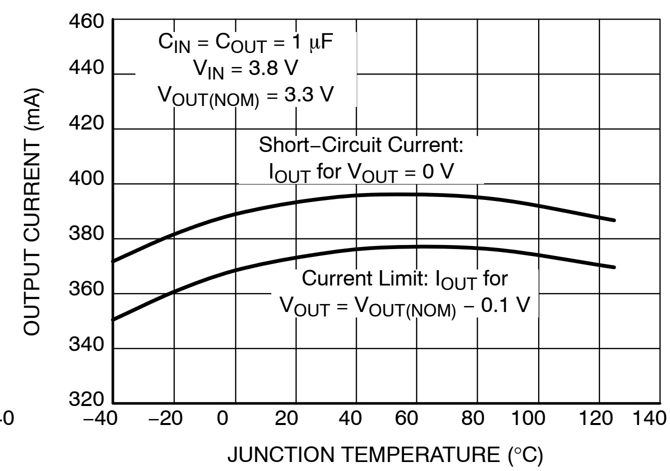


Figure 32. Short−Circuit Limit vs. Temperature V_{OUT} = 3.3 V

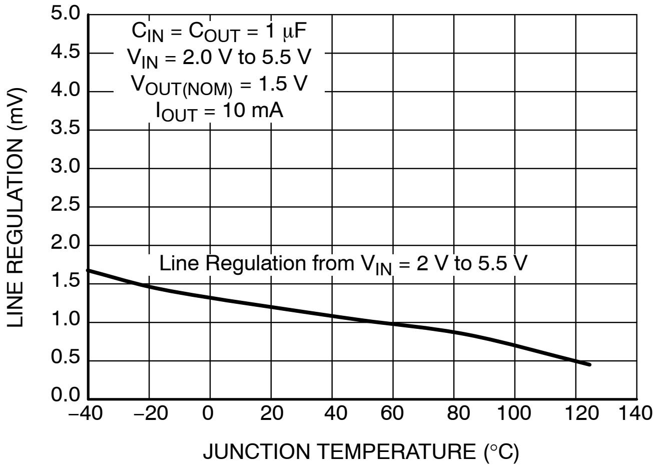


Figure 33. Line Regulation vs. Temperature V_{OUT} = 1.5 V

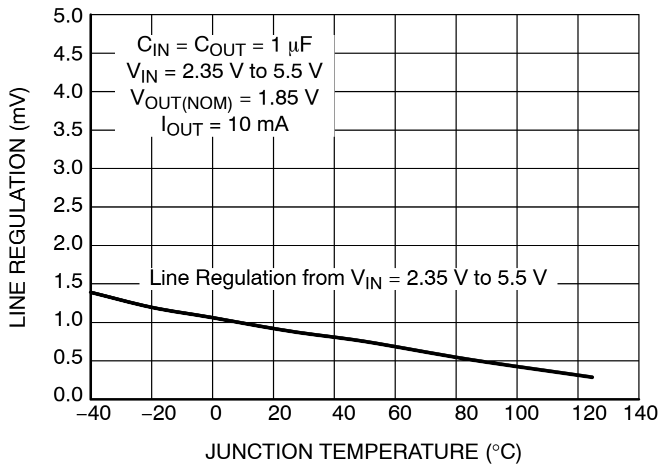


Figure 34. Line Regulation vs. Temperature V_{OUT} = 1.85 V

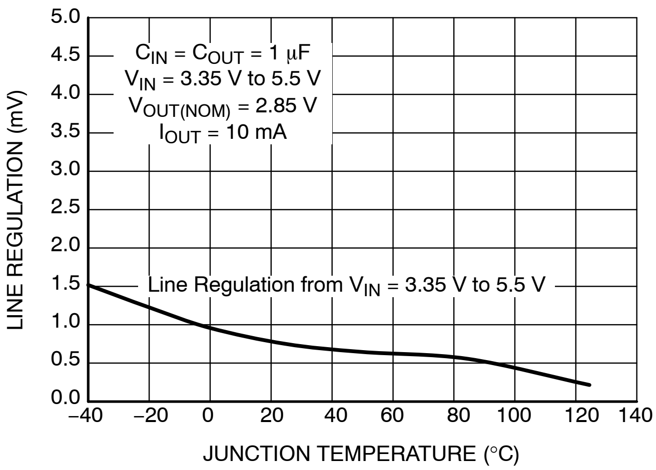


Figure 35. Line Regulation vs. Temperature V_{OUT} = 2.85 V

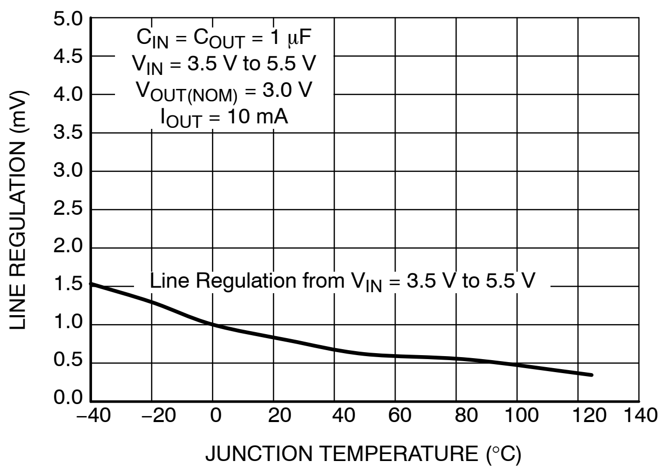


Figure 36. Line Regulation vs. Temperature V_{OUT} = 3.0 V

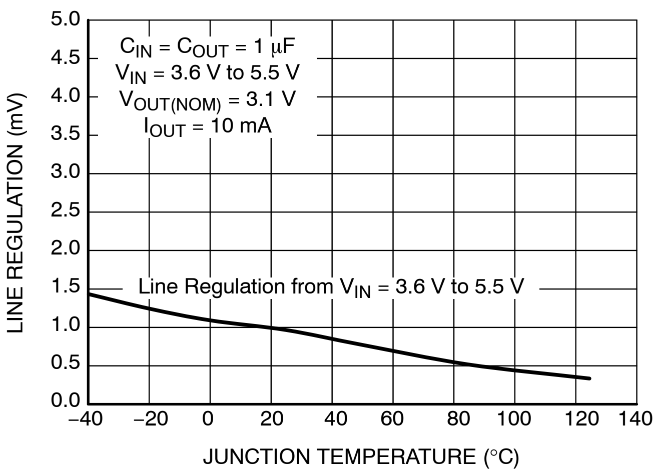


Figure 37. Line Regulation vs. Temperature V_{OUT} = 3.1 V

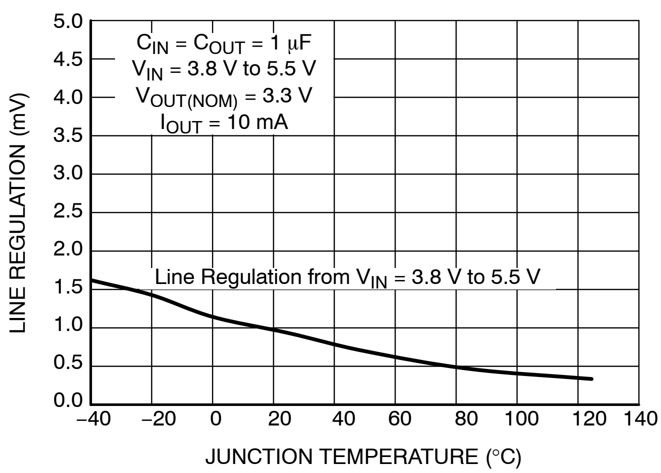


Figure 38. Line Regulation vs. Temperature V_{OUT} = 3.3 V

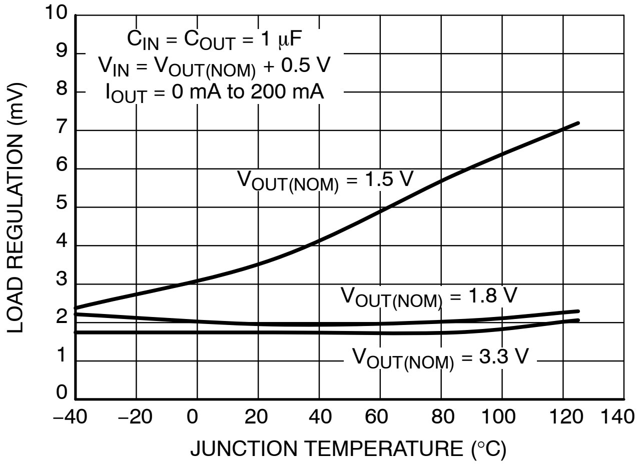


Figure 39. Load Regulation vs. Temperature

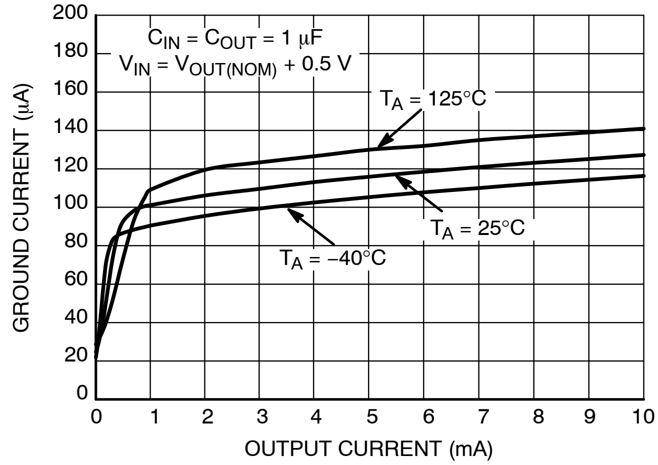


Figure 40. Ground Current vs. Output Current

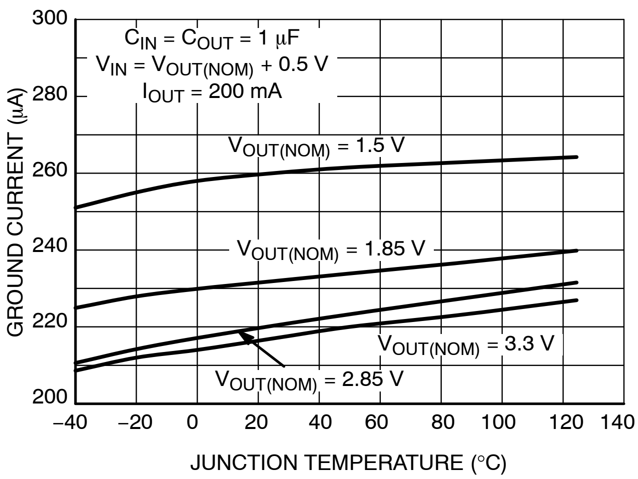


Figure 41. Ground Current vs. Temperature

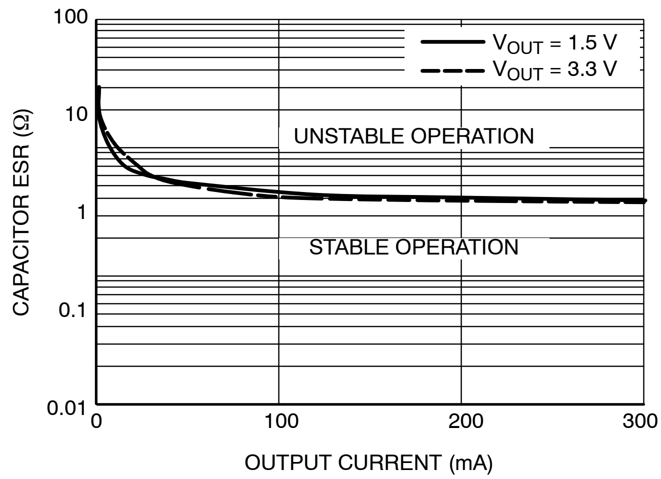


Figure 42. Stability vs. Output Capacitor ESR

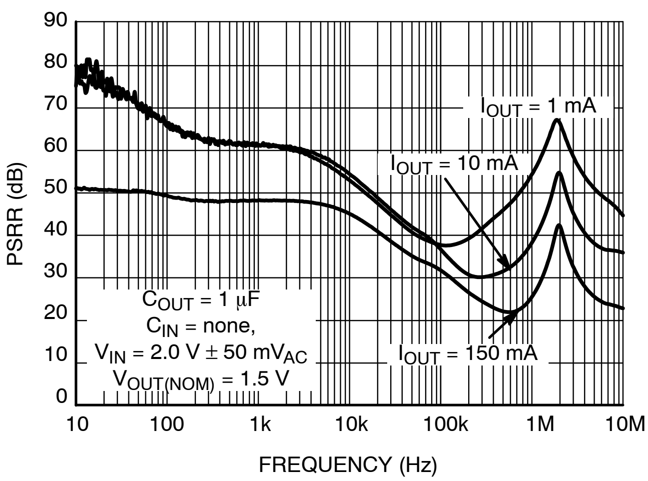


Figure 43. PSRR vs. Frequency V_{OUT} = 1.5 V

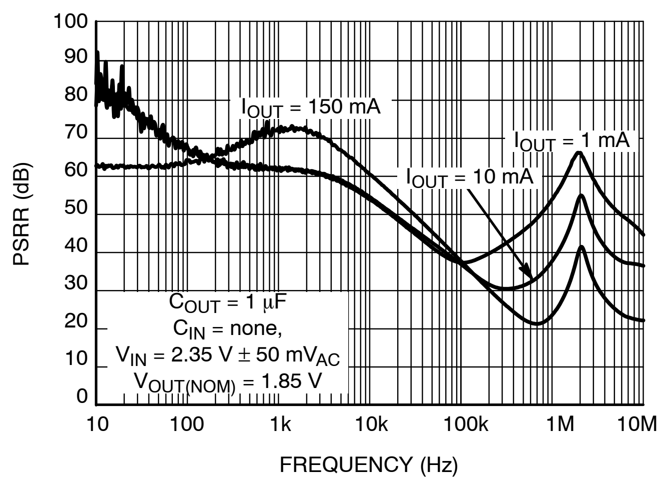


Figure 44. PSRR vs. Frequency V_{OUT} = 1.85 V

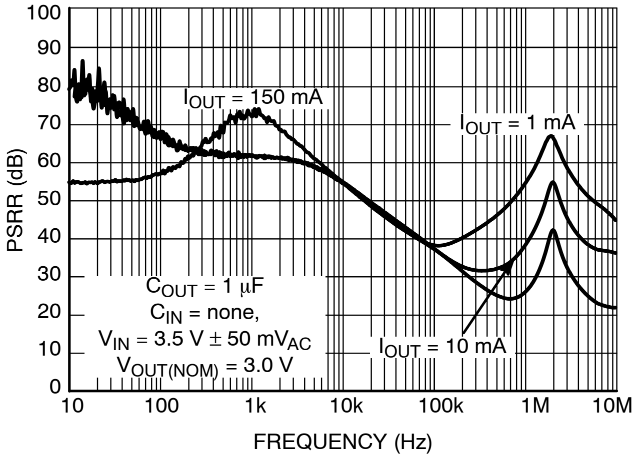


Figure 45. PSRR vs. Frequency
V_{OUT} = 3.0 V

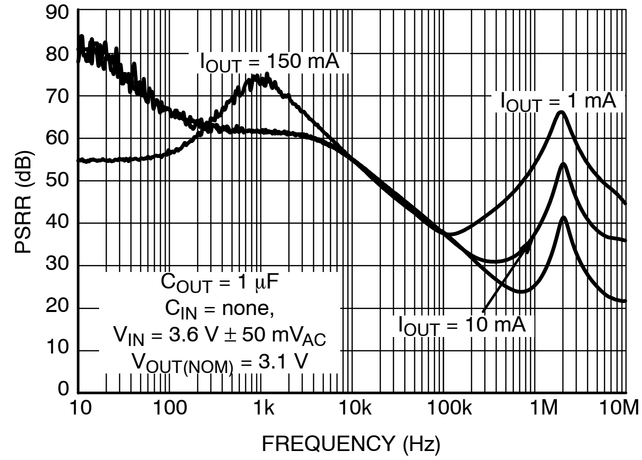


Figure 46. PSRR vs. Frequency
V_{OUT} = 3.1 V

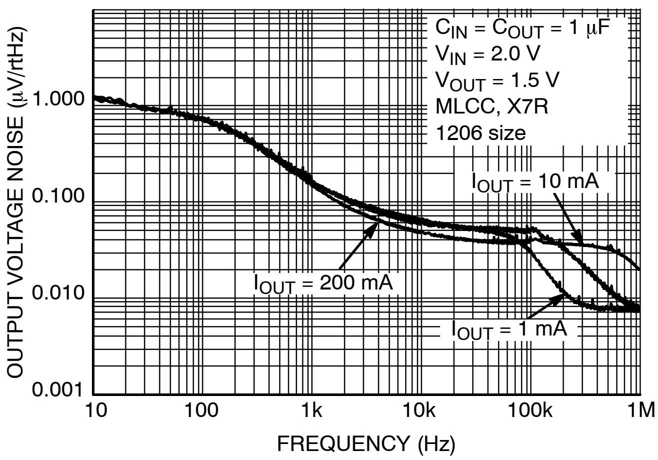


Figure 47. Output Noise Density vs. Frequency
V_{OUT} = 1.5 V

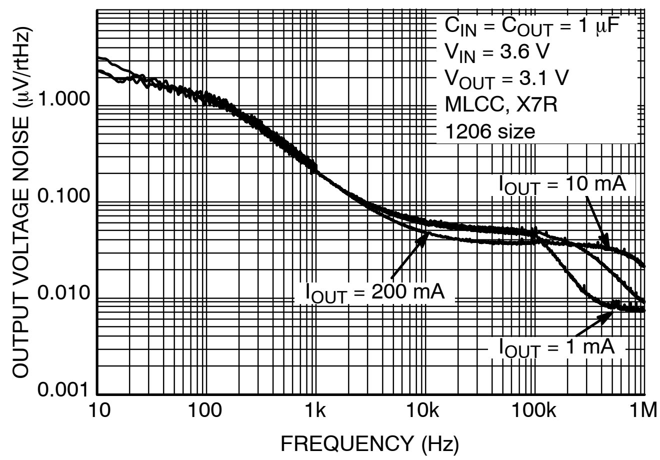


Figure 48. Output Noise Density vs. Frequency
V_{OUT} = 3.1 V

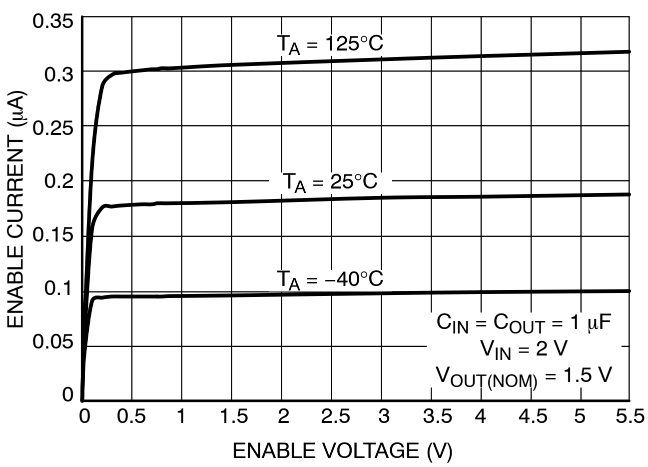


Figure 49. Enable Input Current vs. Enable Voltage

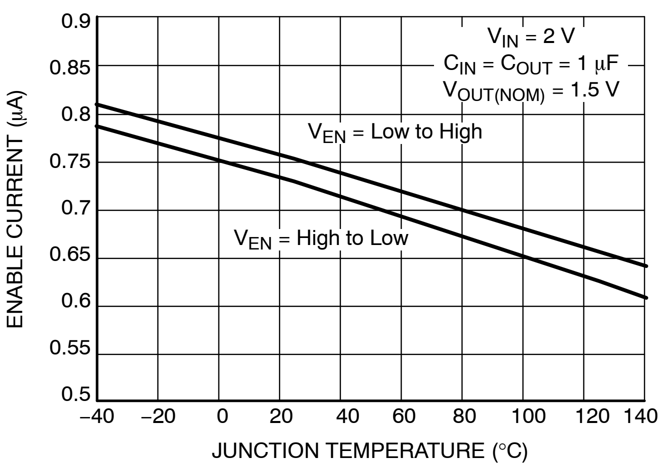


Figure 50. Enable Threshold Voltage vs. Temperature

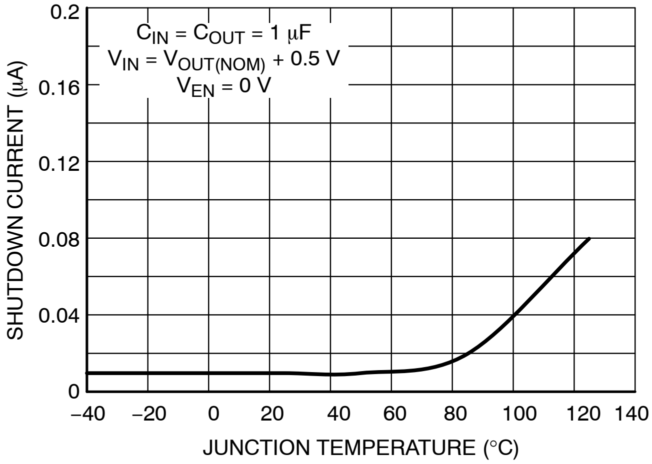


Figure 51. Shutdown Current vs. Temperature

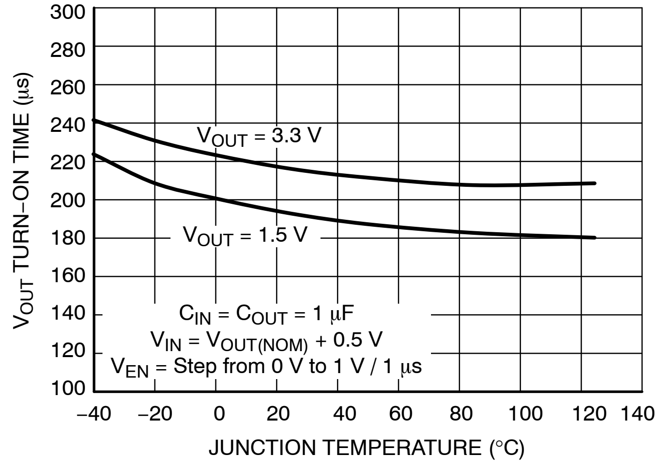


Figure 52. V_{OUT} Turn−on Time vs. Temperature

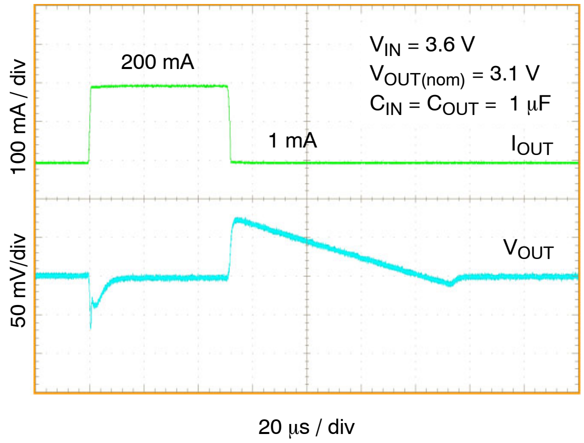


Figure 53. Load Transient Response
I_{OUT} = 1 mA to 200 mA, C_{OUT} = 1 µF

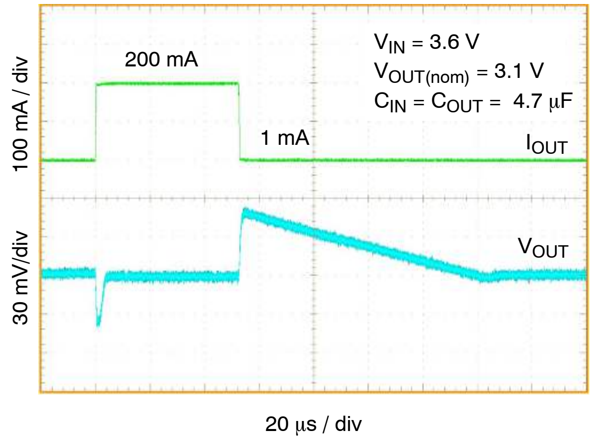


Figure 54. Load Transient Response
I_{OUT} = 1 mA to 200 mA, C_{OUT} = 4.7 µF

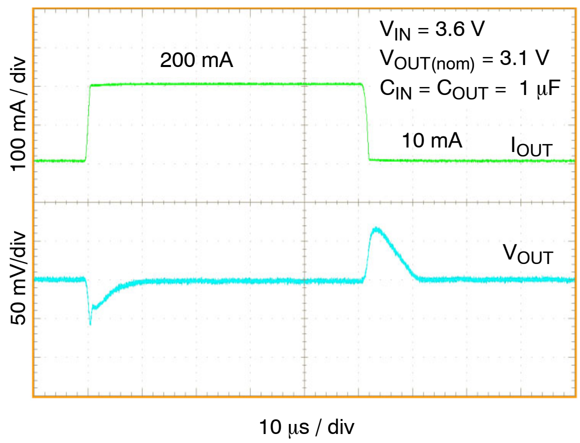


Figure 55. Load Transient Response
I_{OUT} = 10 mA to 200 mA, C_{OUT} = 1 µF

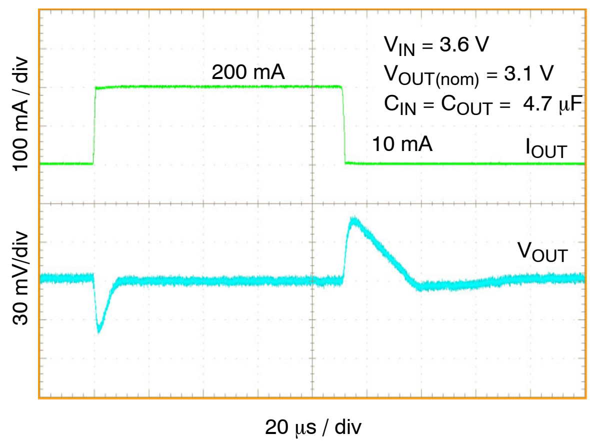


Figure 56. Load Transient Response
I_{OUT} = 10 mA to 200 mA, C_{OUT} = 4.7 µF

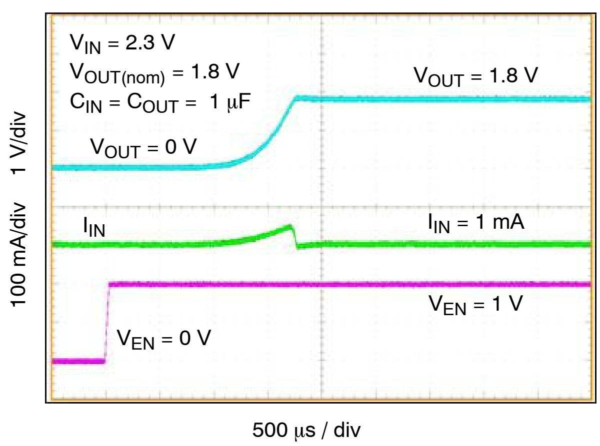


Figure 57. Enable Turn−On Response
V_{OUT} = 1.8 V, C_{OUT} = 1 µF

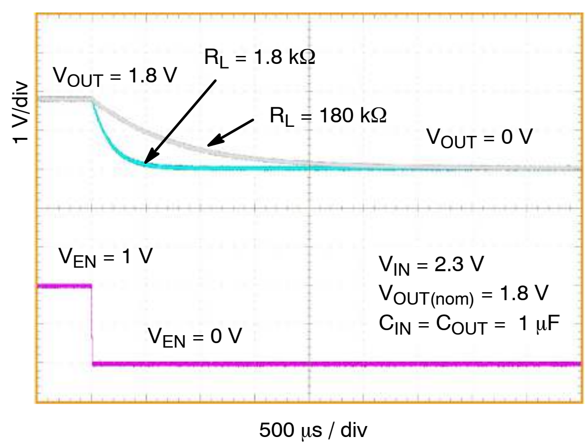


Figure 58. Enable Turn−Off Response
V_{OUT} = 1.8 V, C_{OUT} = 1 µF (A Version)

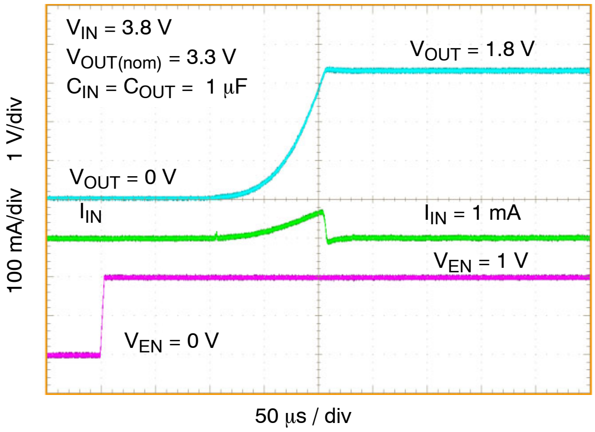


Figure 59. Enable Turn−On Response V_{OUT} = 3.3 V, C_{OUT} = 1 µF

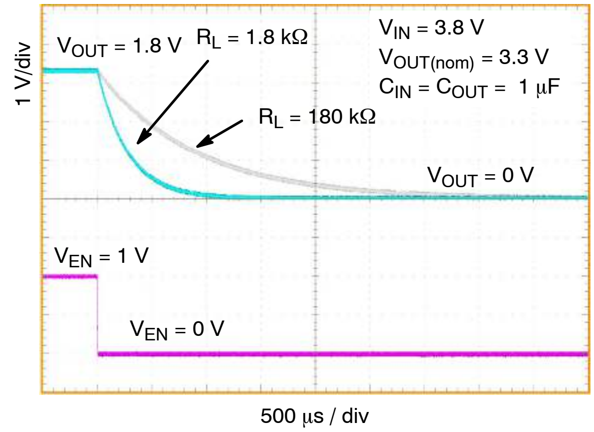


Figure 60. Enable Turn−Off Response V_{OUT} = 3.3 V, C_{OUT} = 1 µF (A Version)

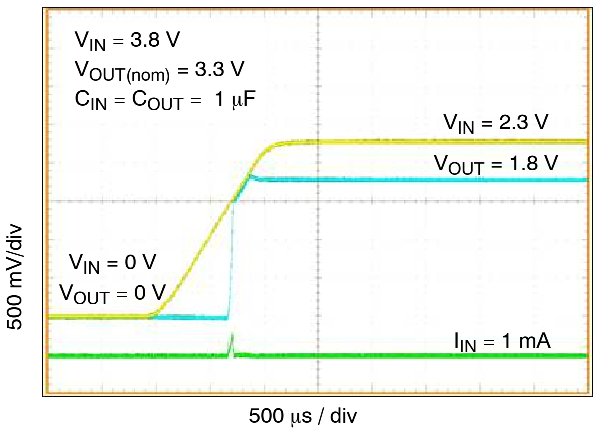


Figure 61. Enable Turn−On Response V_{OUT} = 1.8 V, C_{OUT} = 1 µF

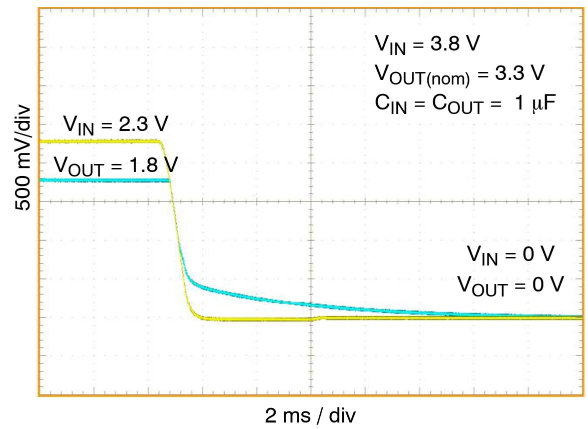


Figure 62. Enable Turn−Off Response V_{OUT} = 1.8 V, C_{OUT} = 1 µF (A Version)

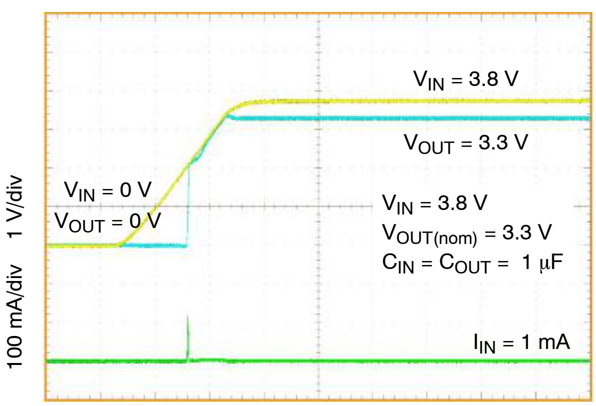


Figure 63. Enable Turn−On Response V_{OUT} = 3.3 V, C_{OUT} = 1 µF

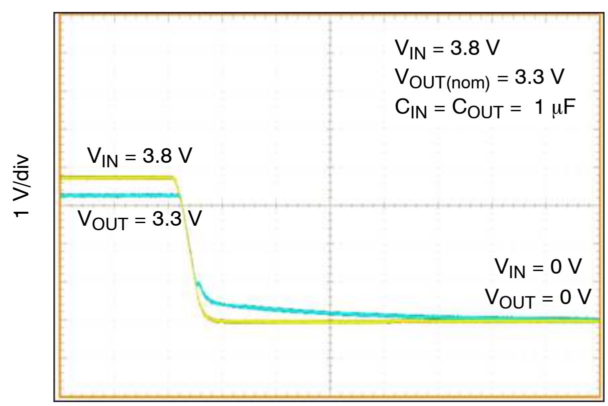


Figure 64. Enable Turn−Off Response V_{OUT} = 3.3 V, C_{OUT} = 1 µF (A Version)

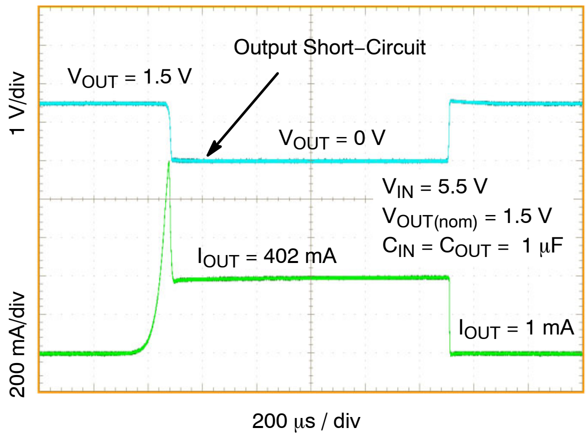


Figure 65. Short−Circuit Response V_{OUT} = 1.5 V, C_{OUT} = 1 μF

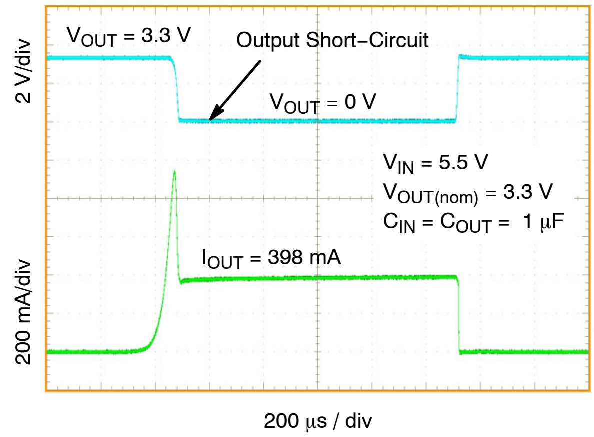


Figure 66. Short−Circuit Response V_{OUT} = 1.5 V, C_{OUT} = 1 μF

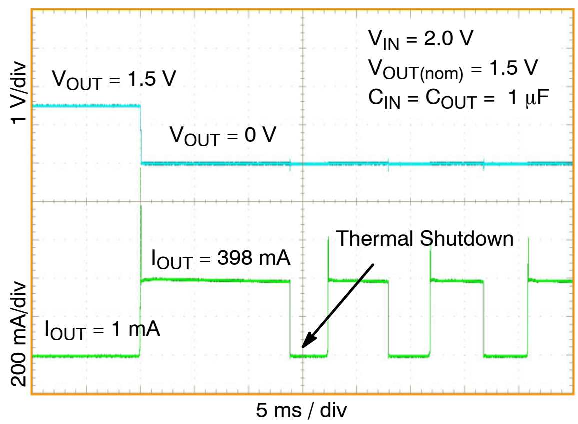


Figure 67. Short−Circuit Response V_{OUT} = 1.5 V, C_{OUT} = 1 μF

APPLICATIONS INFORMATION

The NCP707 is a high performance, small package size, 200 mA LDO voltage regulator. This device delivers very good noise and dynamic performance. Thanks to its adaptive ground current feature the device consumes only 25 μA of quiescent current at no−load condition. The regulator features very*low noise of 22 μVRMS, PSRR of typ. 70dB at 1kHz and very good load/line transient response. The device is an ideal choice for space constrained portable applications.

A logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typ. 10 nA from the IN pin.

The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

Input Capacitor Selection (C_{IN})

It is recommended to connect a minimum of 1 μF Ceramic X5R or X7R capacitor close to the IN pin of the device. Larger input capacitors may be necessary if fast and large load transients are encountered in the application. There is no requirement for the min./max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL.

Output Capacitor Selection (C_{OUT})

The NCP707 is designed to be stable with small 1.0 μF and larger ceramic capacitors on the output. The minimum effective output capacitance for which the LDO remains stable is 100 nF. The safety margin is provided to account for capacitance variations due to DC bias voltage, temperature, initial tolerance. There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 700 mΩ.

Larger output capacitors could be used to improve the load transient response or high frequency PSRR characteristics. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature. The tantalum capacitors are generally more costly than ceramic capacitors.

No−load Operation

The regulator remains stable and regulates the output voltage properly within the ±2% tolerance limits even with no external load applied to the output.

Enable Operation

The NCP707 uses the EN pin to enable/disable its output and to control the active discharge function. If the EN pin voltage is < 0.4 V the device is guaranteed to be disabled. The pass transistor is turned − off so that there is virtually no current flow between the IN and OUT. In case of the option equipped with active discharge − the active discharge transistor is turned−on and the output voltage V_{OUT} is pulled to GND through a 1.2 kΩ resistor for A options or 120 Ω resistor for C options. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}. If the EN pin voltage > 0.9 V the device is guaranteed to be enabled. The NCP707 regulates the output voltage and the active discharge transistor is turned − off. The EN pin has an internal pull−down current source with typ. value of 180 nA which assures that the device is turned−off when the EN pin is not connected. A build in 56 mV of hysteresis and deglitch time in the EN block prevents from periodic on/off oscillations that can occur due to noise on EN line. In the case that the EN function isn't required the EN pin should be tied directly to IN.

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases where the extended reverse current condition is anticipated the device may require additional external protection.

Output Current Limit

Output Current is internally limited within the IC to a typical 379 mA. The NCP707 will source this amount of current measured with the output voltage 100 mV lower than the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 390 mA (typ). The current limit and short circuit protection will work properly up to V_{IN} =5.5 V at T_A = 25°C. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (TSD − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (TSDU − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCP707 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. The maximum power dissipation the NCP707 can handle is given by:

$$P_{D(MAX)} = \frac{\left[125 - T_A\right]}{\theta_{JA}} \quad \text{(eq. 1)}$$

For reliable operation junction temperature should be limited to +125°C.

The power dissipated by the NCP707 for given application conditions can be calculated as follows:

$$P_{D(MAX)} = V_{IN} I_{GND} + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

Figure 68 shows the typical values of θ_{JA} vs. heat spreading area.

Load Regulation

The NCP707 features very good load regulation of typical 2 mV in the 0 mA to 200 mA range. In order to achieve this very good load regulation a special attention to PCB design is necessary. The trace resistance from the OUT pin to the point of load can easily approach 100 mΩ which will cause a 20 mV voltage drop at full load current, deteriorating the excellent load regulation.

Line Regulation

The IC features very good line regulation of 0.4 mV/V measured from $V_{IN} = V_{OUT} + 0.5$ V to 5.5 V.

Power Supply Rejection Ratio

At low frequencies the PSRR is mainly determined by the feedback open−loop gain. At higher frequencies in the range 100 kHz – 10 MHz it can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

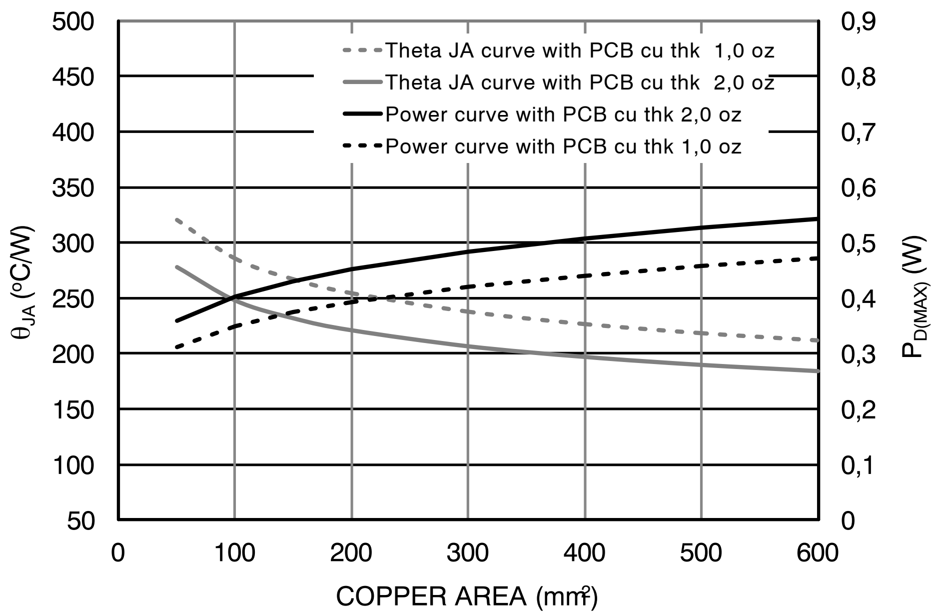


Figure 68. Thermal Parameters vs. Copper Area

Output Noise

The IC is designed for very−low output voltage noise. The typical noise performance of 22 μV_{RMS} makes the device suitable for noise sensitive applications.

Internal Soft Start

The Internal Soft−Start circuitry will limit the inrush current during the LDO turn−on phase. Please refer to typical characteristics section for typical inrush current values. The soft−start function prevents from any output voltage overshoots and assures monotonic ramp−up of the output voltage.

PCB Layout Recommendations

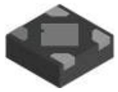
To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated by the formula given in Equation 2.

ORDERING INFORMATION

Device	Voltage Option	Marking	Marking Rotation	Option	Package	Shipping†
NCP707AMX150TCG	1.5 V	A	0°	With active output discharge function (R_{DIS} = 1.2 kΩ)	XDFN4 (Pb-Free)	3000 or 5000 / Tape & Reel (Note 6)
NCP707AMX180TCG	1.8 V	D	0°			
NCP707AMX185TCG	1.85 V	E	0°			
NCP707AMX250TCG	2.5 V	K	180°			
NCP707AMX280TCG	2.8 V	F	0°			
NCP707AMX285TCG	2.85 V	J	0°			
NCP707AMX300TCG	3.0 V	K	0°			
NCP707AMX310TCG	3.1 V	L	0°			
NCP707AMX330TCG	3.3 V	P	0°			
NCP707BMX150TCG	1.5 V	A	90°	Without active output discharge function		
NCP707BMX180TCG	1.8 V	D	90°			
NCP707BMX185TCG	1.85 V	E	90°			
NCP707BMX250TCG	2.5 V	K	270°			
NCP707BMX280TCG	2.8 V	F	90°			
NCP707BMX285TCG	2.85 V	J	90°			
NCP707BMX300TCG	3.0 V	K	90°			
NCP707BMX310TCG	3.1 V	L	90°			
NCP707BMX330TCG	3.3 V	P	90°			
NCP707CMX150TCG	1.5 V	L	180°	With active output discharge function (R_{DIS} = 120 Ω)		
NCP707CMX180TBG	1.8 V	P	180°			
NCP707CMX180TCG	1.8 V	P	180°			
NCP707CMX185TCG	1.85 V	Q	180°			
NCP707CMX250TCG	2.5 V	V	180°			
NCP707CMX280TCG	2.8 V	Y	180°			
NCP707CMX285TCG	2.85 V	2	180°			
NCP707CMX300TBG (Note 6)	3.0 V	3	180°			
NCP707CMX300TCG (Note 6)	3.0 V	3	180°			
NCP707CMX310TCG	3.1 V	4	180°			
NCP707CMX320TCG	3.2 V	5	180°			
NCP707CMX330TBG	3.3 V	6	180°			
NCP707CMX330TCG	3.3 V	6	180°			

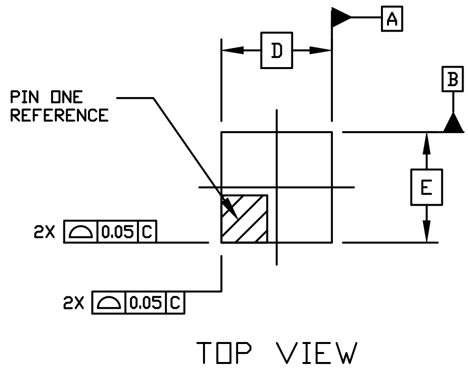
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

6. Products processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel.



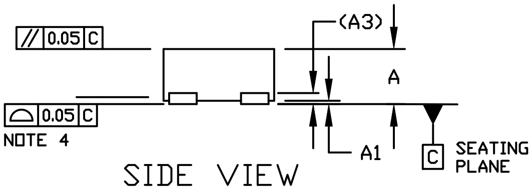
XDFN4 1.0x1.0, 0.65P
CASE 711AJ
ISSUE C

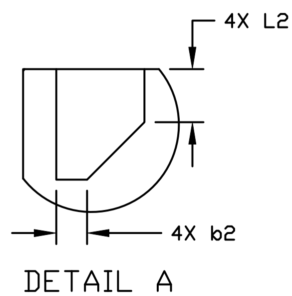
DATE 08 MAR 2022



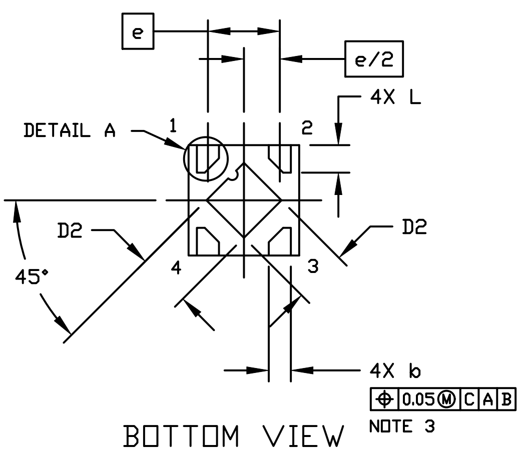
NOTES:

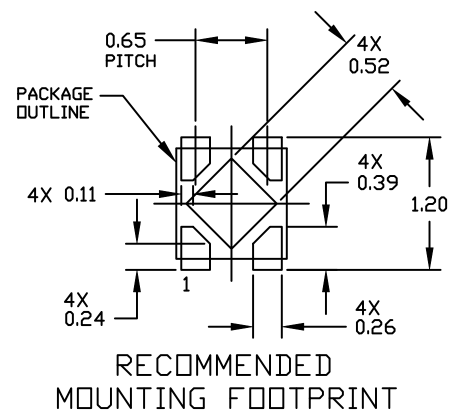
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.20 FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.





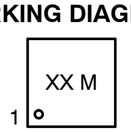
DIM	MILLIMETERS MIN	NOM	MAX
A	0.33	0.38	0.43
A1	0.00	---	0.05
A3	0.10 REF		
b	0.15	0.20	0.25
b2	0.02	0.07	0.12
D	0.90	1.00	1.10
D2	0.43	0.48	0.53
E	0.90	1.00	1.10
e	0.65 BSC		
L	0.20		0.30
L2	0.07		0.17





* FOR ADDITIONAL INFORMATION ON OUR Pb-FRE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNT TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON67179E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**XDFN4, 1.0X1.0, 0.65P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

◊