MP2236

18V, 6A, High-Efficiency, Synchronous Step-Down Converter

DESCRIPTION

The MP2236 is a high-frequency, synchronous, rectified, step-down switch-mode converter. The MP2236 offers a fully integrated solution that achieves 6A of continuous output current with excellent load and line regulation over a wide input supply range.

Constant-on-time (COT) control operation provides fast transient response. Full protection features include hiccup over-current protection (OCP) and thermal shutdown.

The MP2236 requires a minimal number of readily available, standard external components and is available in a space-saving TSOT23-8 package.

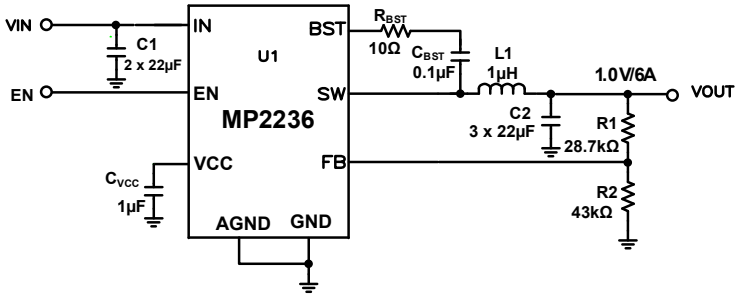
FEATURES

- Wide 3V to 18V Operating Input Range
- 6A Continuous Output Current
- 25mΩ/12mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Default 600mV Reference Voltage
- Adjustable Output Voltage
- 600kHz Switching Frequency
- t_{ON} Extension
- Hiccup Over-Current Protection (OCP)
- Thermal Shutdown Protection
- Available in TSOT23-8 Package

APPLICATIONS

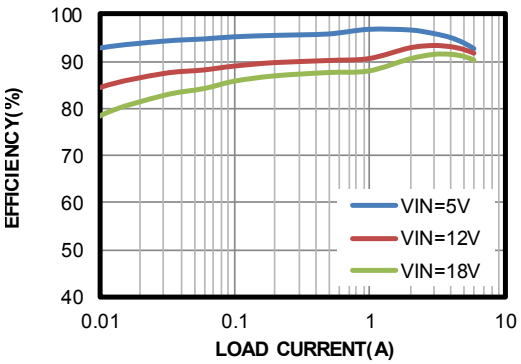
- Flat-Panel Television and Monitors
- Digital TV Power Supplies
- Digital Set-Top Boxes
- Distributed Power Systems

TYPICAL APPLICATION



Efficiency

V_{OUT} = 3.3V, L = 2.2µH, DCR = 11.4mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2236GJ	TSOT23-8	*See Below*

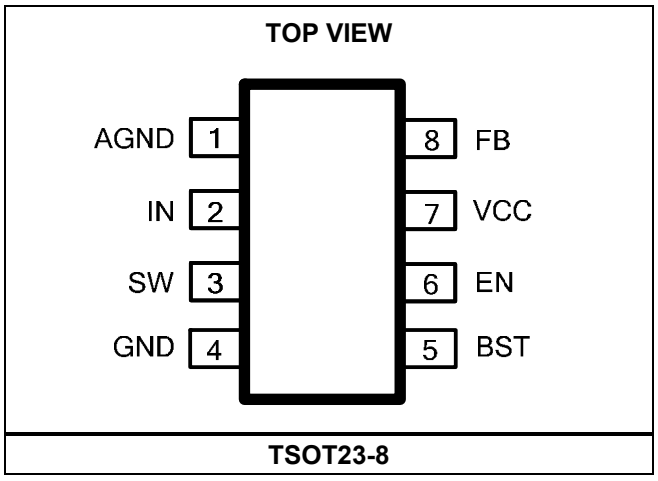
For Tape & Reel, add suffix -Z (e.g. MP2236GJ-Z).

TOP MARKING

|AUAY

AUA: Product code of MP2236GJ
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	AGND	**Analog ground.** Connect AGND to GND using a short and wide PCB trace.
2	IN	**Supply voltage.** The MP2236 operates from a 3V to 18V input rail. Use a ceramic capacitor to decouple the input rail. Connect IN using a wide PCB trace.
3	SW	**Switch output.** Connect SW using a wide PCB trace.
4	GND	**System power ground.** GND is the reference ground of the regulated output voltage and requires special consideration during the PCB layout. Connect GND to the ground plane with copper traces and vias.
5	BST	**Bootstrap.** Connect a 0.1µF capacitor between SW and BST to form a floating supply across the high-side switch driver.
6	EN	**Enable.** Drive EN high to enable the MP2236. EN has a 2MΩ pull-down resistor to GND.
7	VCC	**Internal bias supply.** Decouple VCC with a 1µF capacitor. The VCC capacitor should be placed close to VCC and GND.
8	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 20V
V_{SW} ..... -0.3V (-6.5V for <10ns) to V_{IN} + 0.7V (25V for <25ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} 20V
All other pins ..... -0.3V to 4V
Continuous power dissipation (T_A = 25°C) (2) (5)
TSOT23-8 ..... 1.89W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3V to 18V
Output voltage (V_{OUT}) ..... 0.6V to 8V or V_{IN} x D_{MAX} (4)
Operating junction temp (T_J) ..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
TSOT23-8			
EV2236-J-00A (5)	66	23	°C/W
JESD51-7 (6)	100	55	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) For more information of Dmax, please refer to the Low Dropout Operation section on page 13.
5) Measured on EV2236-J-00A, 4-layer PCB, 63.5mmx63.5mm.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to 125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V, T_J = 25°C			1	μA
Supply current (quiescent)	I_Q	V_{FB} = 0.63V, PFM mode		150	210	μA
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 3.3V		25		mΩ
LS switch on resistance	$LS_{RDS(ON)}$			12		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V, T_J = 25°C			1	μA
Low-side valley current limit	I_{LIMIT_L}		6	7.5		A
Low-side ZCD threshold	I_{ZCD}			50		mA
Switching frequency	f_{SW1}	V_{IN} = 12V, V_{OUT} = 3.3V	480	600	720	kHz
Minimum off time [8]	t_{OFF_MIN}			170		ns
Minimum on time [8]	t_{ON_MIN}			70		ns
Reference voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	mV
FB current	I_{FB}	V_{FB} = 0.63V		10	50	nA
EN rising threshold	V_{EN_RISING}		1.12	1.2	1.28	V
EN hysteresis	V_{EN_HYS}			200		mV
EN to GND pull-down resistor	R_{EN}	V_{EN} = 2V		2		MΩ
V_{IN} under-voltage lockout threshold-rising	$INUV_{Vth}$		2.7	2.8	2.95	V
V_{IN} under-voltage lockout threshold-hysteresis	$INUV_{HYS}$			300		mV
VCC regulator	V_{CC}	I_{CC} = 5mA		3.5		V
UVP1 threshold [8]	UV_{TH1}	Hiccup entry		80%		V_{REF}
Soft-start time	t_{SS}	T_J = 25°C, V_{OUT} from 10% to 90%	0.5	1	1.5	ms
Thermal shutdown [8]	T_{TSD}			150		°C
Thermal hysteresis [8]	T_{TSD_HYS}			20		°C

Notes:

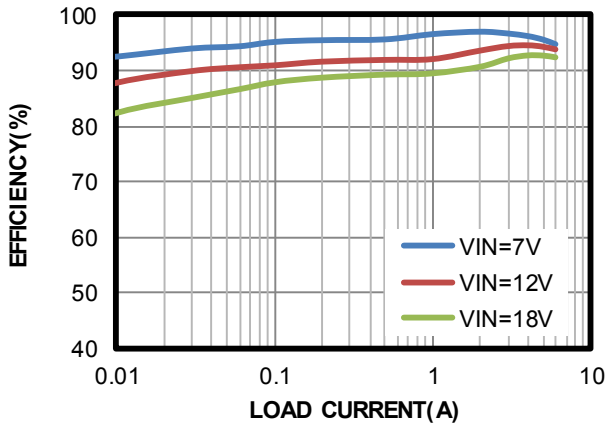
7) Not tested in production. Guaranteed by over-temperature correlation.
8) Derived by sample characterization. Not tested in production

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, T_A = 25°C, unless otherwise noted.

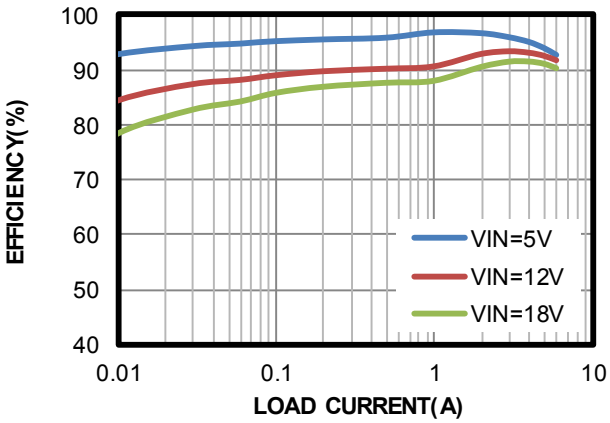
Efficiency

V_{OUT} = 5V, L = 3.3µH, DCR = 9mΩ



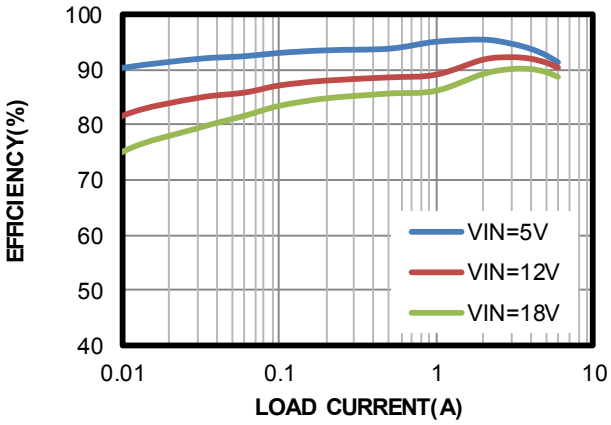
Efficiency

V_{OUT} = 3.3V, L = 2.2µH, DCR = 11.4mΩ



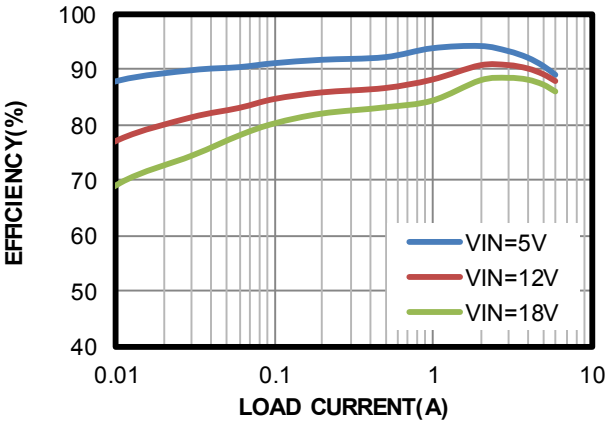
Efficiency

V_{OUT} = 2.5V, L = 1.5µH, DCR = 4.3mΩ



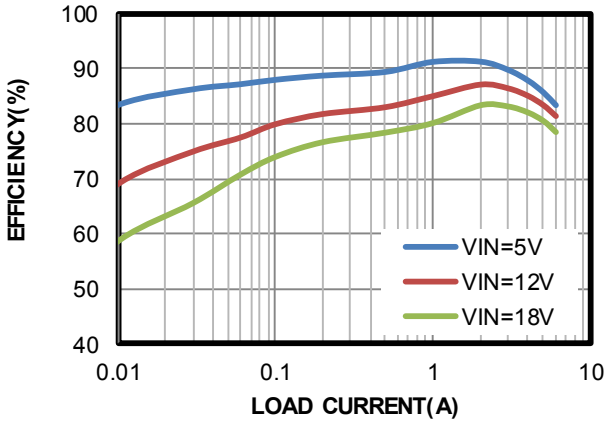
Efficiency

V_{OUT} = 1.8V, L = 1.5µH, DCR = 4.3mΩ



Efficiency

V_{OUT} = 1V, L = 1µH, DCR = 4.6mΩ

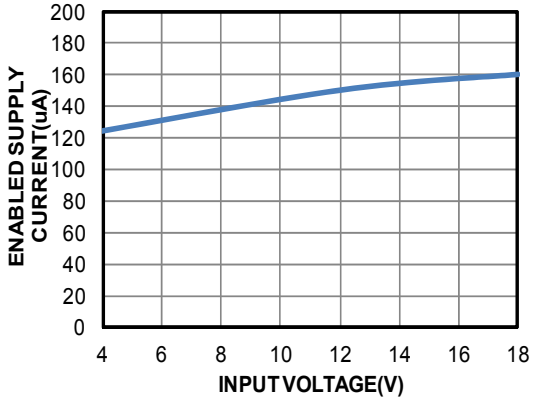


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, T_A = 25°C, unless otherwise noted.

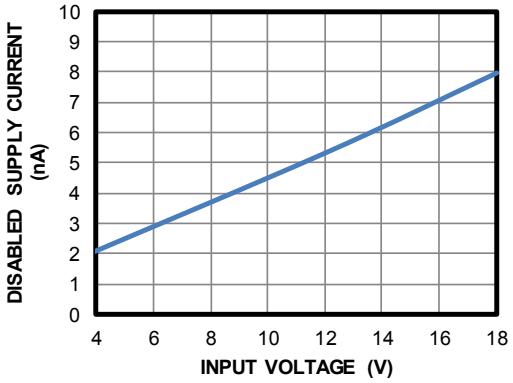
Enabled Supply Current vs. Input Voltage

V_{EN} = 2V, V_{FB} = 0.63V



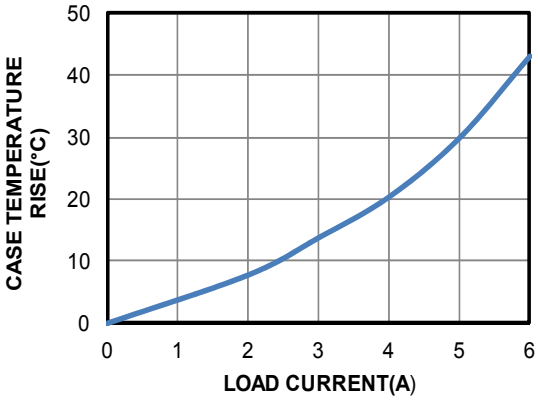
Disabled Supply Current vs. Input Voltage

V_{EN} = 0V



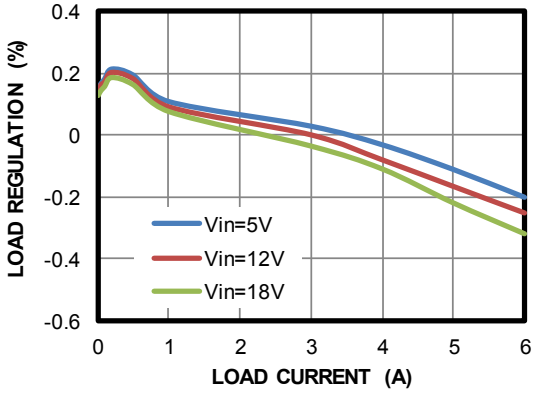
Case Temperature Rise vs. Load Current

V_{OUT} = 3.3V, 4-layer PCB, 63.5mmx63.5mm



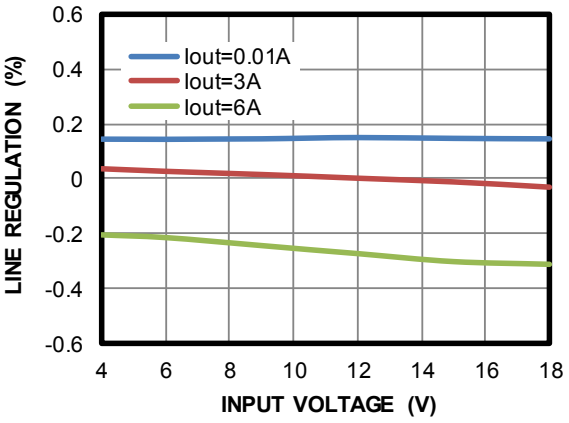
Load Regulation

I_{OUT} = 0.01A to 6A

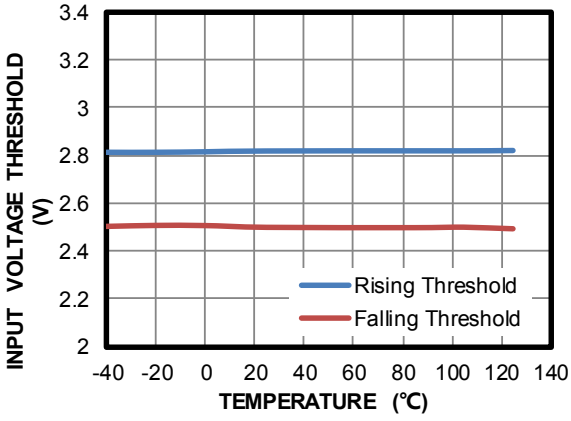


Line Regulation

V_{IN} = 4V to 18V



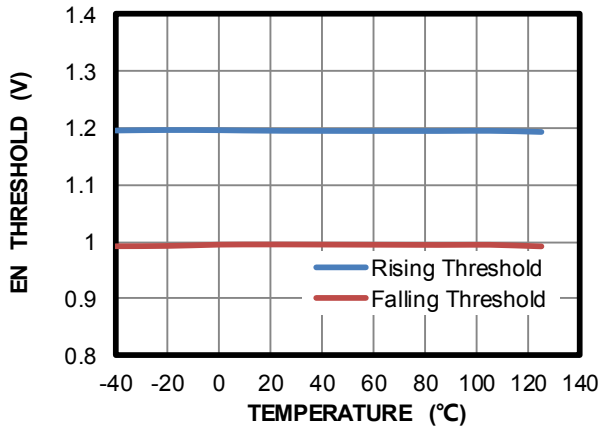
Input Voltage Threshold vs. Temperature



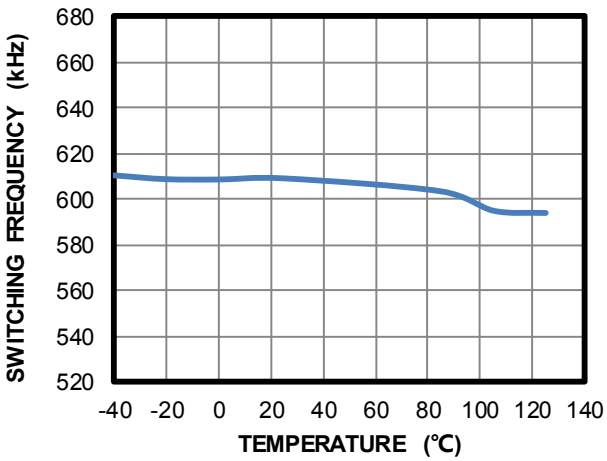
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, T_A = 25°C, unless otherwise noted.

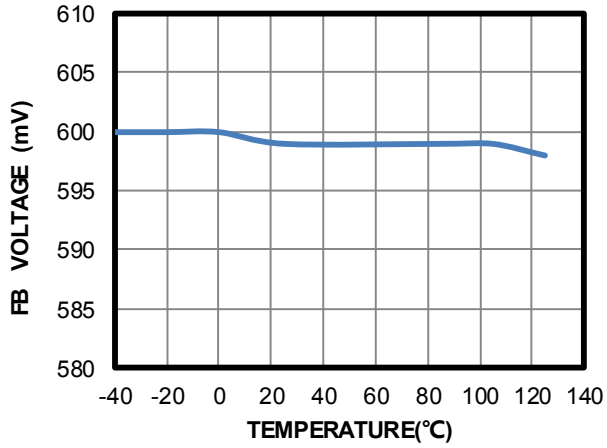
EN Threshold vs. Temperature



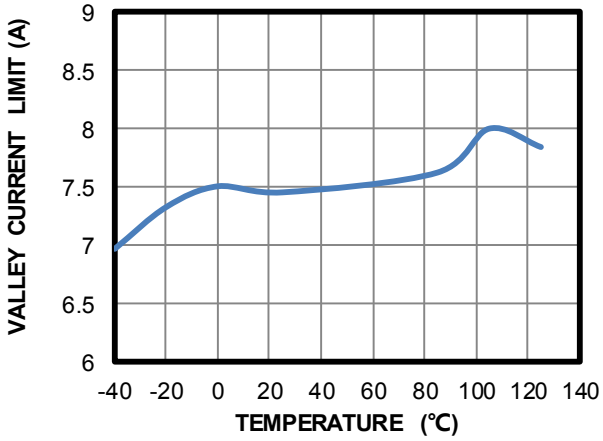
Switching Frequency vs. Temperature



FB Voltage vs. Temperature



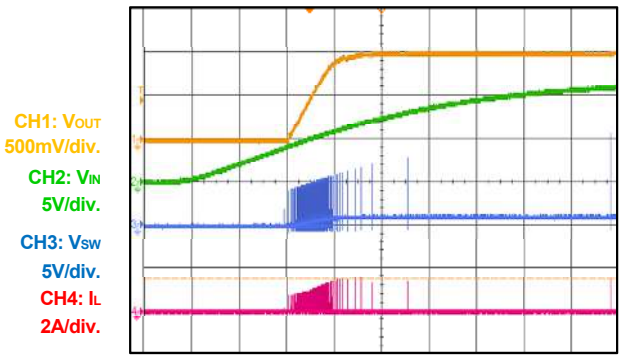
Valley Current Limit vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

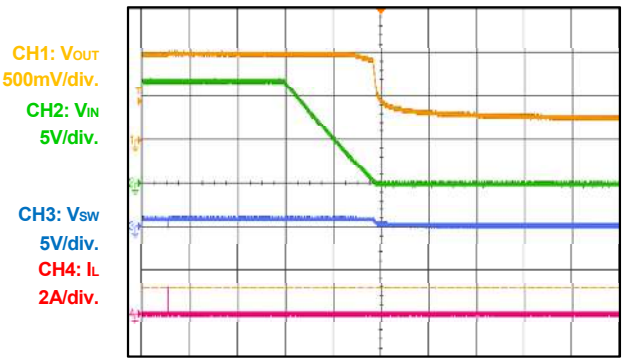
Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1V, T_A = 25°C, unless otherwise noted.

Start-Up through Input Voltage
I_{OUT} = 0A



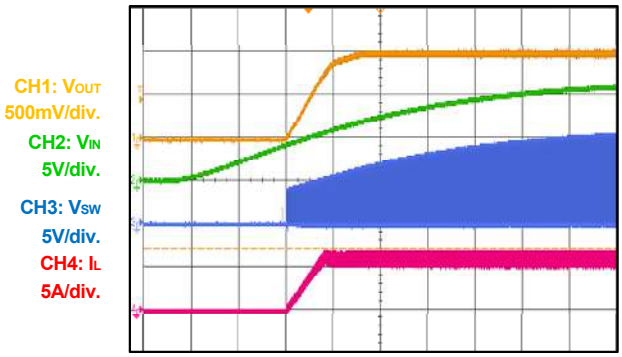
1ms/div.

Shutdown through Input Voltage
I_{OUT} = 0A



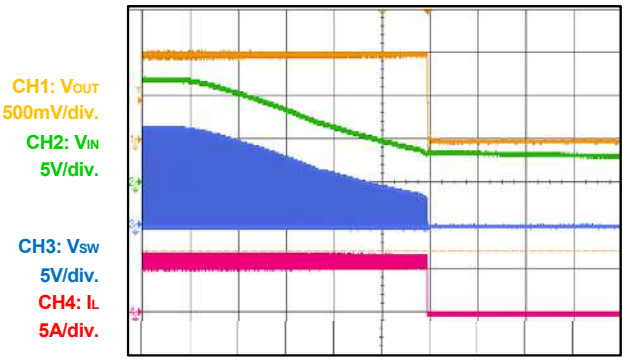
50ms/div.

Start-Up through Input Voltage
I_{OUT} = 6A



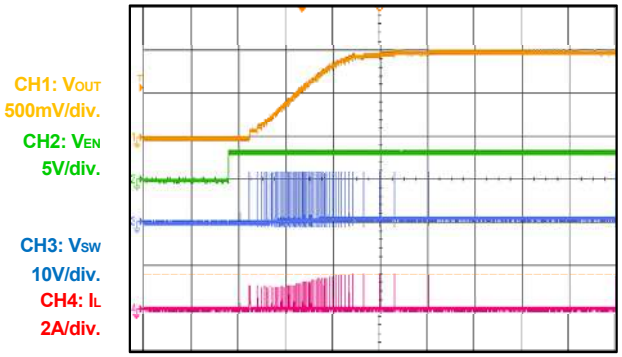
1ms/div.

Shutdown through Input Voltage
I_{OUT} = 6A



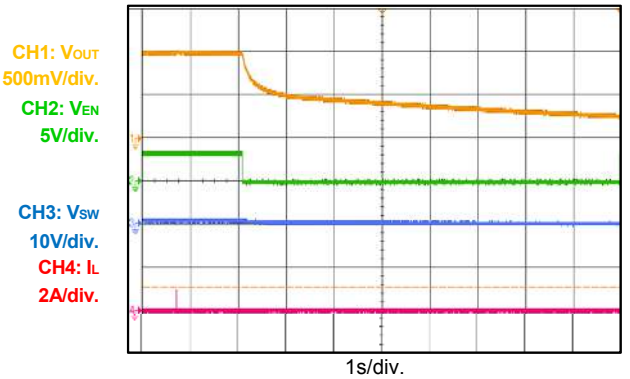
1ms/div.

Start-Up through Enable
I_{OUT} = 0A



500µs/div.

Shutdown through Enable
I_{OUT} = 0A



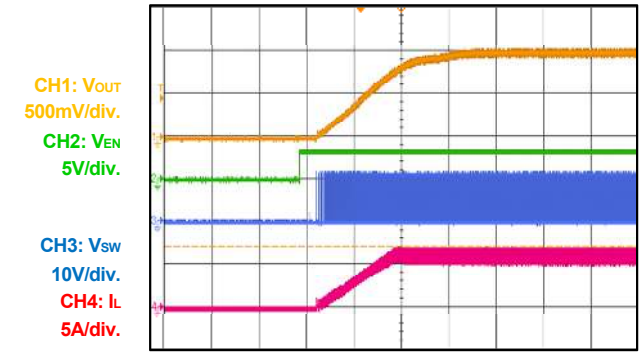
1s/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1V, T_A = 25°C, unless otherwise noted.

Start-Up through Enable

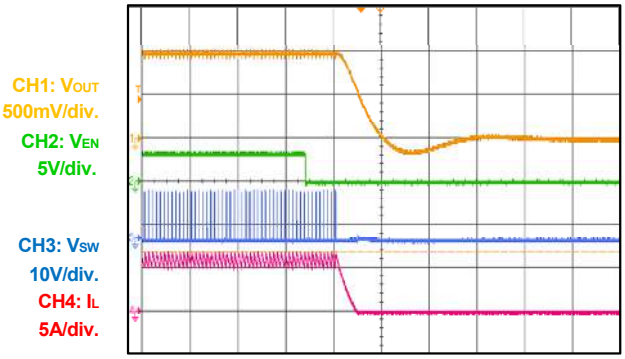
I_{OUT} = 6A



500µs/div.

Shutdown through Enable

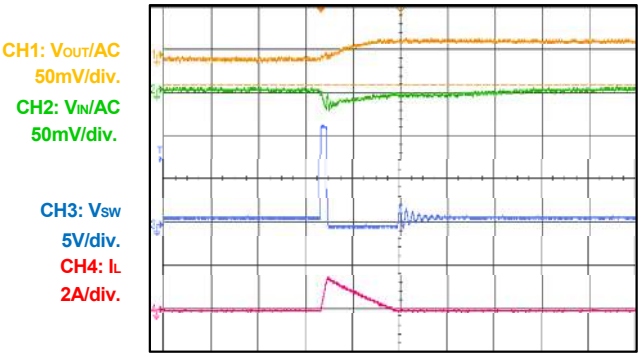
I_{OUT} = 6A



20µs/div.

Input / Output Ripple

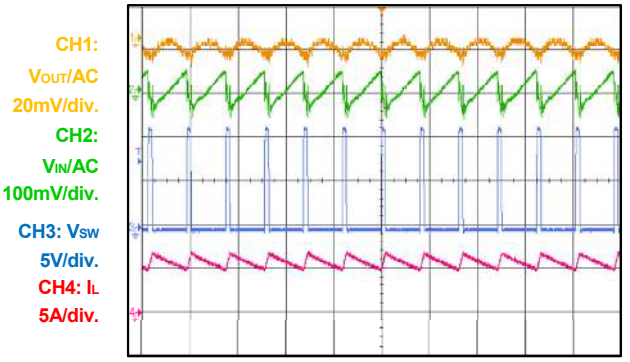
I_{OUT} = 0A



1µs/div.

Input / Output Ripple

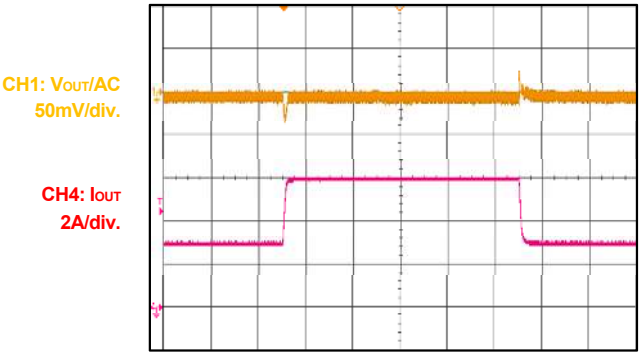
I_{OUT} = 6A



2µs/div.

Transient Response

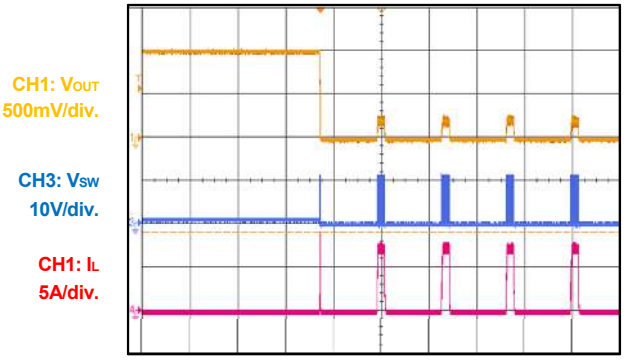
I_{OUT} = 3 - 6A, slew rate = 2.5A/µs by E-load



100µs/div.

Short-Circuit Entry

I_{OUT} = 0A



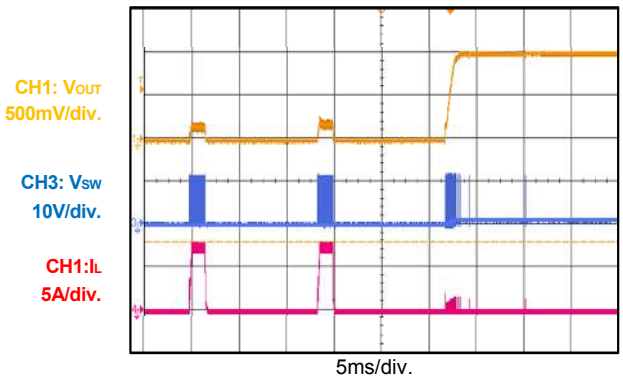
10ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1V, T_A = 25°C, unless otherwise noted.

Short-Circuit Recovery

I_{OUT} = 0A



FUNCTIONAL BLOCK DIAGRAM

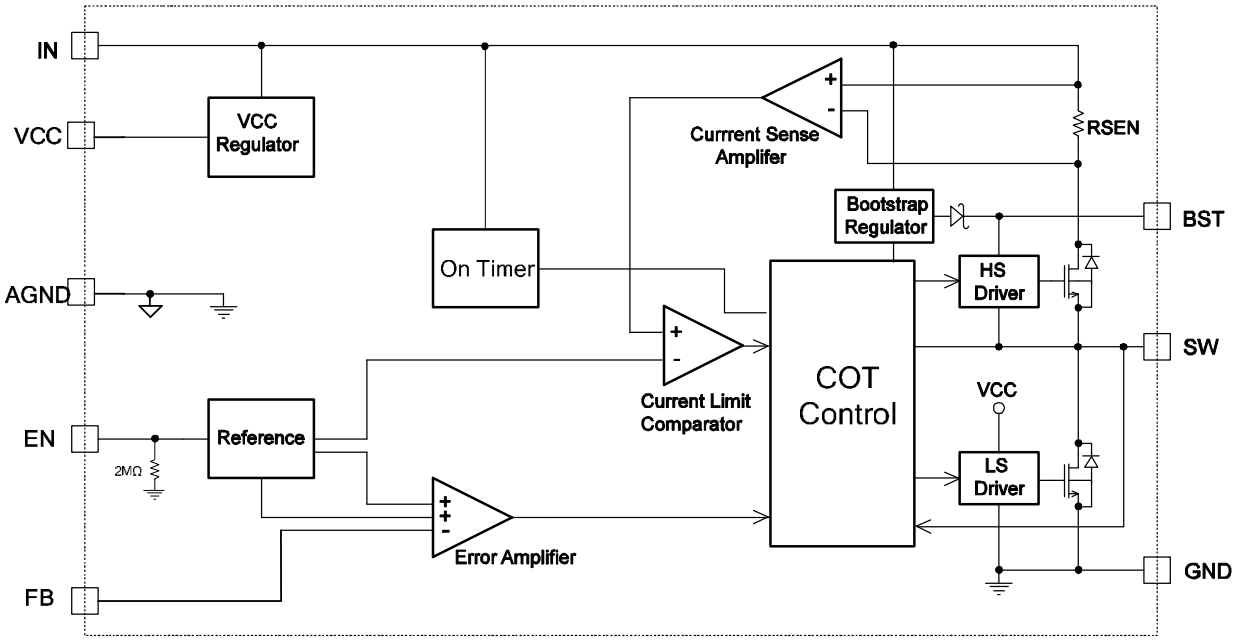


Figure 1: Functional Block Diagram

OPERATION

Pulse-Width Modulation (PWM) Operation

The MP2236 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. The device uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. Figure 2 shows the simplified ramp compensation block in the MP2236. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage (V_{RAMP}) is lower than the error amplifier output voltage (V_{EAO}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET turns off. By cycling the HS-FET between the on and off states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss.

Shoot-through occurs when the HS-FET and LS-FET are turned on at the same time, causing a dead short between the input and GND. Shoot-through reduces efficiency dramatically, so the MP2236 avoids this by generating a dead time (DT) internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period. The MP2236 enters either heavy-load operation or light-load operation depending on the amplitude of the output current.

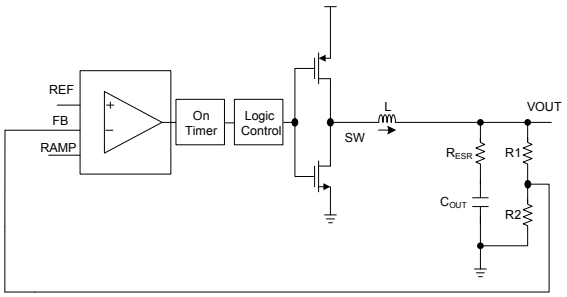


Figure 2: Simplified Compensation Block

Light-Load Operation

When the MP2236 works in pulse-frequency modulation (PFM) mode during light-load operation, the MP2236 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the LS-FET driver enters tri-state (Hi-Z). The output capacitors discharge slowly to GND through the LS-FET and the resistors R1 and R2. This operation improves device efficiency greatly when the output current is low (see Figure 3).

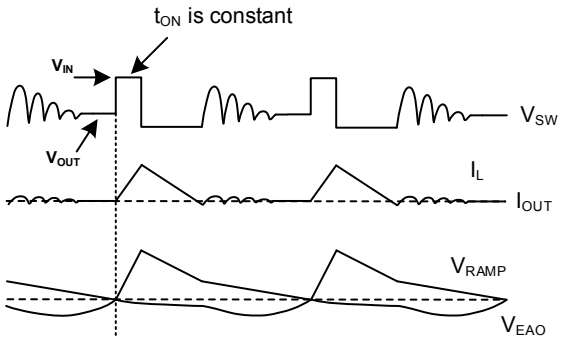


Figure 3: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does during heavy-load conditions. The HS-FET turn-on frequency is a function of the output current. As the output current increases, the current modulation regulation time period becomes shorter, the HS-FET turns on more frequently, and the switching frequency increases in turn. The output current reaches critical levels when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device reverts to pulse-width modulation (PWM) mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Error Amplifier (EA)

The error amplifier compares the FB voltage (V_{FB}) against the internal 0.6V reference voltage (V_{REF}) and outputs a PWM signal. The optimized internal ramp compensation minimizes the external component count and simplifies the control loop design.

Enable (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 2MΩ resistor is connected from EN to ground. EN can operate with a 20V input voltage, which allows EN to be connected to V_{IN} directly for automatic start-up.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating with an insufficient supply voltage. The MP2236 UVLO comparator monitors the input voltage. The MP2236 is active when the input voltage exceeds the UVLO rising threshold.

Soft Start and Pre-Biased Start-Up

Soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to the internal VCC. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, REF takes over.

The soft-start time is set to 1ms internally. If the output of the MP2236 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at FB or V_{OUT}.

Low-Dropout Operation

To improve dropout, the MP2236 is designed to extend its on time when the duty cycle is over 85%. When the HS-FET on time extends, the frequency drops. The typical minimum frequency is 260kHz. When the frequency drops to 260kHz, it cannot reduce any further, and HS-FET off time begins decreasing. The duty cycle reaches the max duty cycle (D_{MAX}) when the off time is at its minimum value. If the input voltage drops, the MP2236 works at the max duty cycle, and the output voltage drops.

Calculate the typical D_{MAX} with Equation (2):

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{SW\_MIN} \quad (2)$$

Where t_{OFF_MIN} = 170ns, and f_{SW_MIN} = 260kHz.

Over-Current Protection (OCP) and Hiccup

The MP2236 has a cycle-by-cycle, over-current limiting control. The current-limit circuit employs a low-side valley current-sensing algorithm. The MP2236 uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element for valley-current limiting. When the LS-FET turns on, the inductor current is monitored by the voltage between GND and SW. GND is used as the positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET. The PWM cannot initiate a new cycle before the inductor current falls to the valley threshold.

After the cycle-by-cycle over-current (OC) limit is reached, the output voltage drops until it is below the under-voltage (UV) threshold. There are two UV thresholds: UV1 (80%) and UV2 (60%). Once UV1 and OC are both triggered, the MP2236 waits for 30 cycles. If OC exits after 31 cycles, the MP2236 enters hiccup mode to restart the part periodically with a 12.5% duty cycle. If UV2 and OC are triggered, the MP2236 enters hiccup mode after three cycles. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP2236 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature drops below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 1.2V with a 150mV hysteresis. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1, and C2 (see Figure 4). If V_{IN} - V_{SW} exceeds 3.3V, U1 regulates M1 to maintain a 3.3V BST voltage across C4.

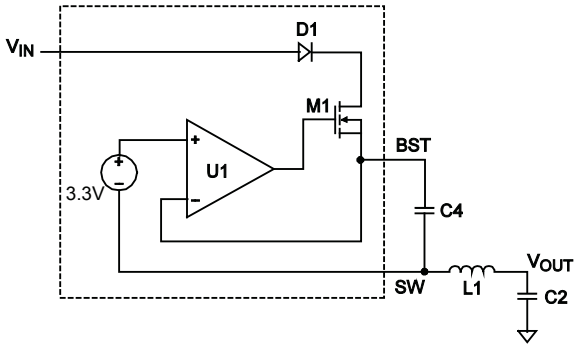


Figure 4: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The internal supply rail is then pulled down.

APPLICATION INFORMATION

Setting the Output Voltage

An external resistor divider can set the output voltage through FB. Calculate R1 and R2 with Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1} \quad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	28.7	43
1.8	86.6	43
2.5	100	31.6
3.3	100	22.1
5	100	13.7

Selecting the Inductor

For most applications, use a 0.47 - 10μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from Equation (4):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (4)$$

Where ΔI_L is the inductor ripple current.

Set the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (5):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (5)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use two 22μF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The traditional COT control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to act as an effective current-sense resistor. The MP2236 uses built-in internal ramp compensation to ensure that the system is stable even without the help of the output capacitor's ESR. The pure ceramic capacitor solution can reduce the output ripple, total BOM cost, and board area significantly.

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (9)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2236 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- V_{IN} is below 5V
- V_{OUT} is 3.3V
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, add an external BST diode from VCC to BST (see Figure 5).

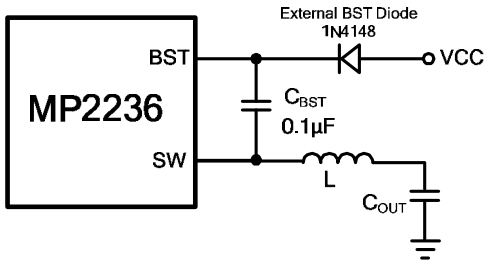


Figure 5: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is 1N4148, and the recommended BST capacitor value is 0.1µF.

Design Example

Table 2 shows a design example following the application guidelines for the specifications below.

Table 2: Design Example

V_{IN}	12V
V_{OUT}	1 V
I_{OUT}	6 A

The detailed application schematics are shown in Figure 7 through Figure 11. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 6 and follow the guidelines below.

1. Connect the input ground to GND using the shortest and widest trace possible.
2. Connect the input capacitor to IN using the shortest and widest trace possible.
3. Ensure that all feedback connections are short and direct.
4. Place the feedback resistors and compensation components as close to the chip as possible.
5. Route SW away from sensitive analog areas, such as VOUT.
6. Connect AGND to PGND using the shortest and widest trace possible.

Note:

9) The recommended layout is based on the Typical Application Circuits shown in Figure 7 to Figure 11.

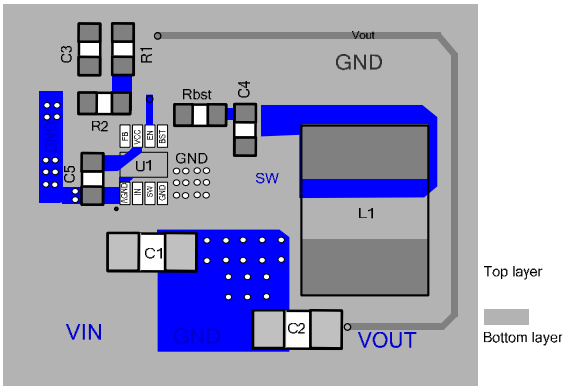


Figure 6: Recommended Layout

TYPICAL APPLICATION CIRCUITS

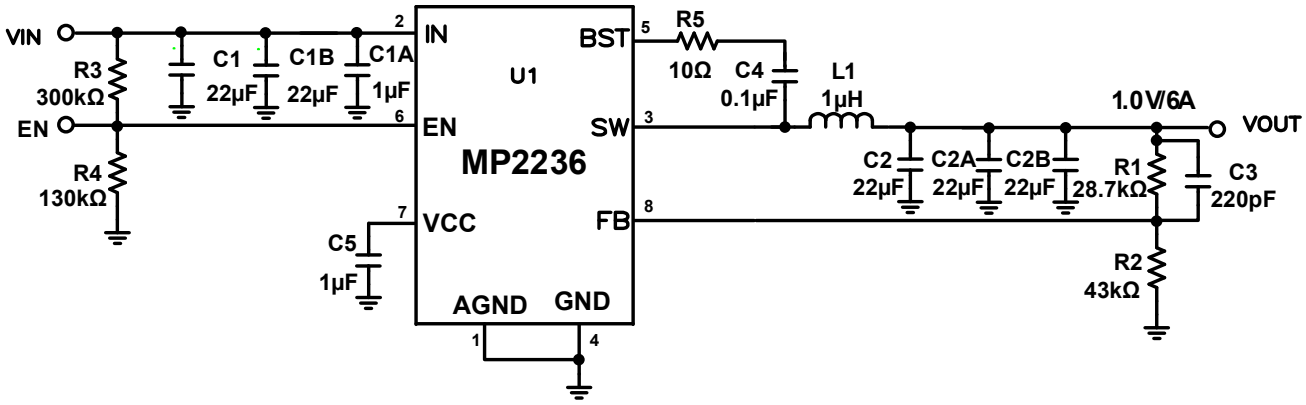


Figure 7: 12V V_{IN}, 1.0V/6A Output

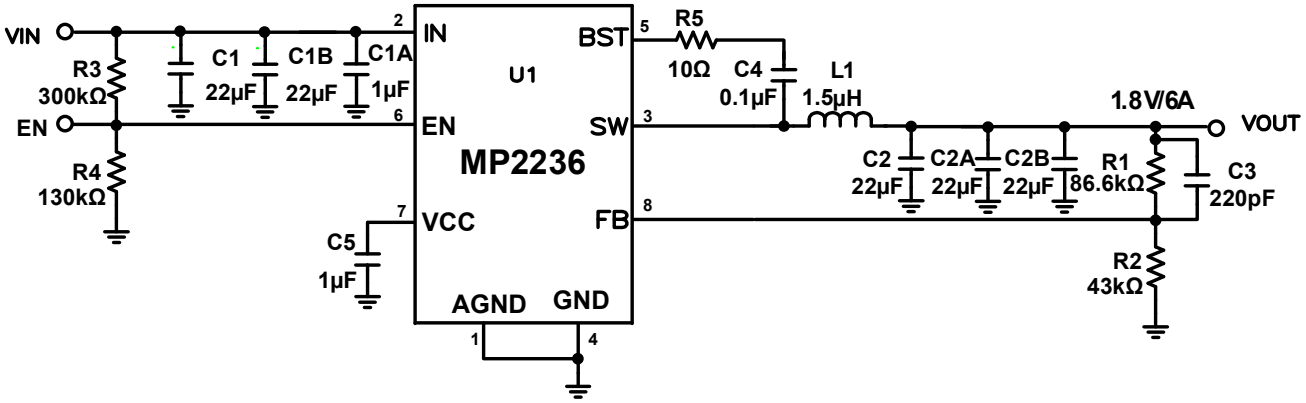


Figure 8: 12V V_{IN}, 1.8V/6A Output

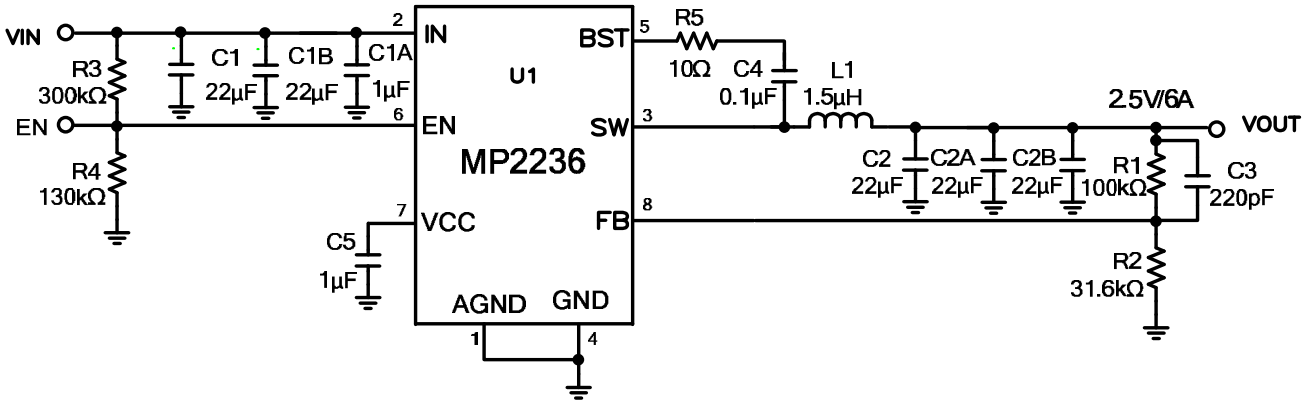


Figure 9: 12V V_{IN}, 2.5V/6A Output

TYPICAL APPLICATION CIRCUITS *(continued)*

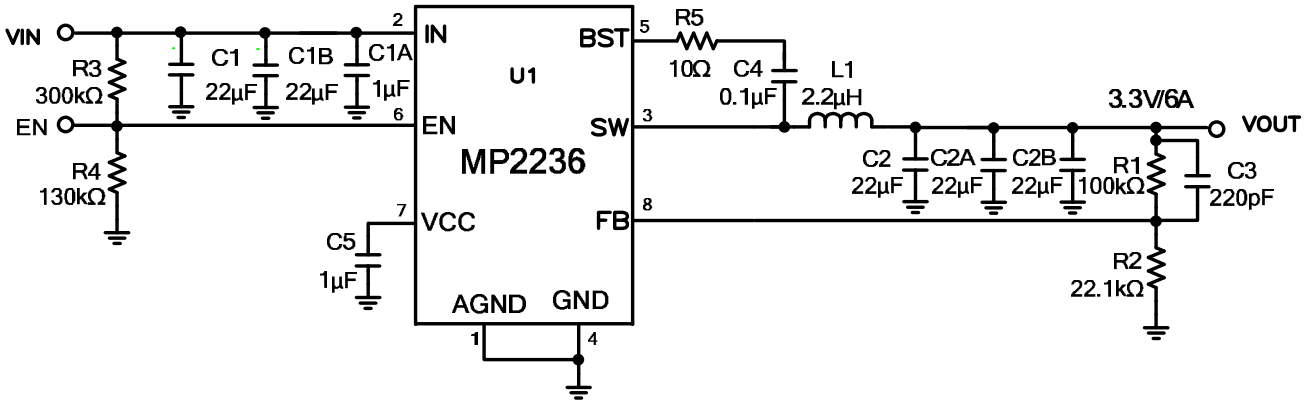


Figure 10: 12V V_{IN}, 3.3V/6A Output

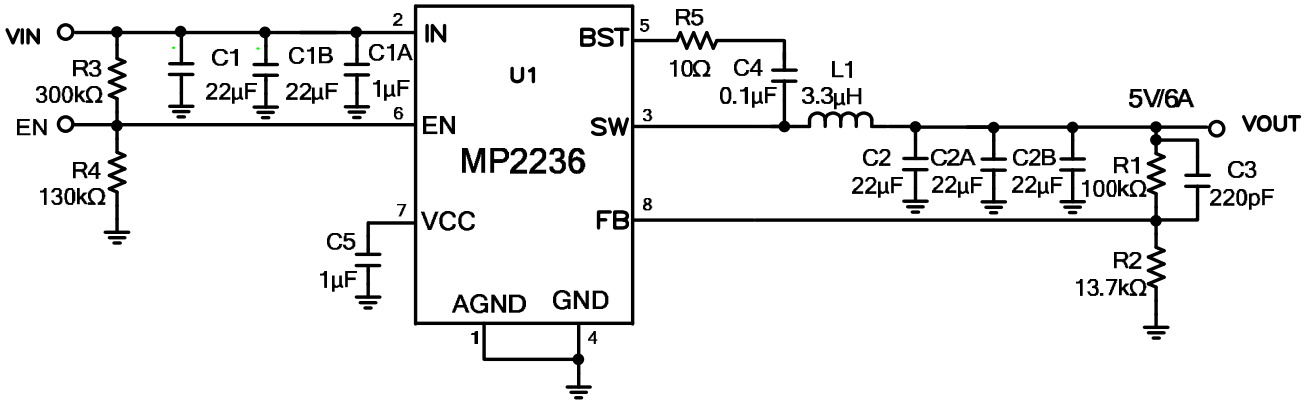
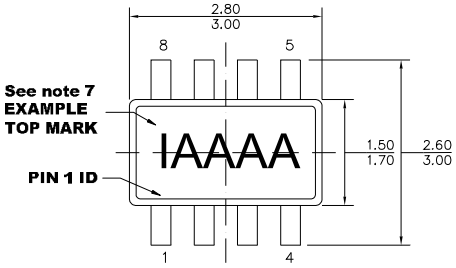


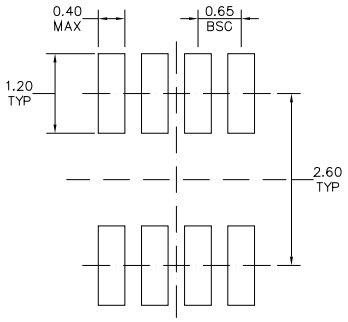
Figure 11: 12V V_{IN}, 5V/6A Output

PACKAGE INFORMATION

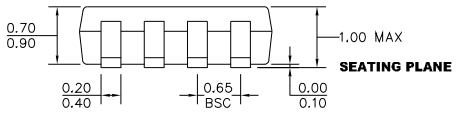
TSOT23-8



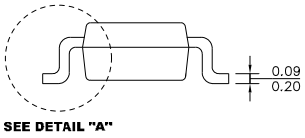
TOP VIEW



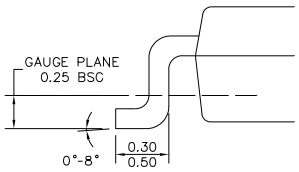
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/01/2018	Initial Release	-
1.1	08/04/2021	Updated typical application circuit. V_{OUT} = 1V, change R1 to 28.7kΩ, change R2 to 43kΩ. V_{OUT} = 1.8V, change R1 to 86.6kΩ, change R2 to 43kΩ	Pages 1, 15, and 18
		Update the output voltage (V_{OUT}) range. 0.6V to 12V to (V_{OUT}) 0.6V to 8V	Page 3