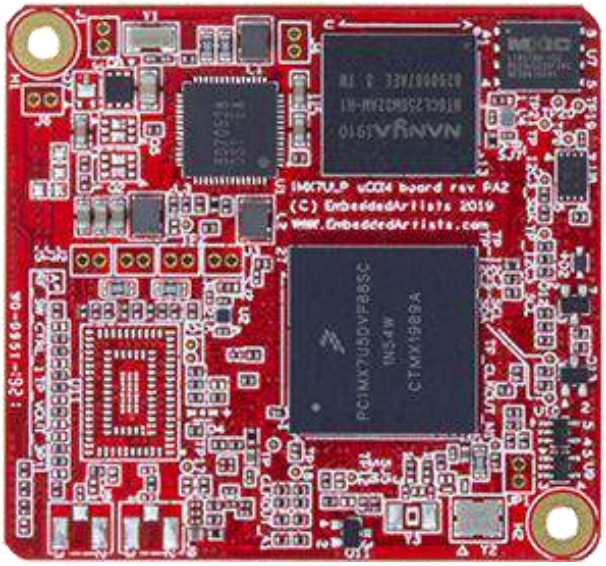
iMX7ULP uCOM Board Datasheet



Get Up-and-Running Quickly and
Start Developing Your Application On Day 1!

Embedded Artists

Embedded Artists AB
Jörgen Ankersgatan 12
211 45 Malmö
Sweden

https://www.EmbeddedArtists.com

Disclaimer

Embedded Artists AB makes no representation or warranties with respect to the contents hereof and specifically disclaim any implied warranties or merchantability or fitness for any particular purpose. The information has been carefully checked and is believed to be accurate, however, no responsibility is assumed for inaccuracies.
Information in this publication is subject to change without notice and does not represent a commitment on the part of Embedded Artists AB.

Feedback

We appreciate any feedback you may have for improvements on this document.

Trademarks

All brand and product names mentioned herein are trademarks, services marks, registered trademarks, or registered service marks of their respective owners and should be treated as such.

Table of Contents

1 Document Revision History

Revision	*Date*	*Description*
PA1	2019-10-04	First version.
PA2	2019-10-09	Corrected measurement in Figure 10.
PA3	2019-10-15	Added information about USB multiplexing.
PA4	2020-07-30	Added section 13.5

2 Introduction

This document is a datasheet that specifies and describes the *iMX7ULP uCOM Board* mainly from a hardware point of view. Some basic software related issues are also addressed, like booting and functional verification, but there are separate software development manuals that should also be consulted.

2.1 Hardware

The *iMX7ULP uCOM Board* is a Computer-on-Module (COM) based on NXP's ARM Cortex-A7 / M4 i.MX 7ULP System-on-Chip (SoC) application processor. The board provides a quick and easy solution for implementing a high-performance ARM Cortex-A7 / M4 based design. The Cortex-A7 core runs at up to 720MHz (650MHz for industrial version) and the Cortex-M4 core at up to 200 MHz.

The heterogeneous core architecture enables the system to run an OS like Linux on the Cortex-A7 core and a Real-Time OS (RTOS) on the Cortex-M4. This architecture is ideal for real time applications where Linux cannot be used for all time critical tasks. The Cortex-M4 can handle (real time) critical tasks and can also be used to lower the power consumption.

The *iMX7ULP uCOM Board* delivers high computational and graphical performance at low power consumption. The on-board PMIC, supporting DVFS (Dynamic Voltage and Frequency Scaling), together with a LPDDR3 memory sub-system reduce the power consumption.

The SoC is part of the scalable i.MX 6/7/8 product family. There is a range of i.MX 6/7/8 (u)COM Boards from Embedded Artists with single, dual and quad Cortex-A cores, with or without a heterogeneous Cortex-M core. Groups of boards (uCOM and COM) share the same basic pinning for maximum flexibility and performance scalability.

The *iMX7ULP uCOM Board* has an ultra-small form factor and shields the user from a lot of complexity of designing a high performance system. It is a robust and proven design that allows the user to focus the product development, shorten time to market and minimize the development risk.

The *iMX7ULP uCOM Board* targets a wide range of applications, such as:

- Portable systems
- HMI/GUI solutions
- Portable medical and health care
- Connected vending machines
- Point-of-Sale (POS) applications
- Access control panels
- Audio
- IP phones
- Smart appliances
- Wearables
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

The picture below illustrates the block diagram of the *iMX7ULP uCOM Board*.

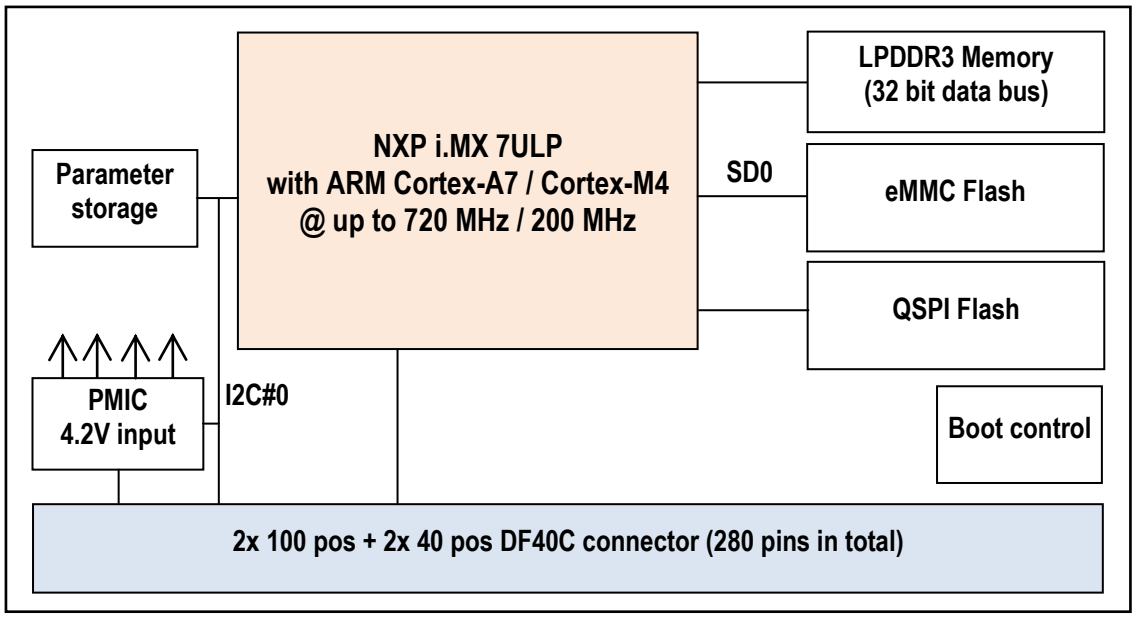


Figure 1 – iMX7ULP uCOM Board Block Diagram

The *iMX7ULP uCOM Board* pin assignment focus on direct connection to (carrier board) interface connectors and minimize trace and layer crossing. This is important for high speed, serial interfaces with impedance controlled differential pairs. As a result, carrier boards can be designed with few routing layers. In many cases, a four layer PCB is enough to implement advanced and compact carrier boards. The pin assignment is common for the *iMX7/8 uCOM Boards* from Embedded Artists and the general, so called, EAuCOM specification is found in separate document.

2.2 Software

The *iMX7ULP uCOM Board* has a Board Support Package (BSP) for Linux and an SDK for the Cortex-M4 side. Precompiled images are available. Embedded Artists work with partners that can provide support for other operating systems (OS). For more information contact Embedded Artists support.

This document has a hardware focus and does not cover software development. See other documents related to the *iMX7ULP uCOM Board* for more information about software development.

2.3 Features and Functionality

The i.MX 7ULP is a powerful SoC. The full specification can be found in NXP's *i.MX 7ULP Datasheet* and *i.MX 7ULP Reference Manual*. The table below lists the main features and functions of the *iMX7ULP uCOM board* - which represents Embedded Artists integration of the i.MX 7ULP SoC. Due to pin configuration some functions and interfaces of the i.MX 7ULP many not be available at the same time. See i.MX 7ULP SoC datasheet and reference manual for details. Also see pin multiplexing Excel sheet for details.

Group	Feature		iMX7ULP uCOM Board
CPUs	NXP SoC	commercial temp. range industrial temp. range	MCIMX7U5DVP07S (0 - 70° C) MCIMX7U5CVP06S (-40 - 85° C)
	CPU Cores		1x Cortex-A7 1x Cortex-M4F with MPU/FPU
	L1 Instruction cache		32 KByte on Cortex-A7 8 KByte on Cortex-M4

	L1 Data cache	32 KByte on Cortex-A7 8 KByte on Cortex-M4
	L2 Cache on Cortex-A7 core	256 KByte
	On-chip SRAM	256 KByte
	NEON SIMD media accelerator on Cortex-A7	✓
	Maximum CPU frequency	650/720 MHz on Cortex-A7 in overdrive mode (note: currently not supported) 500 MHz max on Cortex-A7 in standard mode 200 MHz on Cortex-M4
Security Functions	High Assurance Boot	✓
	Cryptographic Acceleration and Assurance Module	✓
	Secure Non-Volatile Storage	✓
	System JTAG controller	✓
	Extended Resource Domain Controller (XRDC)	✓
Memory	LPDDR3 RAM Size	1 GByte, default. Other on request.
	LPDDR3 RAM Speed	720 MT/s
	LPDDR3 RAM Memory Width	32 bit
	eMMC NAND Flash (8 bit)	8 GByte, default. Other on request.
	QSPI	4 MByte, default. Other on request.
Graphical Processing	Multimedia Graphics Processing Unit (GPU)	OpenGL ES2.0/1.1, Desktop OpenGL 2.1, OpenVG1.1
Graphical Output	MIPI-DSI, 2 lanes	✓
Graphical Input	Parallel Camera Sensor Interface	✓
Analog I/O	2x ADC, 12-bit	✓
	2x DAC, 12-bit	✓
	2x Comparators	✓
Connectivity Interfaces (all functions are not available at the same time)	USB2.0 OTG port with Phy	✓
	HSIC USB	✓
	2x I2S	✓
	1x SD3.0/MMC 5.0	✓ SD0 interface used on-board to eMMC
	2x SPI, 4x UART, 4x I²C	✓
	PWMs, FlexIOs, WDOG	✓
Other	PMIC (BD70528MWV)	✓

	E2PROM storing board information	✓
	On-board RTC via PMIC (BD70528MWV)	✓
	On-board watchdog functionality	✓

2.4 Reference Documents

The following documents are important reference documents and should be consulted when integrating the *iMX7ULP uCOM board*:

- EACOM Board Specification
- EACOM Board Integration Manual

The following NXP documents are also important reference documents and should be consulted for functional details:

- IMX7ULPCEC, i.MX 7ULP Applications Processors - Consumer Products Data Sheet, latest revision
- IMX7ULPIEC, i.MX 7ULP Applications Processors - Industrial Products Data Sheet, latest revision
- IMX7ULPRM, i.MX 7ULP Applications Processors Reference Manual, latest revision
- IMX7ULPSRM, Security Reference Manual for i.MX 7ULP, latest revision
- IMX7ULPCE, Chip Errata for the i.MX 7ULP, latest revision
  Note: It is the user's responsibility to make sure all errata published by the manufacturer are taken note of. The manufacturer's advice should be followed.
- AN12573, i.MX 7ULP Power Consumption Measurement, latest revision
- i.MX 7ULP Product Lifetime Usage, latest revision

The following documents are external industry standard reference documents and should also be consulted when applicable:

- eMMC (Embedded Multi-Media Card) the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org)
- The I2C Specification, Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com)
- I2S Bus Specification, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- JTAG (Joint Test Action Group) defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org)
- MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org)
- SD Specifications Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org)
- SPI Bus – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)

- DSI (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (www.mipi.org)
- USB Specifications (www.usb.org)

3 Board Pinning

Embedded Artists has defined the EAuCOM board standard with 42 x 45 mm boards that use Hirose DF40C connectors. Note that this is not the same as the EACOM board standard with module size 82 x 50 mm. Chapter 4 describes an adapter board that converts an EAuCOM board into an EACOM board. This way, the same carrier board can be used for all iMX Developer's Kits. See the *EAuCOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EAuCOM**.

There are four Hirose DF40C expansion connectors; two 100 pos and two 40 pos connectors. The 0.4mm pitch connectors have a board-to-board stacking height of only 1.5mm. There are also versions of the receptacle connectors that give 3.0mm stacking height.

3.1 Pin Numbering

The figure below illustrates the location of the four expansion connectors and their respective pin numbering on the bottom side of the *iMX7ULP uCOM Board*.

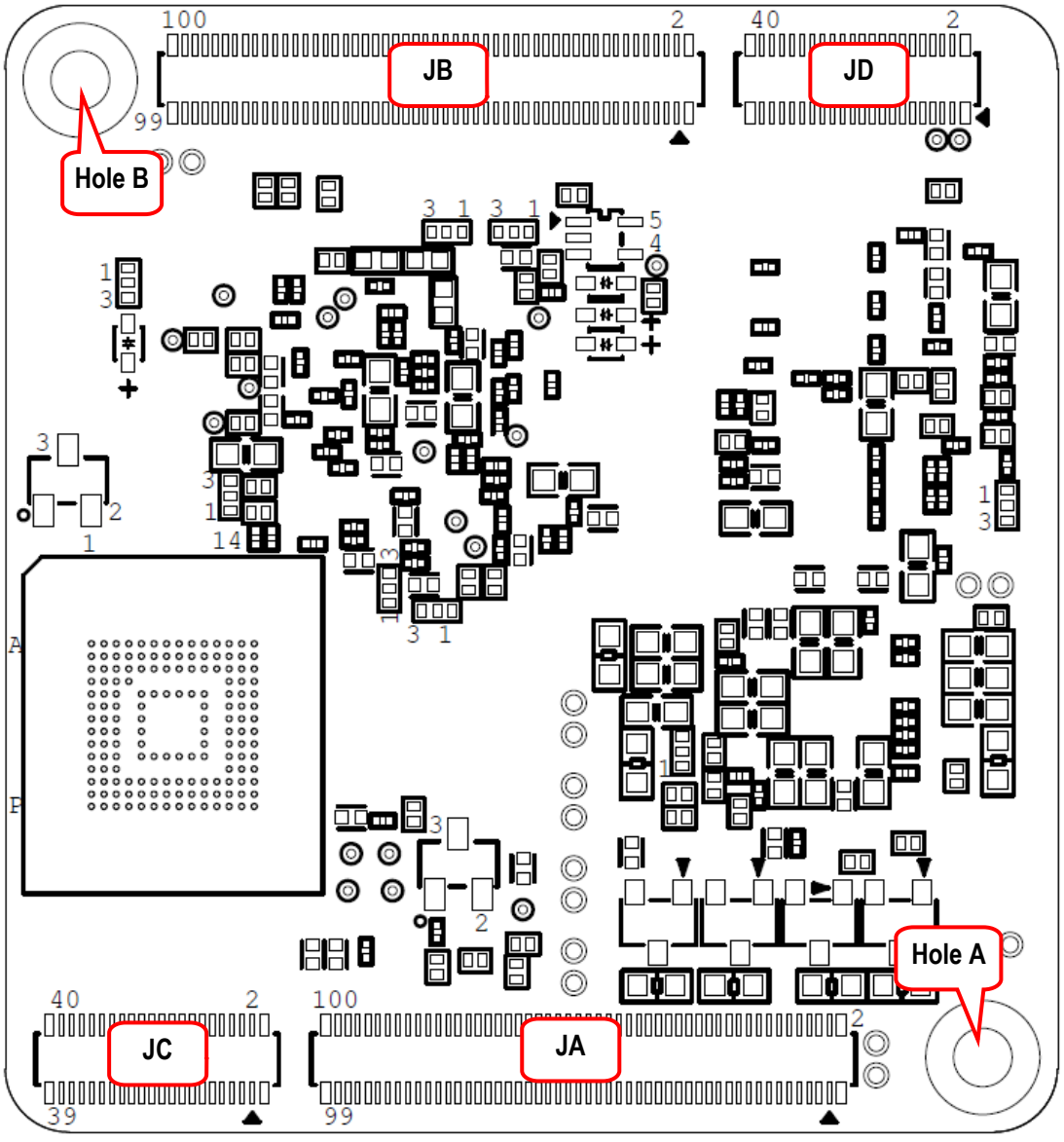


Figure 2 – iMX7ULP uCOM (EAuCOM standard) Board Pin Numbering, Bottom Side

3.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Connector and Pin number	The pin numbers are listed in consecutive order. Odd pin numbers are on one row and even numbers on the other row.
Non-i.MX 7ULP signals	Lists signals that are not directly connected to the i.MX 7ULP SoC. These signals are typically related to powering and connected to the on-board Power Management IC (PMIC), BD70528MWV.
i.MX 7ULP Ball Name	The name of the ball of the i.MX 7ULP SoC that is connected to this pin.
Alternative Pin Function	Information if the signal is a dedicated interface or a general pin that can multiples different signals. See separate Excel sheet for details about available multiplexing alternatives.
Notes	When relevant, the preferred pin function is listed.

Note that some pins are EAuCOM board *type specific*, meaning that these pins might not be compatible with other EAuCOM boards. Using these may result in lost compatibility between EAuCOM boards, but not always. Check details between EAuCOM boards of interest.

The table below lists the pins on expansion connector JA (100-pos connector).

JA Pin Number	EAuCOM Board Signal	i.MX 7ULP Ball Name	Alternative Pin Function?	Notes
1-8	VIN_VBAT	PMIC: VBAT		System supply voltage, see chapter 8 for more details.
9-16	GND			
17	VDD1	PMIC: VOLDO3		Voltage rail, see chapter 8 for more details.
18	VDD_RTC			Not connected. On-board RTC powered via VIN.
19, 21, 23, 25, 27, 29	VDD_1V8	PMIC: BUCK2		1.8V voltage rail, see chapter 8 for more details.
20, 22, 24, 26, 28, 30	VDD_3V3	PMIC: BUCK1		3.3V voltage rail, see chapter 8 for more details.
31-32	GND			
33	Board specific	DAC0_OUT	No	
34, 36, 38, 40, 42	VDD_RF			Not connected per default. Can optionally power on-board RF-module. Requires special order for this mounting option.
35	Board specific	DAC1_OUT	No	
37	Board specific	PTF14	Yes	
39	Board specific	PTF4	Yes	
41	GND			
43	Board specific	PTF5	Yes	
44	GND			
45	Board specific	PTF6	Yes	
46	GND			
47	Board specific	PTF7	Yes	
48	VBAT_TEMP	PMIC: NTC		Battery temperature, see chapter 8 for more details.
49	Board specific	PTF8		
50	VBAT_CURRP	PMIC: VBAT_FB		Battery feedback voltage, see chapter 8 for more details.

51	GND			
52	VBAT_CURRN	-		Not connected
53	Board specific	PTF9	Yes	
54, 56, 58, 60	PSU_5V	PMIC		Charge voltage supply, see chapter 8 for more details.
55	Board specific	PTF10	Yes	
57	Board specific	PTF11	Yes	
59	Board specific	PTF15	Yes	
61	GND			
62, 64, 66, 68	VBUS_USB	PMIC		Charge voltage supply, see chapter 8 for more details.
63	Board specific	PTF0	Yes	
65	Board specific	PTA14	Yes	
67	Board specific	PTA12	Yes	
69	Board specific	PTA13	Yes	
70-71	GND			
72	Board specific	TAMPER	No	
73	Board specific	PTA15	Yes	
74	Board specific	A7_POR_B		Internal power enable signal for Cortex-A7 side. Active low. Is connected to PTA25. Signal is controlled by BSP.
75	Board specific	PTF1	Yes	
76	Board specific	-		Note connected
77	Board specific	PTF2	Yes	
78	Board specific	PMIC: VINLED1		
79	Board specific	PTF3	Yes	
80	Board specific	PMIC: VINLED2		
81-82	GND			
83	Board specific	PTA3	Yes	
84	Board specific	PTC11	Yes	
85	Board specific	PTA4	Yes	
86	Board specific	PTB0	Yes	Note. This signal is 1.8V logic level.
87	Board specific	PTA6	Yes	
88	Board specific	PTB11	Yes	Note. This signal is 1.8V logic level.
89	Board specific	PTA5	Yes	
90	Board specific	PTB14	Yes	Note. This signal is 1.8V logic level.
91-92	GND			
93	Board specific	PTA7	Yes	
94	Board specific	PTF16	Yes	
95	Board specific	PTA1	Yes	
96	Board specific	PTF17	Yes	
97	Board specific	PTA0	Yes	
98	Board specific	PTF18	Yes	
99	Board specific	PTA2	Yes	

100	Board specific	PTF19	Yes	

The table below lists the pins on expansion connector JB (100-pos connector).

JB Pin Number	EAuCOM Board Signal	i.MX 7ULP Ball Name	Alternative Pin Function?	Notes
1	UART-B_RXD	PTE11	Yes	Not connected if Wi-Fi/BT module mounted
2	GPIO-A	PTC8	Yes	
3	UART-B_TXD	PTE10	Yes	Not connected if Wi-Fi/BT module mounted
4	GPIO-B	PTC9	Yes	
5	UART-A_RXD	PTC3	Yes	
6	GPIO-C	PTC10	Yes	
7	UART-A_TXD	PTC2	Yes	
8	GPIO-D	PTC14	Yes	
9	UART-B_CTS	PTE9	Yes	Not connected if Wi-Fi/BT module mounted
10	GPIO-E	PTC15	Yes	
11	UART-B_RTS	PTE8	Yes	Not connected if Wi-Fi/BT module mounted
12	GPIO-F	PTA24	Yes	
13	UART-C_RXD	PTA19	Yes	
14	GPIO-G	PTA31	Yes	
15	UART-C_TXD	PTA18	Yes	
16	GPIO-H	PTC0	Yes	
17	GND			
18	GPIO-J	PTC1	Yes	
19	SD-A_VDD	-		Not connected
20	GPIO-K	PTC6	Yes	
21	GND			
22	GPIO-L	PTC7	Yes	
23	SD-A_CLK	-		Not connected
24	GPIO-M	CLK32K		
25	SD-A_CMD	-		Not connected
26	GND			
27	SD-A_DATA0	-		Not connected
28	SPI-A_SCLK	PTA17	Yes	
29	SD-A_DATA1	-		Not connected
30	SPI-A_MISO	PTA20	Yes	
31	SD-A_DATA2	-		Not connected
32	SPI-A_MOSI	PTA16	Yes	
33	SD-A_DATA3	-		Not connected
34	SPI-A_SS0	PTA23	Yes	
35	GND			
36	GND			

37	SD-A_WP	-		Not connected
38	SPI-B_SCLK	PTC18	Yes	
39	SD-A_NCD	PTA11	Yes	
40	SPI-B_MISO	PTC16	Yes	
41	SD-A_NRST	PTA10	Yes	
42	SPI-B_MOSI	PTC17	Yes	
43	USB-A_OC	PTE14	Yes	
44	SPI-B_SS0	PTC19	Yes	
45	USB-A_PWR	PTE15	Yes	
46	GND			
47	USB-A_VBUS	USB_OTG_VBUS		
48	I2C-A_SCL	PTC4	No	Note: Do not change pin function. Must be an I2C channel since the interface is used on-board.
49	USB-A_DN	USB_OTG_DN		
50	I2C-A_SDA	PTC5	No	Note: Do not change pin function. Must be an I2C channel since the interface is used on-board.
51	USB-A_DP	USB_OTG_DP		
52	I2C-B_SCL	PTF12	Yes	This signal as a 4.7Kohm pull-up resistor to 3.3V
53	USB-A_ID	PTC13	Yes	
54	I2C-B_SDA	PTF13	Yes	This signal as a 4.7Kohm pull-up resistor to 3.3V
55	GND			
56	I2C-C_SCL	PTA8	Yes	This signal as a 4.7Kohm pull-up resistor to 3.3V
57	USB-B_OC	-		Not connected
58	I2C-C_SDA	PTA9	Yes	This signal as a 4.7Kohm pull-up resistor to 3.3V
59	USB-B_PWR	-		Not connected
60	I2C-D_SCL	PTB12	Yes	Note. This signal is 3.3V logic level. There is an on-board voltage level translator to the 1.8V logic of PTB. This signal as a 4.7Kohm pull-up resistor to 3.3V
61	USB-B_VBUS	-		Not connected
62	I2C-D_SDA	PTB13	Yes	Note. This signal is 3.3V logic level. There is an on-board voltage level translator to the 1.8V logic of PTB. This signal as a 4.7Kohm pull-up resistor to 3.3V
63	USB-B_DN	-		Not connected
64	GND			
65	USB-B_DP	-		Not connected
66	GND			
67	USB-B_ID	-		Not connected
68	PERI_PWR_EN	PTA21	No	**Power enable signal for external peripherals. No external must drive any signal to the i.MX7ULP SoC before this signal is active.** Signal is active high and is connected to PTA25. Signal is controlled by BSP.
69	GND			
70	POR_B	POR_B		Connected to RESET0_B on the i.MX 7ULP SoC. Signal shall normally only be used to connect to debug interface connector. Use signals RESET_IN (JB pin 74) to cause a power cycle reset of the board.

				Note. This signal is 1.8V logic level.
71	ETH_LED_10/100	-		Not connected
72	ONOFF	PMIC_ONOFF		Connects to PMIC (BD70528MWV) PWRON input.
73	ETH_LED_1000	-		Not connected
74	PWRON_B	RESET_IN		A falling edge on this input cause a power cycle reset of the board. Connects to PMIC (BD70528MWV) GPIO4 (that is the RESET_IN input).
75	ETH_LED_ACT	-		Not connected
76	BOOT_MODE0	PTB4-BOOT_MODE0	Yes	This signal shall be left unconnected under normal operation. The Boot Mode is controlled by signals ISP_ENABLE (JB pin 100) and BOOT_CTRL (JB pin 98). Note. This signal is 1.8V logic level.
77	GND			
78	BOOT_MODE1	PTB5-BOOT_MODE1	Yes	This signal shall be left unconnected under normal operation. The Boot Mode is controlled by signals ISP_ENABLE (JB pin 100) and BOOT_CTRL (JB pin 98). Note. This signal is 1.8V logic level.
79	ETH_TRXP1	-		Not connected
80	TEST_MODE			
81	ETH_TRXN1	-		Not connected
82	JTAG_VCC	VDD_PTA		The supply voltage of the JTAG debug interface. Is connected to the supply voltage of PTA (default is 3.3V).
83	GND			
84	GND			
85	ETH_TRXP0	-		Not connected
86	JTAG_TCK	PTA29	Yes	
87	ETH_TRXN0	-		Not connected
88	JTAG_TMS	PTA26	Yes	
89	GND			
90	JTAG_TDI	PTA28	Yes	
91	ETH_TRXN3	-		Not connected
92	JTAG_TDO	PTA27	Yes	
93	ETH_TRXP3	-		Not connected
94	JTAG_TRST	PTA30	Yes	
95	GND			
96	JTAG_MOD	-		Not connected
97	ETH_TRXN2	-		Not connected
98	BOOT_CTRL			Pull input low to ground to boot with default settings (controlled by on-board pullup/pulldown resistors. This is the default mode. Leave floating/open to boot from OTP fuses (on the i.MX 7ULP SoC). Note that the OTP fuses must first be programmed, typically via UUU. See chapter 7 for more details about boot control and options.
99	ETH_TRXP2	-		Not connected
100	ISP_ENABLE			Leave floating/open for normal boot. Pull low to ground to place i.MX 7ULP SoC in USB OTG boot mode (during next power cycle). See chapter 7 for more detail

				about boot control and options.

The table below lists the pins on expansion connector JC (40-pos connector). Note that this connector is not mounted if the Murata 1LV Wi-Fi/BT module is mounted (because the signals available on this connector are all used to connect to the 1LV Wi-Fi/BT module).

JC Pin Number	EAuCOM Board Signal	i.MX 7ULP Ball Name	Alternative Pin Function?	Notes
1	SD-B_VCC	VDD_PTE		Supply voltage for port E. This is a output, not an input.
2	GND			
3	SD-B_CLK	PTE2	Yes	
4	Board specific	-		Not connected
5	SD-B_CMD	PTE3	Yes	
6	Board specific	-		Not connected
7	SD-B_DATA0	PTE1	Yes	
8	Board specific	-		Not connected
9	SD-B_ DATA1	PTE0	Yes	
10	Board specific	-		Not connected
11	SD-B_ DATA2	PTE5	Yes	
12	GND			
13	SD-B_ DATA3	PTE4	Yes	
14	Board specific	-		Not connected
15	Board specific	PTE13	Yes	
16	Board specific	-		Not connected
17	Board specific	PTE12	Yes	
18	Board specific	-		Not connected
19	Board specific	PTE7	Yes	
20	Board specific	-		Not connected
21	Board specific	PTC12	Yes	
22	GND			
23	Board specific	PTE6	Yes	
24	Board specific	-		Not connected
25	Board specific	PTB9	Yes	Note. This signals is 1.8V logic level.
26	Board specific	-		Not connected
27	SAI_TXFS	PTB2	Yes	Note. This signals is 1.8V logic level.
28	Board specific	-		Not connected
29	SAI_TXD	PTB3	Yes	Note. This signals is 1.8V logic level.
30	Board specific	-		Not connected
31	SAI_TXC	PTB1	Yes	Note. This signals is 1.8V logic level.
32	GND			
33	SAI_RXD	PTB10	Yes	Note. This signals is 1.8V logic level.
34	Board specific	-		Not connected
35	Board specific	-		Not connected
36	Board specific	-		Not connected
37	Board specific	PTA22	No	Note: Leave signal unconnected. Is an on-board signal used

			for watchdog reset of the board.
38	Board specific	-	Not connected
39	Board specific	-	Not connected
40	Board specific	-	Not connected

The table below lists the pins on expansion connector JD (40-pos connector).

JD Pin Number	EAuCOM Board Signal	i.MX 7ULP Ball Name	Alternative Pin Function?	Notes
1	DSI_DN3	TEST_CLK_N	No	
2	CSI_CKN	-		Not connected
3	DSI_DP3	TEST_CLK_P	No	
4	CSI_CKP	-		Not connected
5	GND			
6	GND			
7	DSI_DN0	DSI_DATA0_N	No	
8	CSI_DN0	-		Not connected
9	SDI_DP0	DSI_DATA0_P	No	
10	CSI_DP0	-		Not connected
11	GND			
12	GND			
13	DSI_DN2	-		Not connected
14	CSI_DN1	-		Not connected
15	DSI_DP2	-		Not connected
16	CSI_DP1	-		Not connected
17	GND			
18	GND			
19	DSI_DN1	DSI_DATA1_N	No	
20	CSI_DN2	-		Not connected
21	DSI_DP1	DSI_DATA1_P	No	
22	CSI_DP2	-		Not connected
23	GND			
24	GND			
25	DSI_CKN	DSI_CLK_N	No	
26	CSI_DN3	-		Not connected
27	DSI_CKP	DSI_CLK_P	No	
28	CSI_DP3	-		Not connected
29	GND			
30	GND			
31	Board specific	-		Not connected
32	PCIE_RXN	-		Not connected
33	PCIE_CLKREQ_B	-		Not connected
34	PCIE_RXP	-		Not connected

35	GND			
36	GND			
37	PCIE_CLKN			Not connected
38	PCIE_TXN	USB_HSIC_DATA	No	
39	PCIe_CLKP			Not connected
40	PCIE_TXP	USB_HSIC_STROBE	No	

4 uCOM Adapter Board

Embedded Artists has defined the EACOM board standard that is based on the SMARC form factor; module size 82 x 50 mm. Note that pinning is different from the SMARC standard. See the *EACOM Board specification* document for details and background information. Hereafter this standard will be referred to as **EACOM**.

Embedded Artists has also defined the **EAuCOM** board standard with 42 x 45 mm boards that use Hirose DF40C connectors. The *uCOM Adapter Board* has been designed to convert an EAuCOM board into an EACOM board. This way, the same carrier board can be used for all *iMX Developer's Kits*.

The *iMX7ULP uCOM Developers Kit V2* consists of:

- One *iMX7ULP uCOM Board, mounted on*
- One *uCOM Adapter Board* , mounted on
- One *COM Carrier Board V2*

The *uCOM Adapter Board* contains the following functions (see schematic for details):

- MIPI-DSI to HDMI bridge
- MIPI-DSI interface directly to LCD, including backlight LED driver and touch interface
- Boot control
- Battery connector
- JTAG connector
- Optional 3.6V RF supply voltage for uCOM boards with on-board Wi-Fi/BT module
- Possibility to measure input and output currents on supply nets
- Voltage level translation on some signals
- USB multiplexor (for iMX7ULP, which only have one USB interface)

The carrier board connector has 314 pins with 0.5 mm pitch and the *uCOM Adapter Board* is inserted in a right angle (R/A) style. The connector is originally defined for use with MXM3 graphics cards. There are multiple sources for carrier board (MXM3) connectors due to the popular standard. The signal integrity is excellent and suitable for data rates up to 5 GHz.

4.1 Pin Numbering

The figures below show the pin numbering for *uCOM Adapter Board*, which is compatible with EACOM boards. Top side edge fingers are numbered P1-P156. Bottom side edge fingers are numbered S1-S158. There is an alternative pin numbering that follows the MXM3 standard with even numbers on the bottom and odd numbers on the top. This numbering is from 1-321, with 7 numbers/pins (150-156) removed due to the keying.

The picture below also illustrates where the *iMX7ULP uCOM board* is mounted on the *uCOM Adapter Board*.

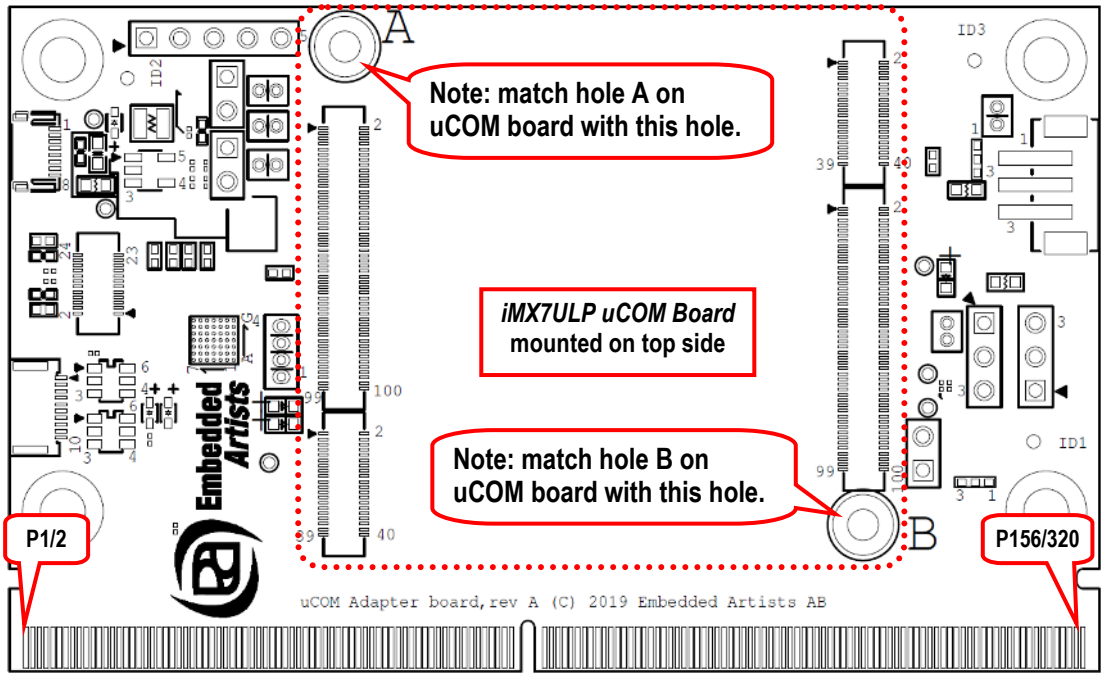


Figure 3 – uCOM Adapter Board Pin Numbering, Top Side

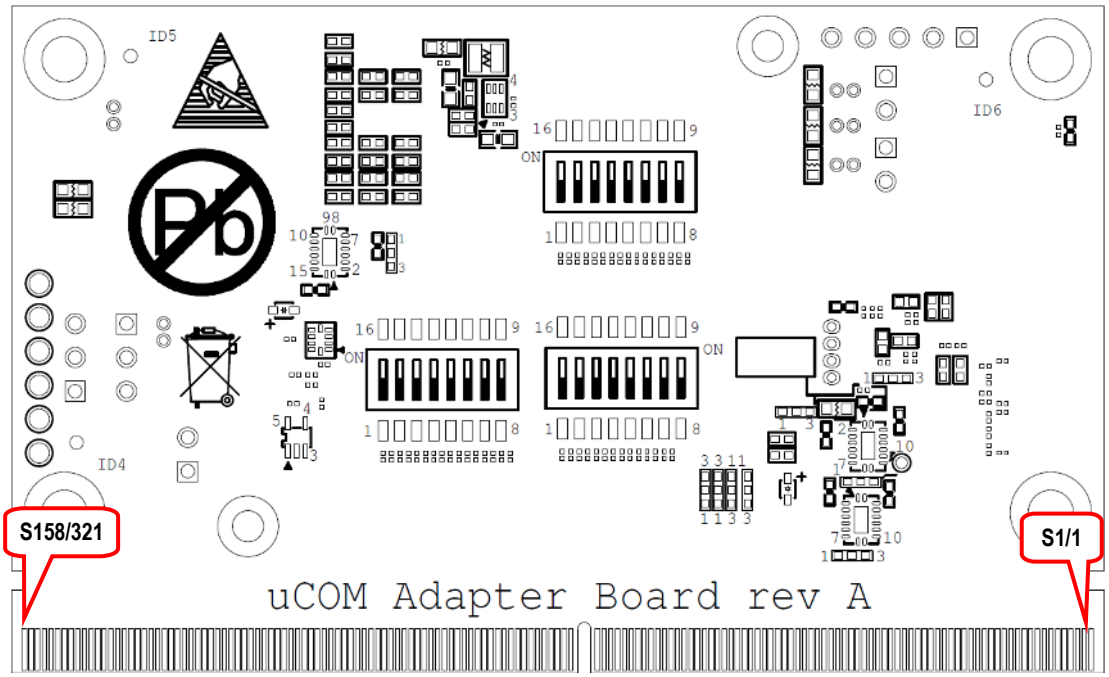


Figure 4 – uCOM Adapter Board Pin Numbering, Bottom Side

4.2 Pin Assignment

This section describes the pin assignment of the board, with the following columns:

Pin number	**Px** are top side edge fingers. **Sx** are bottom side edge fingers. An alternative, consecutive, numbering is also shown with odd numbers on the top and even numbers on the bottom side.

EACOM Board	Describe the typical usage of the pin according to EACOM. This pin usage should be followed to get compatibility between different COM boards. If this is not needed, then any of the alternative functions on the pin can also be used.
i.MX 7ULP Ball Name	The name of the ball of the i.MX 7ULP SoC (or other component on the uCOM board) that is connected to this pin.
Notes	When relevant, the preferred pin function is listed.

There are 45 ground pins, which equal to about 15%, and 10 input voltage supply pins.

Note that some pins are EACOM board *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using these may result in lost compatibility between EACOM boards, but not always. Check details between EACOM boards of interest.

Note that not all EACOM-defined pins are connected on anything, typically because an interface is not supported or there are not enough free pins in the i.MX 7ULP SoC.

Further, some pins are *COM board type specific*, meaning that these pins might not be compatible with other EACOM boards. Using *type specific* pins may result in lost compatibility between EACOM boards, but not always. Check details between EACOM boards of interest.

The table below lists the top side pins, P1-P156, odd numbers.

Top Side Pin Number	EAuCOM Board	EACOM Board	i.MX 7ULP Ball Name	Alternative pin functions?	Notes
P1/2	JC pin 025 SD-B_STROBE	GPIO-F	PTB9	Yes	Via 3.3V to 1.8V level translator Hardwired as output from uCOM board (via U7 on uCOM Adapter board) **Note**: If NVCC_SD2 is 1.8V, the logic level of this signal will be 1.8V (and not 3.3V). NVCC_SD2 will be 1.8V when accessing an ultra-high speed SD memory card.
P2/4	JD pin 033	GPIO-E			Not connected
P3/6	JB pin 039 SD-A_NCD	GPIO-D	PTA11	Yes	**Note**: If NVCC_SD2 is 1.8V, the logic level of this signal will be 1.8V (and not 3.3V). NVCC_SD2 will be 1.8V when accessing an ultra-high speed SD memory card.
P4/8	JB pin 041 SD-A_NRST	GPIO-C	PTA10	Yes	**Note**: If NVCC_SD2 is 1.8V, the logic level of this signal will be 1.8V (and not 3.3V). NVCC_SD2 will be 1.8V when accessing an ultra-high speed SD memory card.
P5/10	JC pin 009 SD-B_DATA1	SD_D1	PTE0	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P6/12	JC pin 007 SD-B_DATA0	SD_D0	PTE1	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P7/14	JC pin 003 SD-B_CLK	SD_CLK	PTE2	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P8/16	JC pin 005 SD-B_CMD	SD_CMD	PTE3	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P9/18	JC pin 013 SD-B_DATA3	SD_D3	PTE4	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P10/20	JC pin 011 SD-B_DATA2	SD_D2	PTE5	Yes	**Note**: Logic level (3.3V or 1.8V depends on NVCC_SD2, which is controlled by the Linux BSP.
P11/22	JB pin 019 NVCC_SD	SD_VCC	NVCC_SD		Supply voltage for SD interface (1.8V or 3.3V). This is an output but should never be used to anything else than the SD interface.
P12/24	JB pin 029 SD-A_DATA1	MMC_D1			Not connected
P13/26	JB pin 027	MMC_D0			Not connected

	SD-A_DATA0		
P14/28	Not connected	MMC_D7	Not connected
P15/30	Not connected	MMC_D6	Not connected
P16/32	JB pin 023 SD-A_CLK	MMC_CLK	Not connected
P17/34	Not connected	MMC_D5	Not connected
P18/36	JB pin 025 SD-A_CMD	MMC_CMD	Not connected
P19/38	Not connected	MMC_D4	Not connected
P20/40	JB pin 033 SD-A_DATA3	MMC_D3	Not connected
P21/42	JB pin 031 SD-A_DATA2	MMC_D2	Not connected
P22/44		GND	
P23/46		HDMI_TXC_N	Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P24/48		HDMI_TXC_P	Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P25/50		GND	
P26/52		HDMI_TXD0_N	Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P27/54		HDMI_TXD0_P	Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P28/56		HDMI_HPD	Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P29/58		HDMI_TXD1_N	Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P30/60		HDMI_TXD1_P	Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P31/62		GND	
P32/64		HDMI_TXD2_N	Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P33/66		HDMI_TXD2_P	Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
P34/68		HDMI_CEC	No connection
P35/70		GND	
P36/72	JB pin 079 ETH_TRXP1	ETH1_MD1_P	Not connected
P37/74	JB pin 081 ETH_TRXN1	ETH1_MD1_N	Not connected
P38/76		GND	
P39/78	JB pin 085 ETH_TRXP0	ETH1_MD0_P	Not connected
P40/80	JB pin 087 ETH_TRXN0	ETH1_MD0_N	Not connected
P41/82	JB pin 073 ETH_LED_1000	ETH1_LINK1000	Not connected
P42/84	JB pin 075 ETH_LED_ACT	ETH1_ACT	Not connected
P43/86	JB pin 071 ETH_LED_10_1	ETH1_LINK	Not connected

	00				
P44/88	JB pin 091 ETH_TRXN3	ETH1_MD3_N			Not connected
P45/90	JB pin 093 ETH_TRXP3	ETH1_MD3_P			Not connected
P46/92		GND			
P47/94	JB pin 097 ETH_TRXN2	ETH1_MD2_N			Not connected
P48/96	JB pin 099 ETH_TRXP2	ETH1_MD2_P			Not connected
P49/98		GND			
P50/100	Not connected	ETH2_MD1_P			Not connected
P51/102	Not connected	ETH2_MD1_N			Not connected
P52/104		GND			
P53/106	Not connected	ETH2_MD0_P			Not connected
P54/108	Not connected	ETH2_MD0_N			Not connected
P55/110	Not connected	ETH2_LINK1000			Not connected
P56/112	Not connected	ETH2_ACT			Not connected
P57/114	Not connected	ETH2_LINK			Not connected
P58/116	Not connected	ETH2_MD3_N			Not connected
P59/118	Not connected	ETH2_MD3_P			Not connected
P60/120		GND			
P61/122	Not connected	ETH2_MD2_N			Not connected
P62/124	Not connected	ETH2_MD2_P			Not connected
P63/126		GND			
P64/128	JB pin 049 USB-A_DN	USB_O1_DN	USB_OTG_DN	No	
P65/130	JB pin 051 USB-A_DP	USB_O1_DP	USB_OTG_DP	No	
P66/132	JB pin 053 USB-A_ID	USB_O1_OTG_ID	PTC13	Yes	
P67/134	Not connected	USB_O1_SSTXN			Not connected
P68/136	Not connected	USB_O1_SSTXP			Not connected
P69/138		GND			
P70/140	Not connected	USB_O1_SSRXN			Not connected
P71/142	Not connected	USB_O1_SSRXP			Not connected
P72/144	JB pin 047 USB-A_VBUS	USB_O1_VBUS	USB_OTG_VBUS	No	
P73/146	JB pin 045 USB-A_PWR	USB_O1_PWR_EN	PTE15	Yes	
P74/148	JB pin 043 USB-A_OC	USB_O1_OC	PTE14	Yes	
150		Non existing pin			
152		Non existing pin			
154		Non existing pin			
156		Non existing pin			

P75/158	JB pin 059 USB-B_PWR	USB_H1_PWR_EN			
P76/160	JB pin 057 USB-B_OC	USB_H1_OC			
P77/162		GND			
P78/164	JB pin 063 USB-B_DN	USB_H1_DN			
P79/166	JB pin 065 USB-B_DP	USB_H1_DP			
P80/168	Not connected	USB_H1_SSTXN			Not connected
P81/170	Not connected	USB_H1_SSTXP			Not connected
P82/172		GND			
P83/174	Not connected	USB_H1_SSRXN			Not connected
P84/176	Not connected	USB_H1_SSRXP			Not connected
P85/178	JB pin 061 USB-B_VBUS	USB_H1_VBUS			
P86/180	JA pin 072 Board specific	USB_H2_PWR_EN	TAMPER_DETECT	No	
P87/182	JB pin 072 ONOFF	USB_H2_OC	PMIC: ONOFF	No	
P88/184		GND			Not connected
P89/186	Not connected	USB_H2_DN			
P90/188	Not connected	USB_H2_DP			Not connected
P91/190		GND			
P92/192	JC pin 015 SD-B_DATA4	COM board specific	PTE13	Yes	
P93/194	JC pin 017 SD-B_DATA5	COM board specific	PTE12	Yes	
P94/196	JC pin 023 SD-B_NRST	COM board specific	PTE6	Yes	
P95/198	Not connected	COM board specific			Not connected
P96/200	Not connected	COM board specific			Not connected
P97/202	Not connected	COM board specific			Not connected
P98/204	Not connected	COM board specific			Not connected
P99/206	Not connected	COM board specific			Not connected
P100/208	Not connected	COM board specific			Not connected
P101/210	Not connected	COM board specific			Not connected
P102/212	Not connected	COM board specific			Not connected
P103/214	Not connected	COM board specific			Not connected
P104/216	Not connected	COM board specific			Not connected
P105/218	Not connected	COM board specific			Not connected
P106/220	Not connected	COM board specific			Not connected
P107/222	Not connected	COM board specific			Not connected
P108/224	Not connected	COM board specific			Not connected
P109/226	Not connected	COM board specific			Not connected
P110/228	JB pin 058 I2C-C_SDA	COM board specific	PTA9	Yes	**Note**: This signal has as 4.7Kohm pullup resistor to an internally generated 3.3V supply.

P111/230	JB pin 056 I2C-C_SCL	COM board specific	PTA8	Yes	**Note**: This signal has as 4.7Kohm pullup resistor to an internally generated 3.3V supply.
P112/232	Not connected	COM board specific			Not connected
P113/234	JB pin 012 GPIO-F	COM board specific	PTA24	Yes	
P114/236	Not connected	COM board specific			Not connected
P115/238	JB pin 062 I2C-D_SDA	COM board specific	PTB13	Yes	**Note**: This signal has as 4.7Kohm pullup resistor to an internally generated 3.3V supply.
P116/240	JB pin 060 I2C-D_SCL	COM board specific	PTB12	Yes	**Note**: This signal has as 4.7Kohm pullup resistor to an internally generated 3.3V supply.
P117/242	JB pin 002 GPIO-A	COM board specific	PTC8	Yes	
P118/244		GND			
P119/246	JB pin 044 SPI-B_SSEL	SPI-B_SSEL	PTC19	Yes	
P120/248	JB pin 042 SPI-B_MOSI	SPI-B_MOSI	PTC17	Yes	
P121/250	JB pin 040 SPI-B_MISO	SPI-B_MISO	PTC16	Yes	
P122/252	JB pin 038 SPI-B_CLK	SPI-B_CLK	PTC18	Yes	
P123/254	JB pin 034 SPI-A_SSEL	SPI-A_SSEL	PTA23	Yes	
P124/256	JB pin 032 SPI-A_MOSI	SPI-A_MOSI	PTA16	Yes	
P125/258	JB pin 030 SPI-A_MISO	SPI-A_MISO	PTA20	Yes	
P126/260	JB pin 028 SPI-A_CLK	SPI-A_CLK	PTA17	Yes	
P127/262		GND			
P128/264	JB pin 013 UART-C_RXD	UART-C_RXD	PTA19	Yes	
P129/266	JB pin 015 UART-C_TXD	UART-C_TXD	PTA18	Yes	
P130/268	JB pin 001 UART-B_RXD	UART-B_RXD	PTE11	Yes	
P131/270	JB pin 009 UART-B_CTS	UART-B_CTS	PTE9	Yes	
P132/272	JB pin 011 UART-B_RTS	UART-B_RTS	PTE8	Yes	
P133/274	JB pin 003 UART-B_TXD	UART-B_TXD	PTE10	Yes	
P134/276	JB pin 005 UART-A_RXD	UART-A_RXD	PTC3	Yes	
P135/278	JB pin 018 GPIO-J	UART-A_CTS	PTC1	Yes	
P136/280	JB pin 016 GPIO-H	UART-A_RTS	PTC0	Yes	
P137/282	JB pin 007 UART-A_TXD	UART.A_TXD	PTC2	Yes	
P138/284	JB pin 004 GPIO-B	PWM	PTC9	Yes	

P139/286	JC pin 019 SD-B_DATA6	GPIO-B	PTE7	Yes	
P140/288	JC pin 021 SD-B_DATA7	GPIO-A	PTC12	Yes	
P141/290	JB pin 068	PERI_PWR_EN	PTA21	No	Enable signal (active high) for carrier board peripheral power supplies. More information about carrier board design can be found in *EACOM Board specification*. This signal is a copy of the on-board generated 3.3V supply.
P142/292	JB pin 074 RESET_IN	RESET_IN	PMIC: RESET_IN/GPIO4		Reset input, active low. Pull signal low to activate reset. There is no need to pull signal high externally.
P143/294		RESET_OUT	Copy of POR_B		Reset (open drain) output, active low. Driven low during reset. Has a 10Kohm pull-up resistor to on-board generated 3.3V supply.
P144/296		VIN_SELECT			This output is connected to VIN via a 1Kohm resistor to signal that supply voltage VIN shall be 4.2V. This is for carrier boards that can support EACOM boards that require 3.3V on VIN (in this case, this pin is connected to ground).
P145/298	JA pin 018 VBAT_RTC	VBAT_RTC			Supply voltage from coin cell battery for keeping PMIC and RTC functioning during standby.
P146/300	JB pin 100 ISP_ENABLE	ISP_ENABLE			Should be left open (will write protect the on-board parameter storage E2PROM), or connected to GND (will enable writes to the on-board parameter storage E2PROM and place the i.MX 7ULP SoC in USB OTG boot mode after a power cycle).
P147/302 P148/304 P149/306 P150/308 P151/310 P152/312 P153/314 P154/316 P155/318 P156/320	JA pin 001 JA pin 002 JA pin 003 JA pin 004 JA pin 005 JA pin 006 JA pin 007 JA pin 008	VIN			Main input voltage supply (4.2V)

The table below lists the bottom side pins, S1-S158, even numbers.

Bottom Side Pin Number	EAuCOM Board	EACOM Board	i.MX 7ULP Ball Name	Alternative pin functions?	Notes
S1/1	JC pin 035 SAI_RXFS	MQS_RIGHT			Not connected
S2/3	JC pin 037 SAI_RXC	MQS_LEFT	PTA22	Yes	
S3/5		GND			
S4/7	JC pin 027 SAI_TXFS	AUDIO_TXFS	PTB2	Yes	
S5/9	JC pin 033 SAI_RXD	AUDIO_RXD	PTB10	Yes	
S6/11	JC pin 031 SAI_TXC	AUDIO_TXC	PTB1	Yes	
S7/13	JC pin 029 SAI_TXD	AUDIO_TXD	PTB3	Yes	
S8/15	JC pin 039 SAI_MCLK	AUDIO_MCLK			Not connected
S9/17		GND			

S10/19	JA pin 080 SPDIF_RX	SPDIF_IN	PMIC: LED2	No	
S11/21	JA pin 078 SPDIF_TX	SPDIF_OUT	PMIC: LED1	No	
S12/23	JB pin 022 GPIO-L	CAN2_TX	PTC7	Yes	
S13/25	JB pin 020 GPIO-K	CAN2_RX	PTC6	Yes	
S14/27	JA pin 074 Board specific	CAN1_TX	A7_POR_B/ RESET1_B	No	
S15/29	JA pin 076 Board specific	CAN1_RX			
S16/31		GND			
S17/33	Not connected	LVDS1_D3_P			Not connected
S18/35	Not connected	LVDS1_D3_N			Not connected
S19/37	Not connected	GPIO-J			Not connected
S20/39	Not connected	LVDS1_D2_P			Not connected
S21/41	Not connected	LVDS1_D2_N			Not connected
S22/43		GND			
S23/45	Not connected	LVDS1_D1_P			Not connected
S24/47	Not connected	LVDS1_D1_N			Not connected
S25/49		GND			
S26/51	Not connected	LVDS1_D0_P			Not connected
S27/53	Not connected	LVDS1_D0_N			Not connected
S28/55		GND			
S29/57	Not connected	LVDS1_CLK_P			Not connected
S30/59	Not connected	LVDS1_CLK_N			Not connected
S31/61		GND			
S32/63	Not connected	LVDS0_D3_P			Not connected
S33/65	Not connected	LVDS0_D3_N			Not connected
S34/67	Not connected	GPIO-H			Not connected
S35/69	Not connected	LVDS0_D2_P			Not connected
S36/71	Not connected	LVDS0_D2_N			Not connected
S37/73		GND			
S38/75	Not connected	LVDS0_D1_P			Not connected
S39/77	Not connected	LVDS0_D1_N			Not connected
S40/79		GND			
S41/81	Not connected	LVDS0_D0_P			Not connected
S42/83	Not connected	LVDS0_D0_N			Not connected
S43/85		GND			
S44/87	Not connected	LVDS0_CLK_P			Not connected
S45/89	Not connected	LVDS0_CLK_N			Not connected
S46/91	JB pin 050 I2C-A_SDA	I2C-A_SDA	PTC5	No	Signal must be I2C5_SDA since the signal is connected to on-board PMIC. **Note**: This signal has as 2.2Kohm pullup resistor to an internally generated 3.3V supply.

S47/93	JB pin 048 I2C-A_SCL	I2C-A_SCL	PTC4	No	Signal must be I2C5_SCL since the signal is connected to on-board PMIC. **Note**: This signal has as 4.7Kohm pullup resistor to an internally generated 3.3V supply.
S48/95	JB pin 054 I2C-B_SDA	I2C-B_SDA	PTF13	Yes	**Note**: This signal has as 4.7Kohm pullup resistor to an internally generated 3.3V supply.
S49/97	JB pin 052 I2C-B_SCL	I2C-B_SCL	PTF12	Yes	**Note**: This signal has as 4.7Kohm pullup resistor to an internally generated 3.3V supply.
S50/99		HDMI/I2C-C_SDA			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
S51/101		HDMI/I2C-C_SCL			Connected to DSI-to-HDMI bridge (ADV7533) on uCOM Adapter
S52/103	JB pin 006 GPIO-C	TP_RST	PTC10	Yes	
S53/105	JA pin 100 Board specific	TP_IRQ	PTF19	Yes	
S54/107	JA pin 098 Board specific	DISP_PWR_EN	PTF18	Yes	
S55/109	JA pin 096 Board specific	BL_PWR_EN	PTF17	Yes	
S56/111	JA pin 094 Board specific	BL_PWM	PTF16	Yes	
S57/113		GND			
S58/115	JA pin 099 Board specific	LCD_R0	PTA2	Yes	
S59/117	JA pin 097 Board specific	LCD_R1	PTA0	Yes	
S60/119	JA pin 095 Board specific	LCD_R2	PTA1	Yes	
S61/121	JA pin 093 Board specific	LCD_R3	PTA7	Yes	
S62/123	JA pin 089 Board specific	LCD_R4	PTA5	Yes	
S63/125	JA pin 087 Board specific	LCD_R5	PTA6	Yes	
S64/127	JA pin 085 Board specific	LCD_R6	PTA4	Yes	
S65/129	JA pin 083 Board specific	LCD_R7	PTA3	Yes	
S66/131	JA pin 079 Board specific	LCD_G0	PTF3	Yes	
S67/133	JA pin 077 Board specific	LCD_G1	PTF2	Yes	
S68/135	JA pin 075 Board specific	LCD_G2	PTF1	Yes	
S69/137	JA pin 073 Board specific	LCD_G3	PTA15	Yes	
S70/139	JA pin 069 Board specific	LCD_G4	PTA13	Yes	
S71/141	JA pin 067 Board specific	LCD_G5	PTA12	Yes	
S72/143	JA pin 065 Board specific	LCD_G6	PTA14	Yes	

S73/145	JA pin 063 Board specific	LCD_G7	PTF0	Yes	
S74/147		GND			
S75/149	JA pin 059 Board specific	LCD_B0	PTF15	Yes	
151		Non existing pin			
153		Non existing pin			
155		Non existing pin			
S76/157	JA pin 057 Board specific	LCD_B1	PTF11	Yes	
S77/159	JA pin 055 Board specific	LCD_B2	PTF10	Yes	
S78/161	JA pin 053 Board specific	LCD_B3	PTF9	Yes	
S79/163	JA pin 049 Board specific	LCD_B4	PTF8	Yes	
S80/165	JA pin 047 Board specific	LCD_B5	PTF7	Yes	
S81/167	JA pin 045 Board specific	LCD_B6	PTF6	Yes	
S82/169	JA pin 043 Board specific	LCD_B7	PTF5	Yes	
S83/171	JA pin 033 Board specific	LCD_CLK	DAC_OUT0	No	
S84/173	JB pin 014 GPIO-G	GPIO-G	PTA31	Yes	
S85/175	JA pin 035 Board specific	LCD_HSYNC	DAC_OUT1	No	
S86/177	JA pin 037 Board specific	LCD_VSYNC	PTF14	Yes	
S87/179	JA pin 039 Board specific	LCD_ENABLE	PTF4	Yes	
S88/181		GND			
S89/183	Not connected	AIN_VREF			Not connected
S90/185	Not connected	AIN7			Not connected
S91/187	Not connected	AIN6			Not connected
S92/189	JA pin 090 Board specific	AIN5	PTB14	Yes	
S93/191	JA pin 088 Board specific	AIN4	PTB11	Yes	
S94/193	JA pin 086 Board specific	AIN3	PTB0	Yes	
S95/195	JA pin 084 Board specific	AIN2	PTC11	Yes	
S96/197	JD pin 019 DSI_DN1	AIN1	DSI_DATA1N	No	
S97/199	JD pin 021 DSI_DP1	AIN0	DSI_DATA1P	No	
S98/201		GND			
S99/203	JD pin 007 DSI_DN0	COM board specific	DSI_DATA0N	No	

S100/205	JD pin 009 DSI_DP0	COM board specific	DSI_DATA0P	No	
S101/207		GND			
S102/209	JD pin 025 DSI_CKN	COM board specific	DSI_CLK_N	No	
S103/211	JD pin 027 DSI_CKP	COM board specific	DSI_CLK_P	No	
S104/213		GND			
S105/215	Not connected	COM board specific			
S106/217	Not connected	COM board specific			
S107/219	Not connected	COM board specific			
S108/221	Not connected	COM board specific			
S109/223	Not connected	COM board specific			
S110/225	Not connected	COM board specific			
S111/227	JB pin 037 SD-A_WP	COM board specific			Not connected
S112/229	JB pin 010 GPIO-E	COM board specific	PTC15	Yes	
S113/231	JB pin 008 GPIO-D	COM board specific	PTC14	Yes	
S114/233	Not connected	CSI_HSYNC			Not connected
S115/235	Not connected	CSI_VSYNC			Not connected
S116/237	Not connected	CSI_MCLK			Not connected
S117/239	Not connected	CSI_PCLK			Not connected
S118/241		GND			
S119/243	Not connected	CSI_D0			Not connected
S120/245	Not connected	CSI_D1			Not connected
S121/247	Not connected	CSI_D2			Not connected
S122/249	Not connected	CSI_D3			Not connected
S123/251	Not connected	CSI_D4			Not connected
S124/253	Not connected	CSI_D5			Not connected
S125/255	Not connected	CSI_D6			Not connected
S126/257	Not connected	CSI_D7			Not connected
S127/259		GND			
S128/261	JD pin 026 CSI_DN3	CSI_D3_M	CSI_D3_M	No	
S129/263	JD pin 028 CSI_DP3	CSI_D3_P	CSI_D3_P	No	
S130/265		GND			
S131/267	JD pin 020 CSI_DN2	CSI_D2_M	CSI_D2_M	No	
S132/269	JD pin 022 CSI_DP2	CSI_D2_P	CSI_D2_P	No	
S133/271		GND			
S134/273	JD pin 014 CSI_DN1	CSI_D1_M	CSI_D1_M	No	
S135/275	JD pin 016	CSI_D1_P	CSI_D1_P	No	

	CSI_DP1				
S136/277		GND			
S137/279	JD pin 008 CSI_DN0	CSI_D0_M	CSI_D0_M	No	
S138/281	JD pin 010 CSI_DP0	CSI_D0_P	CSI_D0_P	No	
S139/283		GND			
S140/285	JD pin 002 CSI_CKN	CSI_CLK_M	CSI_CLK_M	No	
S141/287	JD pin 004 CSI_CKP	CSI_CLK_P	CSI_CLK_P	No	
S142/289		GND			
S143/291	Not connected	SATA_TX_P			Not connected
S144/293	Not connected	SATA_TX_N			Not connected
S145/295		GND			
S146/297	Not connected	SATA_RX_N			Not connected
S147/299	Not connected	SATA_RX_P			Not connected
S148/301		GND			
S149/303		GND			
S150/305	JD pin 039 PCIE_CLKP	PCIE_CLK_P			Not connected
S151/307	JD pin 037 PCIE_CLKN	PCIE_CLK_N			Not connected
S152/309		GND			
S153/311	JD pin 040 PCIE_TXP	PCIE_TX_P	USB_HSIC_STROBE	No	
S154/313	JD pin 038 PCIE_TXN	PCIE_TX_N	USB_HSIC_DATA	No	
S155/315		GND			
S156/317	JD pin 034 PCIE_RXP	PCIE_RX_P			Not connected
S157/319	JD pin 032 PCIE_RXN	PCIE_RX_N			Not connected
S158/321		GND			

5 Pin Mapping

5.1 Functional Multiplexing on I/O Pins

There are a lot of different peripherals inside the i.MX 7ULP SoC. Many of these peripherals are connected to the IOMUX block, that allows the I/O pins to be configured to carry one of many (up to nine different) alternative functions. This leave great flexibility to select a function multiplexing scheme for the pins that satisfy the interface need for a particular application.

Some interfaces with specific voltage levels/drivers/transceivers have dedicated pins, like MIPI-DSI, MIPI-CSI and USB. i.MX 7ULP pins carrying these signals do not have any functional multiplexing possibilities. These interfaces are fixed.

To keep compatibility between EACOM boards the EACOM specified pinning should be followed, but in general there are no restrictions to select alternative pin multiplexing schemes on the *iMX7ULP uCOM Board*. Note that all EACOM-defined pins are not connected on some EACOM boards, typically because an interface is not supported or there are not enough free pins in the SoC. Further, some EACOM board pins are *type specific*, meaning that these pins might not be compatible with other EACOM boards. Using *type specific* pins may result in lost compatibility between EACOM boards, but not always. Always check details between EACOM boards of interest.

If switching between EACOM boards is not needed, then pin multiplexing can be done without considering the EACOM pin allocation. A custom carrier board design is needed in this case.

Functional multiplexing is normally controlled via the Linux BSP. It can also be done directly via register `IOMUXC_SW_MUX_CTL_PAD_xxx` where `xxx` is the name of the i.MX 7ULP pin. For more information about the register settings, see the *i.MX 7ULP Application Processor Reference Manual* from NXP.

Note that input functions that are available on multiple pins will require control of an input multiplexer. This is controlled via register `IOMUXC_xxx_SELECT_INPUT` where `xxx` is the name of the input function. Again, for more information about the register settings, see the *i.MX 7ULP Application Processor Reference Manual* from NXP.

5.1.1 Alternative I/O Function List

There is an accompanying Excel document that lists all alternative functions for each available I/O pin. The reset state is shown as well as the EACOM function allocation. The reset state is typically GPIO, ALT5 function, except for the GPIO1_IO01-15 signals that are ALT0 functions, but that is the GPIO function.

5.2 I/O Pin Control

Each pin also has an additional control register for configuring input hysteresis, pull up/down resistors, push-pull/open-drain driving, drive strength and more. Also in this case, configuration is normally done via the Linux BSP but it is possible to directly access the control registers, which are called `IOMUXC_SW_PAD_CTL_PAD_xxx` where `xxx` is the name of the i.MX 7ULP pin. For more information about the register settings, see the *i.MX 7ULP Application Processor Reference Manual* from NXP.

As a general recommendation, select slow slew rate and lowest drive strength (that still result in acceptable signal edges for the system) in order to reduce problems with EMC.

Note that after reset many pins (but not all) are configured as GPIO inputs, some with 20-50Kohm pull-down resistor and some without. Some pins are configures as Hi-Z outputs. When the bootloader (typically u-boot) executes it is possible to reconfigure the pins.

6 Interface Description

This chapter presents the different interfaces. The **i.MX 7ULP datasheet and user manual shall always be consulted** for details about different functions and interfaces. Many interfaces are multiplexed on different pins and not available simultaneously. There is an accompanying Excel document that lists all alternative functions for each available I/O pin. It is recommended to study this document to get an overview of the available pin multiplexing options.

The process of defining the pin/function for a system is:

1. Define which interfaces are needed in the system.
2. Allocate each needed interface to either Cortex-A7 or M4 side.
3. Consult the Excel sheet and allocate the interfaces to different pins.
    a. The i.MX7ULP SoC architecture and associated BSP promote the following port allocation:
        i. Ports A and B are used by the Cortex-M4 core.
        ii. Ports C, E and F are used by the Cortex-A7 core.
    b. Note that ports B and E have 1.8V logic level while the rest have 3.3V logic level. Only a few pins of port B are available for external use. Most of them are used internally.
    c. Note that most of port E is used if on-board Wi-Fi/BT module is mounted.
    d. If possible, follow the EAuCOM pin and interface allocation. It is not strictly needed, but will simplify if the uCOM board will be replaced in a future update/upgrade.
4. When an suitable pin/function allocation has been done, update the *.dts file under Linux to enable the interfaces that shall be controlled from the A7/Linux side. On the M4 side, peripherals are enabled and initialized via function calls, see the SDK for details.
    a. If pin/function allocation is impossible, the basic architecture under 1) must be reexamined and updated.

6.1 EAuCOM Standard Pin and Interface Allocation

The table below lists the standard pin and interface allocation according to the EAuCOM standard.

EAuCOM Interface	i.MX 7ULP Signal Allocation	Peripheral	Port Side	Remarks
UART-A	PTC2/3	UART4	A7	Typically used as console for the A7 core.
UART-B	PTE8/9/10/11	UART6	A7	UART-B definition also includes RTS/CTS. Typically used UART interface for BT (Bluetooth) interface.
UART-C	PTA18/19	UART0	M4	Typically used as console for the M4 core.
SPI-A	PTA16/17/20/23	LPSPI0	M4	
SPI-B	PTC16/17/18/19	LPSPI3	A7	
I2C-A	PTC4/5	LPI2C5	A7	
I2C-B	PTF12/13	LPI2C7	A7	
I2C-C	PTA8/9	LPI2C2	M4	
I2C-D	PTB12/13	LPI2C3	M4	Voltage signaling level is 3.3V even though port B has 1.8V logic level. There is an on-board voltage translator.

I2S	PTB1/2/3/10	I2S1	M4

The more complex interfaces, like USB, SD, MIPI and camera input are all allocated for the A7 side.

The following sections present interfaces that requires some additional comments.

6.2 Display Interface

The i.MX 7ULP SoC only has a MIPI-DSI display output. If a display is needed and the display has a MIPI-DSI interface then the two interfaces can be connected directly. Alternatively, a MIPI-DSI to HDMI or MIPI-DSI to LVDS bridge is used to connect to a display with HDMI or LVDS interface.

The MIPI-DSI interface with two data lanes is allocated to connector JD, see the fourth table in section 3.2 .

The *uCOM Adapter Board* has a MIPI-DSI to HDMI bridge that is connected to the MIPI-DSI interface of the i.MX7ULP SoC by default. The HDMI connector on the *COM Carrier Board* will carry the HDMI display output.

See section 13.3 for a special note about COM Carrier Board versions and how the HDMI DDC I2C channel is connected.

6.3 JTAG

This section lists signals related to the JTAG debug interface.

The i.MX 7ULP SoC has a module called System JTAG Controller (SJC) that provides a JTAG interface to internal logic, including the ARM Cortex-A7 core and Cortex-M4 core. The SJC complies with JTAG TAP standards. The i.MX 7ULP SoC use the JTAG port for production, testing, and system debugging.

The i.MX 7ULP JTAG interface is located on the following pins on connector JB.

JB Pin Number	EAuCOM Board Signal	i.MX 7ULP Ball Name	Alternative Pin Function?	Notes
JB pin 70	POR_B	POR_B		Connected to RESET0_B on the i.MX 7ULP SoC. Signal shall normally only be used to connect to debug interface connector. Signal has a 10K ohm pull-up resistor. Since the voltage level of POR_B is 1.8V, a level translator must be implemented. See the *uCOM Adapter Board* schematic for a reference design.
JB pin 82	JTAG_VCC	VDD_PTA		The supply voltage of the JTAG debug interface. Is connected to the supply voltage of PTA (default is 3.3V).
JB pin 86	JTAG_TCK	PTA29	Yes	Signal has a 10K ohm pull-down resistor.
JB pin 88	JTAG_TMS	PTA26	Yes	
JB pin 90	JTAG_TDI	PTA28	Yes	
JB pin 92	JTAG_TDO	PTA27	Yes	
JB pin 94	JTAG_TRST	PTA30	Yes	

The JTAG signals are not available on the MXM3 edge connector. Instead the signals are available via a 10 pos FPC connector, see picture below for location and orientation.

When using the the *uCOM Adapter Board*, there is a 10 pos FPC connector that is used on all EACOM boards for JTAG access, see picture below for location and orientation.

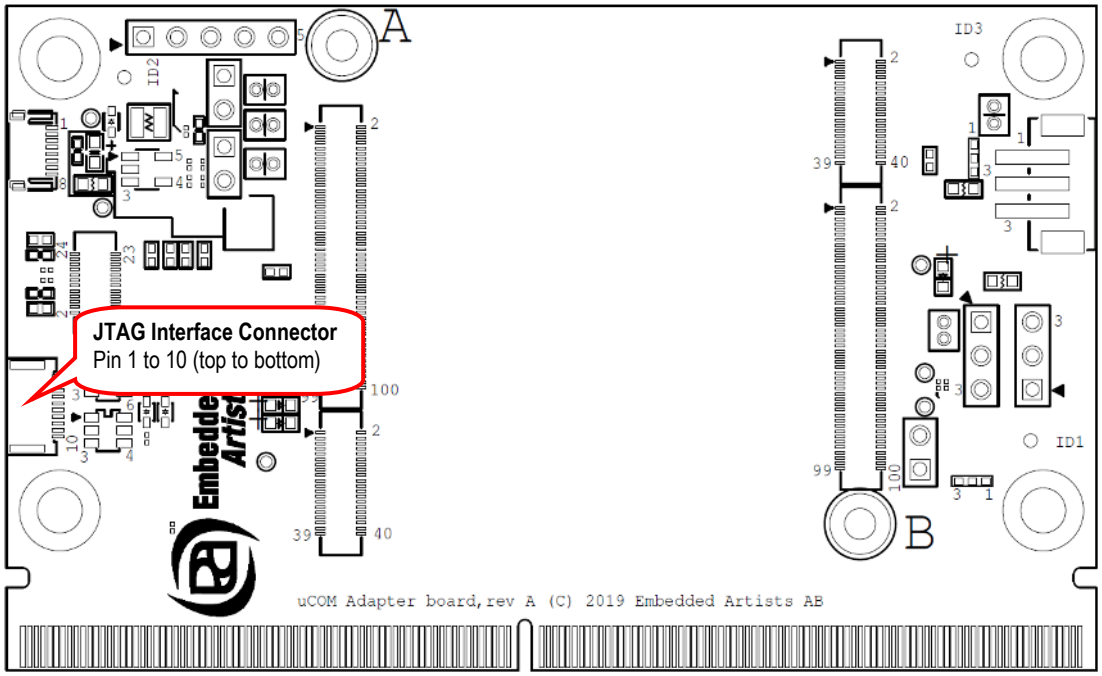


Figure 5 – uCOM Adapter Board, Location of JTAG Interface Connector

The table below lists the 10 signals on the JTAG connector.

JTAG connector Pin Number	Connected to i.MX 7ULP Ball Name	I/O	Description	Remarks
1	VDD_PTA	O	NVCC_JTAG Logic level supply voltage	Used by external debugger to detect logic level to use for signaling. Typically 3.3V.
2	PTA26-JTAG_TMS	I	JTAG signal TMS	
3			Ground	
4	PTA29-JTAG_TCK	I	JTAG signal TCK	Signal has a 10K ohm pull-down resistor.
5			Ground	
6	PTA27-JTAG_TDO	O	JTAG signal TDO	
7		I	JTAG_MOD	Not connected
8	PTA28-JTAG_TDI	I	JTAG signal TDI	
9	PTA30-JTAG_TRST	I	JTAG signal TRST	
10	POR_B	I	System reset	Signal is active low and controls internal system reset. Signal has a 10K ohm pull-up resistor.

There is on-board ESD protection of the JTAG interface, but it is still important to observe ESD precaution when connecting to this interface. There is no need for external pull-up or pull-down resistors.

The *iMX7ULP Developer's Kit* contains an adapter board for connection to common debug connectors. The 10 pos connector is Molex 512811094 and has 0.5 mm (20 mil) pitch. FPC length should be kept less than 7 cm.

6.4 USB

The i.MX 7ULP SoC has two USB interfaces, one normal and one HSIC interface.

The *COM Carrier Board* (that is part of the *iMX 7ULP uCOM Developer's Kit*) connects the first USB interface to a USB OTG interface and the second to a USB hub. In order to make use of the two USB interfaces (OTG and HOST, respectively) the *uCOM Adapter Board* has a USB multiplexor that either connects the i.MX 7ULP SoC USB interface to the OTG or HOST interface. Slider S3:8 control the USB multiplexor. Slider S3 can be found on the bottom side of the *uCOM Adapter Board*, see picture below.

In position OFF the i.MX 7ULP USB interface is connected to the USB OTG connector and in position ON it is connected to the USB HOST (hub) interface.

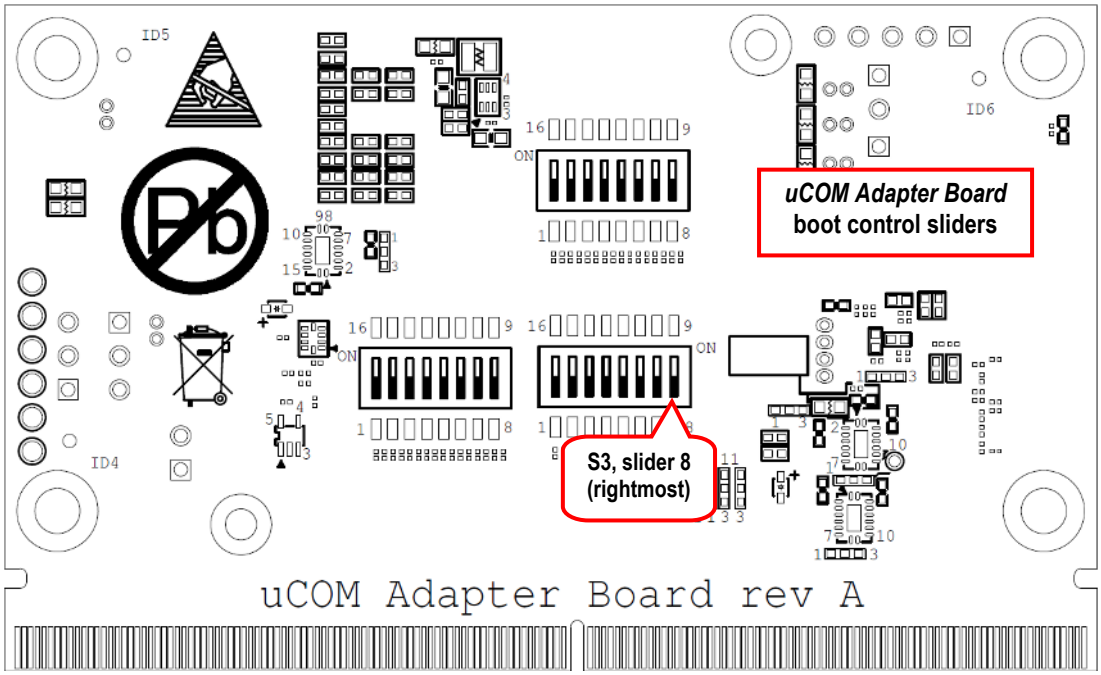


Figure 6 – uCOM Adapter Board, Bottom Side

Note that signals PTE14 and PTE15 have been allocated according to the EAuCOM standard to be USB_OTG_OC and USB_OTG_PWR, respectively. Configure these pins as GPIOs (instead of the alternative USB functions) in the Linux *.dts file.

Note that when the USB interface is connected to the USB Host interface (and hence the USB hub on the *COM Carrier Board*) the *uCOM Adapter Board* rev A does not pull USB1_ID low. This is needed in order for the USB Hub to be detected. A solution to this issue is to connect a USB-A to USB-micro cable in the USB OTG connector on the COM Carrier Board. This cable will by itself pull the ID pin low.

This issue has been corrected on the *uCOM Adapter Board* rev A1, which do pull signal USB1_ID low when USB2 interface has been selected by placing slider 3:8 in ON position.

7 Boot Control

This chapter presents the different boot settings that the *iMX7ULP uCOM Board* supports.

The i.MX 7ULP SoC has two boot-ROMs; one running on the Cortex-A7 core and another one on the Cortex-M4 core. The boot ROM supports the following boot devices/sources:

- QuadSPI flash for M4 ROM
- eMMC (or SD) for A7 ROM

The M4 core always starts first and holds off the A7 core until the M4 core determines the next step in the boot process. The default boot flow is "Dual Memory Boot", which means that the M4 loads from the QSPI flash and the A7 starts (kicked by M4 boot-ROM) loading from the eMMC.

During development the default boot is controlled by slider switches, see section 0for details. In an end product environment it is common to control the boot process by programming the OTP fuses.

The *iMX7ULP uCOM Board* supports booting (i.e., from where the i.MX 7ULP SoC starts downloading code to start executing from) from different sources:

1. On-board eMMC/QSPI Flash in "Dual Memory Boot", which is the default
2. USB OTG download (also called 'serial download') that only boots the A7 core
3. Other sources, like external SD/MMC memory cards, etc.
   Note that the OTP fuses must be programmed to set the specific source.

Two signals controls the booting source/process, BOOT_CTRL and ISP_ENABLE, see table below:

Boot source	BOOT_CTRL	ISP_ENABLE
Boot from on-board eMMC (A7) and QSPI (M4) The board boots according to the default settings of signals PTA0-PTA15 and PTF1 - PTF11, which have been setup to boot from eMMC/QSPI in "Dual Memory Boot" mode. Note that these signals may not be driven externally during just after reset. The reason why the pins must not be driven externally is that on-board resistors pull these signals high/low to select eMMC/QSPI booting. Driving any of these signals can change this default behavior. **If any of the signals are driven externally the on-chip OTP fuses must be programmed to control the boot operation.**	LOW (grounded) J27 shorted	Floating J2 open
Boot according to OTP fuses (eFuses) • Any boot mode supported by the i.MX 7ULP SoC and the hardware connected to it can be selected. See *i.MX7ULP Applications Processor Reference Manual* for details about available sources and OTP fuse settings. • Note that OTP fuse BT_FUSE_SEL must be set to 1 in order to have OTP fuse settings controlling boot source. If not set to 1, the USB OTG boot mode (aka "Serial download") is activated. • Programming OTP fuses is a critical operation. If wrong fuses are programmed boards will likely become unusable and there is no recovery. • Note that *iMX7ULP uCOM Boards* are delivered without	Floating J27 open	Floating J2 open

programmed on-chip OTP fuses. Users have full control over these.		
USB OTG on A7 side (M4 is idle) This is known as "Serial Download" or "Recovery" mode. This mode is used during development and in production to download the first stage bootloader. It is typically not used by the end-product during normal operation. This mode is activated by pulling signal ISP_ENABLE low regardless of signal BOOT_CTRL.	Do not care	LOW (grounded) J2 shorted

To summarize:

1. **The *iMX7ULP uCOM board* is setup to boot from eMMC/QSPI in "Dual Memory Boot" mode as default. If another source is needed, program the OTP fuses.**
   Leave signal ISP_ENABLE floating and BOOT_CTRL grounded for this mode.
2. **If using the default setup ("Dual Memory Boot" from eMMC/QSPI), make sure the boot control pins (PTA0-PTA15 and PTF1 - PTF11) are not driven externally.**
3. If signal ISP_ENABLE is pulled low (grounded), the i.MX 7ULP SoC boots into USB OTG mode. This mode it typically used during development and also during production (when the program images shall be downloaded the first time). **It is recommended to add a feature on the custom carrier board so that pin ISP_ENABLE can be optionally grounded.**
4. To boot from OTP fuses, leave signal BOOT_CTRL floating and program OTP fuses.

7.1 COM Carrier Board Boot Control Jumpers

This section describes where to find the two boot control jumpers on the COM Carrier Board. Note that J27 only exist on COM Carrier Board rev E, or later.

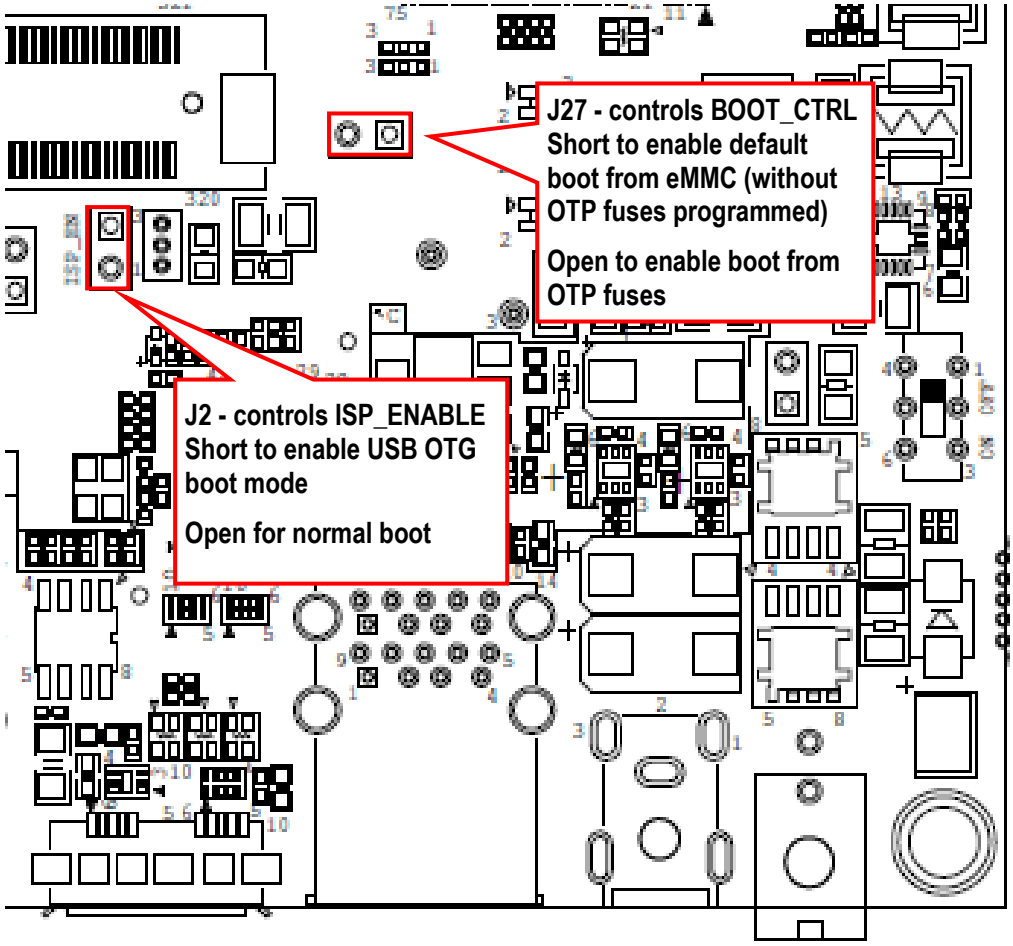


Figure 7 – COM Carrier Board rev E/E1, Boot Control Jumpers

7.2 uCOM Adapter Board Boot Sliders

This section describes how to set the slider switches on the uCOM Adapter Board bottom side for correct boot control.

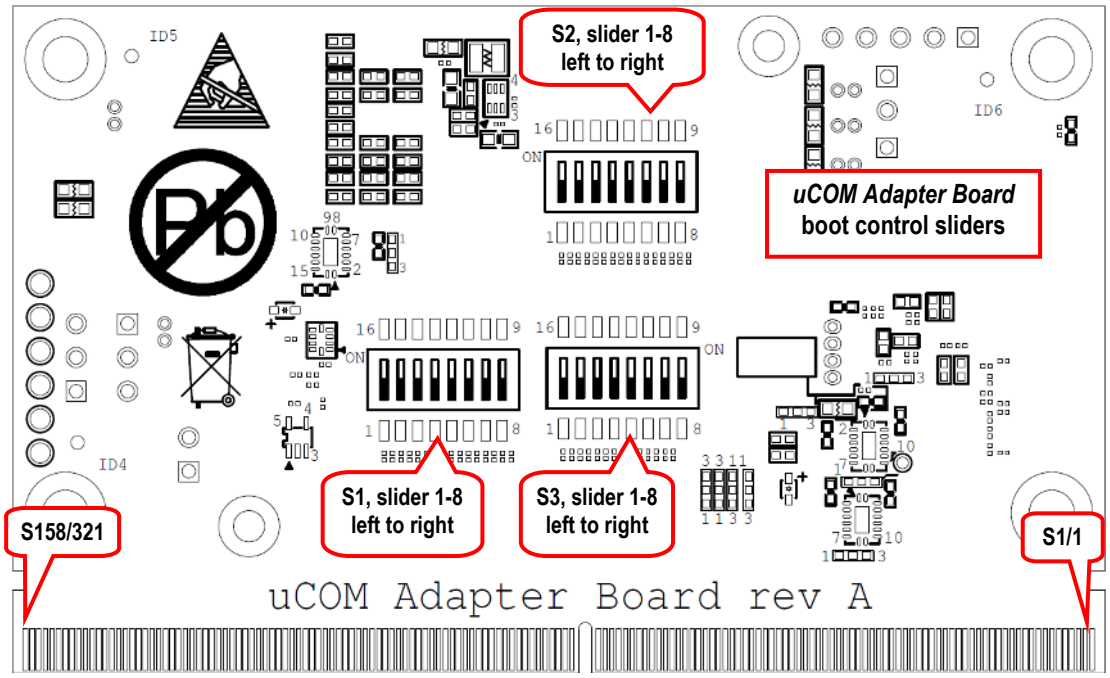


Figure 8 – uCOM Adapter Board Slider Numbering, Bottom Side

Slider Switch	Boot config pin	Default	Description (ON = upper position in Figure 8, OFF = lower position)
S1: 1	BT1_CFG4 (PTF4)	OFF	OFF
S1:2	BT1_CFG5 (PFT5)	OFF	OFF
S1:3	BT1_CFG6 (PFT6)	ON	ON
S1:4	BT1_CFG7 (PFT7)	OFF	OFF
S1:5	BT1_CFG8 (PFT8)	OFF	OFF: uSDHCx device type is eMMC ON: uSDHCx device type is SD card
S1:6	BT1_CFG9 (PFT9)	OFF	OFF: Boot from uSDHC0 (on-board eMMC) ON: Boot from uSDHC1
S1:7	BT1_CFG10 (PFT10)	OFF	OFF
S1:8	BT1_CFG11 (PFT11)	OFF	OFF
S2:1	BT0_CFG14 (PTA14)	OFF	OFF
S2:2	BT0_CFG12 (PTA12)	OFF	OFF
S2:3	BT0_CFG13 (PTA13)	OFF	OFF
S2:4	BT0_CFG15 (PTA15)	OFF	OFF
S2:5	BT1_CFG1 (PTF1)	OFF	OFF
S2:6	BT1_CFG2 (PTF2)	OFF	OFF

S2:7	BT1_CFG3 (PTF3)	OFF	OFF
S2:8	BT0_CFG3 (PTA3)	OFF	OFF
S3:1	BT0_CFG4 (PTA4)	OFF	OFF
S3:2	BT0_CFG6 (PTA6)	OFF	OFF
S3:3	BT0_CFG5 (PTA5)	OFF	OFF
S3:4	BT0_CFG7 (PTA7)	OFF	OFF
S3:5	BT0_CFG1 (PTA1)	ON	ON: Dual Memory Boot: Boot A7 from eMMC/SD and M4 from QSPI OFF: Single Memory Boot (if BT0_CFG0 = OFF), where both A7 and M4 boot image is stored on eMMC/SD flash
S3:6	BT0_CFG0 (PTA0)	OFF	Low-Power Boot OFF: Dual Memory Boot = No low-power boot ON: Boot M4 from QSPI, with A7 on demand
S3:7	BT0_CFG2 (PTA2)	OFF	OFF
S3:8	USB_SELECT	OFF	OFF: USB-A on uCOM connected to USB-1 (OTG) ON: USB-A on uCOM connected to USB-2 (HOST)

8 Powering and PMIC Integration

The i.MX 7ULP SoC is tightly integrated with the PMIC (BD70528MWV) in order to achieve high-performance and low-power operation of the *iMX7ULP uCOM Board*. The BD70528MWV PMIC is an ultra-low Iq design for (optionally) battery powered systems. It also includes a real-time clock. There are other functions as well that are not directly used on the *iMX7ULP uCOM Board*, but rather left as an option for the board integration to utilize. The optional functions of the PMIC are:

- 1S LiPo battery charger with scalable charge currents (10-500mA), supporting Temperature Battery Charging Profile with thermal control of charging current and voltage settings
- Dual input power-path with battery charger, USB VBUS and +5V wall socket
- Dual (white) LED programmable current sources
- Voltage Measurement for Thermistor
- Battery Monitoring
- Voltage regulators that can be used to power the carrier board electronics

See the BD70528MWV datasheet for details about each function.

The PMIC has multiple linear and DC/DC voltage regulators. Some are available for the carrier board design, reducing integration cost. Designs with moderate power consumptions may not need any external power supply at all. Everything can be handled by the on-board PMIC. Section 8.1 presents the available power rails.

There are two ways to power the *iMX7ULP uCOM Board* - with, or without, using a rechargeable Li-ion battery:

- See section 8.2 for a description how to power the *iMX7ULP uCOM Board* without adding a rechargeable Li-ion battery to the design.
- For battery powered applications, see section 8.3 for a description how to make the integration.

8.1 Available Power Supply Rails

The table below presents the available power rails that can be used on the carrier board that the *iMX7ULP uCOM Board* is integrated on.

Power Rail Output	Description	Voltage Range	Max Current
NVCC_3V3 **on JA pins 20/22/24/26/28/30**	3.3V for external use.	3.3V	500mA
NVCC_1V8 **on JA pins 19/21/23/25/27/29**	1.8V for external use.	1.8V	200mA
VLDO3 **on JA pin 17**	LDO3 on PMIC. Startup as disabled. Must be enabled during run-time.	1.65 to 3.3V in 50-100mV steps	200mA
PMIC_LED1 **on JA pin 78**	Programmable current source for LED, typically used on display backlight.	Up to 5.5V on LED anode	300mA
PMIC_LED2 **on JA pin 80**	Programmable current source for LED, typically used on display backlight.	Up to 5.5V on LED anode	300mA

Note that each pin on the Hirose DF40C expansion connectors can carry 300mA maximum. Connect to all pins on the expansion connectors that carry a specific power rail. High current power rails have more than one pin.

Note that external load variations can affect the PMIC operation and potentially disturb the i.MX 7ULP SoC operation. Make sure that the carrier board electronics does not have abrupt consumption variations and does not generate noise on the power rails. Also **calculate the heat dissipation** of the PMIC in case the carrier board has high current consumption.

8.2 Integration without Battery

This setup is very simple. An external 3.45-5.5V supply is basically all that is needed.

- Supply the 3.45-5.5V input voltage to **VSYS_4V2** (connect to all eight pins on connector JA)
- There is no need to supply a 3.3V input voltage to **VBAT_RTC_IN** to power the real-time clock (RTC) and keep it running. The RTC is powered from VSYS_4V2 supply input.
- Leave signals BAT_TEMP, BAT_CURRP and BAT_CURRN unconnected.
- Leave supply inputs PSU_5V on JA pin 54/56/58/60 and VBUS_USB on JA pin 62/64/66/68 unconnected.

8.3 Integration with 1S LiPo Rechargeable Battery

This setup is also simple and straight forward.

- Connect the positive terminal of the 1S LiPo battery to VSYS_4V2 (connect to all eight pins on connector JA). The nominal battery voltage is 3.7V but can be up to 4.2V when fully charged.
- Connect the negative terminal of the 1S battery to ground.
- Connect BAT_TEMP (JA pin 48) to the 1S battery temperature connector. Also connect a 100Kohm NTC thermistor (see BD70528MWV datasheet for details) between BAT_TEMP and ground.
- Connect pin BAT_CURRP (JA pin 50) to the positive terminal of the 1S battery. Do not share the same wire as the connection to VSYS_4V2.
- Select one or both solutions below for charging:
    - To support USB charging, connect USB VBUS of the USB input connector to signals VBUS_USB on JA pin 62/64/66/68 (all five pins shall be connected).
    - To support charging from an external +5V supply, connect the input supply to signals PSU_5V on JA pin 54/56/58/60 (all five pins shall be connected). See BD70528MWV datasheet for details about possible need for input ripple filter.
- There is no need to supply a 3.3V input voltage to **VBAT_RTC_IN** to power the real-time clock (RTC) and keep it running. The RTC is powered from VSYS_4V2 supply input.

See the BD70528MWV datasheet for details about the battery charger functionality and programmable options.

9 Power Modes

One of the primary features of the i.MX7ULP SoC is ultra-low power consumption. Several low-power techniques are implemented to enable power efficient applications:

- Multiple power domains and low-power modes, allowing applications to optimize power consumptions when possible
- Voltage and frequency scaling in dynamic operating modes
- Software-controlled clock gating for cores and peripherals
- Efficient on-chip LDO regulators and power management control

There are two main power domains that are completely separate:

- Application domain, Cortex-A7 core, typically running a feature rich OS like Linux
- Real-time domain, Cortex-M4 core, typically running a responsive real-time operating system like FreeRTOS

Either domain can be placed in several different power modes almost completely independently. Both domains can access the clock and power management system. The *iMX7ULP uCOM Board* is designed for Dual-memory Boot, which means that it is the M4 core that is the primary core that controls the power modes. The A7 core is the secondary core.

The two domains complement each other. An application will have Application Processor performance when needed, typically during short periods of time, and MCU low-power during the rest of the time, which is typically the majority of the time. This creates a very power efficient application. The table below lists a common scenario for many applications.

Activity	Duration	A7 core	M4 core	Comment
User interaction, communication , graphics or heavy computing	Short periods of time.	RUN mode	RUN mode	The A7 core runs at top speed when needed, but can go into power save modes.
Monitor/sample sensors	Repetitive short periods of time (sample period or interrupt trigged). Background task executed more frequently than above.	Low-power mode	RUN mode	Most silicon can be shut down while M4 is still executing.
Deep sleep	Long periods of time.	Low-power mode	Low-power mode	Main objective is to save power so that application can be battery operated.

In addition, there are two more power domains that maintain power on for specific logics in very low power modes:

- VBAT that supplies a small, very low leakage piece of logic that contains a RTC, wake-up logic, temperature and voltage sensors, and a small amount of memory.
- DGO that contains analog comparators and internal reference clocks.

The PMIC (BD70528MWV) has very low Iq. It's real-time clock and wakeup logic has lower Iq than the i.MX 7ULP VBAT domain, so it is the PMIC that handles the real-time clock (32.768 kHz) and wake up logic. The VBAT domain is not powered in lowest power save mode.

The PMIC generates 3.3V, 1.8V and 1.2V that are always on. All ports are always powered (since the power saving when not powering them is minimal).

The i.MX 7ULP provides on-chip LDO regulators to support DVFS on the M4 core and the A7 core. The M4 core always uses the internal LDO to provide power to the core logic in the Real-Time Domain. The A7 core also uses the internal LDO (LDO Enabled mode). **Note that A7 HSRUN mode is not supported on the A7 in LDO Enabled Mode**. Maximum core frequency on the A7 is 500 MHz.

The details of the different power modes (including allowed power modes between the two cores) can be found in the following documents:

- IMX7ULPRM, i.MX 7ULP Applications Processors Reference Manual, latest revision
- AN12573, i.MX 7ULP Power Consumption Measurement, latest revision

10 Murata 1LV Wi-Fi/BT Module Mounting Option

There is a mounting option for the iMX7ULP uCOM board where a very low-power Wi-Fi/BT module, 1LV from Murata is mounted. The picture below illustrates where the 1LV module is mounted in the board. The two u.fl. antenna connectors are located in the lower left corner.

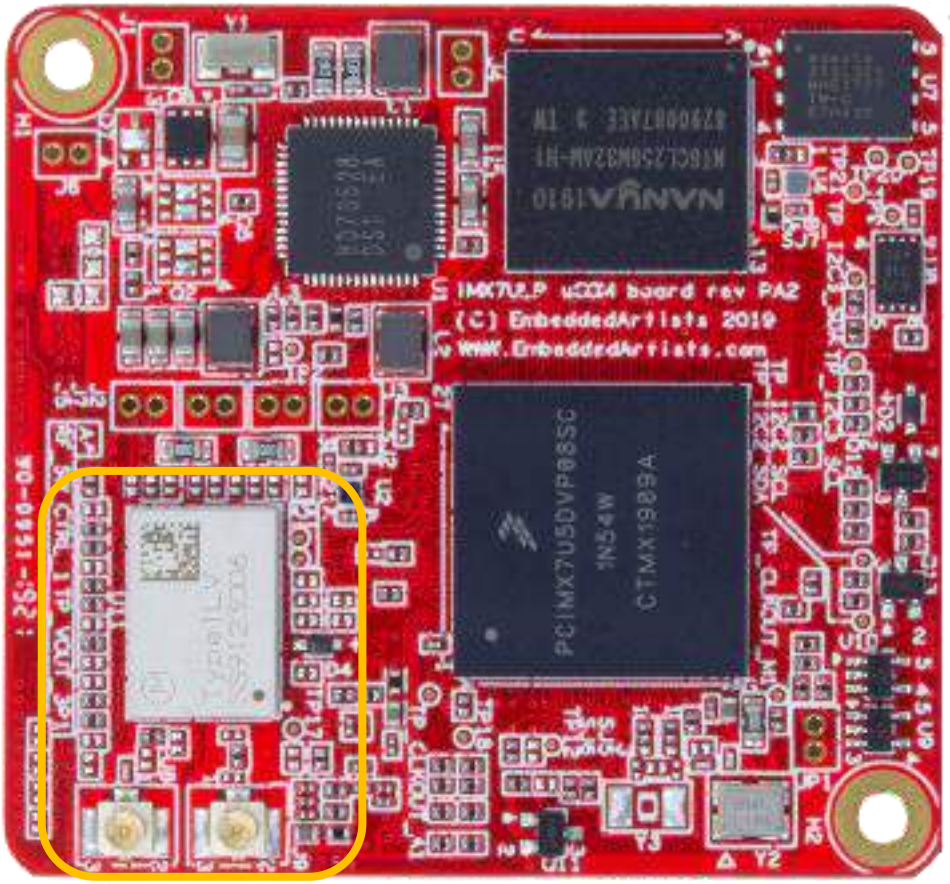


Figure 9 – 1LV Wi-Fi/BT Module Mounted on iMX7ULP uCOM Board

With this mounting option, JC is not mounted. The signals available on this connector are all used to connect to the 1LV Wi-Fi/BT module.

The 1LV Wi/Fi module is powered by default from the on-board generated 3.3V (from PMIC BUCK1). There is mounting option that allows for the Wi-Fi/BT module to be powered from an external 3.3-3.6V supply. Contact Embedded Artists for further information.

Note that this version is not a stocked mounting option. A minimum order quantity (MOQ) will apply. Contact Embedded Artists for further information.

11 Technical Specification

11.1 Absolute Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Stress above these limits may cause malfunction or permanent damage to the board.

Symbol	Description	Min	Max	Unit
VIN	Main input supply voltage	-0.3	5.5	V
VBAT	RTC supply voltage	-0.3	5.5	V
VIO	Vin/Vout (I/O VDD + 0.3): 3.3V IO	0	3.6	V
	Vin/Vout (I/O VDD + 0.3): 1.8V IO	0	1.98	V
USB_xx_VBUS	USB VBUS signals	-0.3	5.25	V
USB_xx_DP/DN	USB data signal pairs	-0.3	3.63	V

11.2 Recommended Operating Conditions

All voltages are with respect to ground, unless otherwise noted.

Symbol	Description	Min	Typical	Max	Unit
VIN	Main input supply voltage Ripple with frequency content < 10 MHz Ripple with frequency content ≥ 10 MHz	3.45	4.2	5.0 50 10	V mV mV
VBAT	RTC supply voltage **Note:** This voltage must remain valid at all times for correct operation of the board (including, but not limited to the RTC).	3.0	3.3	5.5	V
USB_xx_VBUS	USB VBUS signals		5	5.25	V

11.3 Power Ramp-Up Time Requirements

Input supply voltages (VIN and VBAT) shall have smooth and continuous ramp from 10% to 90% of final set-point. Input supply voltages shall reach recommended operating range in 1-20 ms.

11.4 Electrical Characteristics

For DC electrical characteristics of specific pins, see i.MX 7ULP Datasheet. The internal VDD operating point for GPIOs is 3.3V for all signals except for signals belonging to port B (PTB), which has 1.8V logic level.

11.4.1 Reset Output Voltage Range

The reset output is an open drain output with a 1500 ohm pull-up resistor to VIN. Maximum output voltage when active is 0.4V.

11.4.2 Reset Input

The reset input is triggered by pulling the reset input low (0.2 V max) for 10 uS minimum. The internal reset pulse will be 140-560 mS long, before the i.MX 7ULP boot process starts.

11.5 Power Consumption

There are several factors that determine power consumption of the *iMX7ULP uCOM Board*, like input voltage, operating temperature, LPDDR3 activity, operating frequencies for the different cores, DVFS levels and software executed (i.e., Linux distribution).

The values presented are typical values and should be regarded as an estimate. Always measure current consumption in the real system to get a more accurate estimate.

Symbol	Description (VIN = 4.2V, Toperating = 25°C)	Typical	Max Observed	Unit
I_{VIN}_MAX	Maximum CPU load, 500MHz ARM frequency, without Ethernet		TBD	mA
I_{VIN}_IDLE	System idle state, uBoot prompt Linux prompt		TBD TBD	mA
I_{VIN}_DSM	Deep-Sleep mode (DSM), aka "Dormant mode" or "Suspend-to-RAM" in Linux BSP	TBD		mA
I_{VIN}_STB	Linux standby	TBD		mA
I_{VBAT}_BACKUP	Current consumption to keep internal RTC running	TBD		uA

11.6 Mechanical Dimensions

The table below presents the mechanical dimensions of the module.

Dimension	Value (±0.1 mm)	Unit
Module width	42	mm
Module height	45	mm
Module top side height	2.0	mm
Module bottom side height	1.4	mm
PCB thickness	1.4	mm
Mounting hole diameter	2.3	mm
Module weight	2 ±0.5 gram	gram

The picture below shows the mechanical details of the *iMX7ULP uCOM Board*. The outer measurement is 42 x 45 mm. Note that the picture is seen from the bottom side.

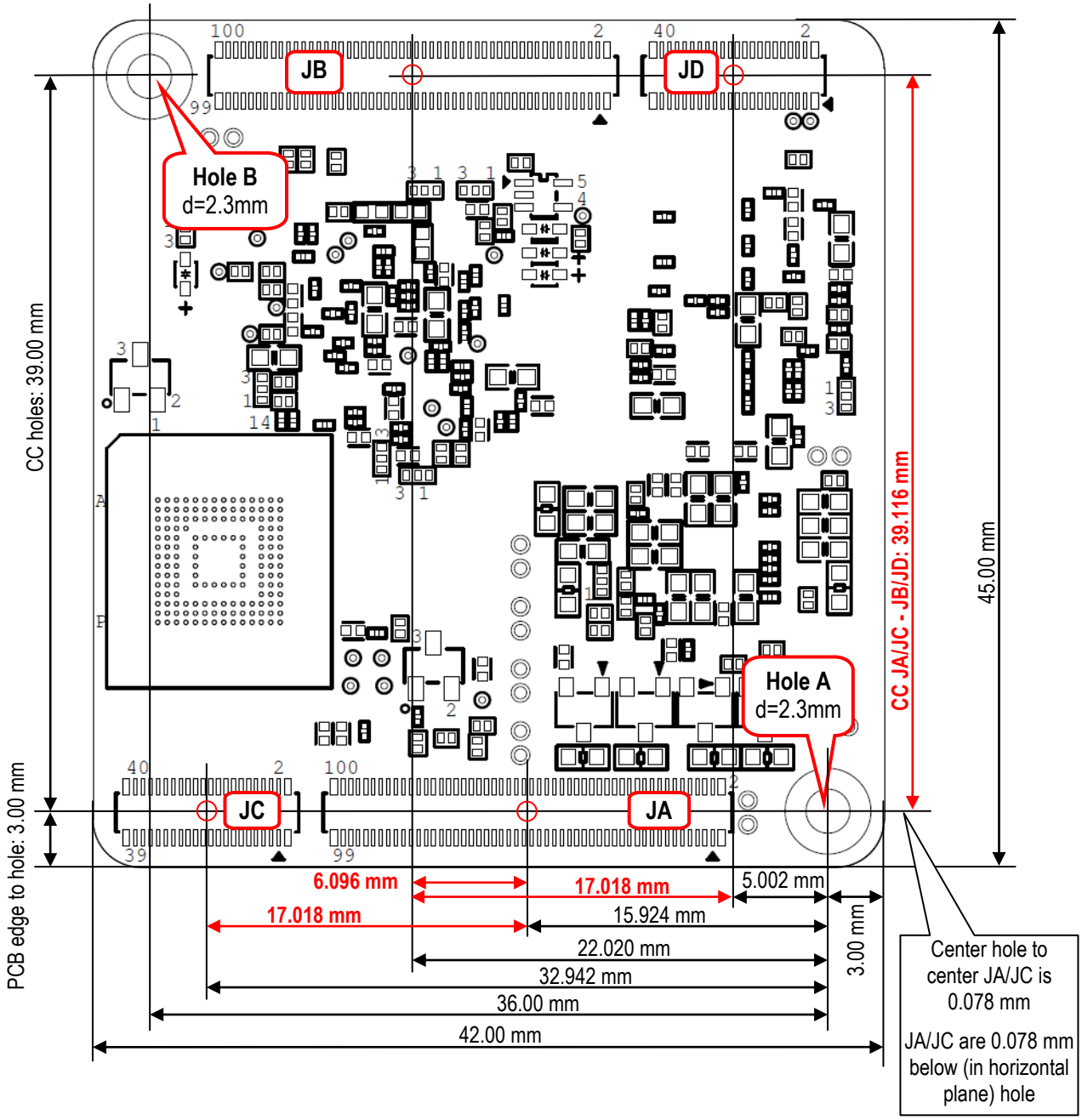


Figure 10 – iMX7ULP uCOM Board Mechanical Outline, View from Bottom Side

Note that placement of the connectors on the carrier board is very important. They must be parallel and have a placement tolerance of +-0.1mm (non-accumulative). Make sure the relative measures between the connectors (marked with red in the picture above) are correct.

Note that the mounting hole location shall be measured relative to the three connectors, not relative to the pcb edge.

Since the stacking height is only 1.5mm in normal case, make sure no components other than the three connectors are within the dotted red line. When using 3mm stacking height it is possible to have low-profile components under the *iMX7ULP uCOM Board*. The picture below illustrates the principal dimensions.

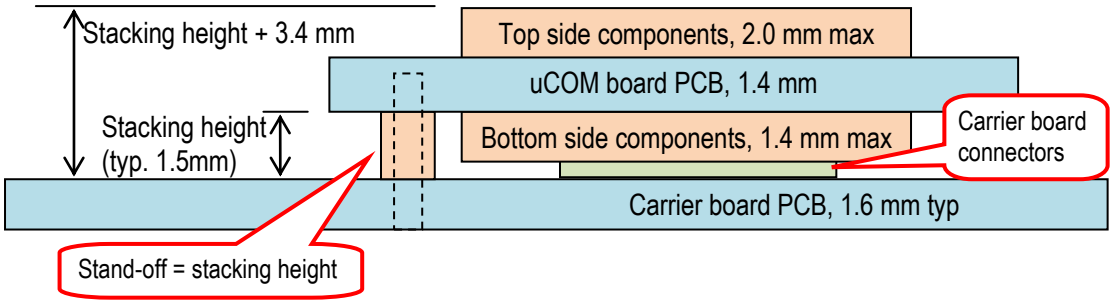


Figure 11 – uCOM Board Mounting on Carrier Board, Stacking Height

11.6.1 DF40C Socket

The headers mounted on the *iMX7ULP uCOM Board* are DF40C-100DP-0.4V(51) (for JA / JB) and DF40C-40DP-0.4V(51) (for JC / JD).

The receptacles that are needed on the carrier board are, depending on stacking height:

Connector	1.5 mm stacking height (standard)	3.0 mm stacking height
100-pos (JA / JB)	DF40C-100DS-0.4V(51) HRS number: 684-4033-4 51	DF40HC(3.0)-100DS-0.4V(51) HRS number: 684-4151-0 51
40-pos (JC / JD)	DF40C-40DS-0.4V(51) HRS number: 684-4008-7 51	DF40HC(3.0)-40DS-0.4V(51) HRS number: 684-4169-6 51

If any of the connectors are not needed on the carrier board design, these do not have to be mounted. This typically apply to JC and JD.

11.6.2 Module Assembly Hardware

The *iMX7ULP uCOM Board* has two 2.3mm mounting holes for securing a good mechanical mounting. Use M2 screws and associated standoffs that have the same height as the stacking height (1.5mm or 3 mm, depending on carrier board connectors).

When mounting the iMX7ULP uCOM board, match hole A on the carrier board with hole A on the uCOM board before the final mounting.

11.7 Environmental Specification

11.7.1 Operating Temperature

Ambient temperature (T_A)

Parameter		Min	Max	Unit
Operating temperature range:	commercial temperature range	0	70[1]	°C
	industrial temperature range	-40	85[1]	°C

Storage temperature range		-40	85	°C
Junction temperature i.MX 7ULP SoC, operating:	comm. temp. range ind. temp. range.	0 -40	95 105	°C °C

[1] Depends on cooling/heat management solution.

11.7.2 Relative Humidity (RH)

Parameter		Min	Max	Unit
Operating: 0°C ≤ T_A ≤ 70°C, non-condensing Operating: -40°C ≤ T_A ≤ 85°C, non-condensing	(comm. temp. range) (ind. temp. range)	10	90	%
Non-operating/Storage: -40°C ≤ T_A ≤ 85°C, non-condensing		5	90	%

11.8 Thermal Design Considerations

Heat dissipation from the i.MX 7ULP SoC depending on many operating conditions, like operating frequency, operating voltage, duty cycle, activity type and cycle duration. Dissipated heat can be up to 0.3 Watt in normal run mode.

If external cooling is needed, or not, depends on dissipated heat and ambient temperature range. In most cases it is possible to operate the *iMX7ULP uCOM Board* without external cooling, at least with ambient temperature up to +60° Celsius. Above this, care must be taken not to exceed max junction temperature of the i.MX 7ULP SoC.

The i.MX 7ULP SoC implement DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling via the Linux BSP. This enables the system to continuously adjust operating frequency and voltage in response to changes in workload and temperature. In general this results in higher performance at lower average power consumption.

The i.MX 7ULP SoC has an integrated temperature sensor for monitoring the junction (i.e., die) temperature, which affects several factors:

- A lower junction temperature, Tj, will result in longer SoC lifetime. See the following document for details: i.MX 7ULP Dual Product Lifetime Usage.
- A lower die temperature will result in lower power consumption due to lower leakage current.

11.8.1 Thermal Parameters

The i.MX 7ULP SoC thermal parameters are listed in the table below.

Parameter	Typical	Unit
Thermal Resistance, CPU Junction to ambient ($R_{\theta JA}$), natural convection	30.7	°C/W
Thermal Resistance, CPU Junction to package top ($R_{\theta JC}$)	11.7	°C/W

11.9 Product Compliance

Visit Embedded Artists' website at http://www.embeddedartists.com/product_compliance for up to date information about product compliances such as CE, RoHS2/3, Conflict Minerals, REACH, etc.

12 Functional Verification and RMA

There is a separate document that presents a number of functional tests that can be performed on the *iMX7ULP uCOM Board* to verify correct operation on the different interfaces. Note that these tests must be performed on the carrier board that is supplied with the *iMX7ULP uCOM Developer's Kit* and with a precompiled kernel from Embedded Artists.

The tests can also be done to troubleshoot a board that does not seem to operate properly. It is strongly advised to read through the list of tests and actions that can be done before contacting Embedded Artists. The different tests can help determine if there is a problem with the board, or not. For return policy, please read Embedded Artists' General Terms and Conditions document (http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf).

13 Things to Note

This chapter presents a number of issues and considerations that users must note.

13.1 Shared Pins and Multiplexing

The i.MX 7ULP SoC has multiple on-chip interfaces that are multiplexed on the external pins. It is not possible to use all interfaces simultaneously and some interface usage is prohibited by the *iMX7ULP uCOM* on-board design. Check if the needed interfaces are available to allocation before starting a design. See chapter 5 for details.

13.2 Use COM Carrier Board rev E/E1, or Later

When using the *iMX7ULP uCOM board*, only use *COM Carrier Board* rev E/E1, or later. Earlier *COM Carrier Board* versions do not support the 4.2V input supply voltage that is needed for the iMX7ULP uCOM board.

Note that *iMX Developer's Kits* that use the *COM Carrier Board* rev E/E1, or later, are called "*iMX Developer's Kits V2*".

13.3 COM Carrier Board Revision and HDMI Interface

Two versions of the COM Carrier board have been released, rev E and rev E1. Of these, only the latest revision (rev E1 and later) will allow the HDMI DDC interface to work correctly, see table below:

Board revisions	COM Carrier Board, rev E HDMI DDC interface connected to I2C-B	COM Carrier Board, rev E1 HDMI DDC interface connected to I2C-C
iMX7ULP uCOM board, rev A plus **uCOM Adapter Board, rev A** HDMI DDC interface connected to I2C-C by default	On *uCOM Adapter Board*, move zero ohm resistors (0402 size) on SJ4, SJ5, SJ7 and SJ8 to 2-3 position (from 1-2 position). The HDMI DDC interface will be using I2C-B interface after the rework. Note that after the rework, the M.2 I2C connection will no longer work (PCA expander).	Will work out-of-the-box.

13.4 uCOM Adapter Board rev A/A1 and Different uCOM Modules

The *uCOM Adapter Board* is designed for different uCOM modules that can have different voltage levels on signals with common pinning. One such example is UART-B, which has 1.8V logic level on the *iMX7ULP uCOM* and 3.3V on the *iMX8M Mini uCOM*.

On rev A of the uCOM Adapter board, SJ10 controls the logic level on UART-B signals and need to be differently set for the two uCOM modules. The picture below illustrates where SJ10 can be found and the two settings available.

Note that SJ10 will be correctly set when buying an *iMX 7ULP uCOM Developer's Kit* or an *iMX 8M Mini uCOM Developer's Kit* but when switching uCOM modules on a *uCOM Adapter Board* SJ10 must be checked and adjusted, if needed.

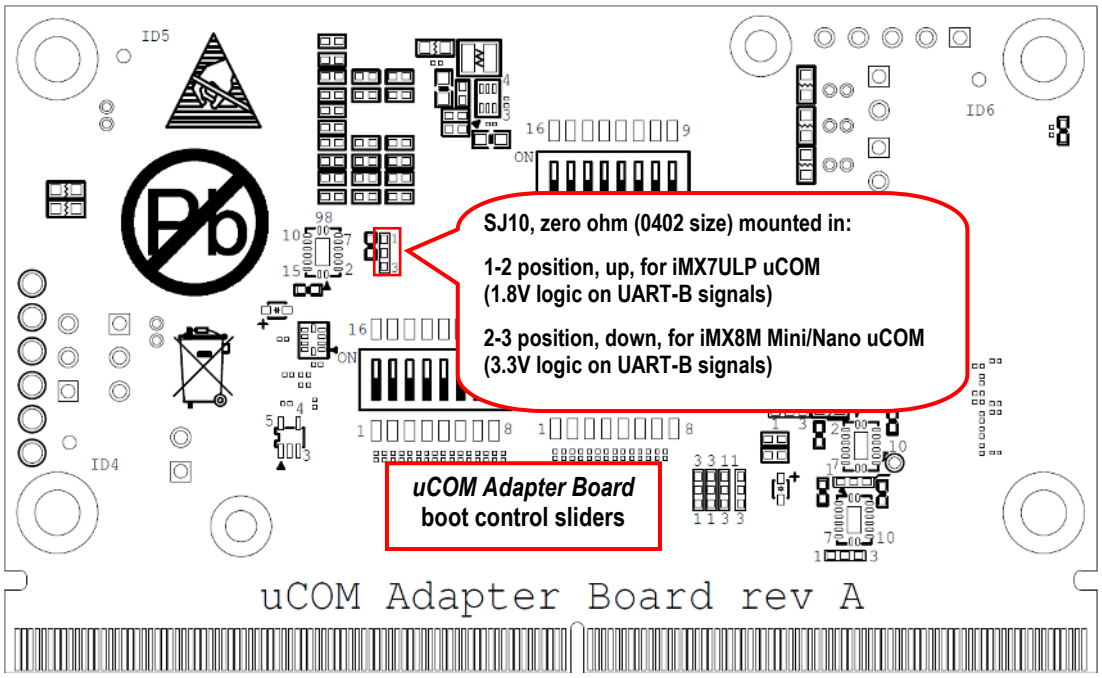


Figure 12 – uCOM Adapter Board SJ10 Location, Bottom Side

On rev A1 of the uCOM Adapter board, J13 controls the logic level on UART-B signals and need to be differently set for the two uCOM modules. The picture below illustrates where J13 can be found and the two settings available.

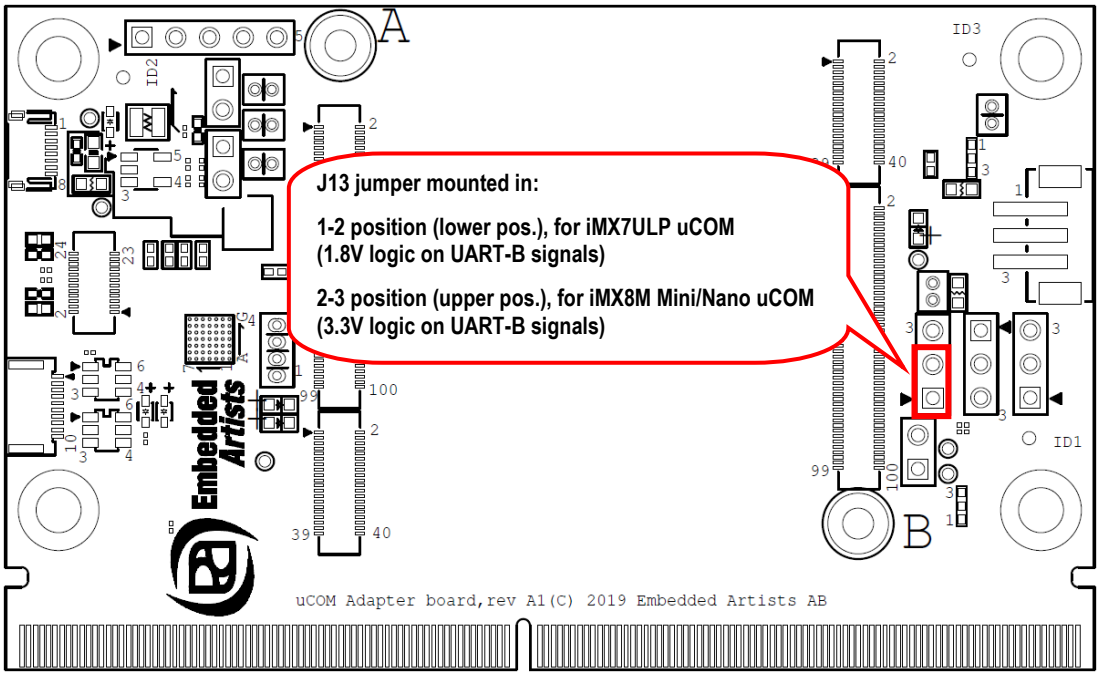


Figure 13 – uCOM Adapter Board rev A1, J13 Location, Top Side

13.5 uCOM Adapter Board rev A/A1 and J12 Usage

The *uCOM Adapter Board* is designed to support different uCOM modules that can have slightly different behavior and functionality. Most uCOM boards control the PERI_PWR_EN signal from

hardware. For these boards J12 shall be in the default 1-2 position. When using UUU to download new images, the console (UART) will work as expected.

When using the iMX7ULP uCOM board, the signal PERI_PWR_EN signal is controlled from the Cortex-M4 application. On an unprogrammed board (from production), signal PERI_PWR_EN is always inactive and the console (UART) communication channel will then not be powered. By moving J12 to 2-3 position, signal PERI_PWR_EN is a copy of the reset signal and will allow the console (UART) will work as expected even though the Cortex-M4 application is not programmed.

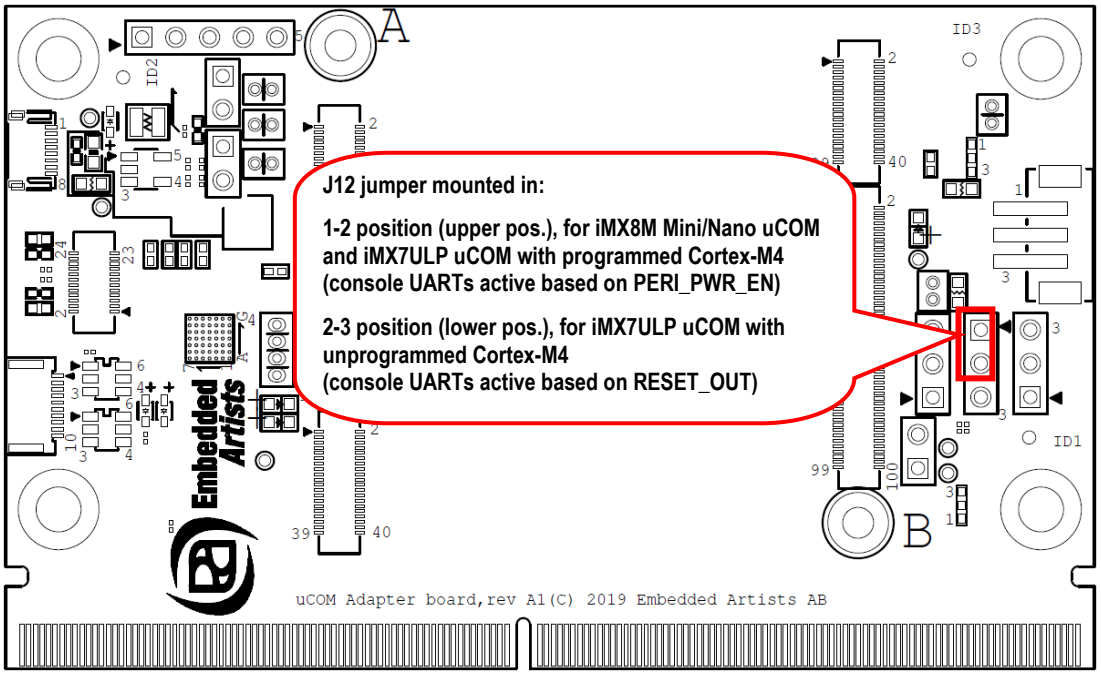


Figure 14 – uCOM Adapter Board rev A/A1, J12 Location, Top Side

13.6 Only Use EA Board Support Package (BSP)

The *iMX7ULP uCOM board* uses multiple on-board interfaces for the internal design, for example PMIC, eMMC and watchdog. Only use the BSP that is delivered from Embedded Artists. Do not change interface initialization and/or pin assignment for the on-board interfaces. Changing BSP settings can result in permanent board failure.

Note that Embedded Artists does not replace iMX7ULP uCOM Boards that have been damaged because of improper interface initialization and/or improper pin assignment.

13.7 OTP Fuse Programming

The i.MX 7ULP SoC has on-chip OTP fuses that can be programmed, see NXP documents *iMX 7ULP Datasheet* and *iMX 7ULP Reference Manual* for details. Once programmed, there is no possibility to reprogram them.

iMX7ULP uCOM Boards are delivered without any OTP fuse programming. It is completely up to the COM board user to decide if OTP fuses shall be programmed and in that case, which ones.

Note that Embedded Artists does not replace iMX7ULP uCOM Boards because of wrong OTP programming. It's the user's responsibility to be absolutely certain before OTP programming and not to program the fuses by accident.

13.8 Write Protect on Parameter Storage E2PROM

The parameter storage E2PROM contains important system data like DDR memory initialization settings and Ethernet MAC addresses. The content should not be erased or overwritten. The E2PROM is write-protected if signal ISP_ENABLE (pin P146/300) is left unconnected, i.e. floating. This should always be the case.

Note that all carrier board design should include the possibility to ground this pin.

The signal ISP_ENABLE has dual functions. By pulling the signal low, the i.MX 7ULP SoC will boot into USB OTG boot mode (also called 'serial download' or 'factory recovery' mode).

13.9 Integration - Contact Embedded Artists

It is strongly recommended to contact Embedded Artists at an early stage in your project. A wide range of support during evaluation and the design-in phase are offered, including but not limited to:

- iMX Developer's Kit to simplify evaluation
- Custom Carrier board design, including 'ready-to-go' standard carrier boards
- Display solutions
- Mechanical solutions
- Schematic review of customer carrier board designs
- Driver and application development

The *iMX7ULP uCOM Board* targets a wide range of applications, such as:

- HMI/GUI solutions
- Connected vending machines
- Point-of-Sale (POS) applications
- Access control panels
- Audio
- IP phones
- Smart appliances
- Home energy management systems
- Industrial automation
- HVAC Building and Control Systems
- Smart Grid and Smart Metering
- Smart Toll Systems
- Data acquisition
- Communication gateway solutions
- Connected real-time systems
- ...and much more

For more harsh use and environments, and where fail-safe operation, redundancy or other strict reliability or safety requirements exists, always contact Embedded Artists for a discussion about suitability.

There are application areas that the *iMX7ULP uCOM Board* is not designed for (and such usage is strictly prohibited), for example:

- Military equipment
- Aerospace equipment
- Control equipment for nuclear power industry
- Medical equipment related to life support, etc.
- Gasoline stations and oil refineries

If not before, **it is essential to contact Embedded Artists before production begins**. In order to ensure a reliable supply for you, as a customer, we need to know your production volume estimates and forecasts. Embedded Artists can typically provide smaller volumes of the *iMX7ULP uCOM Board* directly from stock (for evaluation and prototyping), but **larger volumes need to be planned**.

The more information you can share with Embedded Artists about your plans, estimates and forecasts the higher the likelihood is that we can provide a reliable supply to you of the *iMX7ULP uCOM Board*.

13.10 ESD Precaution when handling iMX7ULP uCOM Board

Please note that the *iMX7ULP uCOM Board* come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.

Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards. That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general touch as little as possible on the boards in order to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

Note that Embedded Artists does not replace boards that have been damaged by ESD.

13.11 EMC / ESD

The *iMX7ULP uCOM Board* has been developed according to the requirements of electromagnetic compatibility (EMC). Nevertheless depending on the target system, additional anti-interference measurement may still be necessary to adherence to the limits for the overall system.

The *iMX7ULP uCOM Board* must be mounted on carrier board (typically an application specific board) and therefore EMC and ESD tests only makes sense on the complete solution.

No specific ESD protection has been implemented on the *iMX7ULP uCOM Board*. ESD protection on board level is the same as what is specified in the i.MX 7ULP SoC datasheet. **It is strongly advised to implement protection against electrostatic discharges (ESD) on the carrier board** on all signals to and from the system. Such protection shall be arranged directly at the inputs/outputs of the system.

14 Custom Design

This document specifies the standard *iMX7ULP uCOM Board* design. Embedded Artists offers many custom design services. Contact Embedded Artists for a discussion about different options.

Examples of custom design services are:

- Mounting a Wi-Fi/BT module.
- Different memory sizes on SDRAM and eMMC Flash.
- Different I/O voltage levels on all or parts of the pins.
- Different mounting options, for example remove Ethernet interface.
- Different pinning on MXM3 edge pins, including but not limited to, SMARC compatible pinning.
- Different board form factor, for example SODIMM-200, high-density connectors on bottom side or MXM3 compatible boards that are higher (>50 mm).
- Different input supply voltage range.
- Single Board Computer solutions, where the core design of the *iMX7ULP uCOM Board* is integrated together with selected interfaces.
- Changed internal pinning to make certain pins available.

Embedded Artists also offers a range of services to shorten development time and risk, such as:

- Standard Carrier boards ready for integration
- Custom Carrier board design
- Display solutions
- Mechanical solutions

15 Disclaimers

Embedded Artists reserves the right to make changes to information published in this document, including, without limitation, specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Customer is responsible for the design and operation of their applications and products using Embedded Artists' products, and Embedded Artists accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Embedded Artists' product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. Customer is required to have expertise in electrical engineering and computer engineering for the installation and use of Embedded Artists' products.

Embedded Artists does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Embedded Artists' products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Embedded Artists does not accept any liability in this respect.

Embedded Artists does not accept any liability for errata on individual components. Customer is responsible to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.

Embedded Artists does not accept any liability and no warranty is given for any unexpected software behavior due to deficient components.

Customer is required to take note of manufacturer's specification of used components, for example PMIC and eMMC. Such specifications, if applicable, contain additional information that must be taken note of for the safe and reliable operation. These documents are stored on Embedded Artists' product support page.

All Embedded Artists' products are sold pursuant to Embedded Artists' terms and conditions of sale: http://www.embeddedartists.com/sites/default/files/docs/General_Terms_and_Conditions.pdf

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by Embedded Artists for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN EMBEDDED ARTISTS' TERMS AND CONDITIONS OF SALE EMBEDDED ARTISTS DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF EMBEDDED ARTISTS PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY THE CEO OF EMBEDDED ARTISTS, PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, NUCLEAR, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE.

Resale of Embedded Artists' products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by Embedded Artists

for the Embedded Artists' product or service described herein and shall not create or extend in any manner whatsoever, any liability of Embedded Artists.

This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

15.1 Definition of Document Status

Preliminary – The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Embedded Artists does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information. The document is in this state until the product has passed Embedded Artists product qualification tests.

Approved – The information and data provided define the specification of the product as agreed between Embedded Artists and its customer, unless Embedded Artists and customer have explicitly agreed otherwise in writing.