

# NTTS2P02R2

## Power MOSFET -2.4 Amps, -20 Volts

Single P-Channel Micro8™

### Features

- Ultra Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Micro-8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Micro8 Mounting Information Provided
- Pb-Free Package is Available

### Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Cellular and Cordless Telephones, and PCMCIA Cards

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-20	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 8.0$	V
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	160	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	0.78	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	$I_D$	-2.4	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	$I_D$	-1.92	A
Pulsed Drain Current (Note 3)	$I_{DM}$	-20	A
Thermal Resistance – Junction-to-Ambient (Note 2)	$R_{\theta JA}$	88	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.42	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	$I_D$	-3.25	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	$I_D$	-2.6	A
Pulsed Drain Current (Note 3)	$I_{DM}$	-30	A
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = -20$ Vdc, $V_{GS} = -4.5$ Vdc, Peak $I_L = -5.0$ Apk, $L = 28$ mH, $R_G = 25 \Omega$ )	EAS	350	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Minimum FR-4 or G-10 PCB, Steady State.
2. Mounted onto a 2" square FR-4 Board (1 IN SQ, 2 oz Cu 0.06" thick single sided), Steady State.
3. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .



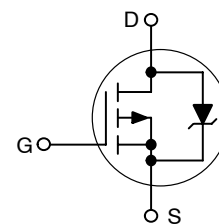
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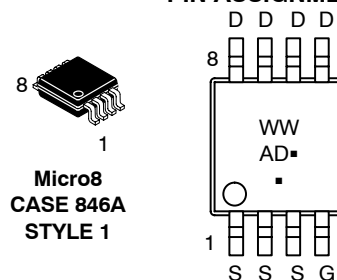
**-2.4 AMPERES  
-20 VOLTS**

**$R_{DS(on)} = 90 \text{ m}\Omega$**

Single P-Channel



### MARKING DIAGRAM & PIN ASSIGNMENT



AD = Specific Device Code  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTTS2P02R2	Micro8	4000/Tape & Reel
NTTS2P02R2G	Micro8 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTTS2P02R2

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted) (Note 4)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = -250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	-20 -	- -12.7	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = -16 Vdc, T <sub>J</sub> = 25°C) (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = -16 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	- -	- -	-1.0 -25	μAdc
Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = -20 Vdc, T <sub>J</sub> = 25°C)	I <sub>DSS</sub>	-	-	-5.0	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = -8 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	-100	nAdc
Gate-Body Leakage Current (V <sub>GS</sub> = +8 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	100	nAdc

### ON CHARACTERISTICS

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μAdc) Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	-0.5 -	-0.90 2.5	-1.4 -	Vdc mV/°C
Static Drain-to-Source On-State Resistance (V <sub>GS</sub> = -4.5 Vdc, I <sub>D</sub> = -2.4 Adc) (V <sub>GS</sub> = -2.7 Vdc, I <sub>D</sub> = -1.2 Adc) (V <sub>GS</sub> = -2.5 Vdc, I <sub>D</sub> = -1.2 Adc)	R <sub>DS(on)</sub>	- - -	0.070 0.100 0.110	0.090 0.130 -	Ω
Forward Transconductance (V <sub>DS</sub> = -10 Vdc, I <sub>D</sub> = -1.2 Adc)	g <sub>FS</sub>	2.0	4.2	-	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = -16 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	-	550	-	pF
Output Capacitance		C <sub>oss</sub>	-	200	-	
Reverse Transfer Capacitance		C <sub>rss</sub>	-	100	-	

### SWITCHING CHARACTERISTICS (Notes 5 & 6)

Turn-On Delay Time	(V <sub>DD</sub> = -10 Vdc, I <sub>D</sub> = -2.4 Adc, V <sub>GS</sub> = -4.5 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	10	-	ns
Rise Time		t <sub>r</sub>	-	31	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	33	-	
Fall Time		t <sub>f</sub>	-	29	-	
Turn-On Delay Time	(V <sub>DD</sub> = -10 Vdc, I <sub>D</sub> = -1.2 Adc, V <sub>GS</sub> = -2.7 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	15	-	ns
Rise Time		t <sub>r</sub>	-	40	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	35	-	
Fall Time		t <sub>f</sub>	-	35	-	
Total Gate Charge	(V <sub>DS</sub> = -16 Vdc, V <sub>GS</sub> = -4.5 Vdc, I <sub>D</sub> = -2.4 Adc)	Q <sub>tot</sub>	-	10	18	nC
Gate-Source Charge		Q <sub>gs</sub>	-	1.5	-	
Gate-Drain Charge		Q <sub>gd</sub>	-	5.0	-	

### BODY-DRAIN DIODE RATINGS (Note 5)

Diode Forward On-Voltage	(I <sub>S</sub> = -2.4 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = -2.4 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- -	-0.88 -0.75	-1.0 -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = -2.4 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	-	37	-	ns
		t <sub>a</sub>	-	16	-	
		t <sub>b</sub>	-	21	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.025	-	μC

4. Handling precautions to protect against electrostatic discharge are mandatory.
5. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperature.

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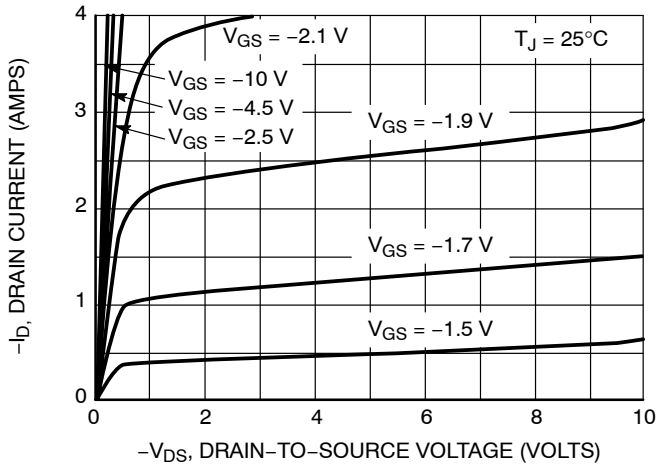


Figure 1. On-Region Characteristics.

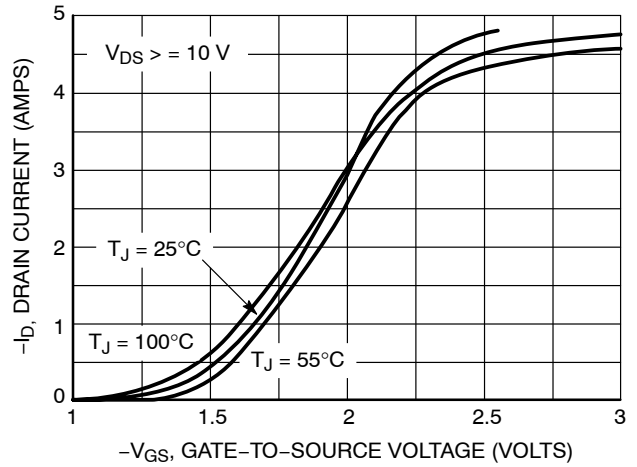


Figure 2. Transfer Characteristics.

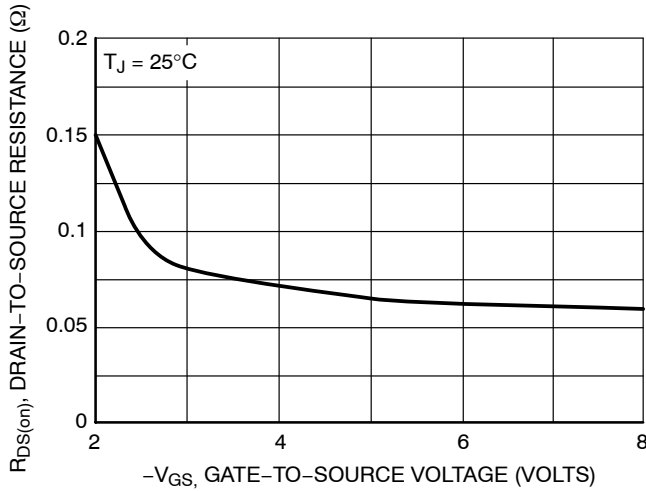


Figure 3. On-Resistance vs. Gate-to-Source Voltage.

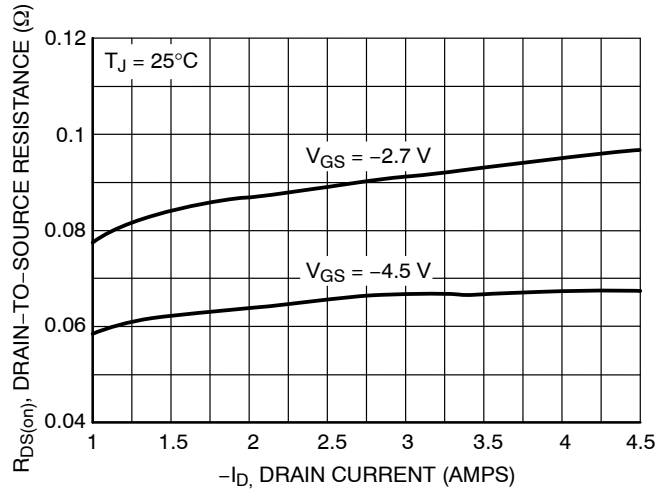


Figure 4. On-Resistance vs. Drain Current and Gate Voltage.

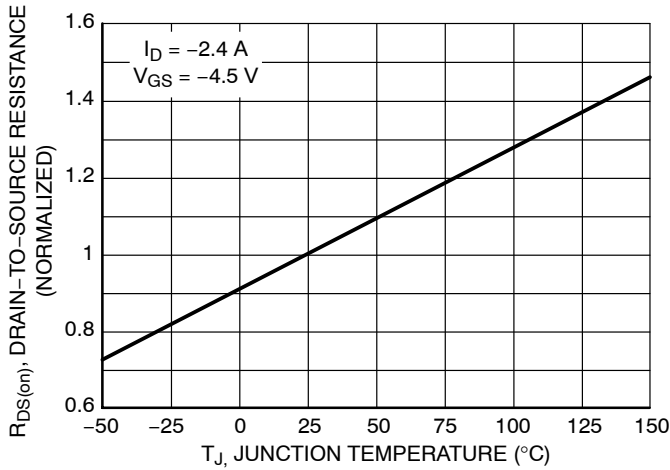


Figure 5. On-Resistance Variation with Temperature.

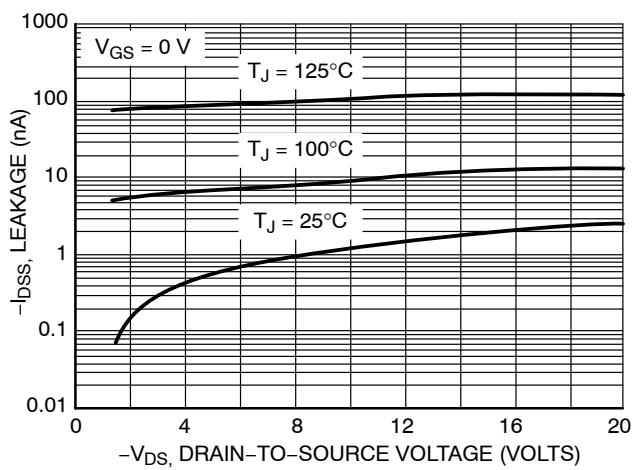
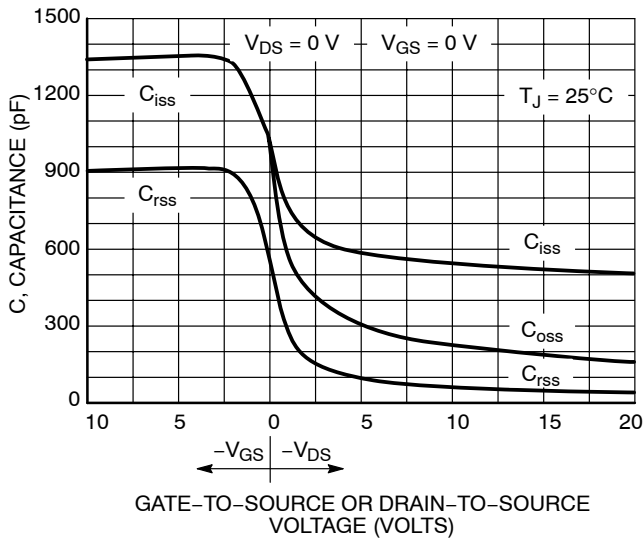
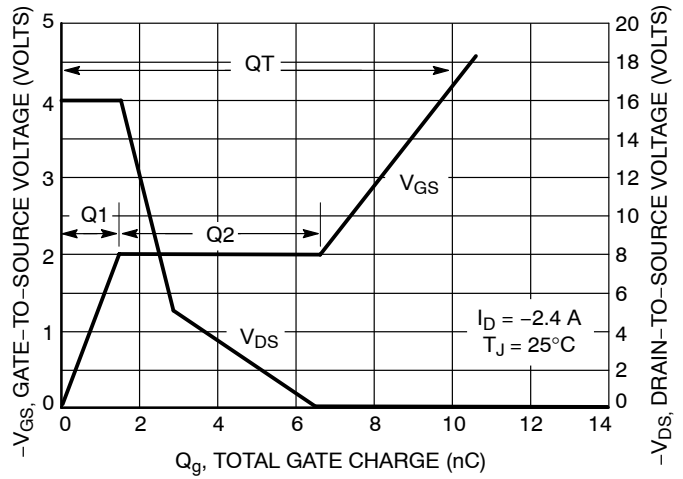


Figure 6. Drain-to-Source Leakage Current vs. Voltage.

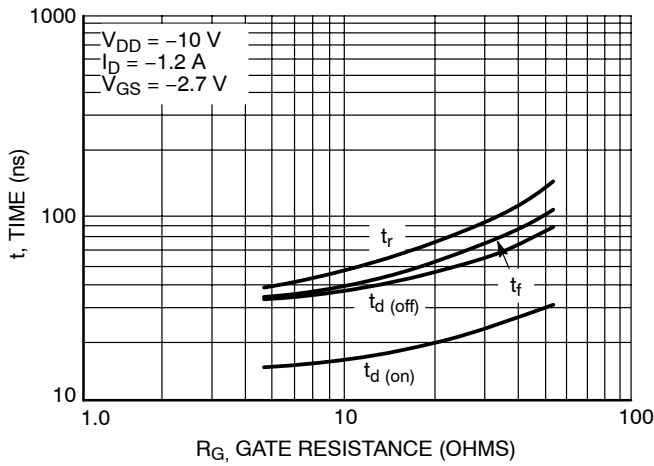
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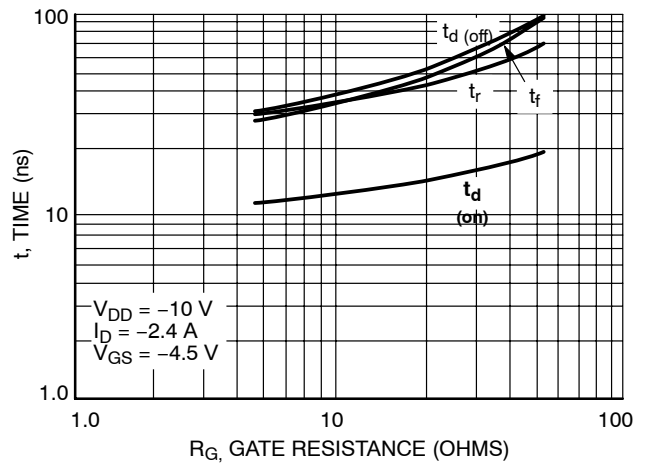
**Figure 7. Capacitance Variation**



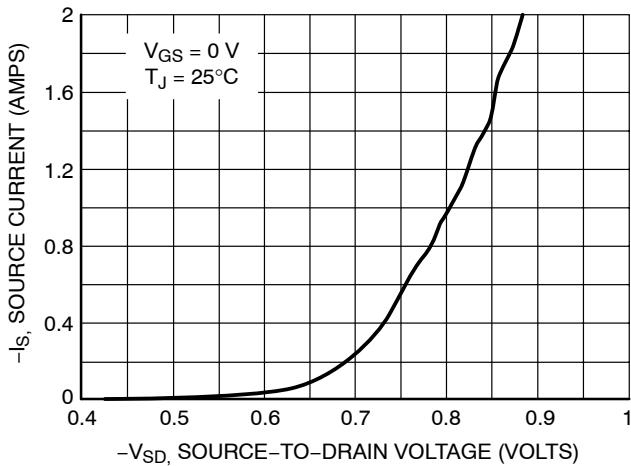
**Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**



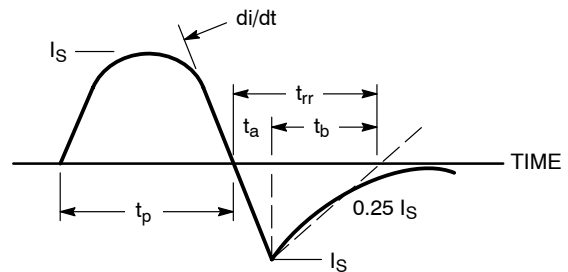
**Figure 9. Resistive Switching Time Variation versus Gate Resistance**



**Figure 10. Resistive Switching Time Variation versus Gate Resistance**



**Figure 11. Diode Forward Voltage versus Current**



**Figure 12. Diode Reverse Recovery Waveform**

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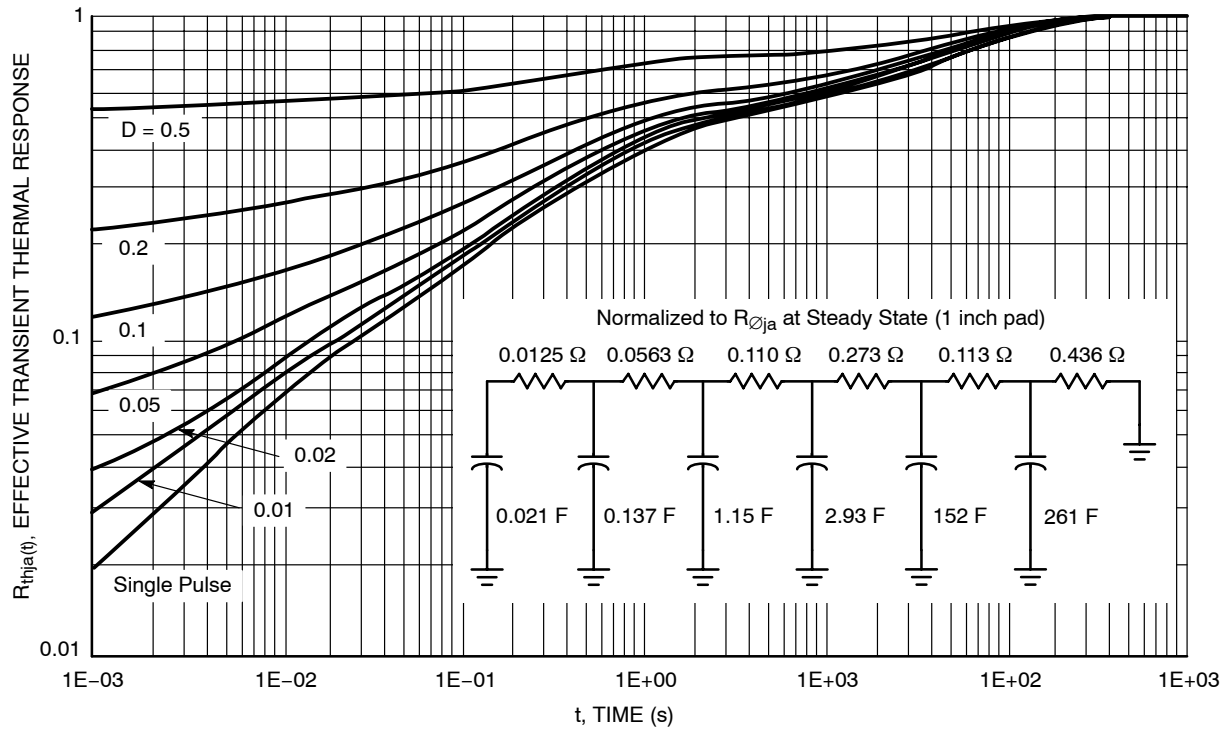


Figure 13. FET Thermal Response.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

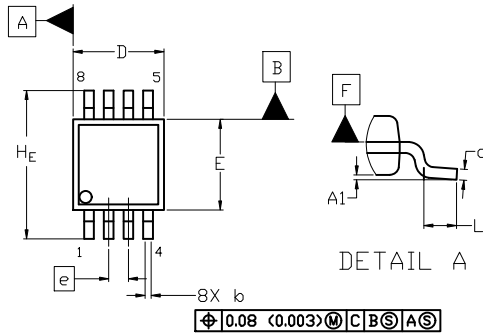
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SCALE 2:1

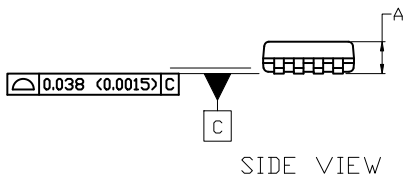
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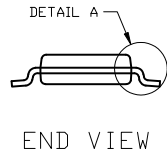


TOP VIEW

NOTE 3



SIDE VIEW



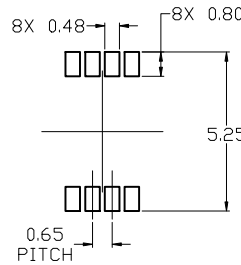
END VIEW

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS *D* AND *E* DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION *E* DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS *D* AND *E* ARE DETERMINED AT DATUM *F*.
5. DATUMS *A* AND *B* ARE TO BE DETERMINED AT DATUM *F*.
6. *A1* IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

⌀ 0.08 (0.003) M C B S A S

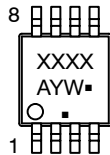
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
<i>b</i>	0.25	0.33	0.40
<i>c</i>	0.13	0.18	0.23
<i>D</i>	2.90	3.00	3.10
<i>E</i>	2.90	3.00	3.10
<i>e</i>	0.65 BSC		
<i>H<sub>E</sub></i>	4.75	4.90	5.05
<i>L</i>	0.40	0.55	0.70



RECOMMENDED  
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLE 1:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

**STYLE 2:**

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

**STYLE 3:**

1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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