CSD18536KCS 60-V N-Channel NexFET™ Power MOSFET

1 Features

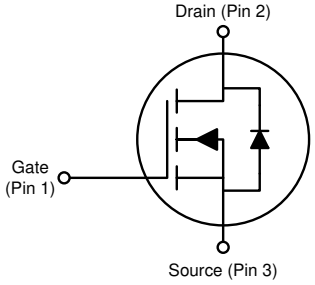
- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free
- TO-220 plastic package

2 Applications

- Secondary side synchronous rectifier
- Motor control

3 Description

This 60-V, 1.3-mΩ, TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	108		nC
Q_{gd}	Gate Charge Gate-to-Drain	14		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	1.7	mΩ
		V_{GS} = 10 V	1.3	mΩ
$V_{GS(th)}$	Threshold Voltage	1.8		V

Ordering Information

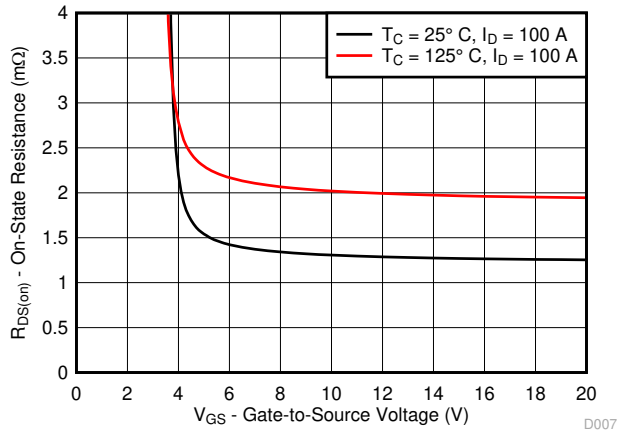
Device(1)	Package	Media	Qty	Ship
CSD18536KCS	TO-220 Plastic Package	Tube	50	Tube

(1) For all available packages, see the orderable addendum at the end of the data sheet.

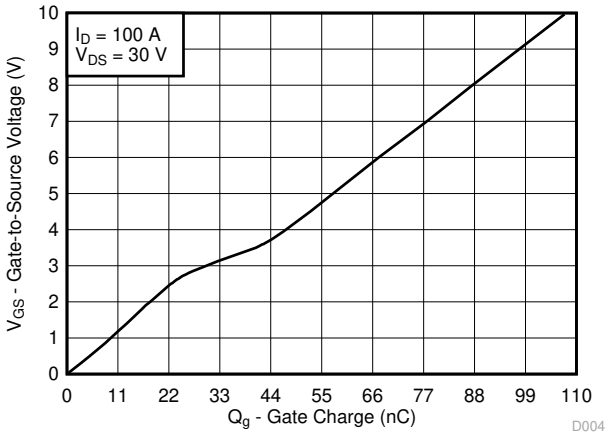
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	200	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	349	
	Continuous Drain Current (Silicon limited), T_C = 100°C	247	
I_{DM}	Pulsed Drain Current (1)	400	A
P_D	Power Dissipation	375	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 175	°C
E_{AS}	Avalanche Energy, single pulse I_D = 128 A, L = 0.1 mH, R_G = 25 Ω	819	mJ

(1) Max $R_{\theta JC}$ = 0.4°C/W, pulse duration ≤100 µs, duty cycle ≤1%.



$R_{DS(on)}$ vs V_{GS}



Gate Charge

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4 Revision History

Changes from Revision A (December 2017) to Revision B (June 2023) **Page**

- Updated Figure 5-10 4

Changes from Revision * (March 2015) to Revision A (December 2017) **Page**

- Updated Gate Charge curve 1
- Changed C_{OSS} values From: TYP = 1700 pF MAX = 2210 pF To: TYP = 1410 pF MAX = 1840 pF in *Dynamic Characteristics* 3
- Changed Q_g values From: TYP = 83 nC MAX = 108 nC To: TYP = 108 nC MAX = 140 nC in the *Dynamic Characteristics* 3
- Changed $Q_{g(th)}$ value From: 12 nC To: 17 nC in the *Dynamic Characteristics* 3
- Changed $t_{d(on)}$ value From: 8 ns To: 11 ns in *Dynamic Characteristics*. 3
- Changed t_r value From: 17 ns To: 5 ns in *Dynamic Characteristics*. 3
- Changed $t_{d(off)}$ value From: 23 ns To: 24 ns in *Dynamic Characteristics*. 3
- Changed t_f value From: 12 ns To: 4 ns in *Dynamic Characteristics* 3
- Updated Figure 5-4. 4
- Updated Figure 5-5 4

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 48 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.4	1.8	2.2	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_D = 100 A		1.7	2.2	mΩ
		V_{GS} = 10 V, I_D = 100 A		1.3	1.6	mΩ
g_{fs}	Transconductance	V_{DS} = 6 V, I_D = 100 A		312		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		8790	11430	pF
C_{oss}	Output Capacitance			1410	1840	pF
C_{rss}	Reverse Transfer Capacitance			39	51	pF
R_G	Series Gate Resistance			0.7	1.4	Ω
Q_g	Gate Charge Total (10 V)	V_{DS} = 30 V, I_D = 100 A		108	140	nC
Q_{gd}	Gate Charge Gate-to-Drain			14		nC
Q_{gs}	Gate Charge Gate-to-Source			18		nC
$Q_{g(th)}$	Gate Charge at V_{th}			17		nC
Q_{oss}	Output Charge	V_{DS} = 30 V, V_{GS} = 0 V		230		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 100 A, R_G = 0 Ω		11		ns
t_r	Rise Time			5		ns
$t_{d(off)}$	Turn Off Delay Time			24		ns
t_f	Fall Time			4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 100 A, V_{GS} = 0 V		0.9	1.0	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 30 V, I_F = 100 A, di/dt = 300 A/µs		323		nC
t_{rr}	Reverse Recovery Time			86		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance			0.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance			62	

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

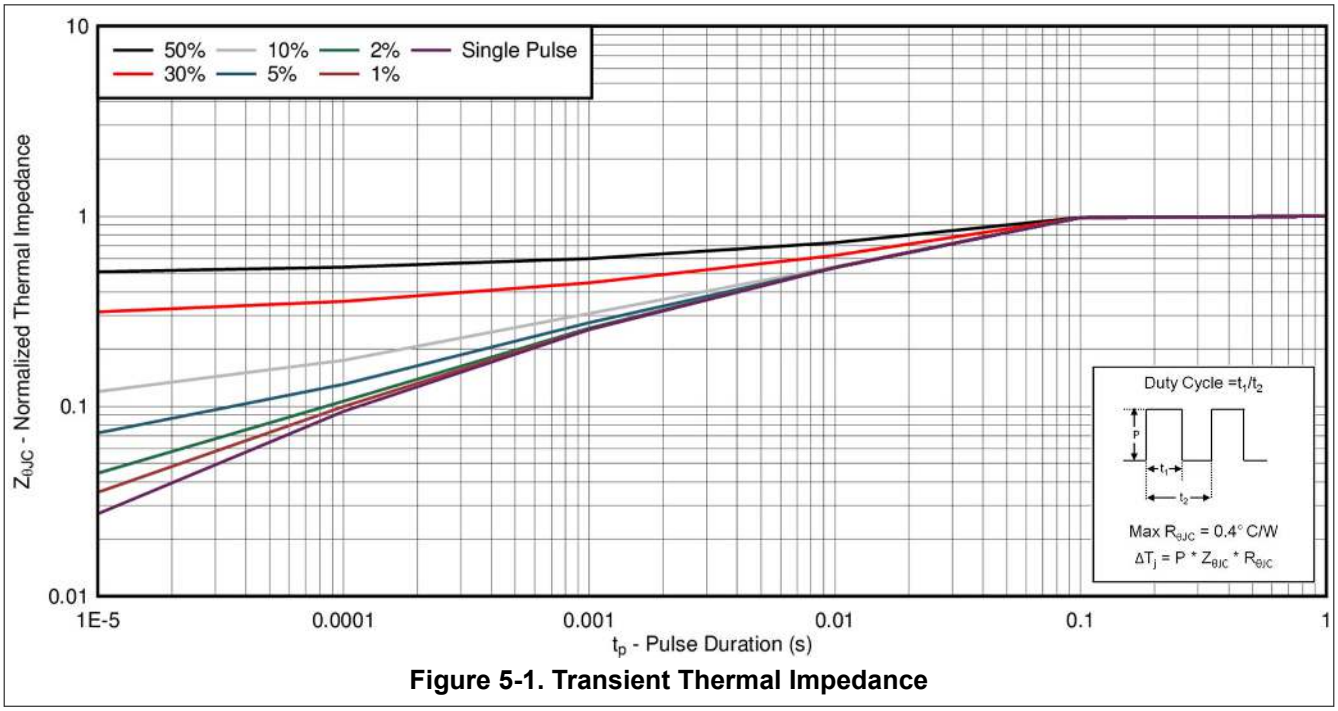


Figure 5-1. Transient Thermal Impedance

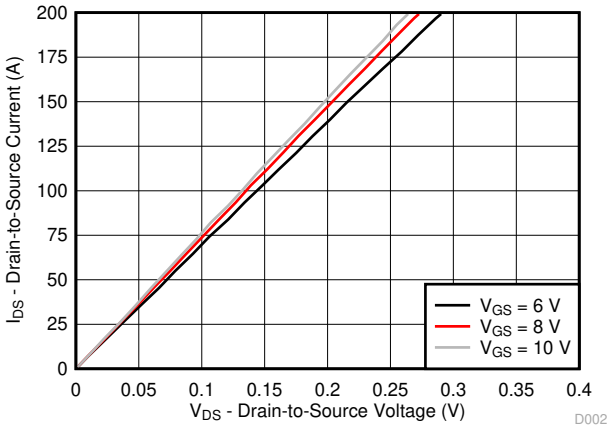
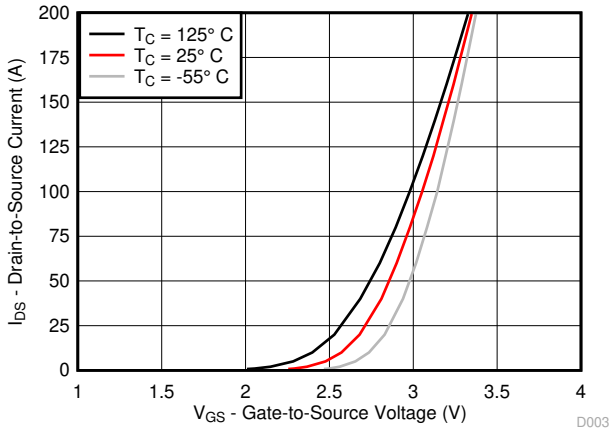
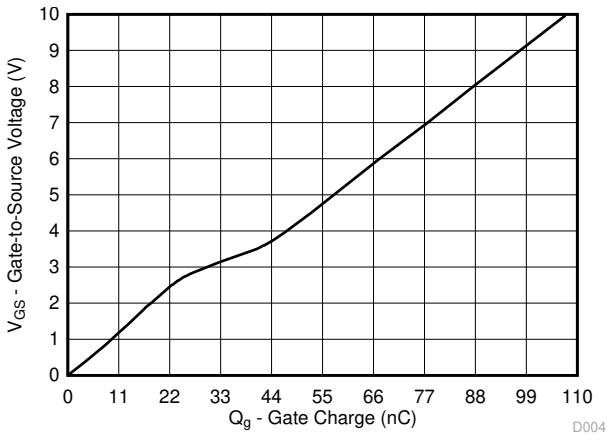


Figure 5-2. Saturation Characteristics



VDS = 5 V

Figure 5-3. Transfer Characteristics



V_{DS} = 50 V I_D = 100 A

Figure 5-4. Gate Charge

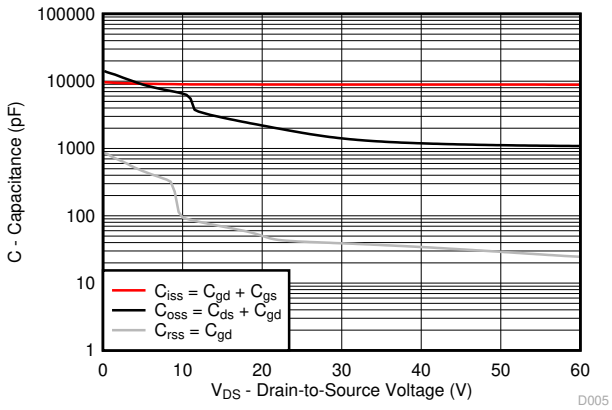
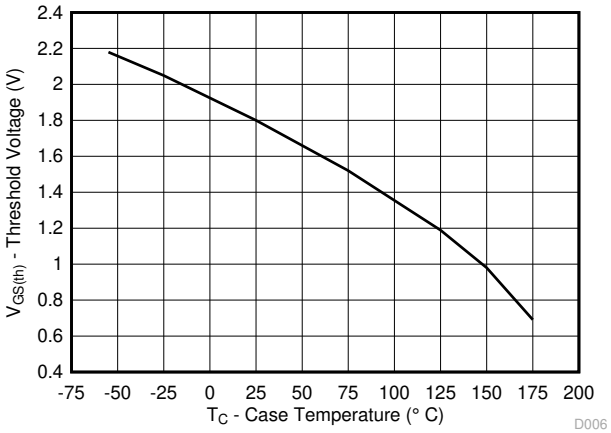


Figure 5-5. Capacitance



I_D = 250 µA

Figure 5-6. Threshold Voltage vs Temperature

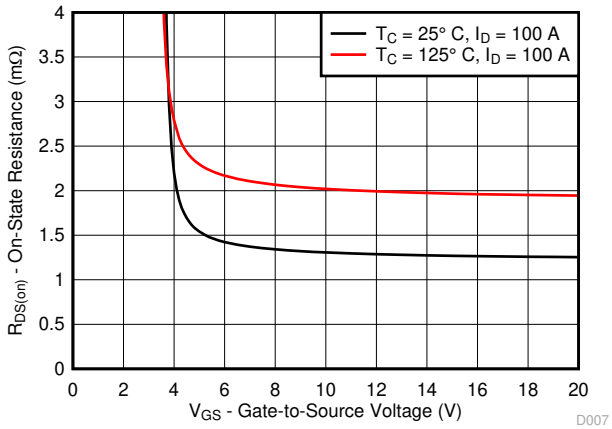
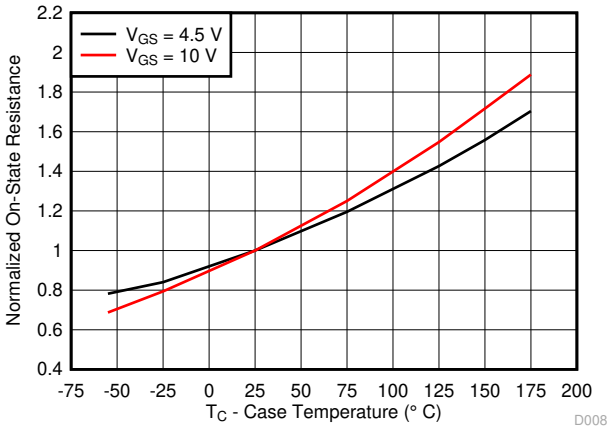


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 100 A

Figure 5-8. Normalized On-State Resistance vs Temperature

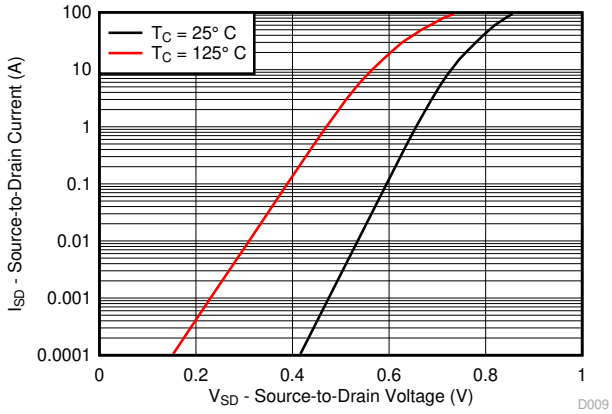
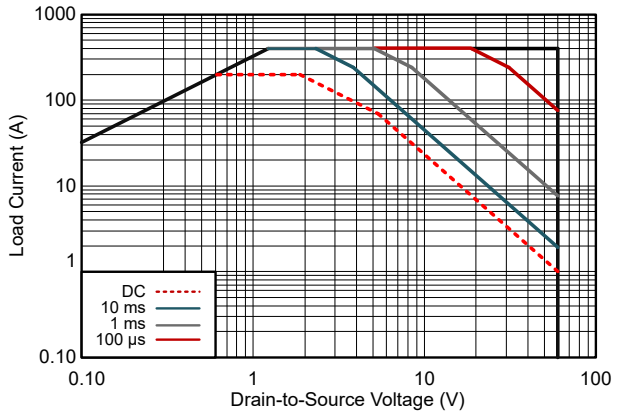


Figure 5-9. Typical Diode Forward Voltage



Single Pulse Max $R_{\theta JC}$ = 0.4°C/W

Figure 5-10. Maximum Safe Operating Area

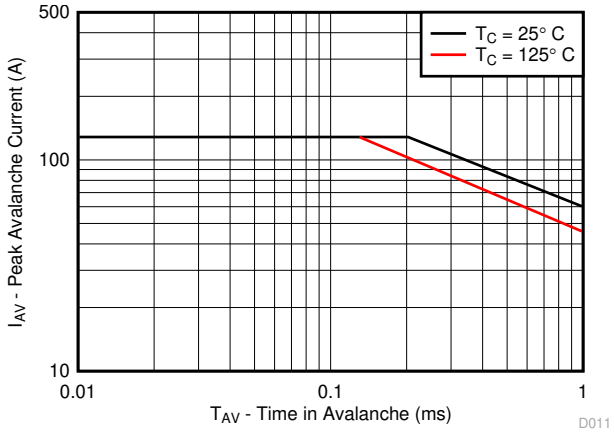


Figure 5-11. Single Pulse Unclamped Inductive Switching

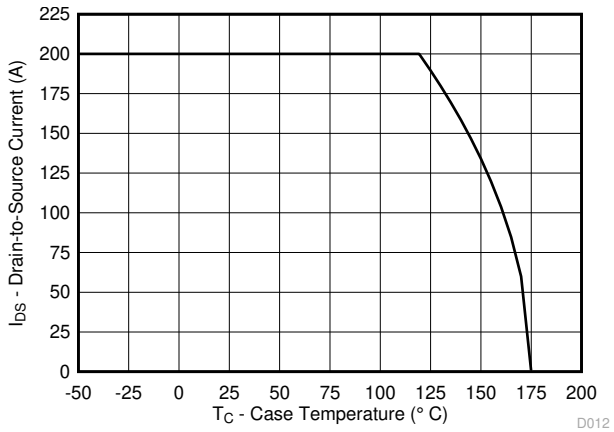


Figure 5-12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

6.2 Trademarks

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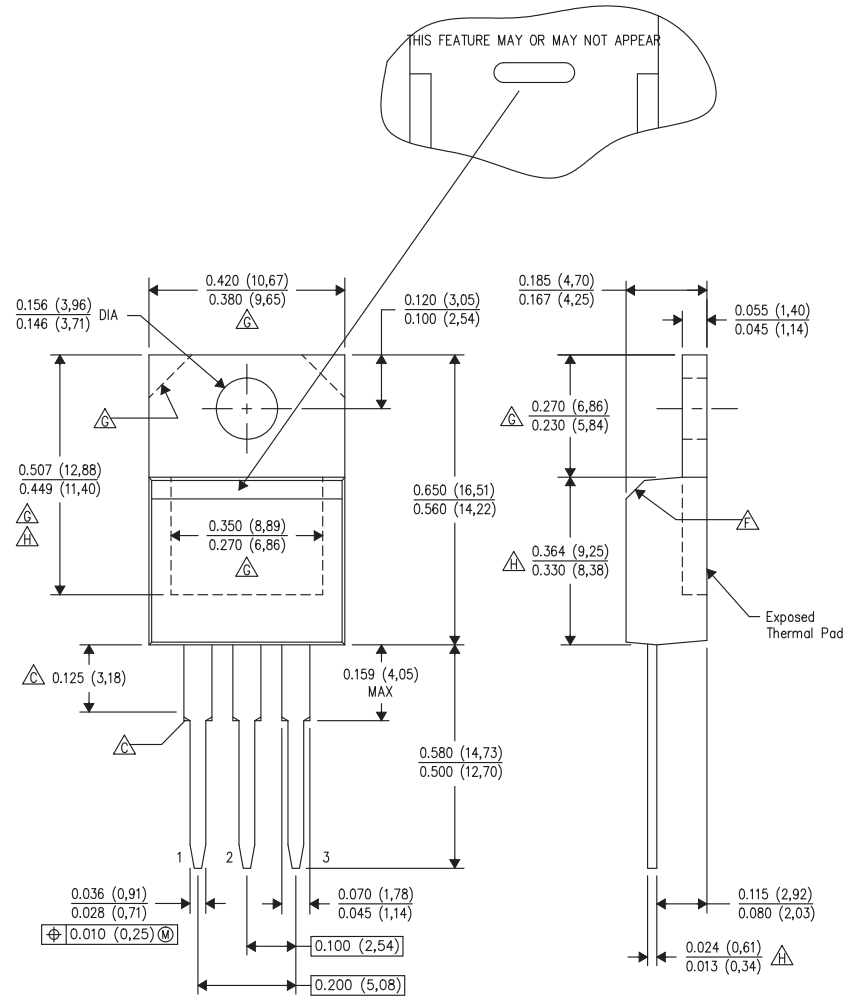
Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KCS Package Dimensions



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area. Chamfer may or may not appear
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.
F. The chamfer is optional.
G. Thermal pad contour optional within these dimensions.
H. Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

7.1.1 Pin Configuration

Position	Designation
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18536KCS	ACTIVE	TO-220	KCS	3	50	RoHS-Exempt & Green	SN	N / A for Pkg Type	-55 to 175	CSD18536KCS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

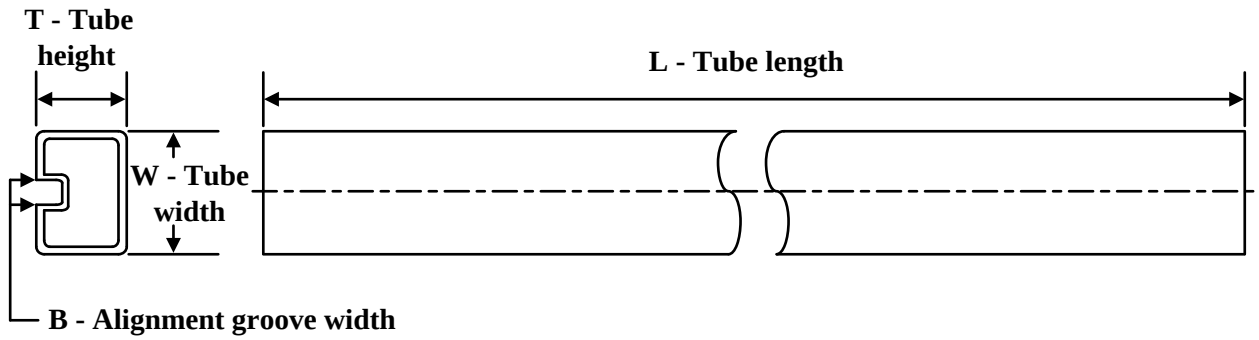
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CSD18536KCS	KCS	TO-220	3	50	532	34.1	700	9.6

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