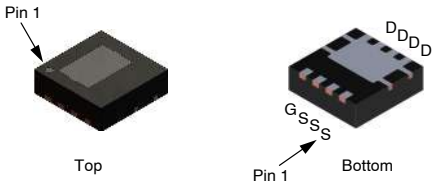
MOSFET – N-Channel, DUAL COOL® 33, POWERTRENCH®
60 V, 40 A, 6.3 mΩ

FDMC86520DC

V_{DS}	$r_{DS(ON)}$ MAX	I_D MAX
60 V	6.3 mΩ @ 10 V	40 A
	8.7 mΩ @ 8 V	



PQFN8 3.3X3.3, 0.65P
CASE 483AL
DUAL COOL 33

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process. Advancements in both silicon and DUAL COOL package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction−to−Ambient thermal resistance.

Features

- DUAL COOL Top Side Cooling PQFN Package
- Max $r_{DS(on)}$ = 6.3 mΩ at V_{GS} = 10 V, I_D = 17 A
- Max $r_{DS(on)}$ = 8.7 mΩ at V_{GS} = 8 V, I_D = 14,5 A
- High Performance Technology for Extremely Low $r_{DS(on)}$
- This Device is Pb−Free, Halide Free and RoHS Compliant

Applications

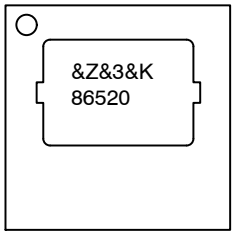
- Primary DC−DC Switch
- Motor Bridge Switch
- Synchronous Rectifier

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter			Rating	Unit
V_{DS}	Drain to Source Voltage			60	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current	Continuous	T_C = 25°C	40	A
		Continuous (Note 1a)	T_A = 25°C	17	
		Pulsed		80	
E_{AS}	Single Pulse Avalanche Energy (Note 3)			128	mJ
P_D	Power Dissipation		T_C = 25°C	73	W
	Power Dissipation (Note 1a)		T_A = 25°C	3.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to + 150	°C

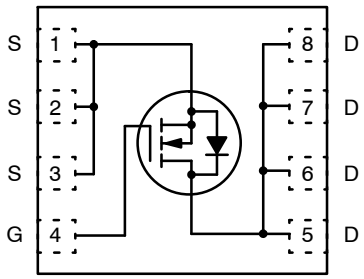
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
86520	= Specific Device Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter		Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	4.2	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.7	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	42	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	105	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	17	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	12	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	60	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	30	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	3.7	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	−10	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 17 A	–	5.1	6.3	mΩ
		V_{GS} = 8 V, I_D = 14.5 A	–	6.5	8.7	
		V_{GS} = 10 V, I_D = 17 A, T_J = 125°C	–	8.2	10.2	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 17 A	–	49	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz	–	2097	2790	pF
C_{oss}	Output Capacitance		–	557	745	pF
C_{rss}	Reverse Transfer Capacitance		–	13	40	pF
R_g	Gate Resistance		0.1	0.5	2.5	Ω
SWITCHING CHARACTERISTICS						
$td_{(on)}$	Turn−On Delay Time	V_{DD} = 30 V, I_D = 17 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	18	33	ns
t_r	Rise Time		–	6.6	14	
$t_{d(off)}$	Turn−Off Delay Time		–	19	35	
t_f	Fall Time		–	4	10	
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 30 V, I_D = 17 A	–	29	40	nC
		V_{GS} = 0 V to 8 V, V_{DD} = 30 V, I_D = 17 A	–	23	33	
Q_{gs}	Gate to Source Charge	V_{DD} = 30 V, I_D = 17 A	–	12	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	5.5	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 17 A (Note 2)	–	0.83	1.3	V
		V_{GS} = 0 V, I_S = 2.5 A (Note 2)	–	0.74	1.2	
t_{rr}	Reverse Recovery Time	I_F = 17 A, di/dt = 100 A/μs	–	41	65	ns
Q_{rr}	Reverse Recovery Charge		–	23	37	nC

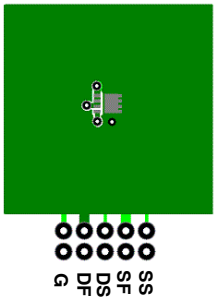
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

THERMAL CHARACTERISTICS

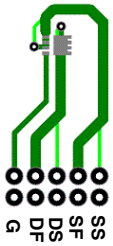
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	4.2	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.7	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	42	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	105	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	29	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1e)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1f)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1g)	30	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1h)	79	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	17	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	12	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1l)	16	

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a FR−4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 42°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 105°C/W when mounted on a minimum pad of 2 oz copper

c. Still air, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

d. Still air, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper

e. Still air, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, 1 in^2 pad of 2 oz copper

f. Still air, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, minimum pad of 2 oz copper

g. 200FPM Airflow, No Heat Sink, 1 in^2 pad of 2 oz copper

h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper

i. 200FPM Airflow, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

j. 200FPM Airflow, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper

k. 200FPM Airflow, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, 1 in^2 pad of 2 oz copper

l. 200FPM Airflow, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 128 mJ is based on starting T_J = 25°C, L = 1 mH, I_{AS} = 16 A, V_{DD} = 54 V, V_{GS} = 10 V, 100% test at L = 0.3 mH, I_{AS} = 24 A.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

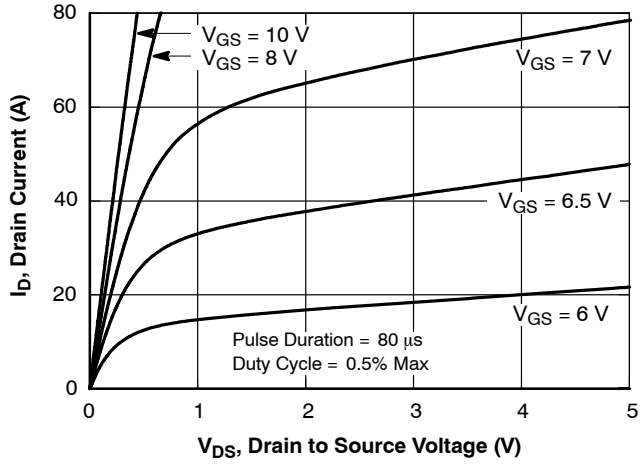


Figure 1. On Region Characteristics

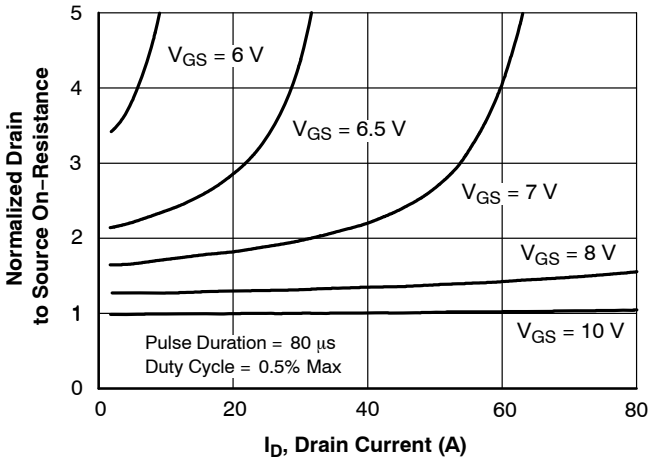


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

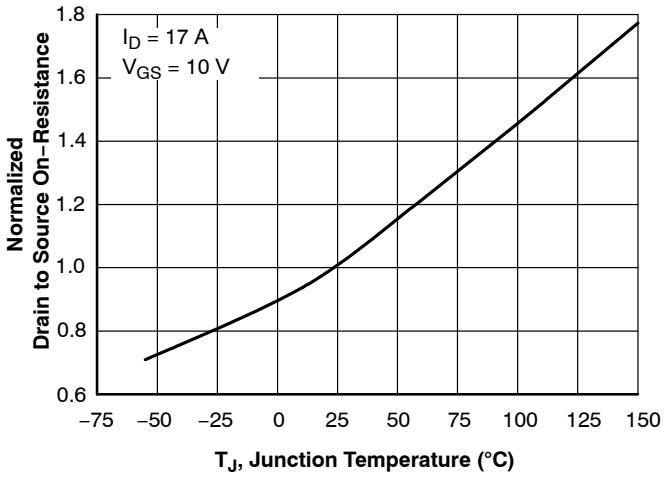


Figure 3. Normalized On Resistance vs. Junction Temperature

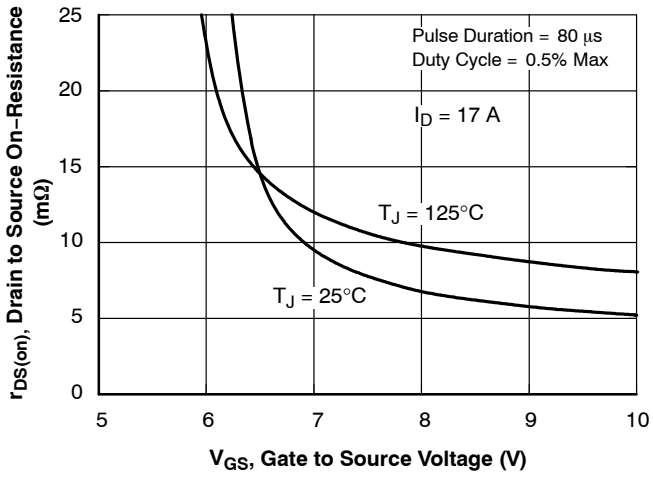


Figure 4. On−Resistance vs. Gate to Source Voltage

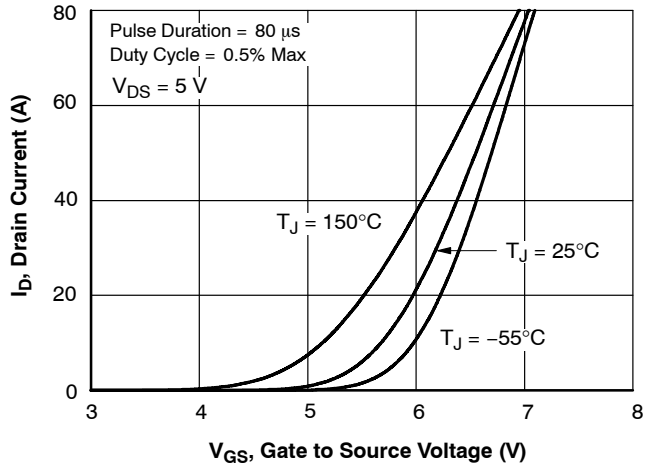


Figure 5. Transfer Characteristics

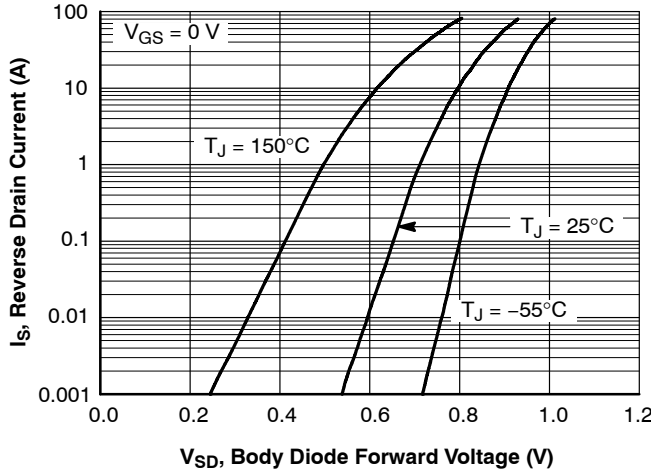


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

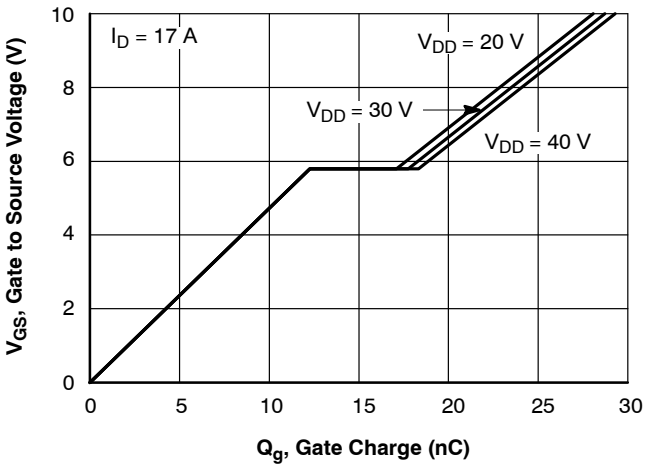


Figure 7. Gate Charge Characteristics

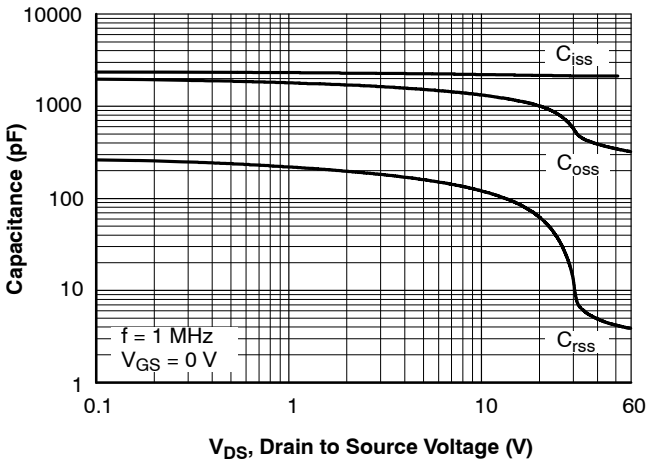


Figure 8. Capacitance vs. Drain to Source Voltage

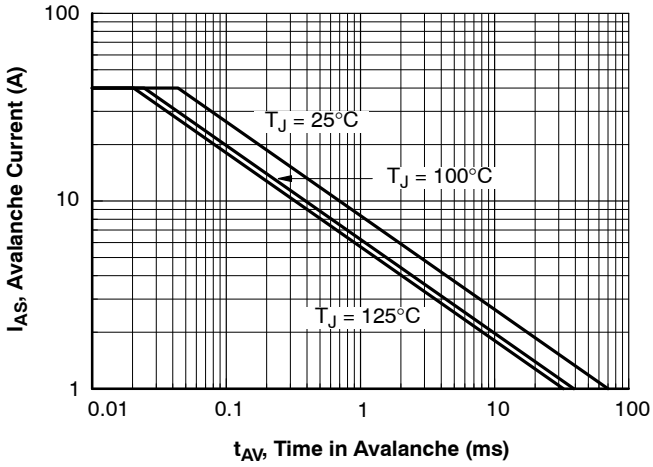


Figure 9. Unclamped Inductive Switching Capability

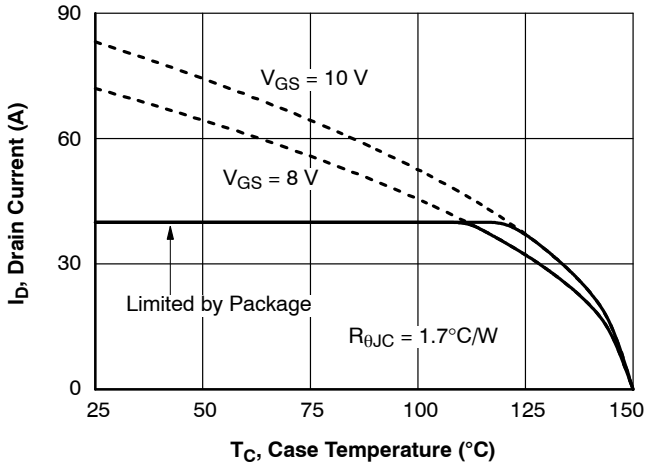


Figure 10. Maximum Continuous Drain Current vs Case Temperature

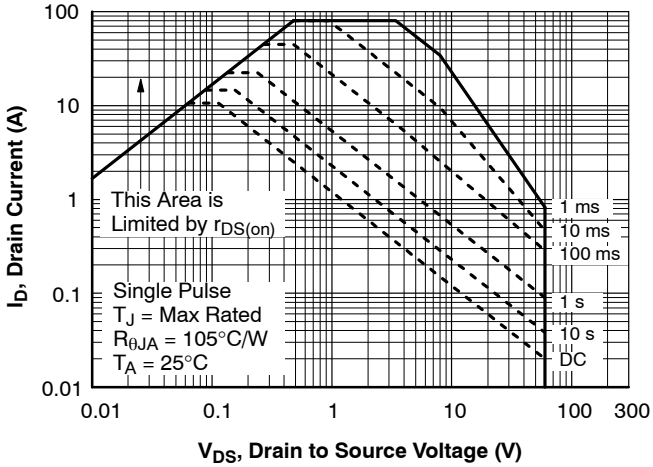


Figure 11. Forward Bias Safe Operating Area

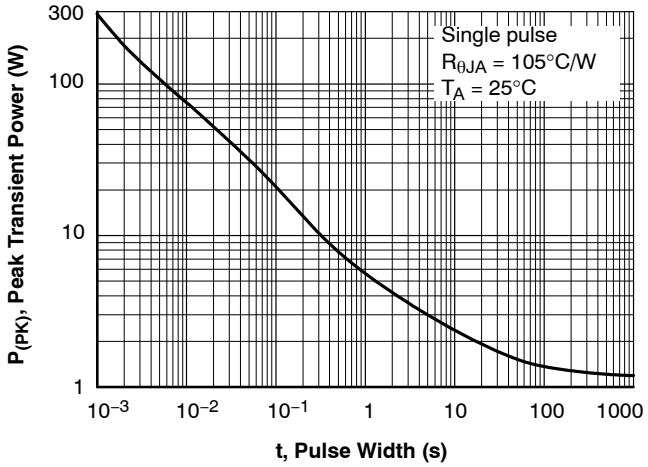


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

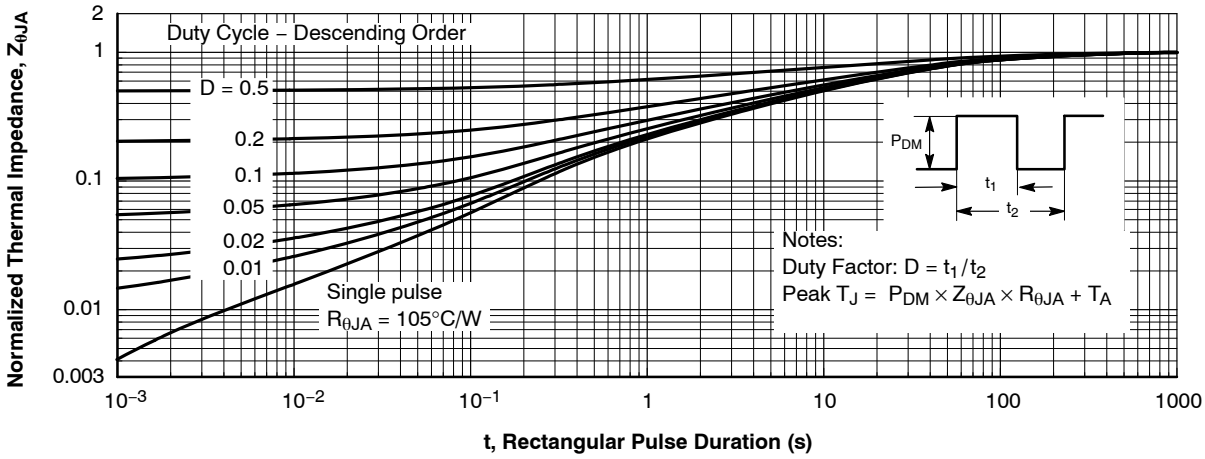


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

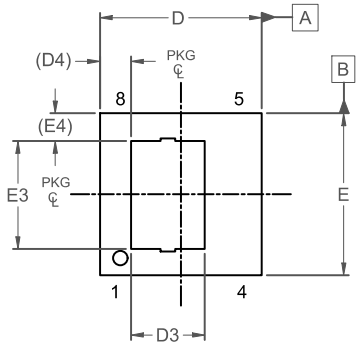
Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FDMC86520DC	86520	DUAL COOL 33	13”	12 mm	3000 Units

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

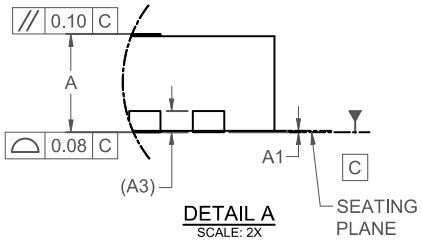
ON Semiconductor®

PQFN8 3.3X3.3, 0.65P
CASE 483AL
ISSUE A

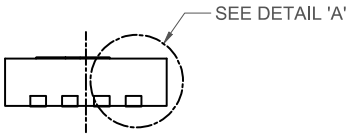
DATE 01 JUN 2021



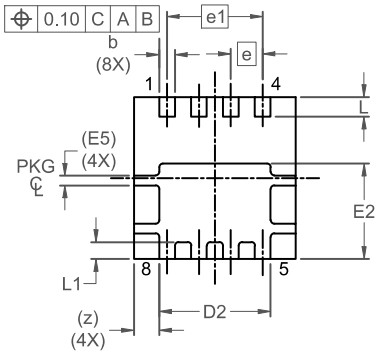
TOP VIEW



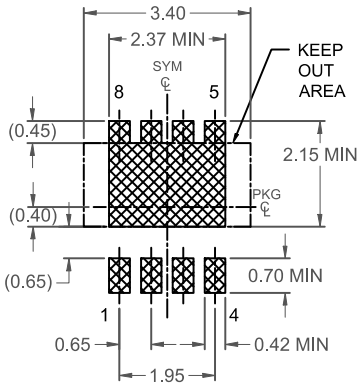
DETAIL A
SCALE: 2X



FRONT VIEW



BOTTOM VIEW



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002CONTROLLING
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.27	0.32	0.37
A3		0.20 REF	
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	1.40	1.55	1.70
D4		0.63 REF	
E	3.20	3.30	3.40
E2	1.90	2.00	2.10
E3	2.10	2.25	2.40
E4		0.56 REF	
E5		0.20 REF	
e		0.65 BSC	
e1		1.95 BSC	
L	0.30	0.40	0.50
L4	0.29	0.39	0.49
z		0.52 REF	

DOCUMENT NUMBER:	**98AON13661G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**PQFN8 3.3X3.3, 0.65P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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