

**AEC-Q101 Qualified 650V GaN FET in TO-247 (source tab)**

**Description**

The TP65H050WS 650V, 50mΩ Gallium Nitride (GaN) FET is a normally-off automotive (AEC-Q101) qualified device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

Transphorm GaN offers improved efficiency over silicon, through lower gate charge, lower crossover loss, and smaller reverse recovery charge.

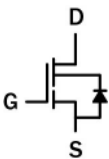
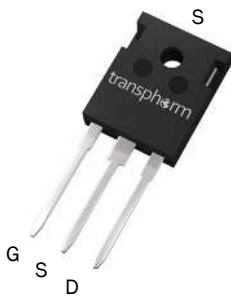
**Related Literature**

- [AN0009](#): Recommended External Circuitry for GaN FETs
- [AN0003](#): Printed Circuit Board Layout and Probing
- [AN0010](#): Paralleling GaN FETs

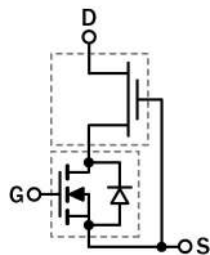
**Ordering Information**

Part Number	Package	Package Configuration
TP65H050WSQA	3 Lead TO-247	Source

TP65H050WSQA  
TO-247  
(top view)



Cascode Schematic Symbol



Cascode Device Structure

**Features**

- AEC-Q101 qualified GaN technology
- Junction temperature rating of 175C
- Dynamic  $R_{DS(on)eff}$  production tested
- Robust design, defined by
  - Intrinsic lifetime tests
  - Wide gate safety margin
  - Transient over-voltage capability
- Very low  $Q_{RR}$
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

**Benefits**

- Improves efficiency/operation frequencies over Si
- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

**Applications**

- Automotive
- Datacom
- Broad industrial
- PV inverter

Key Specifications	
$V_{DSS}$ (V)	650
$V_{DSS(TR)}$ (V)	800
$R_{DS(on)eff}$ (mΩ) max*	60
$Q_{RR}$ (nC) typ	125
$Q_G$ (nC) typ	16

\* Dynamic on-resistance; see Figures 17 and 18

Common Topology Power Recommendations	
CCM bridgeless totem-pole*	3080W max
Hard-switched inverter**	3670W max

Conditions:  $F_{SW}=45kHz$ ;  $T_J=115^\circ C$ ;  $T_{HEATSINK}=90^\circ C$ ; insulator between device and heatsink (6 mil Sil-Pad® K-10); power de-rates at lower voltages with constant current

\*  $V_{IN}=230V_{AC}$ ;  $V_{OUT}=390V_{DC}$

\*\*  $V_{IN}=380V_{DC}$ ;  $V_{OUT}=240V_{AC}$

# TP65H050WSQA

## Absolute Maximum Ratings ( $T_c=25^\circ\text{C}$ unless otherwise stated.)

Symbol	Parameter	Limit Value	Unit	
$V_{DSS}$	Drain to source voltage ( $T_J = -55^\circ\text{C}$ to $150^\circ\text{C}$ )	650	V	
$V_{DSS(TR)}(V)$	Transient drain to source voltage <sup>a</sup>	800		
$V_{GSS}$	Gate to source voltage	$\pm 20$		
$P_D$	Maximum power dissipation @ $T_c=25^\circ\text{C}$	150	W	
$I_D$	Continuous drain current @ $T_c=25^\circ\text{C}$ <sup>b</sup>	36	A	
	Continuous drain current @ $T_c=100^\circ\text{C}$ <sup>b</sup>	25	A	
$I_{DM}$	Pulsed drain current (pulse width: $10\mu\text{s}$ )	150	A	
$(di/dt)_{RDMC}$	Reverse diode $di/dt$ , repetitive <sup>c</sup>	1600	A/ $\mu\text{s}$	
$(di/dt)_{RDMT}$	Reverse diode $di/dt$ , transient <sup>d</sup>	3000	A/ $\mu\text{s}$	
$T_c$	Operating temperature	Case	-55 to +175	$^\circ\text{C}$
$T_J$		Junction	-55 to +175	$^\circ\text{C}$
$T_s$	Storage temperature	-55 to +175	$^\circ\text{C}$	
$T_{SOLD}$	Soldering peak temperature <sup>e</sup>	260	$^\circ\text{C}$	
-	Mounting Torque	80	N cm	

Notes:

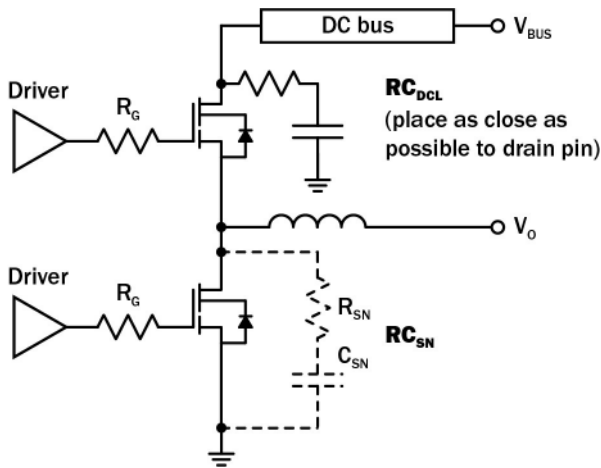
- In off-state, spike duty cycle  $D < 0.01$ , spike duration  $< 1\mu\text{s}$
- For increased stability at high current operation, see Circuit Implementation on page 3
- Continuous switching operation
- $\leq 300$  pulses per second for a total duration  $\leq 20$  minutes
- For 10 sec., 1.6mm from the case

## Thermal Resistance

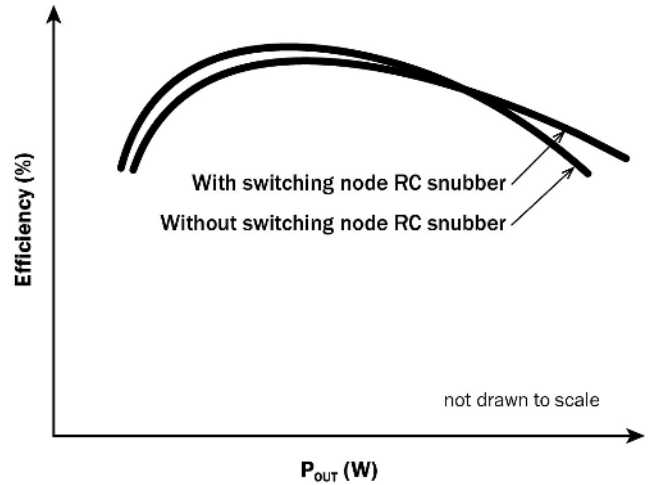
Symbol	Parameter	Maximum	Unit
$R_{\theta JC}$	Junction-to-case	1.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient	40	$^\circ\text{C}/\text{W}$

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## Circuit Implementation



Simplified Half-bridge Schematic



Efficiency vs Output Power

Recommended gate drive: (0V, 12V) with  $R_G = 30\text{-}45\Omega$

Required DC Link RC Snubber ( $RC_{DCL}$ ) <sup>a</sup>	Recommended Switching Node RC Snubber ( $RC_{SN}$ ) <sup>b, c</sup>
$[10\text{nF} + 8\Omega] \times 2$	$100\text{pF} + 10\Omega$

Notes:

- $RC_{DCL}$  should be placed as close as possible to the drain pin
- A switching node RC snubber (C, R) is recommended for high switching currents ( $>70\%$  of  $I_{RDMC1}$  or  $I_{RDMC2}$ ; see page 5 for  $I_{RDMC1}$  and  $I_{RDMC2}$ )
- $I_{RDM}$  values can be increased by increasing  $R_G$  and  $C_{SN}$

Layout Recommendations: ( See also [AN0009](#))

Gate Loop:

- Gate Driver: SiLab Si823x/Si827x
- Keep gate loop compact
- Minimize coupling with power loop

Power loop:

- Minimize power loop path inductance
- Minimize switching node coupling with high and low power plane
- Add DC bus snubber to reduce to voltage ringing
- Add Switching node snubber for high current operation

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## Electrical Parameters (T<sub>J</sub>=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
<b>Forward Device Characteristics</b>						
V <sub>DSS(BL)</sub>	Drain-source voltage	650	—	—	V	V <sub>GS</sub> =0V
V <sub>GS(th)</sub>	Gate threshold voltage	3.3	4	4.8	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =0.7mA
ΔV <sub>GS(th)/T<sub>J</sub></sub>	Gate threshold voltage temperature coefficient	—	-6.2	—	mV/°C	
R <sub>DS(on)eff</sub>	Drain-source on-resistance <sup>a</sup>	—	50	60	mΩ	V <sub>GS</sub> =10V, I <sub>D</sub> =25A
		—	120	—		V <sub>GS</sub> =10V, I <sub>D</sub> =25A, T <sub>J</sub> =175 °C
I <sub>DSS</sub>	Drain-to-source leakage current	—	2.5	25	μA	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V
		—	25	—		V <sub>DS</sub> =650V, V <sub>GS</sub> =0V, T <sub>J</sub> =175 °C
I <sub>GSS</sub>	Gate-to-source forward leakage current	—	—	100	nA	V <sub>GS</sub> =20V
		—	—	-100		V <sub>GS</sub> =-20V
C <sub>ISS</sub>	Input capacitance	—	1000	—	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =400V, f=1MHz
C <sub>OSS</sub>	Output capacitance	—	130	—		
C <sub>RSS</sub>	Reverse transfer capacitance	—	8	—		
C <sub>O(er)</sub>	Output capacitance, energy related <sup>b</sup>	—	190	—	pF	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V to 400V
C <sub>O(tr)</sub>	Output capacitance, time related <sup>c</sup>	—	310	—		
Q <sub>G</sub>	Total gate charge	—	15	24	nC	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V to 10V, I <sub>D</sub> =25A
Q <sub>GS</sub>	Gate-source charge	—	6	—		
Q <sub>GD</sub>	Gate-drain charge	—	4	—		
Q <sub>OSS</sub>	Output charge	—	124	—	nC	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V to 400V
t <sub>D(on)</sub>	Turn-on delay	—	57	—	ns	V <sub>DS</sub> =400V, V <sub>GS</sub> =0V to 12V, I <sub>D</sub> =25A, R <sub>G</sub> = 40Ω
t <sub>R</sub>	Rise time	—	10	—		
t <sub>D(off)</sub>	Turn-off delay	—	88	—		
t <sub>F</sub>	Fall time	—	11	—		

Notes:

- Dynamic on-resistance; see Figures 17 and 18 for test circuit and conditions
- Equivalent capacitance to give same stored energy as V<sub>DS</sub> rises from 0V to 400V
- Equivalent capacitance to give same charging time as V<sub>DS</sub> rises from 0V to 400V

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## Electrical Parameters (T<sub>J</sub>=25 °C unless otherwise stated)

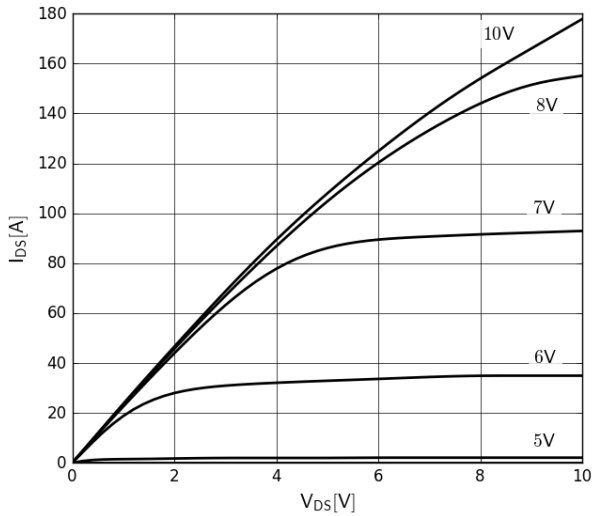
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
<b>Reverse Device Characteristics</b>						
I <sub>S</sub>	Reverse current	—	—	25	A	V <sub>GS</sub> =0V, T <sub>C</sub> =100 °C, ≤20% duty cycle
V <sub>SD</sub>	Reverse voltage <sup>a</sup>	—	1.9	—	V	V <sub>GS</sub> =0V, I <sub>S</sub> =25A
		—	1.4	—		V <sub>GS</sub> =0V, I <sub>S</sub> =11A
t <sub>RR</sub>	Reverse recovery time	—	54	—	ns	I <sub>S</sub> =22A, V <sub>DD</sub> =400V, di/dt=1000A/μs
Q <sub>RR</sub>	Reverse recovery charge	—	125	—	nC	
(di/dt) <sub>RDMC</sub>	Reverse diode di/dt, repetitive <sup>b</sup>	—	—	1600	A/μs	
I <sub>RDMC1</sub>	Reverse diode switching current, repetitive (dc) <sup>c, e</sup>	—	—	24	A	Circuit implementation and parameters on page 3
I <sub>RDMC2</sub>	Reverse diode switching current, repetitive (ac) <sup>c, e</sup>	—	—	28	A	Circuit implementation and parameters on page 3
(di/dt) <sub>RDMT</sub>	Reverse diode di/dt, transient <sup>d</sup>	—	—	3000	A/μs	
I <sub>RDMT</sub>	Reverse diode switching current, transient <sup>d, e</sup>	—	—	36	A	Circuit implementation and parameters on page 3

Notes:

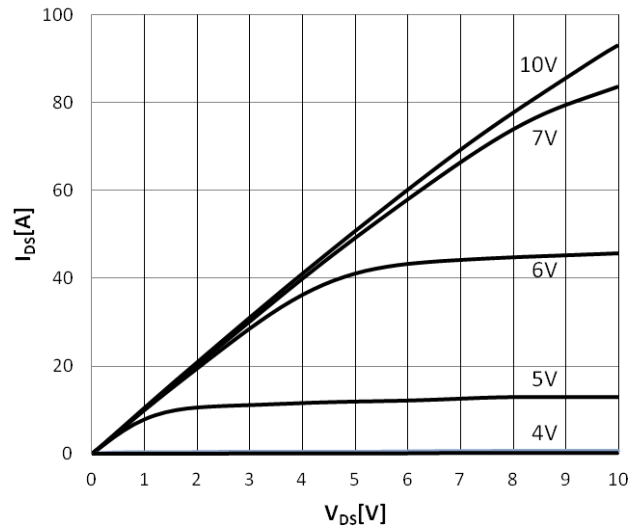
- a. Includes dynamic R<sub>DS(on)</sub> effect
- b. Continuous switching operation
- c. Definitions: dc = dc-to-dc converter topologies; ac = inverter and PFC topologies, 50-60Hz line frequency
- d. ≤300 pulses per second for a total duration ≤20 minutes
- e. I<sub>RDM</sub> values can be increased by increasing R<sub>G</sub> and C<sub>SN</sub> on page 3

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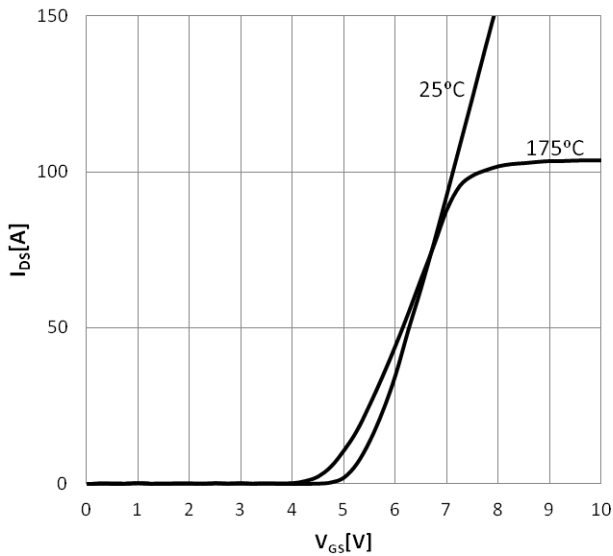
Typical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise stated)



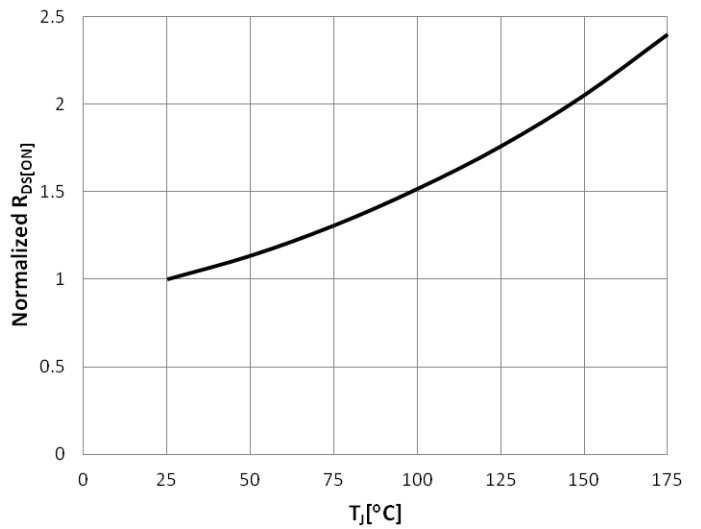
**Figure 1. Typical Output Characteristics  $T_J=25^\circ\text{C}$**   
Parameter:  $V_{GS}$



**Figure 2. Typical Output Characteristics  $T_J=175^\circ\text{C}$**   
Parameter:  $V_{GS}$



**Figure 3. Typical Transfer Characteristics**  
 $V_{DS}=10\text{V}$ , parameter:  $T_J$



**Figure 4. Normalized On-resistance**  
 $I_D=25\text{A}$ ,  $V_{GS}=10\text{V}$

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Typical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise stated)

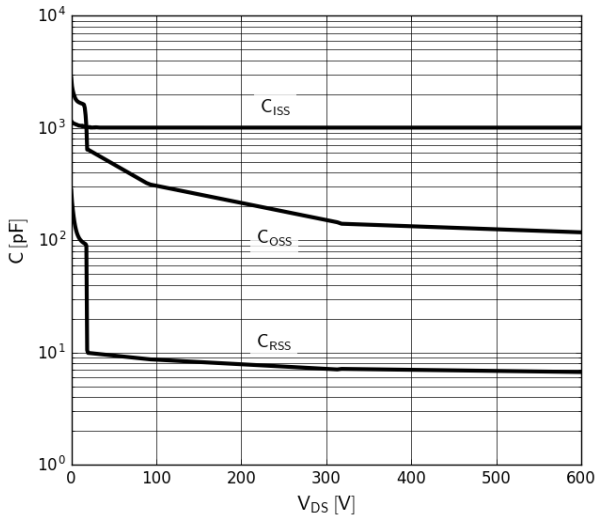


Figure 5. Typical Capacitance

$V_{GS}=0V$ ,  $f=1\text{MHz}$

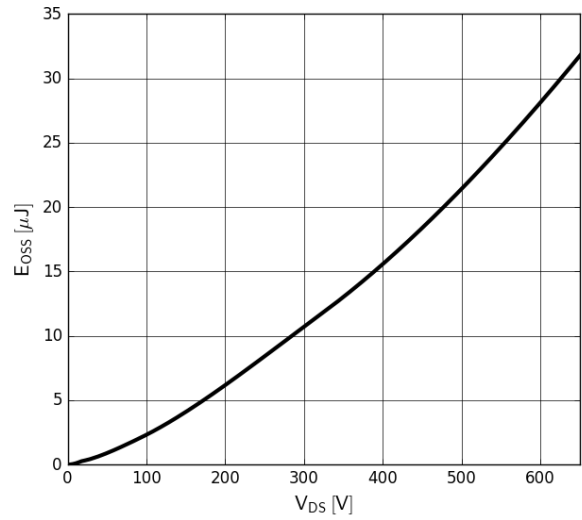


Figure 6. Typical  $C_{OSS}$  Stored Energy

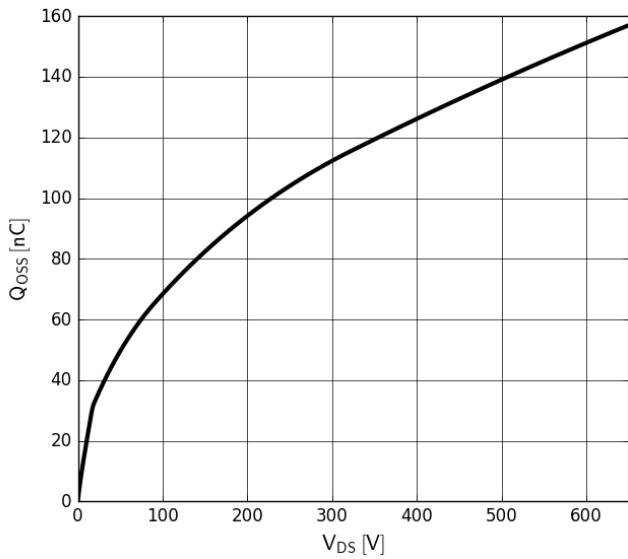


Figure 7. Typical  $Q_{OSS}$

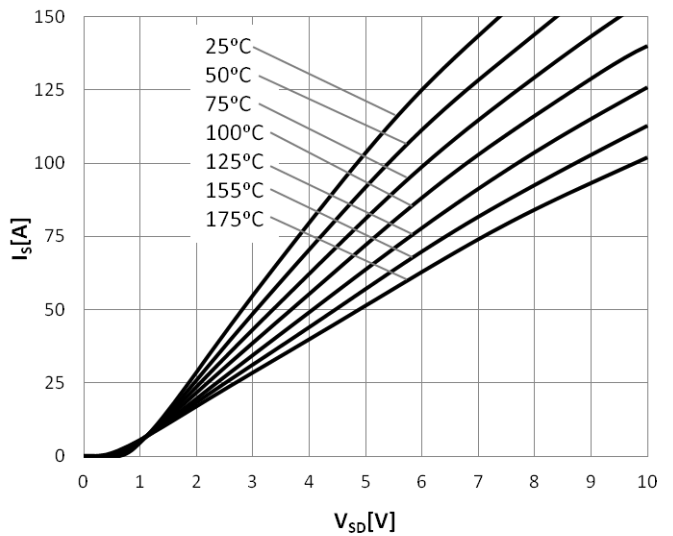


Figure 8. Forward Characteristics of Rev. Diode

$I_S=f(V_{SD})$ , parameter:  $T_J$

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Typical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise stated)

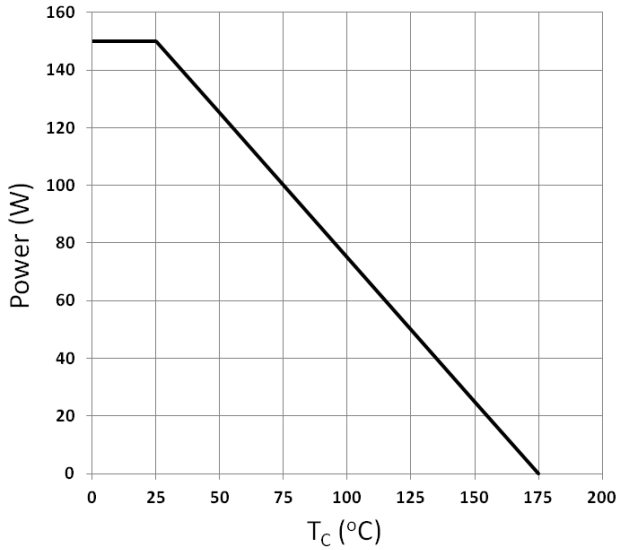


Figure 9. Power Dissipation

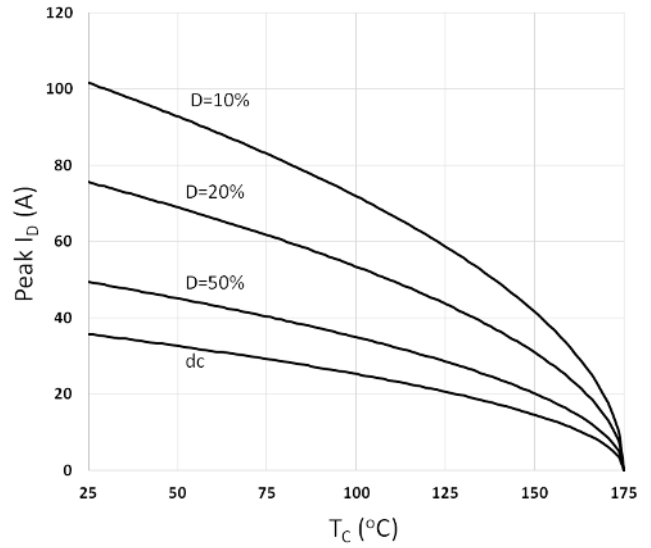


Figure 10. Current Derating  
Pulse width  $\leq 10\mu\text{s}$ ,  $V_{GS} \geq 10\text{V}$

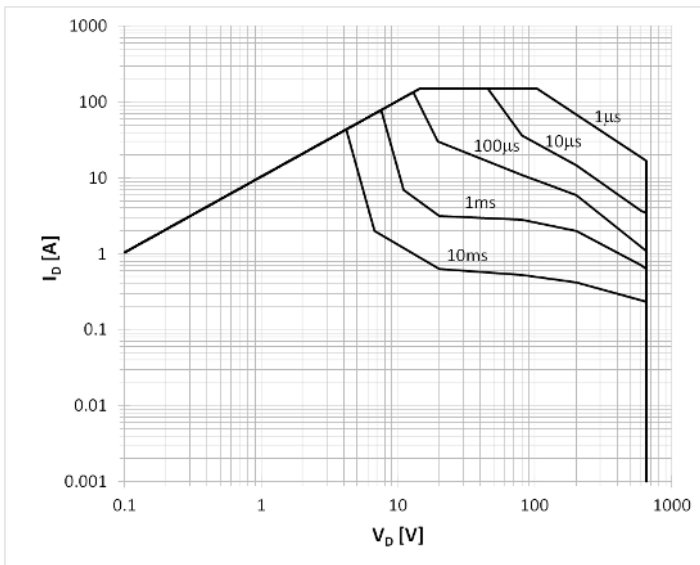


Figure 11. Safe Operating Area  $T_C=25^\circ\text{C}$

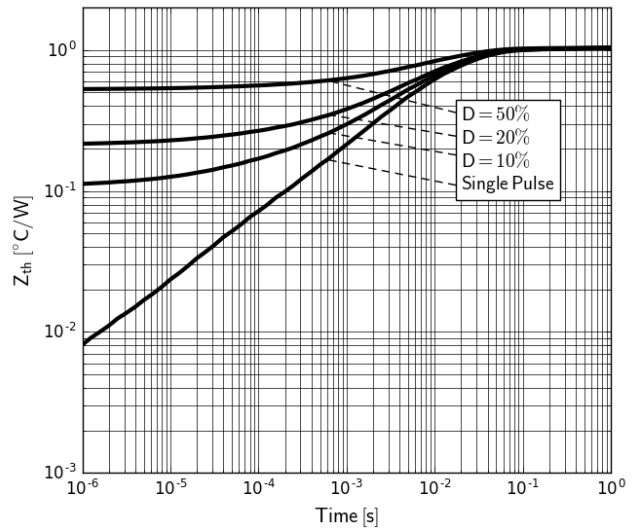
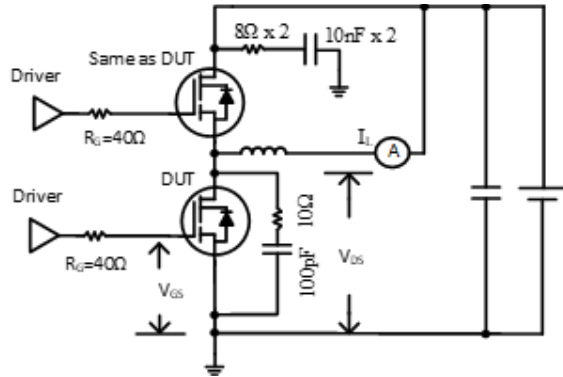


Figure 12. Transient Thermal Resistance

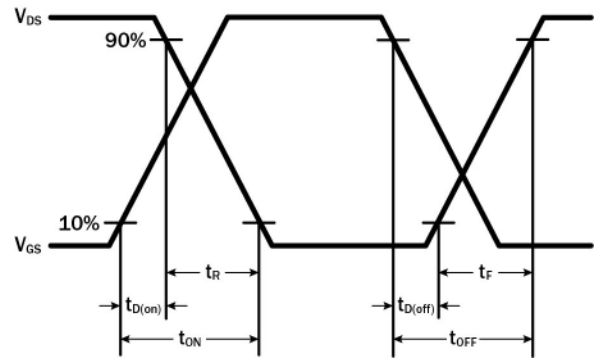


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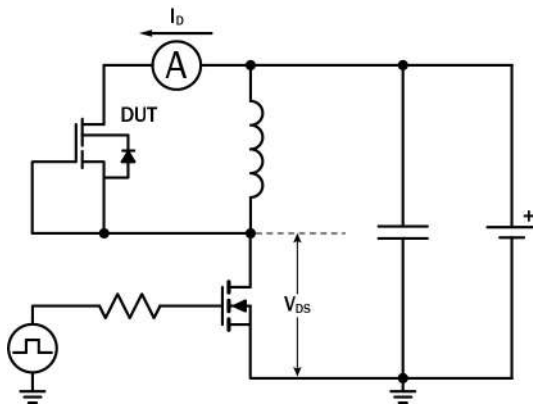
## Test Circuits and Waveforms



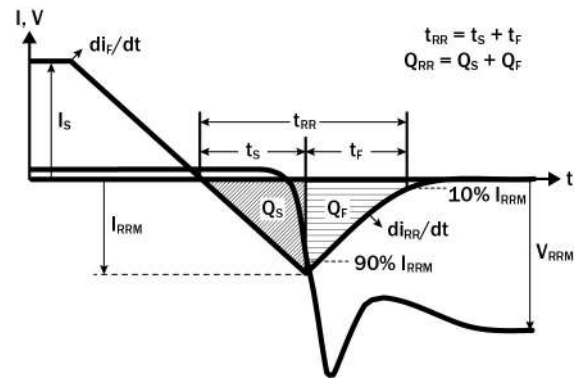
**Figure 13. Switching Time Test Circuit**  
(see circuit implementation on page 3 for methods to ensure clean switching)



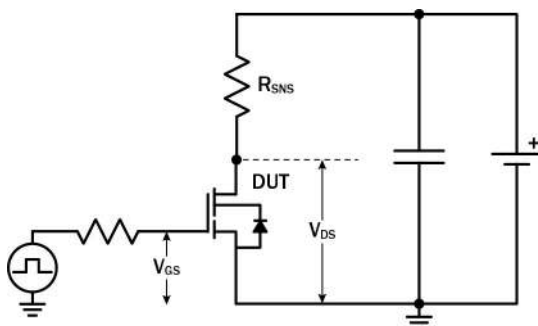
**Figure 14. Switching Time Waveform**



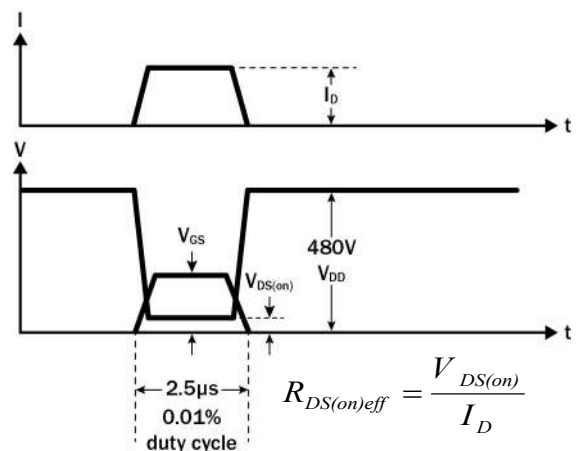
**Figure 15. Diode Characteristics Test Circuit**



**Figure 16. Diode Recovery Waveform**



**Figure 17. Dynamic  $R_{DS(on)eff}$  Test Circuit**



**Figure 18. Dynamic  $R_{DS(on)eff}$  Waveform**

# TP65H050WSQA

## Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

### When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See <a href="#">AN0003</a> : Printed Circuit Board Layout and Probing	

## GaN Design Resources

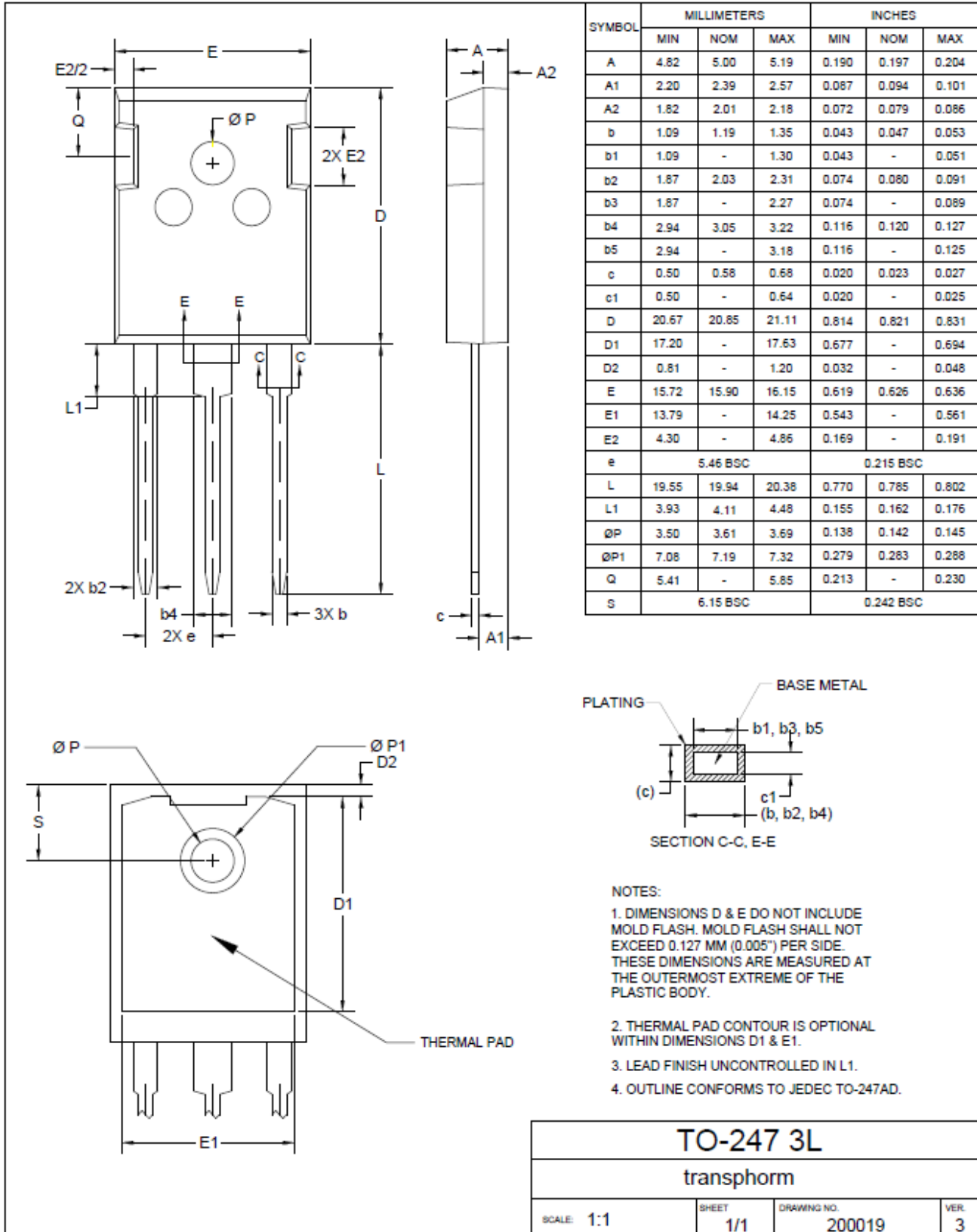
The complete technical library of GaN design tools can be found at [transphormusa.com/design](https://transphormusa.com/design):

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

# TP65H050WSQA

Mechanical

3 Lead TO-247 Package



# TP65H050WSQA

## Revision History

Version	Date	Change(s)
0	12/6/2017	Initial
1	6/13/2018	Datasheet completed
2	12/21/2018	1) Add max mounting torque 2) Update maximum continuous current 3) Update Qoss 4) Switching with current test condition
3	3/31/2021	Update Figure 13 and added layout recommendation on Page3