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NTE74LS192
Integrated Circuit
TTL – Synchronous 4–Bit Up/Down Counter

Description:

The NTE74LS192 is a synchronous BCD reversible up/down counter in a 16–Lead plastic DIP type package having the complexity of 55 equivalent gates. Synchronous operation is provided by having all flip–flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master–slave flip–flops are triggered by a low–to–high transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

This counter is fully programmable; that is, each output may be preset to either level by entering the desired data of the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counter to be used as a modulo–N divider by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

This device was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up–counting and down–counting functions. The borrow output produces a pulse equal in width to the count–up input when an overflow condition exists. The counter can then be easily cascaded by feeding the borrow and carry outputs to the count–down and count–up inputs respectively of the succeeding counter.

Features:

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip–Flop
- Fully Independent Clear Input

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 7V
Power Dissipation, P_D 95mW
Operating Temperature Range, T_A . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	−400	μA
Low−Level Output Current	I_{OL}	–	–	8	mA
Clock Frequency	f_{clock}	0	–	25	MHz
Width of Any Input Pulse	t_w	20	–	–	ns
Clear Inactive Setup Time	t_{su}	15	–	–	ns
Load Inactive Setup Time	t_{su}	15	–	–	ns
Data Setup Time	t_{su}	20	–	–	ns
Data Hold Time	t_h	5	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}			2	–	–	V
Low−Level Input Voltage	V_{IL}			–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA		–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX, I_{OH} = −400μA		2.7	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	–	0.15	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 7V		–	–	0.1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V		–	–	20	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V		–	–	−0.4	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4		−20	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5		–	19	34	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time and duration of short−circuit should not exceed one second.

Note 5. I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5V.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 2kΩ, C_L = 15pF	25	32	–	MHz
Propagation Delay Time (From UP Input to Any $\overline{CO}$ Output)	t_{PLH}		–	17	26	ns
	t_{PHL}		–	18	24	ns
Propagation Delay Time (From DOWN Input to $\overline{BO}$ Output)	t_{PLH}		–	16	24	ns
	t_{PHL}		–	15	24	ns
Propagation Delay Time (From UP or DOWN Input to Q Output)	t_{PLH}		–	27	38	ns
	t_{PHL}		–	30	47	ns
Propagation Delay Time (From $\overline{LOAD}$ Input to Q Output)	t_{PLH}		–	24	40	ns
	t_{PHL}		–	25	40	ns
Propagation Delay Time (From CLR Input to Q Output)	t_{PHL}		–	23	35	ns

Pin Connection Diagram