TRF372017 Integrated IQ Modulator PLL/VCO

1 Features

- Fully Integrated PLL/VCO and IQ Modulator
- LO Frequency from 300 MHz to 4.8 GHz
- 76-dBc Single-Carrier WCDMA ACPR at –8-dBm Channel Power
- OIP3 of 26 dBm
- P1dB of 11.5 dBm
- Integer/Fractional PLL
- Phase Noise –132 dBc/Hz (at 1 MHz, f_{VCO} of 2.3 GHz)
- Low Noise Floor: –160 dBm/Hz
- Input Reference Frequency Range: Up to 160 MHz
- VCO Frequency Divided by 1-2-4-8 Output

2 Applications

- Wireless Infrastructure
  - CDMA: IS95, UMTS, CDMA2000, TD-SCDMA
  - TDMA: GSM, IS-136, EDGE/UWC-136
  - LTE
- Wireless Local Loop
- Point-to-Point Wireless Access
- Wireless MAN Wideband Transceivers

3 Description

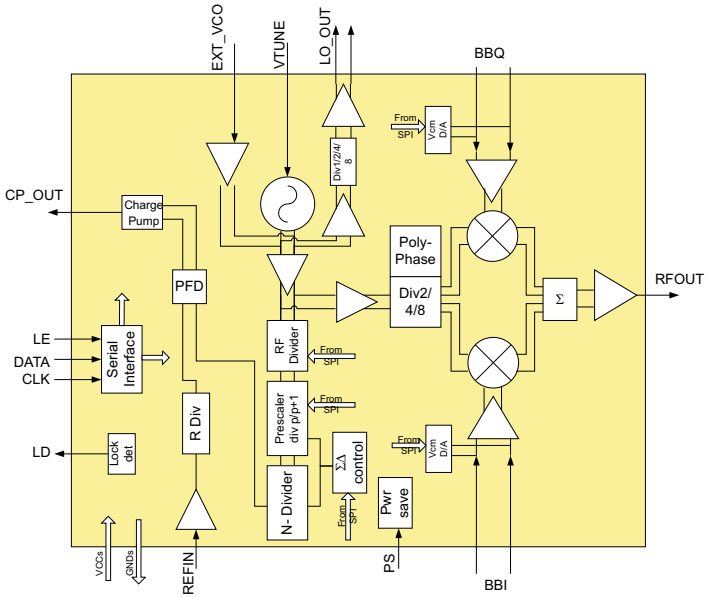
TRF372017 is a high-performance, direct up-conversion device, integrating a high-linearity, low-noise IQ modulator and an integer-fractional PLL/VCO. The VCO uses integrated frequency dividers to achieve a wide, continuous tuning range of 300 MHz to 4800 MHz. The LO is available as an output with independent frequency dividers. The device also accepts input from an external LO or VCO. The modulator baseband inputs can be biased either internally or externally. Internal DC offset adjustment enables carrier cancellation. The device is controlled through a 3-wire serial programming interface (SPI). A control pin invokes power-save mode to reduce power consumption while keeping the VCO locked for fast start-up.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRF372017	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2013) to Revision E — **Page**

- Added *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (May 2012) to Revision D — **Page**

- Changed text string from Reg 1, B[30..28] = [000] to Reg 0, B[30..28] = [000] in the Description column associated with RB_REG<0>, RB_REG<1>, and RB_REG<2> ... 44

Changes from Revision B (March 2012) to Revision C — **Page**

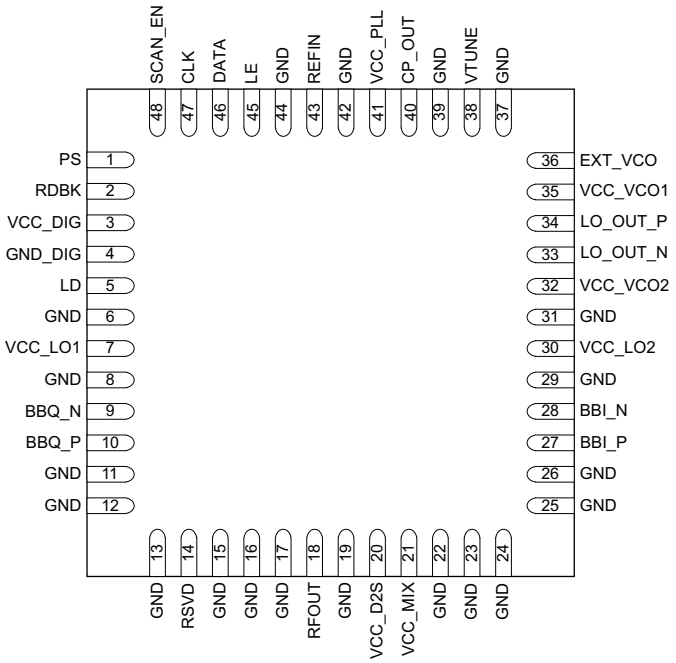
- Added graph titles to Figure 56 and 57 that were missing in Revision B ... 17

Changes from Revision A (August 2010) to Revision B — **Page**

- Deleted Comments column from Table 1 ... 8
- Changed Figures 12 through Figure 27 ... 10
- Changed the text under *Integer and Fractional Mode Selection* through *Practical Limit on Maximum PFD Frequency*. ... 23
- Changed RDIV = 20 to RDIV = 2 in *Setup Example for Fractional Mode*. ... 26
- Changed Recommended Value of EN_LD_ISOURCE from 1 to 0 in Table 1 ... 27
- Changed column heading from Default Value to Reset Value in register tables 1, 2, 3, 4, 5, 6, and 7 ... 34
- Added recommended programming [xx] to various Description statements in register tables 2, 5, 6, and 7. ... 37
- Changed Register 4, Bit21/Bit22 Description statement from Off to Normal. ... 39
- Changed Column heading from Default Value to Reset Value in Readback mode section, Register 0 ... 43
- Changed Bit5 name from CHIP_ID to CHIP_ID _0 and changed Bit6 name from NU to CHIP_ID_1, Reset Value to 1 ... 44
- Changed image in Figure 87. ... 48
- Changed the text in the *Application Layout*, and added link to Figure 95 ... 51

5 Pin Configuration and Functions

RGZ Package
48-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BBI_P	27	I	Base-band in-phase input: positive terminal. Internal 5 kΩ to VCM generator. If VCM is internally generated (PWD_BB_VCM = 0), external AC coupling caps and 100-Ω differential termination to BBI_N is required.
BBI_N	28	I	Base-band in-phase input: negative terminal. Internal 5 kΩ to VCM generator. If VCM is internally generated (PWD_BB_VCM = 0), external AC coupling caps and 100-Ω differential termination to BBI_P is required.
BBQ_N	9	I	Base-band in-quadrature input: negative terminal. Internal 5 kΩ to VCM generator. If VCM is internally generated (PWD_BB_VCM = 0), external AC coupling caps and 100-Ω differential termination to BBQ_P is required.
BBQ_P	10	I	Base-band in-quadrature input: positive terminal. Internal 5 kΩ to VCM generator. If VCM is internally generated (PWD_BB_VCM = 0), external AC coupling caps and 100-Ω differential termination to BBQ_N is required.
CLK	47	I	SPI clock input. Digital input. High impedance.
CP_OUT	40	O	Charge pump output
DATA	46	I	SPI data input. Digital input. High impedance.
EXT_VCO	36	I	External local oscillator input. High impedance. Normally AC-coupled.
GND	6, 8, 11, 12, 13, 15, 16, 17, 19, 22, 23, 24, 25, 26, 29, 31, 37, 39, 42, 44	—	Ground
GND_DIG	4	—	Digital ground
LD	5	O	PLL lock detect output, as configured by MUX_CTRL. Digital output pins can source or sink up to 8 mA of current.
LE	45	I	SPI latch enable. Digital input. High impedance.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
LO_OUT_N	33	O	Local oscillator output: negative terminal. Open collector output. A pullup is required. Normally AC-coupled.
LO_OUT_P	34	O	Local oscillator output: positive terminal. Open collector output. A pullup is required. Normally AC-coupled.
PS	1	I	Power saving mode enable (Low = normal mode; High = power saving mode)
RDBK	2	O	SPI internal registers readback output. Digital output pins can source or sink up to 8 mA of current.
REFIN	43	I	Reference clock input. High impedance. Normally AC-coupled.
RFOUT	18	O	RF output. Internally matched to 50-Ω output. Normally AC-coupled.
RSVD	14	—	Reserved. Normally open.
SCAN_EN	48	I	Internal testing mode digital input. Connect to ground in normal operation
VCC_D2S	20	—	5-V modulator output buffer power supply
VCC_DIG	3	—	3.3-V digital power supply
VCC_LO1	7	—	3.3-V Tx path local oscillator chain power supply
VCC_LO2	30	—	3.3-V output local oscillator chain power supply
VCC_MIX	21	—	5-V modulator power supply
VCC_PLL	41	—	3.3-V PLL power supply
VCC_VCO1	35	—	3.3-V VCO power supply
VCC_VCO2	32	—	3.3-V to 5-V VCO power supply
VTUNE	38	I	VCO control voltage input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
	Supply voltage(3)	–0.3	5.5	V
	Digital I/O voltage	–0.3	V_{CC} + 0.5	V
T_J	Operating virtual junction temperature	–40	150	°C
T_A	Operating ambient temperature	–40	85	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ESD rating not valid for RF sensitive pins.
(3) All voltage values are with respect to network ground terminal.

6.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC5V}	5-V power supply voltage	4.5	5	5.5	V
V_{CC3V}	3.3-V power supply voltage	3	3.3	3.6	V
VCC_VCO2	3.3-V to 5-V power supply voltage	3	3.3	5.5	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating virtual junction temperature	–40		125	°C

6.3 Thermal Information

THERMAL METRIC(1)		TRF372017 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.4 Electrical Characteristics

V_{CC5V} = 5 V, V_{CC3V} = 3.3 V, VCC_VCO2 = 3.3 V, T_A = 25°C, internal LO, internal VCM (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PARAMETERS						
I_{CC}	Total supply current, LO on (1)	3.3-V power supply, LO on		200	250	mA
		5-V power supply, LO on		117	148	mA
	Supply current, LO on (1)	VCC_DIG, LO on		3	5	mA
		VCC_LO1 and VCC_LO2		121	130	mA
		VCC_D2S		43	60	mA
		VCC_MIX		74	90	mA
		VCC_VCO1		20	28	mA
		VCC_VCO2		17	20	
		LO_OUT_N and LO_OUT_P		17	28	mA
		VCC_PLL		24	40	mA
	Total supply current, LO off (1)	3.3-V power supply, LO off		165	204	mA
		5-V power supply, LO off		117	149	mA
	Total supply current, PS on (1)	3.3-V power supply, PS on		65	94	mA
		5-V power supply, PS on		51	73	mA
BASEBAND INPUTS						
V_{cm}	I and Q input DC common voltage (2)	Externally generated		1.7		V
		Set internally	1.6	1.7	1.85	V
BW	1-dB input frequency bandwidth			1000		MHz
Z_I	Input Impedance	Resistance		5		kΩ
		Parallel Capacitance		3		pF
BASEBAND INPUT DC OFFSET CONTROL D/A (3)						
	Number of bits	Programmed through SPI		8		
	Programmable DC offset setting	|BBI_P - BBI_N| or |BBQ_P - BBQ_N|, 100-Ω differential load			0.02	V
DIGITAL INTERFACE						
V_{IH}	High-level input voltage		2	3.3		V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage	Referenced to VCC_DIG	0.8 × Vcc			V
V_{OL}	Low-level output voltage	Referenced to VCC_DIG			0.2 × Vcc	V
REFERENCE OSCILLATOR PARAMETERS						
F_{ref}	Reference frequency				160	MHz
	Reference input sensitivity		0.2		3.3	Vp-p
	Reference input impedance	Parallel capacitance		5		pF
		Parallel resistance	3900			Ω
PFD CHARGE PUMP						
	PFD frequency (4)				100	MHz
I_{CP}	Charge pump current	SPI programmable		1.94		mA
IQ MODULATOR OUTPUT, F_{LO} = 750 MHz						
G	Voltage gain	Output RMS voltage over se input I (or Q) RMS voltage	–4	–3.2	–2.4	dB
P1dB	Output compression point			11		dBm
IP3	Output IP3	2 input tones at 4.5 and 5.5 MHz		26		dBm
IP2	Output IP2	2 input tones at 4.5 and 5.5 MHz		56.5		dBm
	Carrier feedthrough	Unadjusted		–43.5		dBm
	Sideband suppression	Unadjusted		–46		dBc
	Output return loss			10		dB

(1) Maximum current is worst-case overvoltage, temperature, and expected process variations.
(2) The TRF372017 can generate the input common voltage internally or can accept an external common mode voltage. The two modes are selectable through SPI.
(3) When the internal input common mode voltage is selected, it is possible to apply some DC offset with the integrated D/A.
(4) See Application Information for discussion on selection of PFD frequency.

Electrical Characteristics (continued)

V_{CC5V} = 5 V, V_{CC3V} = 3.3 V, VCC_VCO2 = 3.3 V, T_A = 25°C, internal LO, internal VCM (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output noise	DC only to BB inputs; 13-MHz offset from LO; P_{out} = –10 dBm		–162		dBm/Hz
IQ MODULATOR OUTPUT, F_{LO} = 900 MHz						
G	Voltage gain	Output RMS voltage over se input I (or Q) RMS voltage	–4	–3.4	–2.4	dB
P1dB	Output compression point			11		dBm
IP3	Output IP3	2 input tones at 4.5 and 5.5 MHz		26.5		dBm
IP2	Output IP2	2 input tones at 4.5 and 5.5 MHz		56.5		dBm
	Carrier feedthrough	Unadjusted		–43		dBm
	Sideband suppression	Unadjusted		–45		dBc
	Output return loss			10		dB
	Output noise	DC only to BB inputs; 13-MHz offset from LO; P_{out} = –10 dBm		–160		dBm/Hz
IQ MODULATOR OUTPUT, F_{LO} = 2150 MHz						
G	Voltage gain	Output RMS voltage over se input I (or Q) RMS voltage	–4.2	–3.1	–2	dB
P1dB	Output compression point			11.5		dBm
IP3	Output IP3	2 input tones at 4.5 and 5.5 MHz		25		dBm
IP2	Output IP2	2 input tones at 4.5 and 5.5 MHz		56		dBm
	Carrier feedthrough	Unadjusted		–40		dBm
	Sideband suppression	Unadjusted		–32		dBc
	Output return loss			10		dB
	Output noise	DC only to BB inputs; 13-MHz offset from LO; P_{out} = –10 dBm		–158		dBm/Hz
ACPR	Adjacent-channel power ratio	1 WCDMA signal; P_{out} = –8 dBm		–75		dBc
		2 WCDMA signals; P_{out} = –11 dBm per carrier		71		
IQ MODULATOR OUTPUT, F_{LO} = 2700 MHz						
G	Voltage gain	Output RMS voltage over se input I (or Q) RMS voltage	–4.1	–2.7	–1.3	dB
P1dB	Output compression point			12		dBm
IP3	Output IP3	2 input tones at 4.5 and 5.5 MHz		26.5		dBm
IP2	Output IP2	2 input tones at 4.5 and 5.5 MHz		50		dBm
	Carrier feedthrough	Unadjusted		–43		dBm
	Sideband suppression	Unadjusted		–41		dBc
	Output return loss			10		dB
	Output noise	DC only to BB inputs; 13-MHz offset from LO; P_{out} = –10 dBm		–153		dBm/Hz
LOCAL OSCILLATOR						
F_{VCO}	Frequency range	VCO range	2400		4800	MHz
		Divide by 2	1200		2400	
		Divide by 4	600		1200	
		Divide by 8	300		600	
	Free running VCO	10 kHz		–85		dBc/Hz
	Phase noise, Fout = 2.3 GHz	1 MHz		–132		dBc/Hz
		10 MHz		–150		dBc/Hz
		50 MHz		–153		dBc/Hz
P_{LO}	LO output power(5)	100-Ω differential, external load; single-ended	–2.5	3		dBm

(5) With VCO frequency at 4.6 GHz and LO in divide-by-2 mode at 2.3 GHz

6.5 Timing Requirements - SPI: Writing Phase(1)

		MIN	TYP	MAX	UNIT
t_h	Hold time, data to clock	20			ns
t_{SU1}	Setup time, data to clock	20			ns
$T_{(CH)}$	Clock low duration	20			ns
$T_{(CL)}$	Clock high duration	20			ns
t_{SU2}	Setup time, clock to enable	20			ns
$t_{(CLK)}$	Clock period	50			ns
t_W	Enable time	50			ns
t_{SU3}	Setup time, latch to data	70			ns

(1) See Figure 1 for timing diagram.

6.6 Timing Requirements - SPI: Read-Back Phase(1)

		MIN	TYP	MAX	UNIT
t_h	Hold time, data to clock	20			ns
t_{SU1}	Setup time, data to clock	20			ns
$T_{(CH)}$	Clock low duration	20			ns
$T_{(CL)}$	Clock High duration	20			ns
t_{SU2}	Setup time, clock to enable	20			ns
t_d	Delay time, clock to readback data output	10			ns
t_W	Enable time(2)	50			ns
$t_{(CLK)}$	Clock period	50			ns

(1) See Figure 2 for timing diagram.
(2) Equals Clock period

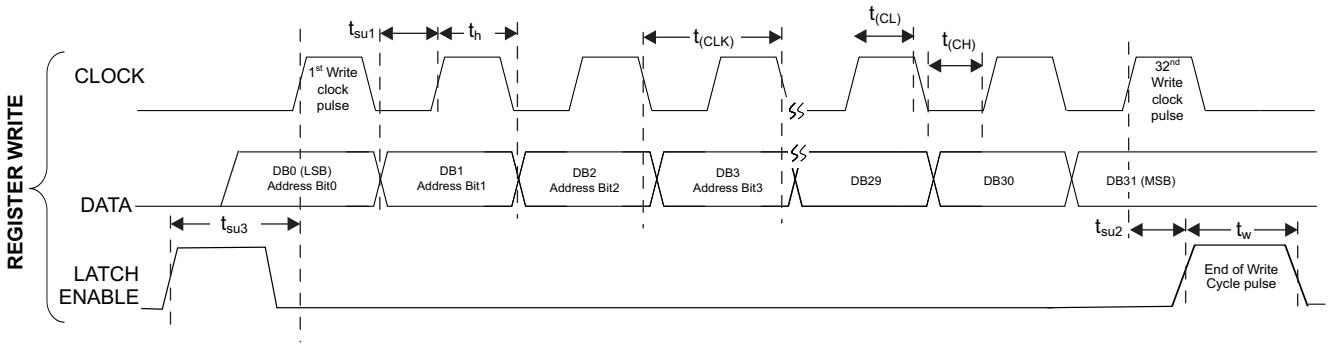


Figure 1. SPI Write Timing Diagram

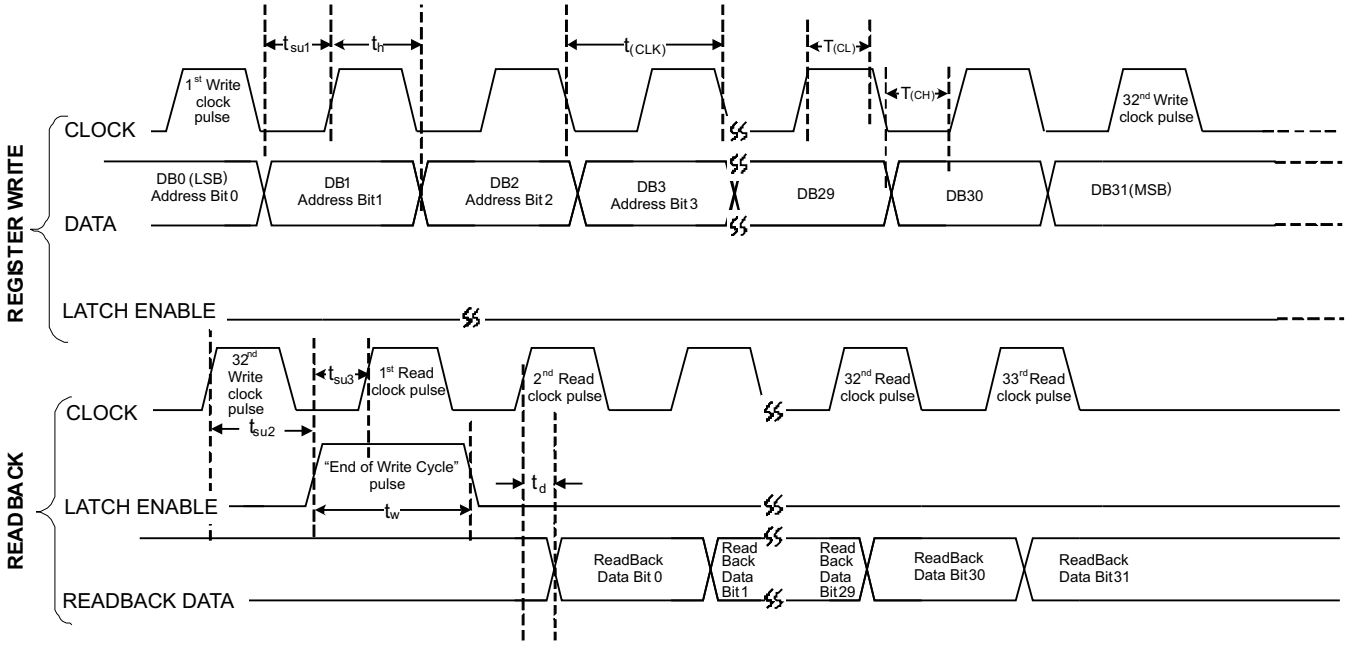


Figure 2. SPI Read-Back Timing Diagram

6.7 Typical Characteristics

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

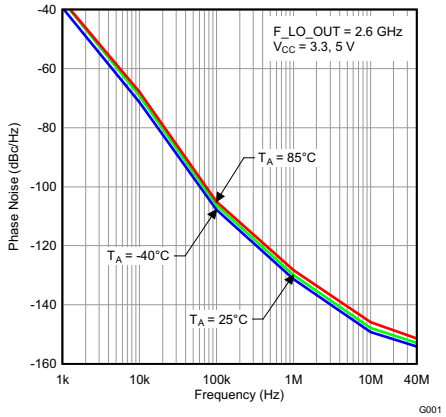


Figure 3. Open-Loop Phase Noise vs Frequency and Temperature

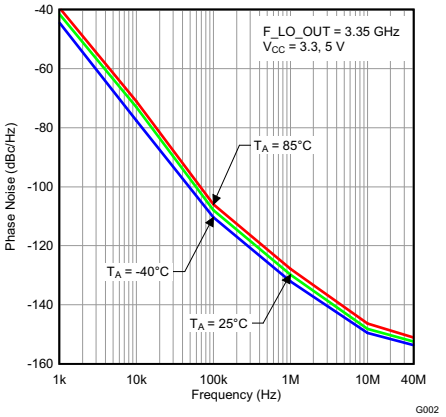


Figure 4. Open Loop Phase Noise vs Frequency and Temperature

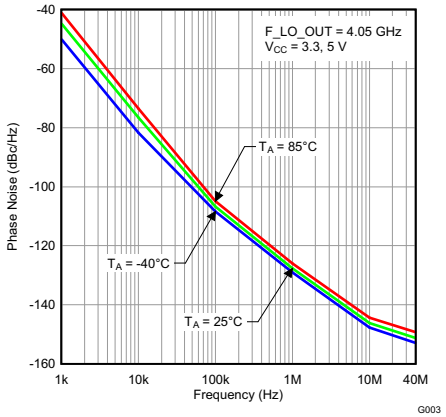


Figure 5. Open Loop Phase Noise vs Frequency and Temperature

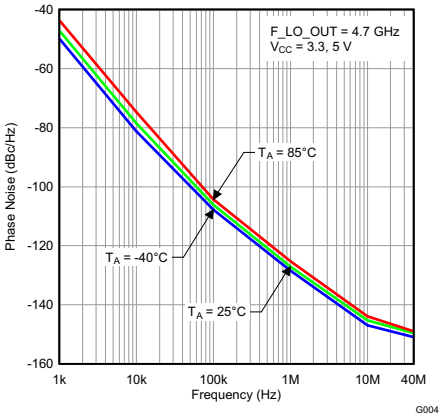


Figure 6. Open Loop Phase Noise vs Frequency and Temperature

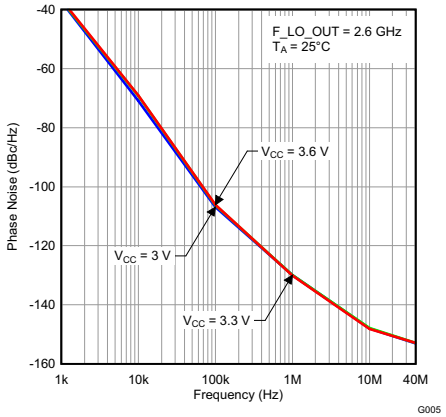


Figure 7. Open Loop Phase Noise vs Frequency and Supply Voltage

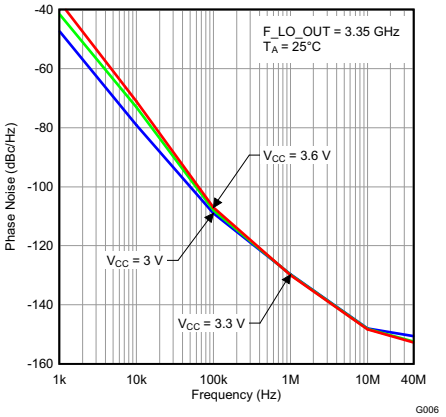


Figure 8. Open Loop Phase Noise vs Frequency and Supply Voltage

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

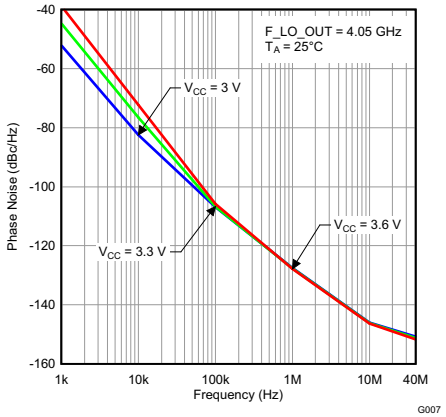


Figure 9. Open Loop Phase Noise vs Frequency and Supply Voltage

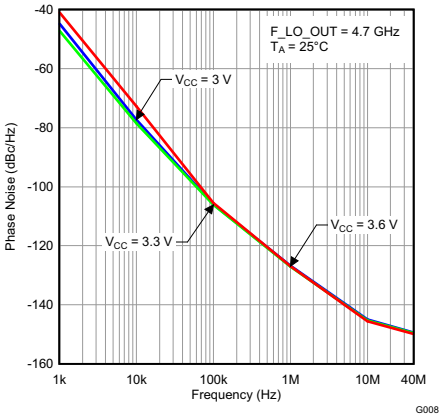


Figure 10. Open Loop Phase Noise vs Frequency and Supply Voltage

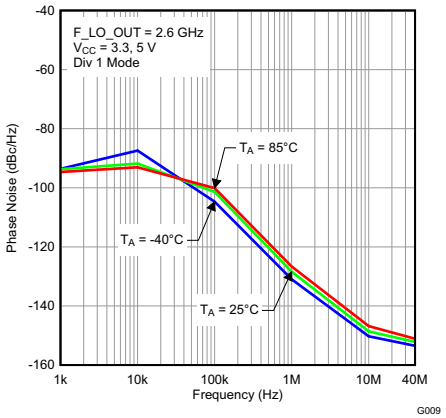


Figure 11. Closed Loop Phase Noise vs Frequency and Temperature

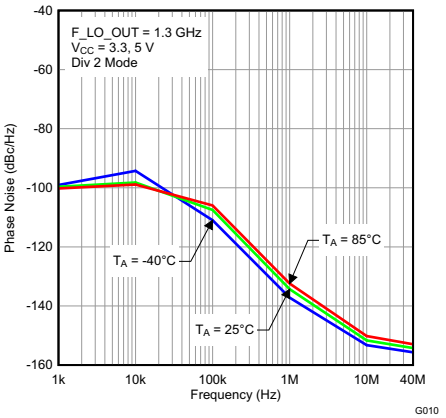


Figure 12. Closed Loop Phase Noise vs Frequency and Temperature

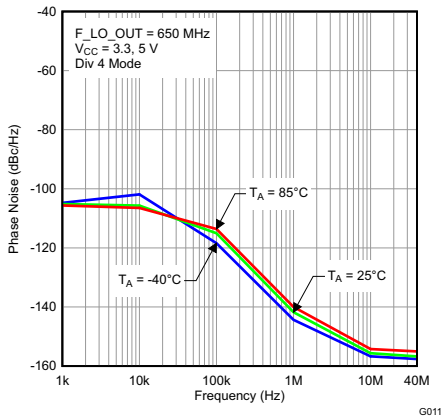


Figure 13. Closed Loop Phase Noise vs Frequency and Temperature

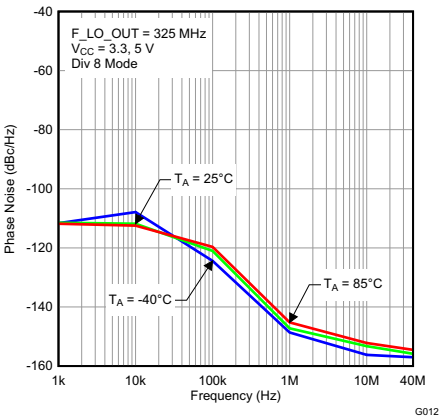


Figure 14. Closed Loop Phase Noise vs Frequency and Temperature

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

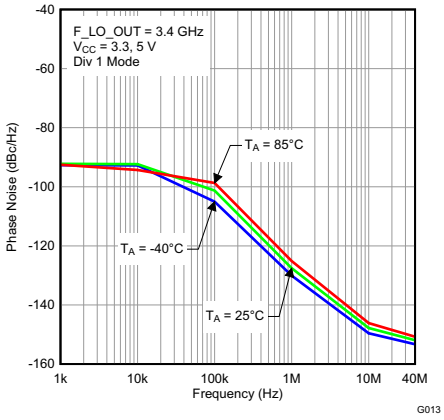


Figure 15. Closed Loop Phase Noise vs Frequency and Temperature

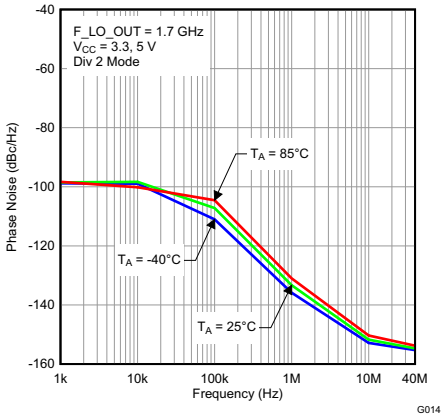


Figure 16. Closed Loop Phase Noise vs Frequency and Temperature

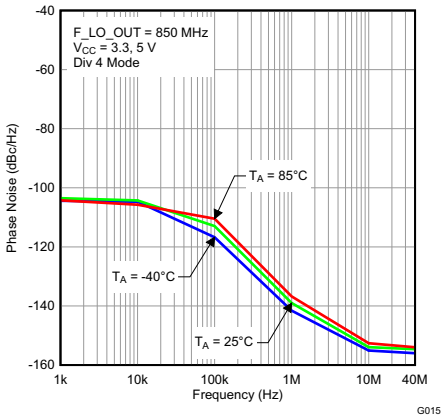


Figure 17. Closed Loop Phase Noise vs Frequency and Temperature

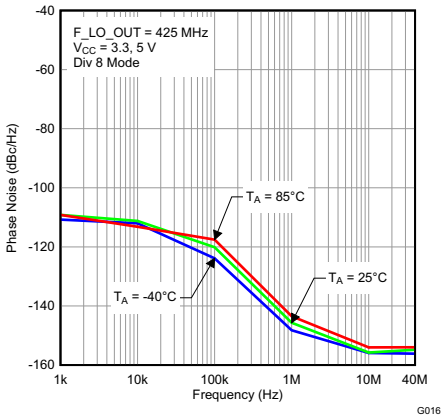


Figure 18. Closed Loop Phase Noise vs Frequency and Temperature

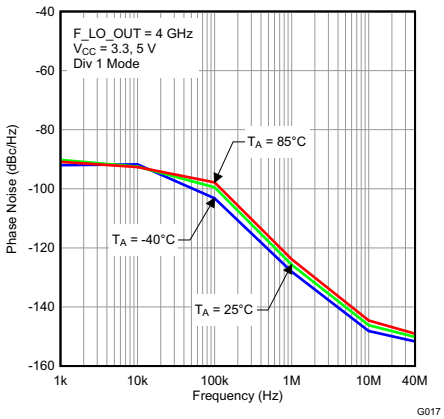


Figure 19. Closed Loop Phase Noise vs Frequency and Temperature

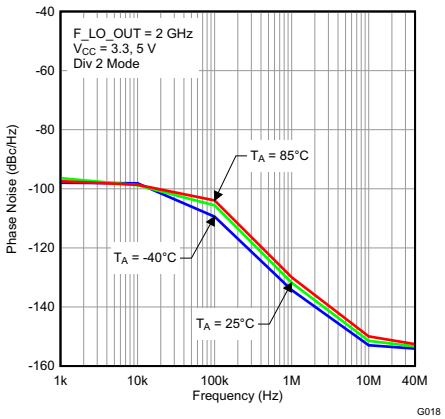


Figure 20. Closed Loop Phase Noise vs Frequency and Temperature

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

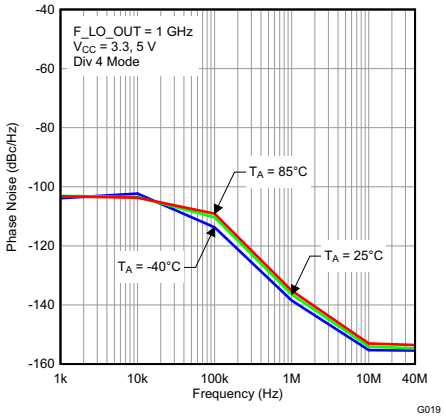


Figure 21. Closed Loop Phase Noise vs Frequency and Temperature

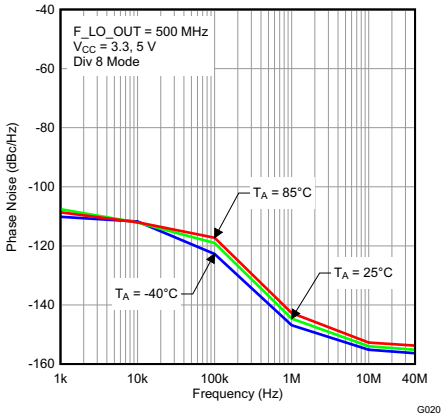


Figure 22. Closed Loop Phase Noise vs Frequency and Temperature

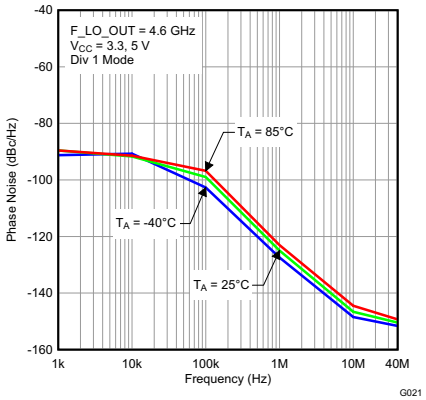


Figure 23. Closed Loop Phase Noise vs Frequency and Temperature

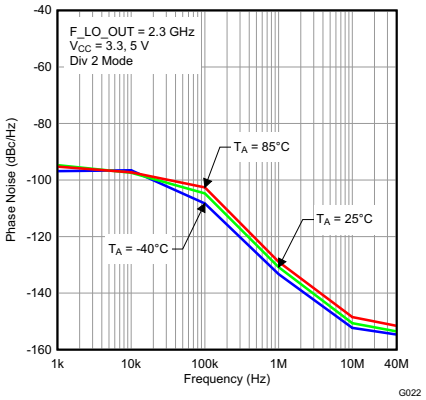


Figure 24. Closed Loop Phase Noise vs Frequency and Temperature

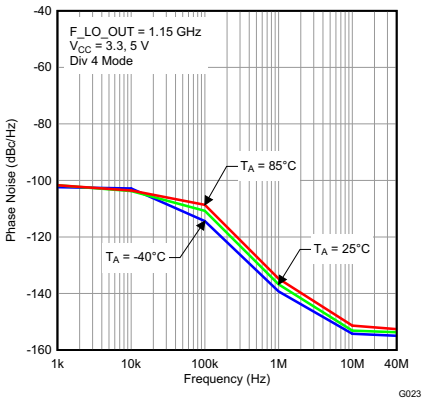


Figure 25. Closed Loop Phase Noise vs Frequency and Temperature

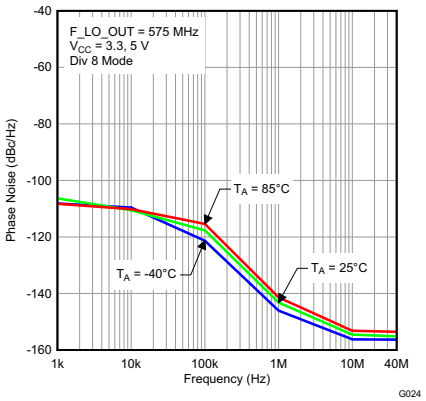


Figure 26. Closed Loop Phase Noise vs Frequency and Temperature

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

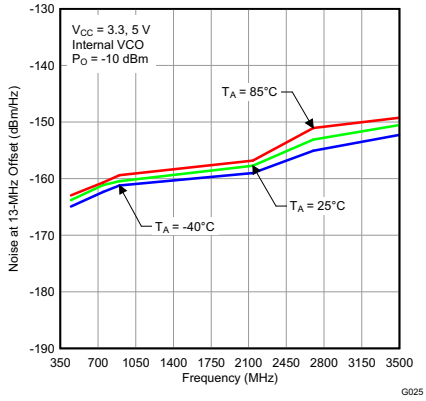


Figure 27. Noise at 13-MHz Offset vs Frequency and Temperature With Internal VCO

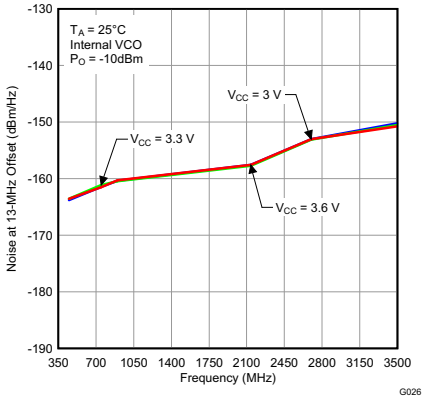


Figure 28. Noise at 13-MHz Offset vs Frequency and Supply Voltage With Internal VCO

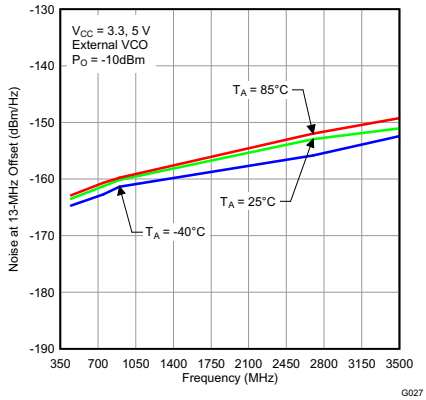


Figure 29. Noise at 13-MHz Offset vs Frequency and Temperature With External VCO

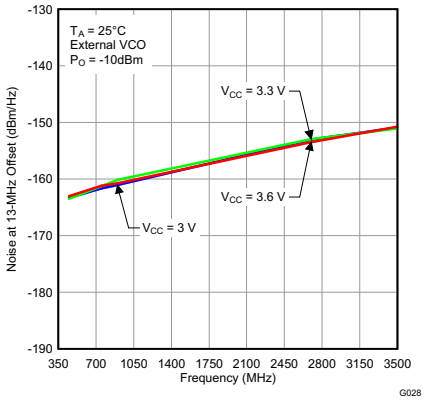


Figure 30. Noise at 13-MHz Offset vs Frequency and Supply Voltage With External VCO

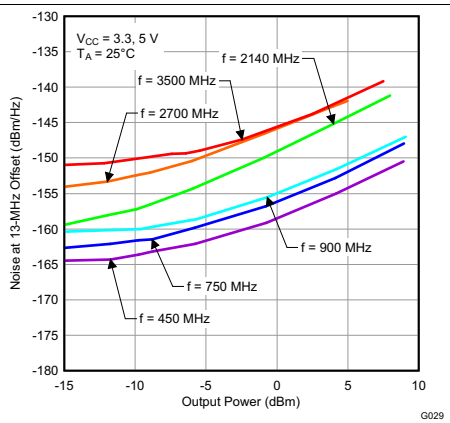


Figure 31. Noise at 13-MHz Offset vs Output Power and Frequency

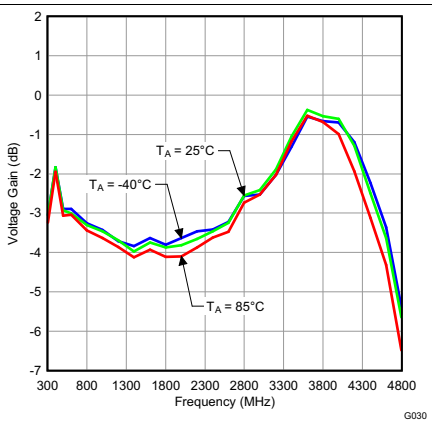


Figure 32. Voltage Gain vs Frequency and Temperature

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

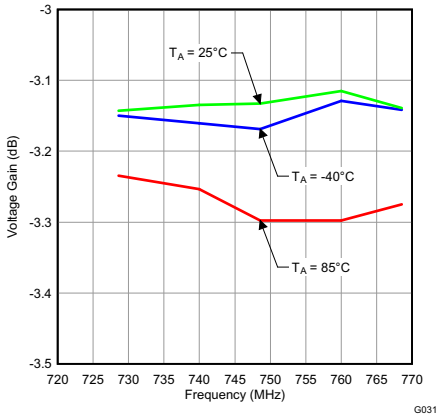


Figure 33. Voltage Gain vs Frequency and Temperature at 750 MHz

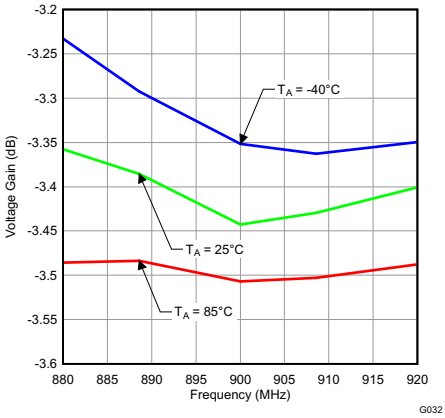


Figure 34. Voltage Gain vs Frequency and Temperature at 900 MHz

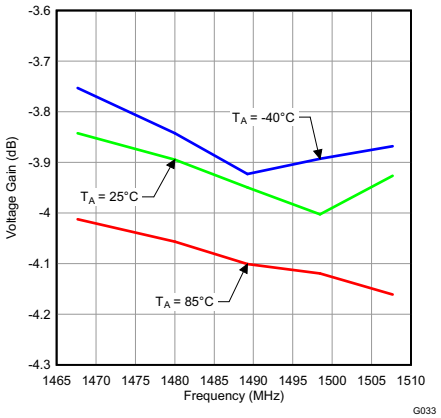


Figure 35. Voltage Gain vs Frequency and Temperature at 1500 MHz

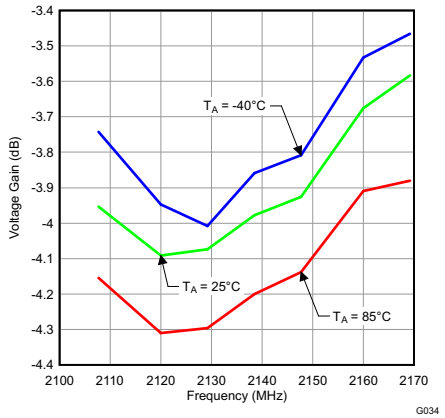


Figure 36. Voltage Gain vs Frequency and Temperature at 2150 MHz

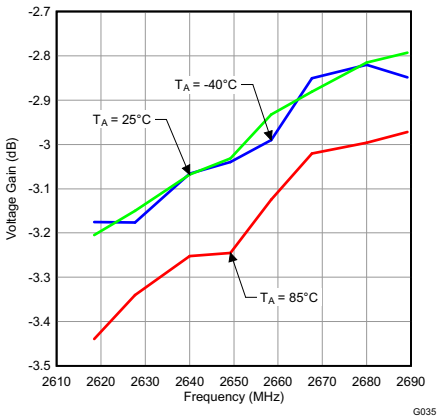


Figure 37. Voltage Gain vs Frequency and Temperature at 2650 MHz

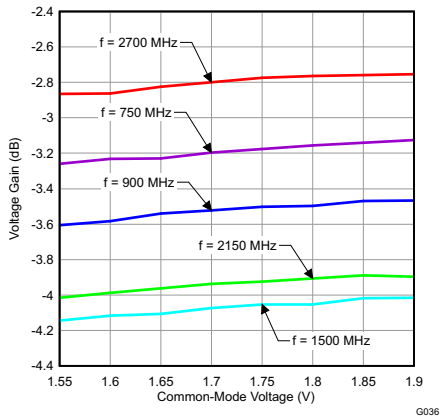


Figure 38. Voltage Gain vs Common-Mode Voltage and Frequency

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

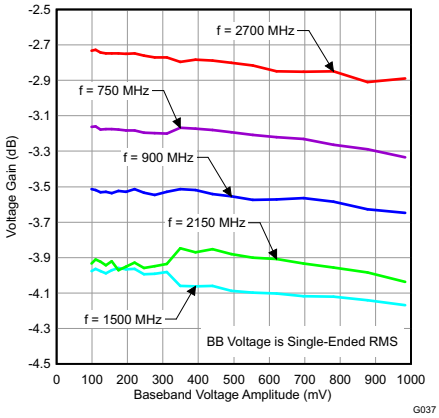


Figure 39. Voltage Gain vs Baseband Voltage Amplitude and Frequency

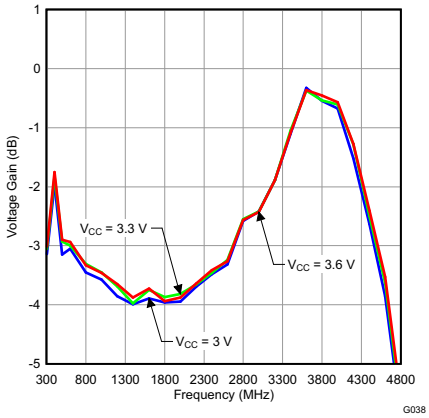


Figure 40. Voltage Gain vs Frequency and Supply Voltage

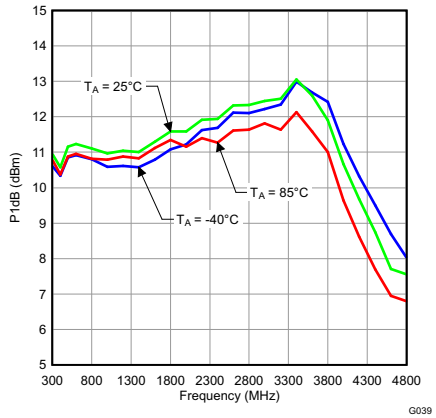


Figure 41. P1dB vs Frequency and Temperature

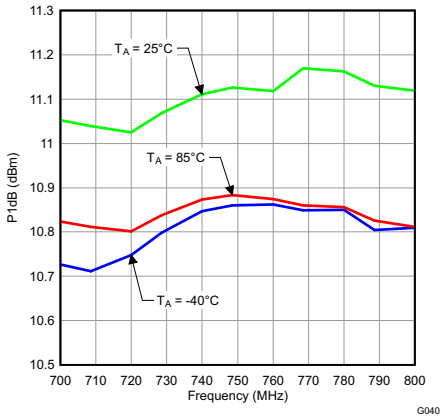


Figure 42. P1dB vs Frequency and Temperature at 750 MHz

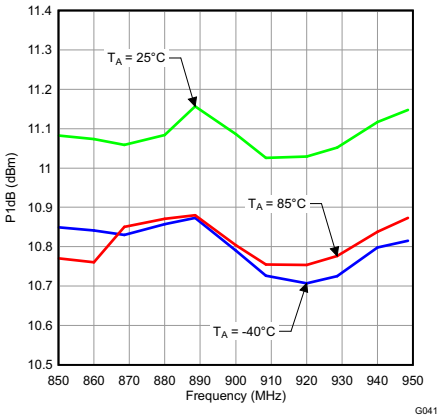


Figure 43. P1dB vs Frequency and Temperature at 900 MHz

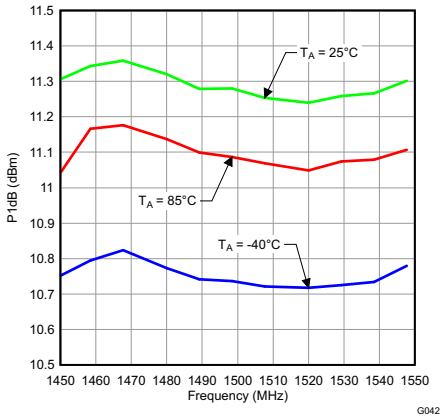


Figure 44. P1dB vs Frequency and Temperature at 1500 MHz

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

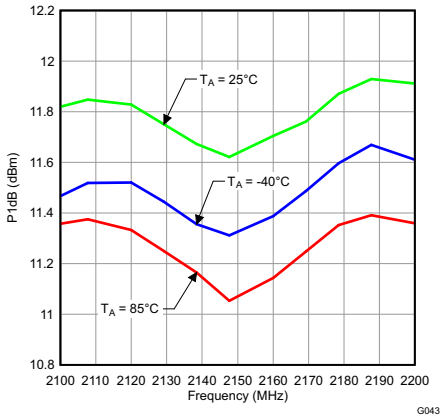


Figure 45. P1dB vs Frequency and Temperature at 2150 MHz

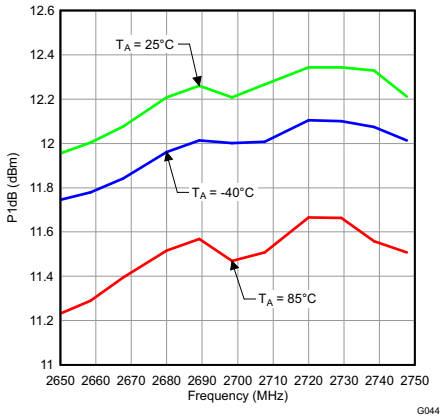


Figure 46. P1dB vs Frequency and Temperature at 2700 MHz

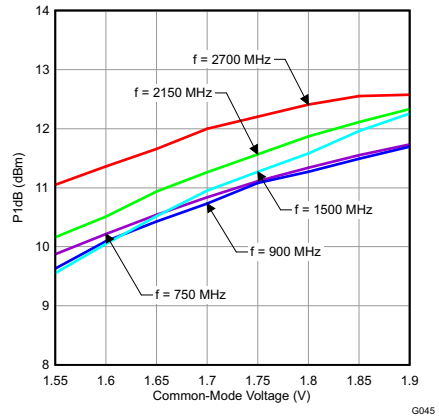


Figure 47. P1dB vs Common-Mode Voltage and Frequency

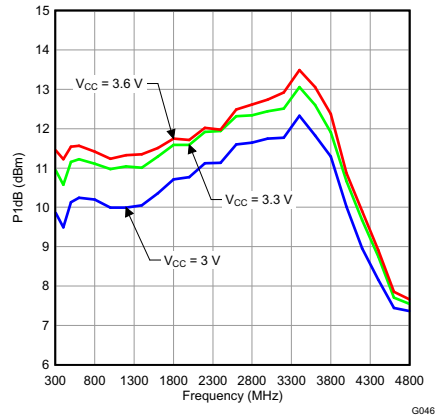


Figure 48. P1dB vs Frequency and Supply Voltage

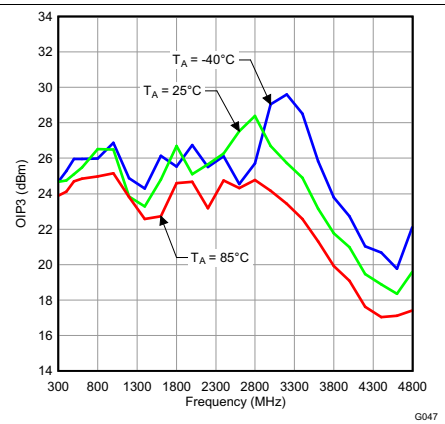


Figure 49. OIP3 vs Frequency and Temperature

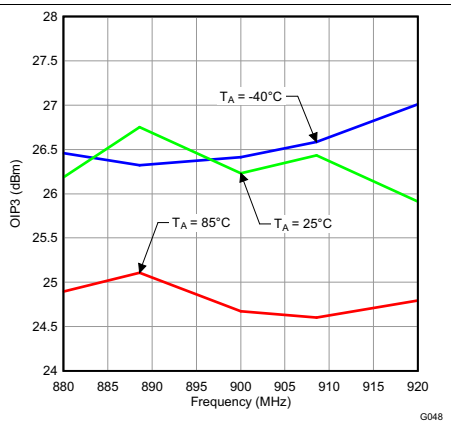


Figure 50. OIP3 vs Temperature and Frequency at 900 MHz

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

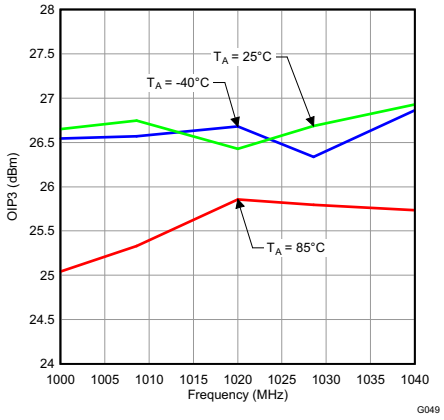


Figure 51. OIP3 vs Frequency and Temperature at 1030 MHz

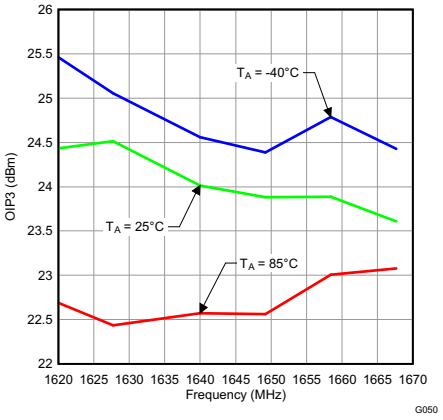


Figure 52. OIP3 vs Frequency and Temperature at 1650 MHz

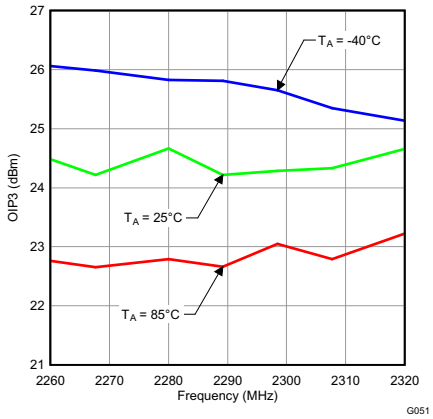


Figure 53. OIP3 vs Frequency and Temperature at 2300 MHz

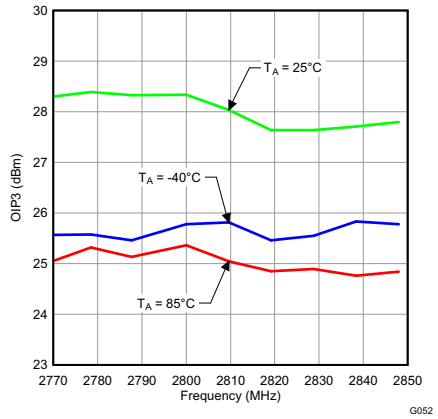


Figure 54. OIP3 vs Frequency and Temperature at 2850 MHz

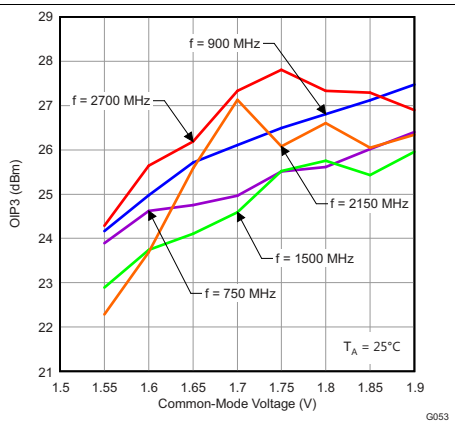


Figure 55. OIP3 vs Common-Mode Voltage and Frequency

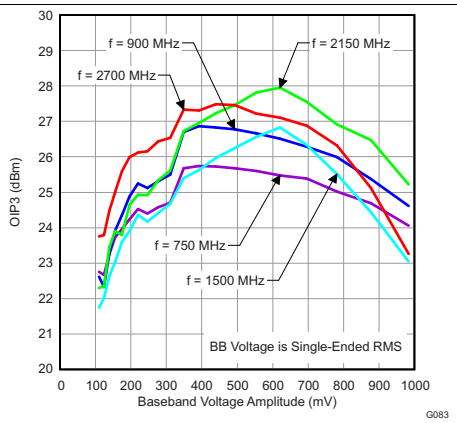


Figure 56. OIP3 vs Baseband Voltage Amplitude and Frequency

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

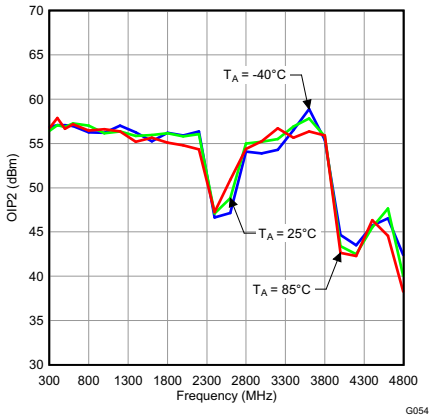


Figure 57. OIP2 vs Frequency and Temperature

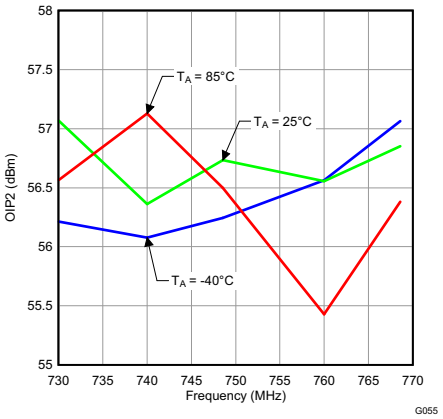


Figure 58. OIP2 vs Frequency and Temperature at 750 MHz

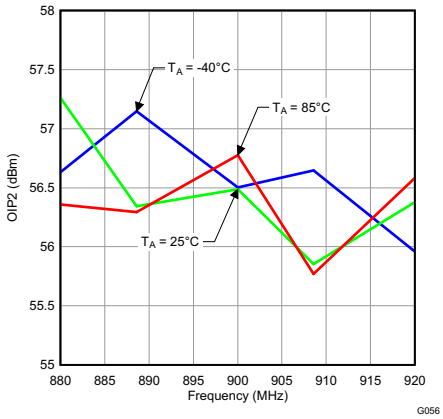


Figure 59. OIP2 vs Frequency and Temperature at 900 MHz

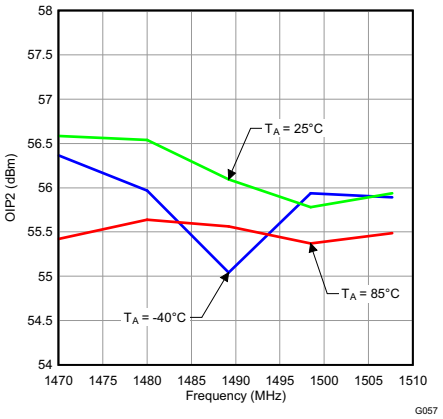


Figure 60. OIP2 vs Frequency and Temperature at 1500 MHz

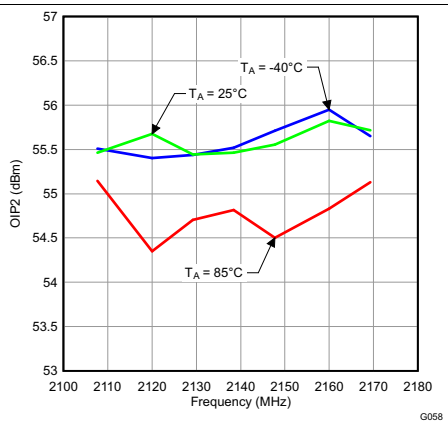


Figure 61. OIP2 vs Frequency and Temperature at 2150 MHz

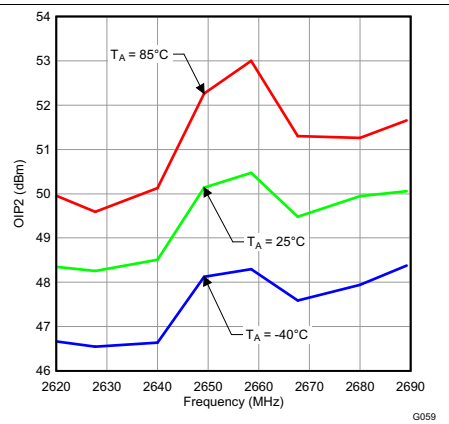


Figure 62. OIP2 vs Frequency and Temperature at 2650 MHz

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

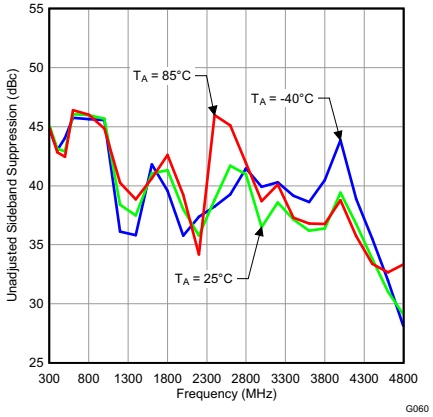


Figure 63. Unadjusted Sideband Suppression vs Frequency and Temperature

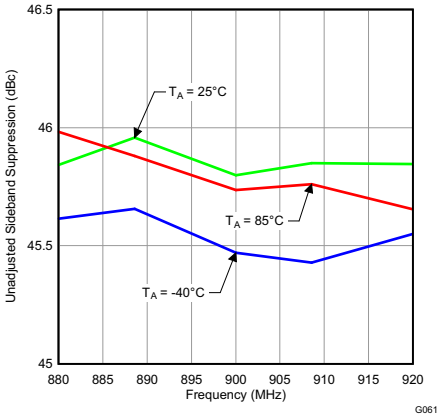


Figure 64. Unadjusted Sideband Suppression vs Frequency and Temperature at 900 MHz

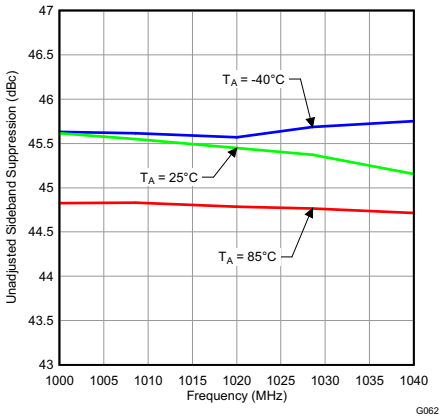


Figure 65. Unadjusted Sideband Suppression vs Frequency and Temperature at 1030 MHz

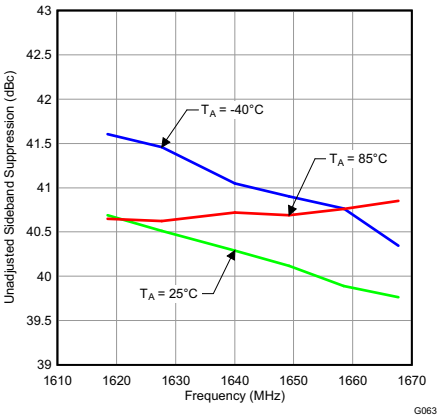


Figure 66. Unadjusted Sideband Suppression vs Frequency and Temperature at 1650 MHz

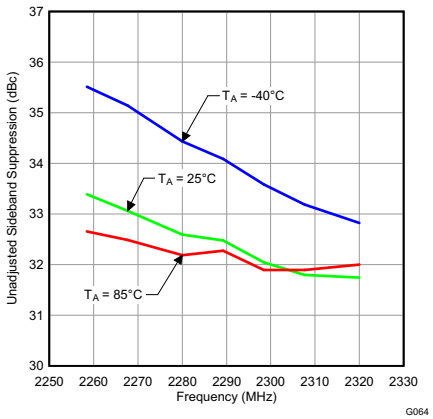


Figure 67. Unadjusted Sideband Suppression vs Frequency and Temperature at 2300 MHz

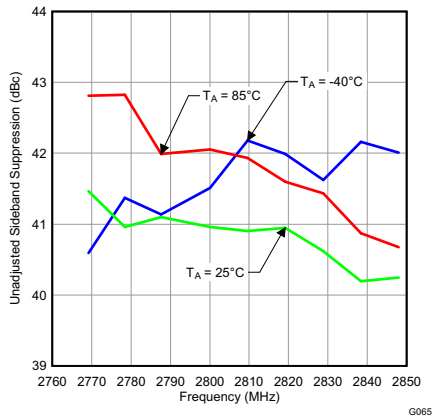


Figure 68. Unadjusted Sideband Suppression vs Frequency and Temperature at 2850 MHz

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

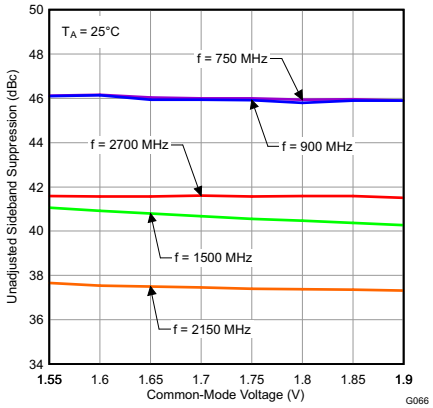


Figure 69. Unadjusted Sideband Suppression vs Common-Mode Voltage and Frequency

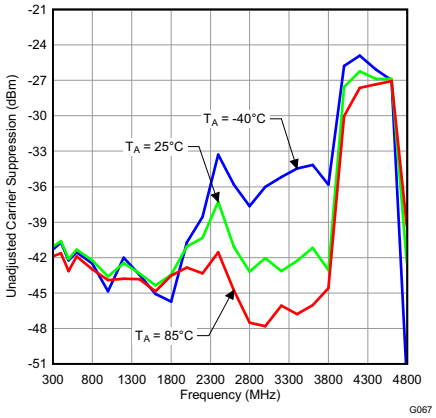


Figure 70. Unadjusted Carrier Suppression vs Frequency and Temperature

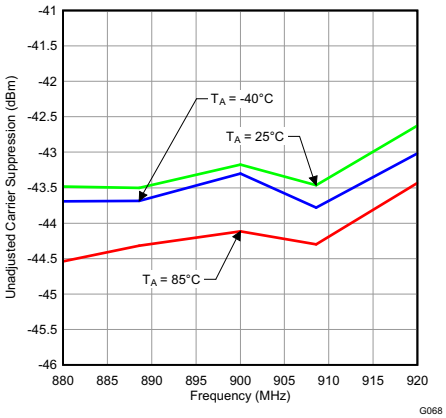


Figure 71. Unadjusted Carrier Suppression vs Frequency and Temperature at 900 MHz

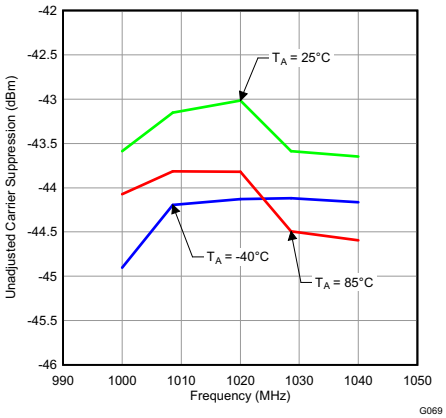


Figure 72. Unadjusted Carrier Suppression vs Frequency and Temperature at 1030 MHz

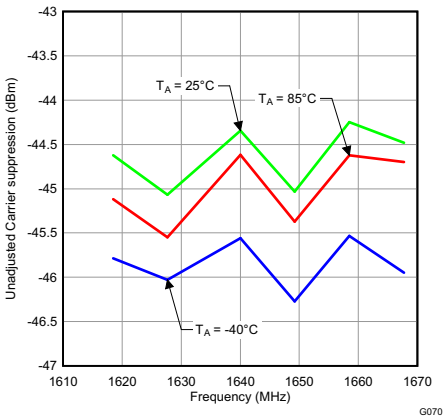


Figure 73. Unadjusted Carrier Suppression vs Frequency and Temperature at 1650 MHz

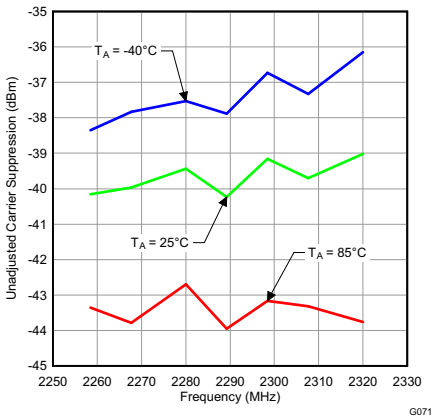


Figure 74. Unadjusted Carrier Suppression vs Frequency and Temperature at 2300 MHz

Typical Characteristics (continued)

V_{CM} = 1.7 V (internal), V_{inBB} = 300 mVrms single-ended sine wave in quadrature, V_{CC3V} = 3.3 V, V_{CC5V} = 5 V, f_{BB} = 4.5 MHz and 5.5 MHz, internal LO, T_A = 25°C; F_{PFD} = 1.6 MHz (unless otherwise noted).

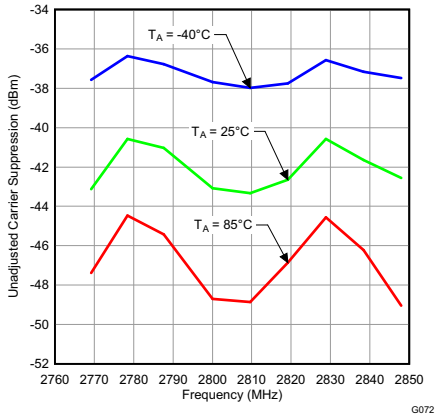


Figure 75. Unadjusted Carrier Suppression vs Frequency and Temperature at 2850 MHz

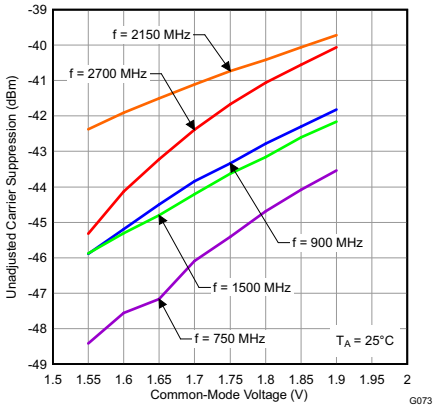


Figure 76. Unadjusted Carrier Suppression vs Common-Mode Voltage and Frequency

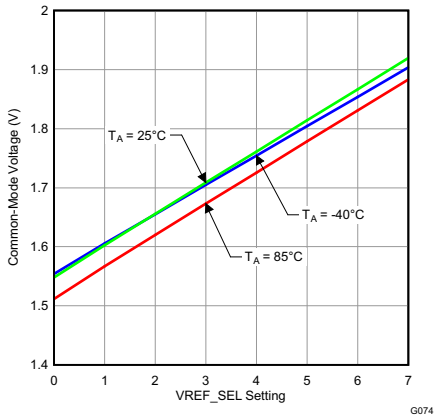


Figure 77. Common-Mode Voltage vs VREF_SEL Setting and Temperature

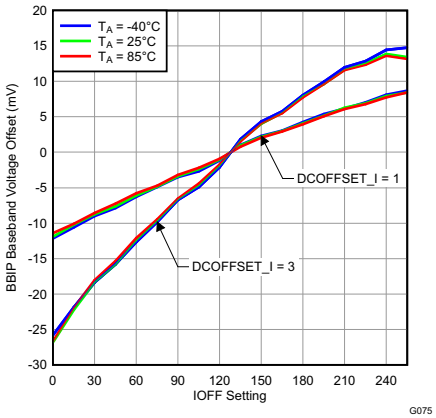


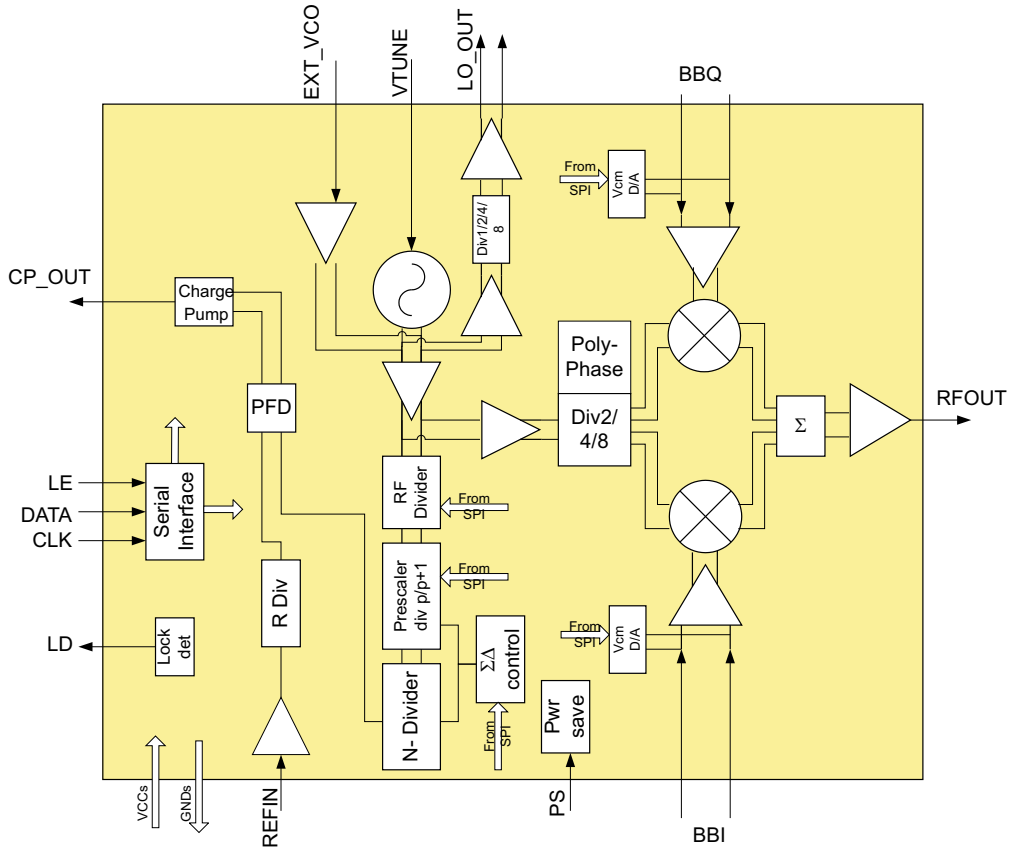
Figure 78. Baseband Voltage Offset vs IOFF Setting and Temperature

7 Detailed Description

7.1 Overview

The TRF372017 is a high-performance, direct up-conversion device, integrating a high-linearity, low-noise IQ modulator and an integer-fractional PLL/VCO. The VCO uses integrated frequency dividers to achieve a wide, continuous tuning range of 300 MHz to 4800 MHz. The LO is available as an output with independent frequency dividers. The device also accepts input from an external LO or VCO. The modulator baseband inputs can be biased either internally or externally. Internal DC offset adjustment enables carrier cancellation. The device is controlled through a 3-wire serial programming interface (SPI). A control pin invokes power-save mode to reduce power consumption while keeping the VCO locked for fast start-up.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Integer and Fractional Mode Selection

The PLL is designed to operate in either Integer mode or Fractional mode. If the desired local oscillator (LO) frequency is an integer multiple of the phase frequency detector (PFD) frequency, f_{PFD}, then Integer mode can be selected. The normalized in-band phase noise floor in Integer mode is lower than in Fractional mode. In Integer mode, the feedback divider is an exact integer, and the fraction is zero. While operating in Integer mode, the register bits corresponding to the fractional control are *don't care*.

In Fractional mode, the feedback divider fractional portion is non-zero on average. With 25-bit fractional resolution, RF stepsize $f_{PFD}/2^{25}$ is less than 1 Hz with a f_{PFD} up to 33 MHz. The appropriate fractional control bits in the serial register must be programmed.

Feature Description (continued)

7.3.2 Description of PLL Structure

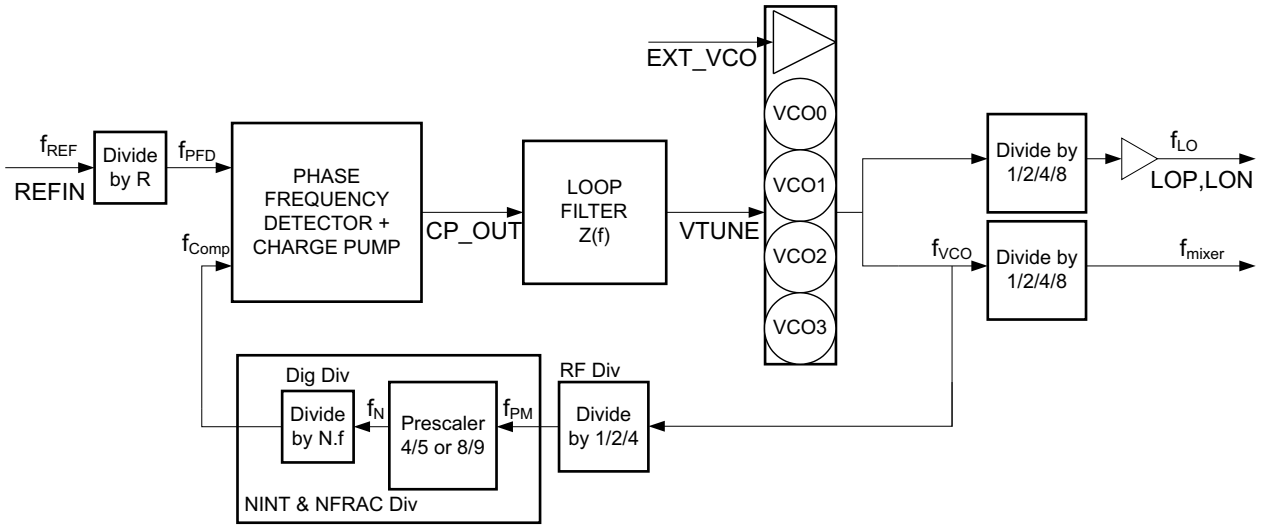


Figure 79. Block Diagram of the PLL Loop

The output frequency is given by Equation 1:

$$f_{VCO} = \frac{f_{REF}}{RDIV} (PLL\_DIV\_SEL)\left[NINT + \frac{NFRAC}{2^{25}}\right] \quad (1)$$

The rate at which phase comparison occurs is f_{REF}/RDIV. In Integer mode, the fractional setting is ignored and Equation 2 is applied.

$$\frac{f_{VCO}}{f_{PFD}} = NINT \times PLL\_DIV\_SEL \quad (2)$$

The feedback divider block consists of a programmable RF divider, a prescaler divider, and an NF divider. The prescaler can be programmed as either a 4/5 or an 8/9 prescaler. The NF divider includes an *A* counter and an *M* counter.

7.3.2.1 Selecting PLL Divider Values

Operation of the PLL requires the LO_DIV_SEL, RDIV, PLL_DIV_SEL, NINT, and NFRAC bits to be calculated. The LO or mixer frequency is related to f_{VCO} according to divide-by-1/-2/-4/-8 blocks and the operating range of f_{VCO}.

a. **LO_DIV_SEL**

$$LO\_DIV\_SEL = \begin{cases} 1 & 2400\ MHz \le f_{RF} \le 4800\ MHz \\ 2 & 1200\ MHz \le f_{RF} \le 2400\ MHz \\ 3 & 600\ MHz \le f_{RF} \le 1200\ MHz \\ 4 & 300\ MHz \le f_{RF} \le 600\ MHz \end{cases}$$

Therefore:

$f_{VCO} = LO\_DIV\_SEL \times f_{RF}$

Feature Description (continued)

b. **PLL_DIV_SEL**

Given f_{VCO}, select the minimum value for PLL_DIV_SEL so that the programmable RF divider limits the input frequency into the prescaler block, f_{PM}, to a maximum of 3000 MHz.

$$PLL\_DIV\_SEL = \min(1, 2, 4) \text{ such that } f_{PM} \leq 3000 \text{ MHz}$$

This calculation can be restated as Equation 3.

$$PLL\_DIV\_SEL = \text{Ceiling}\left(\frac{LO\_DIV\_SEL \times f_{RF}}{3000 \text{ MHz}}\right) \tag{3}$$

Higher values of f_{PFD} correspond to better phase noise performance in Integer mode or Fractional mode. f_{PFD}, along with PLL_DIV_SEL, determines the f_{VCO} stepsize in Integer mode. Therefore, in Integer mode, select the maximum f_{PFD} that allows for the required RF stepsize, as shown by Equation 4.

$$f_{PFD} = \frac{f_{VCO,\ Stepsize}}{PLL\_DIV\_SEL} = \frac{f_{RF,\ Stepsize} \times LO\_DIV\_SEL}{PLL\_DIV\_SEL} \tag{4}$$

In Fractional mode, a small RF stepsize is accomplished through the Fractional mode divider. A large f_{PFD} should be used to minimize the effects of fractional controller noise in the output spectrum. In this case, f_{PFD} may vary according to the reference clock and fractional spur requirements (for example, f_{PFD} = 20 MHz).

c. **RDIV, NINT, NFRAC, PRSC_SEL**

$$RDIV = \frac{f_{REF}}{f_{PFD}}$$

$$NINT = \text{floor}\left(\frac{f_{VCO} RDIV}{f_{REF} PLL\_DIV\_SEL}\right)$$

$$NFRAC = \text{floor}\left(\left[\left(\frac{f_{VCO} RDIV}{f_{REF} PLL\_DIV\_SEL}\right) - NINT\right] 2^{25}\right)$$

The P/(P+1) programmable prescaler is set to 8/9 or 4/5 through the PRSC_SEL bit. To allow proper fractional control, set PRSC_SEL according to Equation 5.

$$PRSC\_SEL = \begin{cases} \frac{8}{9} & NINT \geq 75 \text{ in Fractional Mode or } NINT \geq 72 \text{ in Integer mode} \\ \frac{4}{5} & 23 \leq NINT < 75 \text{ in Fractional mode or } 20 \leq NINT < 72 \text{ in Integer mode} \end{cases} \tag{5}$$

The PRSC_SEL limit at NINT < 75 applies to Fractional mode with third-order modulation. In Integer mode, the PRSC_SEL = 8/9 should be used with NINT as low as 72. The divider block accounts for either value of PRSC_SEL without requiring NINT or NFRAC to be adjusted. Then, calculate the maximum frequency to be input to the digital divider at f_N. Use the lower of the possible prescaler divide settings, P = (4,8), as shown by Equation 6.

Feature Description (continued)

$$f_{N,Max} = \frac{f_{VCO}}{PLL\_DIV\_SEL \times P} \quad (6)$$

Verify that the frequency into the digital divider, f_N, is less than or equal to 375 MHz. If f_N exceeds 375 MHz, choose a larger value for PLL_DIV_SEL and recalculate f_{PFD}, RDIV, NINT, NFRAC, and PRSC_SEL.

7.3.2.2 Setup Example for Integer Mode

Suppose the following operating characteristics are desired for Integer mode operation:

- f_{REF} = 40 MHz (reference input frequency)
- Step at RF = 2 MHz (RF channel spacing)
- f_{RF} = 1600 MHz (RF frequency)

The VCO range is 2400 MHz to 4800 MHz. Therefore:

- LO_DIV_SEL = 2
- f_{VCO} = LO_DIV_SEL × 1600 MHz = 3200 MHz

To keep the frequency of the prescaler less than 3000 MHz:

- PLL_DIV_SEL = 2

The desired stepsize at RF is 2 MHz, so:

- f_{PFD} = 2 MHz
- f_{VCO}, stepsize = PLL_DIV_SEL × f_{PFD} = 4 MHz

Using the reference frequency along with the required f_{PFD} gives:

- RDIV = 20
- NINT = 800

NINT ≥ 75; therefore, select the 8/9 prescaler.

$f_{N,Max}$ = 3200 MHz/(2 × 8) = 200 MHz < 375 MHz

This example shows that Integer mode operation gives sufficient resolution for the required stepsize.

7.3.2.3 Setup Example for Fractional Mode

Suppose the following operating characteristics are desired for Fractional mode operation:

- f_{REF} = 40 MHz (reference input frequency)
- Step at RF = 5 MHz (RF channel spacing)
- f_{RF} = 1,600,000,045 Hz (RF frequency)

The VCO range is 2400 MHz to 4800 MHz. Therefore:

- LO_DIV_SEL = 2
- f_{VCO} = LO_DIV_SEL × 1,600,000,045 Hz = 3,200,000,090 Hz

To keep the frequency of the prescaler less than 3000 MHz:

- PLL_DIV_SEL = 2

Using a typical f_{PFD} of 20 MHz:

- RDIV = 2
- NINT = 80
- NFRAC = 75

NINT ≥ 75; therefore, select the 8/9 prescaler.

$f_{N,Max}$ = 3200 MHz/(2 × 8) = 200 MHz < 375 MHz

Feature Description (continued)

The actual frequency at RF is:

- f_{RF} = 1600000044.9419 Hz

Which yields a frequency error of –0.058 Hz.

7.3.3 Fractional Mode Setup

Optimal operation of the PLL in fractional mode requires several additional register settings. Recommended values are listed in Table 1. Optimal performance may require tuning the MOD_ORD, ISOURCE_SINK, and ISOURCE_TRIM values according to the chosen frequency band.

Table 1. Fractional Mode Register Settings

REGISTER BIT	REGISTER ADDRESSING	RECOMMENDED VALUE
EN_ISOURCE	Reg4B18	1
EN_DITH	Reg4B25	1
MOD_ORD	Reg4B[27..26]	B[27..26] = [10]
DITH_SEL	Reg4B28	0
DEL_SD_CLK	Reg4B[30..29]	B[30..29] = [10]
EN_LD_ISOURCE	Reg5B31	0
ISOURCE_SINK	Reg7B19	0
ISOURCE_TRIM	Reg7B[22..20]	B[22..20] = [100]

7.3.4 Selecting the VCO and VCO Frequency Control

To achieve a broad frequency tuning range, the TRF372017 includes four VCOs. Each VCO is connected to a bank of capacitors that determine its valid operating frequency. For any given frequency setting, the appropriate VCO and capacitor array must be selected.

The device contains logic that automatically selects the appropriate VCO and capacitor bank. Set bit EN_CAL to initiate the calibration algorithm. During the calibration process, the device selects a VCO and a capacitor state so that VTune matches the reference voltage set by VCO_CAL_REF_n. Accuracy of the tune is increased through bits CAL_ACC_n. Because a calibration begins immediately when EN_CAL is set, all registers must contain valid values before initiating calibration.

Calibration logic is driven by a CAL_CLK clock derived from the phase frequency detector frequency scaled according to the setting in CAL_CLK_SEL. Faster CAL_CLK frequency enables faster calibration, but the logic is limited to clock frequencies around 1 MHz. Table 2 provides suggested CAL_CLK_SEL scaling recommendations for several phase frequency detector frequencies. The flag R_SAT_ERR is evaluated during the calibration process to indicate calibration counter overflow errors, which occurs if CAL_CLK runs too fast. If R_SAT_ERR is set during a calibration, the resulting calibration is not valid and CAL_CLK_SEL must be used to slow the CAL_CLK. CAL_CLK frequencies should not be set to less than 0.1 MHz.

Table 2. Example CAL_CLK_SEL Scaling

PFD FREQUENCY (MHz)	CAL_CLK_SEL SCALING	CAL_CLK FREQUENCY (MHz)
20	1/32	0.625
1	1	1
0.1	8	0.8

When VCOSEL_MODE is 0, the device automatically selects both the VCO and capacitor bank within 23 CAL_CLK cycles. When VCOSEL_MODE is 1, the device uses the VCO selected in VCO_SEL_0 and VCO_SEL_1 and automatically selects the capacitor array within 17 CAL_CLK cycles. The VCO and capacitor array settings resulting from calibration cannot be read from the VCO_SEL_n and VCO_TRIM_n bits in registers 2 and 7. They can only be read from register 0.

Automatic calibration can be disabled by setting CAL_BYPASS to 1. In this manual cal mode, the VCO is selected through register bits VCO_SEL_n, while the capacitor array is selected through register bits VCO_TRIM_n. Calibration modes are summarized in Table 3. After calibration is complete, the PLL is released from calibration mode to reach an analog lock.

During the calibration process, the TRF372017 scans through many frequencies. RF and LO outputs should be disabled until calibration is complete. At power up, the RF and LO output are disabled by default.

Once a calibration has been performed at a given frequency setting, the calibration is valid over all operating temperature conditions.

Table 3. VCO Calibration Modes

CAL_BYPASS	VCOSEL_MODE	MAX CYCLES CAL_CLK	VCO	CAPACITOR ARRAY
0	0	46	Automatic	
0	1	34	VCO_SEL_n	automatic
1	*don't care*	*na*	VCO_SEL_n	VCO_TRIM_n

7.3.5 External VCO

An external LO or VCO signal may be applied. EN_EXTVCO powers the input buffer and selects the buffered external signal instead of an internal VCO. Dividers, the pfd, and the charge pump remain enabled and may be used to drive an external VCO. NEG_VCO must correspond to the gain of the external VCO.

7.3.6 VCO Test Mode

Setting VCO_TEST_MODE forces the currently selected VCO to the edge of its frequency range by disconnecting the charge pump input from the pfd and loop filter and forcing its output high or low. The upper or lower edge of the VCO range is selected through COUNT_MODE_MUX_SEL.

VCO_TEST_MODE also reports the value of a frequency counter in COUNT, which can be read back in register 0. COUNT reports the number of digital N divider cycles in the PLL, directly related to the period of fN, that occur during each CAL_CLK cycle. Counter operation is initiated through the bit EN_CAL.

Table 4. VCO Test Mode

VCO_TEST_MODE	COUNT_MODE_MUX_SEL	VCO OPERATION	REGISTER 0 B[30..13]
0	*don't care*	Normal	B[30..24] = *undefined* B[23..22] = VCO_SEL selected during autocal B21 = *undefined* B[20..13] = VCO_TRIM selected during autocal
1	0	Max frequency	B[30..13] = Max frequency counter
1	1	Min frequency	B[30..13] = Min frequency counter

7.3.7 Lock Detect

The lock detect signal is generated in the phase frequency detector by comparing the VCO target frequency against the VCO actual frequency. When the phase of the two compared frequencies remains aligned for several clock cycles, an internal signal goes high. The precision of this comparison is controlled through the LD_ANA_PREC bits. This internal signal is then averaged and compared against a reference voltage to generate the LD signal. The number of averages used is controlled through LD_DIG_PREC. Therefore, when the VCO is frequency locked, LD is high. When the VCO frequency is not locked, LD may pulse high or exhibit periodic behavior.

By default, the internal lock detect signal is driven on the LD terminal. Register bits MUX_CTRL_n can be used to control a mux to output other diagnostic signals on the LD output. The LD control signals are shown in Table 5.

Table 5. LD Control Signals

ADJUSTMENT	REGISTER BITS	BIT ADDRESSING
Lock detect precision	LD_ANA_PREC_0	Register 4 Bit 19
Unlock detect precision	LD_ANA_PREC_1	Register 4 Bit 20
LD averaging count	LD_DIG_PREC	Register 4 Bit 24
Diagnostic Output	MUX_CTRL_n	Register 7 Bits 18..16

Table 6. LD Control Signal Mode Settings

CONDITION	RECOMMENDED SETTINGS
Integer Mode	LD_ANA_PREC_0 = 0 LD_ANA_PREC_1 = 0 LD_DIG_PREC = 1
Fractional Mode	LD_ANA_PREC_0 = 1 LD_ANA_PREC_1 = 1 LD_DIG_PREC = 1

7.3.8 Tx Divider

The Tx divider, illustrated in Figure 80, converts the differential output of the VCO into differential I and Q mixer components. The divide by 1 differential quadrature phases are provided through a polyphase. Divide by 2, 4, and 8 differential quadrature phases are provided through flip-flop dividers. Only one of the dividers operates at a time, and the appropriate output is selected by a mux. DIVn bits are controlled through TX_DIV_SELn.

TX_DIV_I determines the bias level for the divider blocks. The SPEEDUP control is used to bypass a stabilization resistor and reach the final bias level faster after a change in the divider selection. SPEEDUP should be disabled during normal operation.

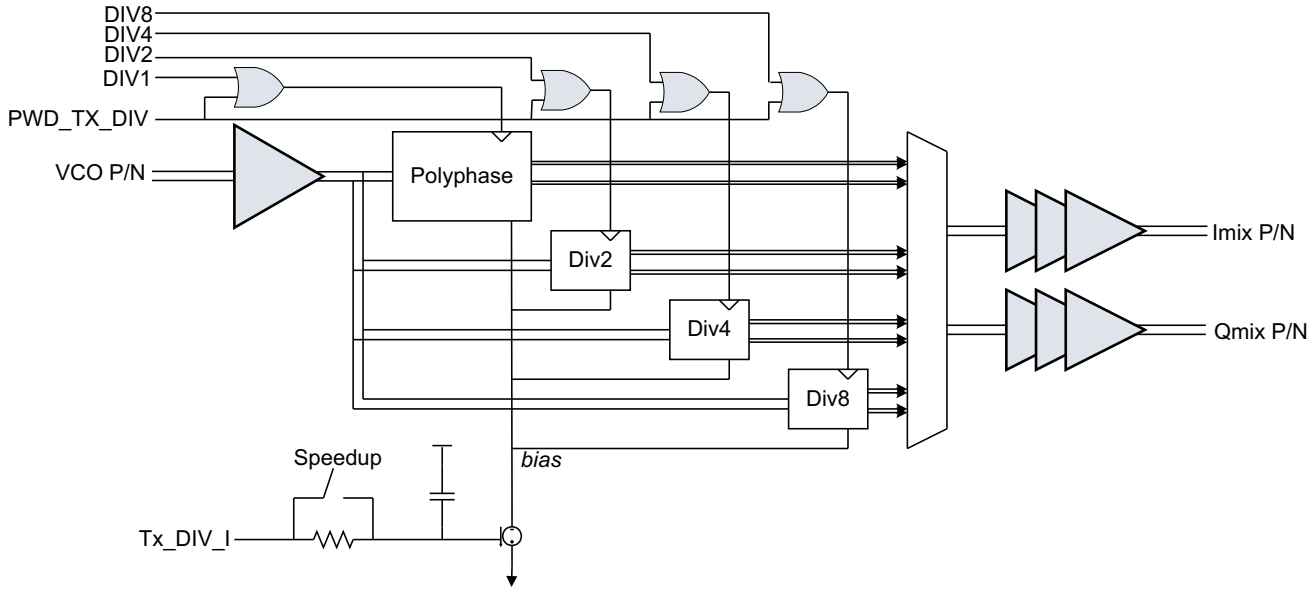


Figure 80. Tx Divider

7.3.9 LO Divider

The LO divider is shown in Figure 81. It frequency divides the VCO output. Only one of the dividers operates at a time, and the appropriate output is selected by a mux. DIVn bits are controlled through LO_DIV_SELn. The output is buffered and provided on output pins LO_OUT_P and LO_OUT_N. The output level is controlled through BUFOUT_BIASn.

LO_DIV_I determines the bias level for the divider blocks. The SPEEDUP control is used to bypass a stabilization resistor and reach the final bias level faster after a change in the divider selection. SPEEDUP should be disabled during normal operation. Although SPEEDUP controls both the Tx and LO divider biases, the Tx and LO divider biases are generated independently.

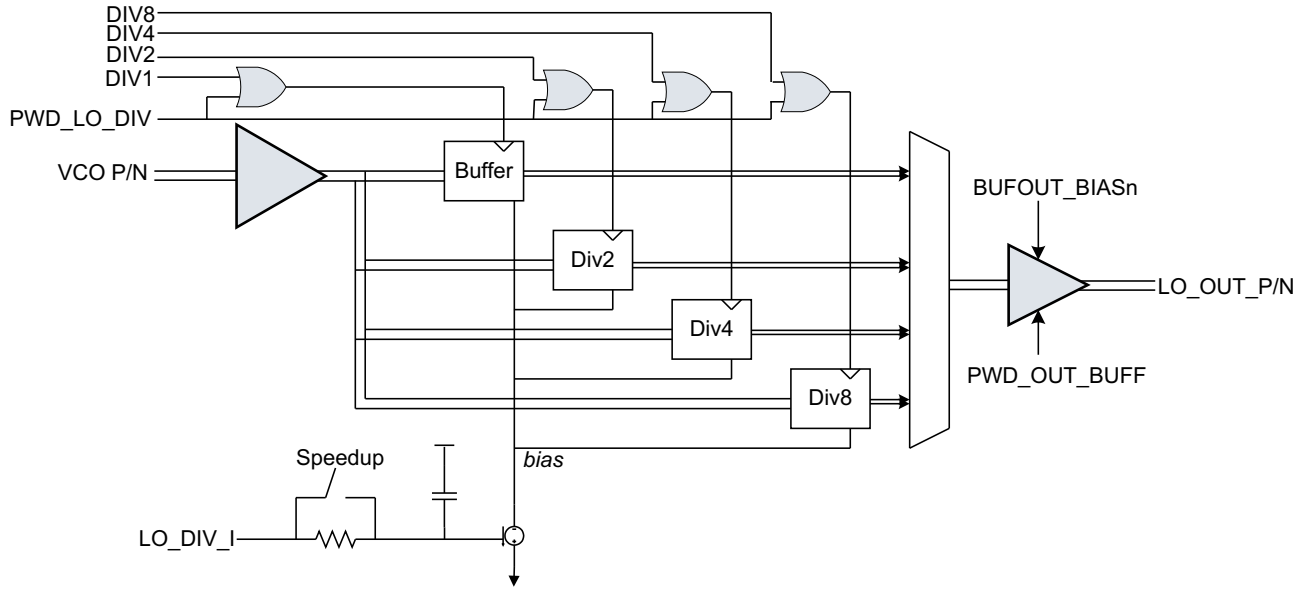


Figure 81. LO Divider

7.3.10 Mixer

A diagram of the mixer is shown in Figure 82. The mixer is followed by a differential to single-ended converter and buffer for output.

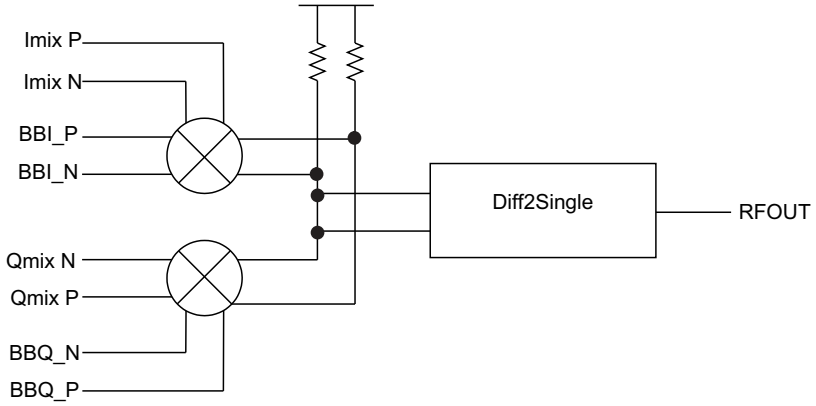


Figure 82. Mixer

7.3.11 Disabling Outputs

RF frequency outputs are generated at the RFOUT and LO* terminals. Unused RF frequency outputs should be disabled to minimize power consumption and noise generation. Table 7 lists settings used to disable the outputs. Power-save mode can also be used to disable outputs.

Table 7. Register Controls for Disabling Outputs

DISABLED OUTPUT	REGISTER BIT	SETTING
RFOUT	PWD_TX_DIV	1
LOP and LON	PWD_OUT_BUFF	1
	PWD_LO_DIV	1

7.3.12 Power Supply Distribution

Power supply distribution for the TRF372017 is shown in Figure 83. Proper isolation and filtering of the supplies is critical for low noise operation of the device. Each supply pin should be supplied with local decoupling capacitance and isolated with a ferrite bead. VCC_VCO2 is tolerant of 5-V supply voltages to permit additional supply filtering.

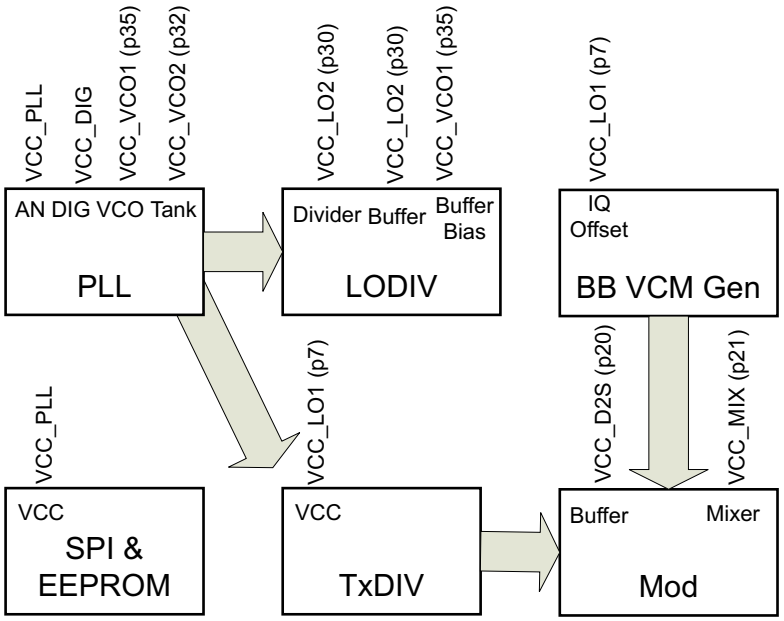


Figure 83. Power Supply Distribution

7.3.13 Carrier Feedthrough Cancellation

The structure of the baseband current DAC is shown in Figure 84. For each input pair, there is a programmable reference current. The reference current for each pair (I and Q) is identical and is programmed through the same register bits, but the reference current source itself is duplicated in the device for both I and Q inputs. This current can be set to change the total current flowing into the P and N nodes, which in turn changes the offset programmability range.

The reference current is then mirrored and multiplied before getting injected into the input node. The total mirrored current is routed into the two sides of the differential pair and routed according to eight programmable bits. As the 8-bit setting is changed, current is shifted from one side of the pair into the other side for each of the I and Q input pairs. In practical usage, the offset current routing distributes the adjustment for each side of the pair, while the reference current sets the range of adjustment. This effect can be seen in Figure 78, which shows that the gain of the current routing is greater when the reference current setting is higher. However the step size also increases with increase in range. Figure 78 shows the effect on common mode voltage of varying the DAC reference current. Adjustment register bits are shown in Table 8.

Offset adjustment may be provided by an external source, such as a DAC QMC block, for DC-coupled systems.

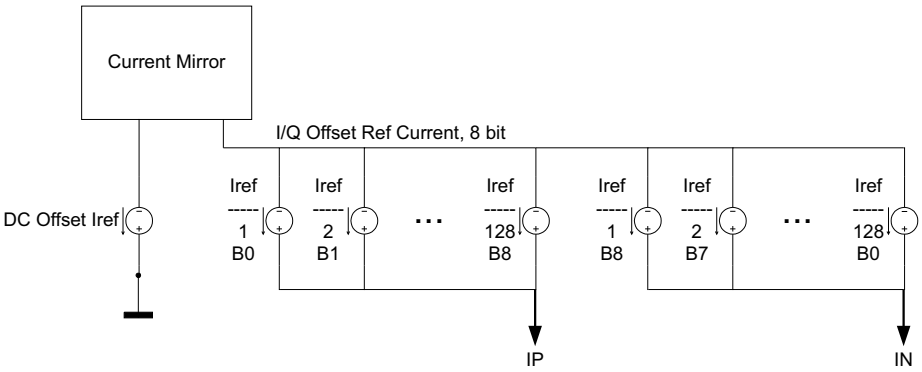


Figure 84. Block Diagram of the Programmable Current DAC

Table 8. Baseband Differential Offset Adjustment Factors

ADJUSTMENT	REGISTER BITS	BIT ADDRESS
I input differential offset programmability	I Offset Ref Curr	IOFF_n Register 6 Bits 12..5
Q input differential offset programmability	Q Offset Ref Curr	QOFF Register 6 Bits 20..13
Offset Programmability Range	DCoffset_I_n	Register 7 Bits 30..29

7.3.14 Internal Baseband Bias Voltage Generation

The TRF372017 has the ability to generate DC voltage levels for its baseband inputs internally. Register settings in the device allow the user to adjust common mode voltage of the I and Q signals separately. There are three adjustment factors for the baseband inputs. These are described in Table 9.

Table 9. Baseband Adjustment Factors

ADJUSTMENT	REGISTER BITS	BIT ADDRESSING
VCM setting	VREF_SEL_n	Register 6 Bits 23..21
VCM Enable	PWD_BB_VCM	Register 4 Bit 15
Bias select	IB_VCM_SEL	Register 7 Bit 25

Each baseband input pair includes the circuitry depicted in Figure 85. The Vref set voltage impacts all four terminals: IP, IN, QP, and QN. The effect of changing the reference voltage is shown in Figure 77. Each node also includes a programmable current DAC that injects current into the positive and negative terminals of each input.

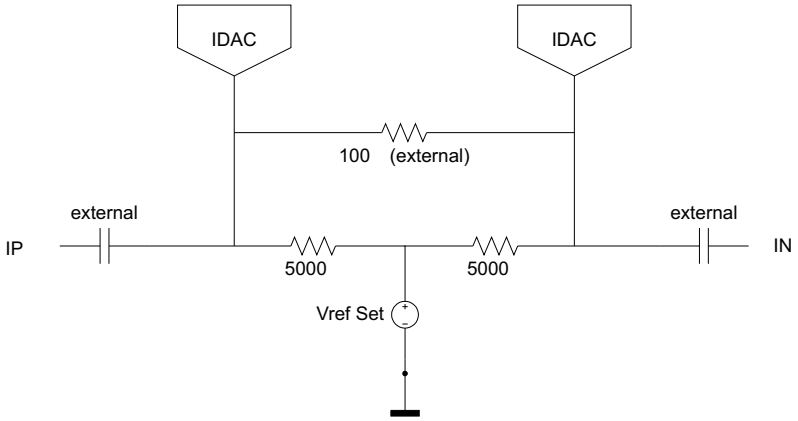


Figure 85. Block Diagram of the Baseband I Input Nodes

Table 10. Frequency Range Operation

VCO FREQUENCY		DIV BY 2		DIV BY 4		DIV BY 8	
Fmin	Fmax	Fmin	Fmax	Fmin	Fmax	Fmin	Fmax
2400	4800	1200	2400	600	1200	300	600

7.4 Device Functional Modes

7.4.1 Powersave Mode

Powersave mode can be used to put the device into a low power consumption mode. The PLL block remains active in Powersave mode, reducing the time required for start-up. However, the modulator, dividers, output buffers, and baseband common mode generation blocks are powered down. The SPI block remains active, and registers are addressable. Use the PS pin to activate powersave mode.

7.5 Register Maps

7.5.1 Serial Interface Programming Registers Definition

The TRF372017 features a 3-wire serial programming interface (SPI) that controls an internal 32-bit shift register. There are a total of 3 signals that must be applied: the clock (CLK, pin 47), the serial data (DATA, pin 46) and the latch enable (LE, pin 45). The TRF372017 has an additional pin (RDBK, pin 2) for read-back functionality. This pin is a digital pin and can be used to read-back values of different internal registers.

The DATA (DB0-DB31) is loaded LSB first and is read on the rising edge of the CLOCK. The LE is asynchronous to the CLOCK and at its rising edge the data in the shift register gets loaded onto the selected internal register. The 5 LSB of the Data field are the address bits to select the available internal registers.

7.5.1.1 PLL SPI Registers

7.5.1.1.1 Register 1

Table 11. Register 1

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
Register address					Reference Clock Divider										

Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31
….		RSV	REF INV	VCO NEG	Charge Pump Current					CP DOUBLE	VCO Cal CLK div/Mult				RSV

Table 12. Register 1 Field Descriptions

REGISTER 1	NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	1	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	RDIV_0	1	13-bit Reference Divider value (minimum value Rmin= 1, B[17..5] = [00 0000 0000 001]; maximum value Rmax=8191, B[17..5] = [11 1111 1111 111];
Bit6	RDIV_1	0	
Bit7	RDIV_2	0	
Bit8	RDIV_3	0	
Bit9	RDIV_4	0	
Bit10	RDIV_5	0	
Bit11	RDIV_6	0	
Bit12	RDIV_7	0	
Bit13	RDIV_8	0	
Bit14	RDIV_9	0	
Bit15	RDIV_10	0	
Bit16	RDIV_11	0	
Bit17	RDIV_12	0	
Bit18	RSV	0	
Bit19	REF_INV	0	Invert Reference Clock polarity; 1 = use falling edge
Bit20	NEG_VCO	1	VCO polarity control; 1= negative slope (negative K_v)
Bit21	ICP_0	0	Program Charge Pump DC current, ICP 1.94mA, B[25..21] = [00 000] 0.47mA, B[25..21] = [11 111] 0.97mA, default value, , B[25..21] = [01 010]
Bit22	ICP_1	1	
Bit23	ICP_2	0	
Bit24	ICP_3	1	
Bit25	ICP_4	0	
Bit26	ICPDOUBLE	0	1 = set ICP to double the current

Table 12. Register 1 Field Descriptions (continued)

REGISTER 1	NAME	RESET VALUE	DESCRIPTION
Bit27	CAL_CLK_SEL_0	0	Multiplication or division factor to create VCO calibration clock from PFD frequency
Bit28	CAL_CLK _SEL_1	0	
Bit29	CAL_CLK _SEL_2	0	
Bit30	CAL_CLK _SEL_3	1	
Bit31	RSV	0	

CAL_CLK_SEL[3..0]: Set the frequency divider value used to derive the VCO calibration clock from the phase detector frequency.

Table 13. Scaling Factors

CAL_CLK_SEL	SCALING FACTOR
1111	1/128
1110	1/64
1101	1/32
1100	1/16
1011	1/8
1010	1/4
1001	½
1000	1
0110	2
0101	4
0100	8
0011	16
0010	32
0001	64
0000	128

ICP[4..0]: Set the charge pump current.

Table 14. ICP and Current

ICP[4..0]	CURRENT (mA)
00 000	1.94
00 001	1.76
00 010	1.62
00 011	1.49
00 100	1.38
00 101	1.29
00 110	1.21
00 111	1.14
01 000	1.08
01 001	1.02
01 010	0.97
01 011	0.92
01 100	0.88
01 101	0.84
01 110	0.81
01 111	0.78
10 000	0.75
10 001	0.72

Table 14. ICP and Current (continued)

ICP[4..0]	CURRENT (mA)
10 010	0.69
10 011	0.67
10 100	0.65
10 101	0.63
10 110	0.61
10 111	0.59
11 000	0.57
11 001	0.55
11 010	0.54
11 011	0.52
11 100	0.51
11 101	0.5
11 110	0.48
11 111	0.47

7.5.1.1.2 Register 2

Table 15. Register 2

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
Register address					N-Divider Value										

Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31
...					PLL divider setting		Prescaler Select	RSV	RSV	VCO select		FCO sel mode	Cal accuracy		CAL

Table 16. Register 2 Field Descriptions

REGISTER 2	NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	1	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	NINT_0	0	PLL N-divider division setting
Bit6	NINT_1	0	
Bit7	NINT_2	0	
Bit8	NINT_3	0	
Bit9	NINT_4	0	
Bit10	NINT_5	0	
Bit11	NINT_6	0	
Bit12	NINT_7	1	
Bit13	NINT_8	0	
Bit14	NINT_9	0	
Bit15	NINT_10	0	
Bit16	NINT_11	0	
Bit17	NINT_12	0	
Bit18	NINT_13	0	
Bit19	NINT_14	0	
Bit20	NINT_15	0	

Table 16. Register 2 Field Descriptions (continued)

REGISTER 2	NAME	RESET VALUE	DESCRIPTION
Bit21	PLL_DIV_SEL0	1	Select division ratio of divider in front of prescaler
Bit22	PLL_DIV_SEL1	0	
Bit23	PRSC_SEL	1	Set prescaler modulus (0 → 4/5; 1 → 8/9)
Bit24	RSV	0	
Bit25	RSV	0	
Bit26	VCO_SEL_0	0	Selects between the four integrated VCOs 00 = lowest frequency VCO; 11 = highest frequency VCO
Bit27	VCO_SEL_1	1	
Bit28	VCOSEL_MODE	0	Single VCO auto-calibration mode (1 = active)
Bit29	CAL_ACC_0	0	Error count during the cap array calibration Recommended programming [00]
Bit30	CAL_ACC_1	0	
Bit31	EN_CAL	0	Execute a VCO frequency auto-calibration. Set to 1 to initiate a calibration. Resets automatically.

PLL_DIV<1,0>: Select division ratio of divider in front of prescaler.

Table 17. Frequency Divider

PLL DIV	FREQUENCY DIVIDER
00	1
01	2
10	4

VCOSEL_MODE<0>: When it is 1, the cap array calibration is run on the VCO selected through bits VCO_SEL<2,1>.

7.5.1.1.3 Register 3

Table 18. Register 3

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
Register address					Fractional N-Divider Value										

Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31
...														RSV	RSV

Table 19. Register 3 Field Descriptions

REGISTER 3	NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	1	Register address bits
Bit1	ADDR_1	1	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	

Table 19. Register 3 Field Descriptions (continued)

REGISTER 3	NAME	RESET VALUE	DESCRIPTION
Bit5	NFRAC<0>	0	Fractional PLL N divider value 0 to 0.99999.
Bit6	NFRAC<1>	0	
Bit7	NFRAC<2>	0	
Bit8	NFRAC<3>	0	
Bit9	NFRAC<4>	0	
Bit10	NFRAC<5>	0	
Bit11	NFRAC<6>	0	
Bit12	NFRAC<7>	0	
Bit13	NFRAC<8>	0	
Bit14	NFRAC<9>	0	
Bit15	NFRAC<10>	0	
Bit16	NFRAC<11>	0	
Bit17	NFRAC<12>	0	
Bit18	NFRAC<13>	0	
Bit19	NFRAC<14>	0	
Bit20	NFRAC<15>	0	
Bit21	NFRAC<16>	0	
Bit22	NFRAC<17>	0	
Bit23	NFRAC<18>	0	
Bit24	NFRAC<19>	0	
Bit25	NFRAC<20>	0	
Bit26	NFRAC<21>	0	
Bit27	NFRAC<22>	0	
Bit28	NFRAC<23>	0	
Bit29	NFRAC<24>	0	
Bit30	RSV	0	
Bit31	RSV	0	

7.5.1.1.4 Register 4

Table 20. Register 4

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
Register address					PD PLL	Power-Down PLL blocks									PD VCM

Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31
PD DC off	EXT VCO	PLL Test Control							ΣΔ Mode order			ΣΔ Mode controls			EN Fract mode

Table 21. Register 4 Field Descriptions

REGISTER 4	NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	1	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	PWD_PLL	0	Power-down all PLL blocks (1 = off)
Bit6	PWD_CP	0	When 1, charge pump is off

Table 21. Register 4 Field Descriptions (continued)

REGISTER 4	NAME	RESET VALUE	DESCRIPTION
Bit7	PWD_VCO	0	When 1, VCO is off
Bit8	PWD_VCOMUX	0	Power-down the 4 VCO mux block (1 = Off)
Bit9	PWD_DIV124	0	Power-down programmable RF divider in PLL feedback path (1 = off)
Bit10	PWD_PRESC	0	Power-down programmable prescaler (1 = off)
Bit11	RSV	0	
Bit12	PWD_OUT_BUFF	1	Power-down LO output buffer (1 = off).
Bit13	PWD_LO_DIV	1	Power-down frequency divider in LO output chain 1 (1 = off)
Bit14	PWD_TX_DIV	1	Power-down frequency divider in modulator chain (1 = off)
Bit15	PWD_BB_VCM	1	Power-down baseband input DC common block (1 = off)
Bit16	PWD_DC_OFF	1	Power-down baseband input DC offset control block (1 = off)
Bit17	EN_EXTVCO	0	Enable external LO/VCO input buffer (1 = enabled)
Bit18	EN_ISOURCE	0	Enable offset current at Charge Pump output (to be used in fractional mode only, 1 = on).
Bit19	LD_ANA_PREC_0	0	Control precision of analog lock detector (1 1 = low; 0 0 = high). See Lock Detect section of Application Information for usage details.
Bit20	LD_ANA_PREC_1	0	
Bit21	CP_TRISTATE_0	0	Set the charge pump output in Tristate mode. Normal, B[22..21] = [00] Down, B[22..21] = [01] Up, B[22..21] = [10] Tristate, B[22..21] = [11]
Bit22	CP_TRISTATE_1	0	
Bit23	SPEEDUP	0	Speed up PLL and Tx blocks by bypassing bias stabilizer capacitors.
Bit24	LD_DIG_PREC	0	Lock detector precision (increases sampling time if set to 1)
Bit25	EN_DITH	1	Enable ΔΣ modulator dither (1=on)
Bit26	MOD_ORD_0	0	ΔΣ modulator order (1 through 4). Not used in integer mode. 1st order, B[27..26] = [00] 2nd order, B[27..26] = [01] 3rd order, B[27..26] = [10] 4th order, B[27..26] = [11]
Bit27	MOD_ORD_1	1	
Bit28	DITH_SEL	0	Select dither mode for ΔΣ modulator (0 = const; 1 = pseudo-random)
Bit29	DEL_SD_CLK_0	0	ΔΣ modulator clock delay. Not used in integer mode. Min delay = 00 Max delay = 11
Bit30	DEL_SD_CLK_1	1	
Bit31	EN_FRAC	0	Enable fractional mode (1 = fractional enabled)

7.5.1.1.5 Register 5

Table 22. Register 5

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
Register address					VCO_R Trim			PLL_R_Trim		VCO Current				VCOBUF BIAS	

Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31
VCOMUX BIAS		OUTBUF BIAS		RSV		BIAS SEL	VCO CAL REF			VCOMUX AMPL		VCO Bias Voltage		RSV	EN_LD ISRC

Table 23. Register 5 Field Descriptions

REGISTER 5	NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	1	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	1	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	

Table 23. Register 5 Field Descriptions (continued)

REGISTER 5	NAME	RESET VALUE	DESCRIPTION
Bit5	VCOBIAS_RTRIM_0	0	VCO bias resistor trimming. Recommended programming [100].
Bit6	VCOBIAS_RTRIM_1	0	
Bit7	VCOBIAS_RTRIM_2	1	
Bit8	PLLBIAS_RTRIM_0	0	PLL bias resistor trimming. Recommended programming [10].
Bit9	PLLBIAS_RTRIM_1	1	
Bit10	VCO_BIAS_0	0	VCO bias reference current. 300 µA, B[13..10] = [00 00] 600 µA, B[13..10] = [11 11] Bias current varies directly with reference current Recommended programming 400 µA, B[13..10] = [0101] with VCC_VCO2 = 3.3 V 600 µA, B[13..10] = [1111] with VCC_VCO2 = 5 V
Bit11	VCO_BIAS_1	0	
Bit12	VCO_BIAS_2	0	
Bit13	VCO_BIAS_3	1	
Bit14	VCOBUF_BIAS_0	0	VCO buffer bias reference current. 300 µA, B[15..14] = [00] 600 µA, B[15..14] = [11] Bias current varies directly with reference current Recommended programming [10]
Bit15	VCOBUF_BIAS_1	1	
Bit16	VCOMUX_BIAS_0	0	VCO's muxing buffer bias reference current. 300 µA, B[17..16] = [00] 600 µA, B[17..16] = [11] Bias current varies directly with reference current Recommended programming [11]
Bit17	VCOMUX_BIAS_1	1	
Bit18	BUFOUT_BIAS_0	0	PLL output buffer bias reference current. 300 µA, B[19..18] = [00] 600 µA, B[19..18] = [11] Bias current varies directly with reference current
Bit19	BUFOUT_BIAS_1	1	
Bit20	RSV	0	
Bit21	RSV	1	
Bit22	VCO_CAL_IB	0	Select bias current type for VCO calibration circuitry 0 = PTAT; 1 = constant over temperature Recommended programming [0]
Bit23	VCO_CAL_REF_0	0	VCO calibration reference voltage trimming. 0.9 V, B[25..23] = [000] 1.4 V, B[25..23] = [111] Recommended programming [010]
Bit24	VCO_CAL_REF_1	0	
Bit25	VCO_CAL_REF_2	1	
Bit26	VCO_AMPL_CTRL_0	0	Adjust the signal amplitude at the VCO mux input Recommended programming [11]
Bit27	VCO_AMPL_CTRL_1	1	
Bit28	VCO_VB_CTRL_0	0	VCO core bias voltage control 1.2 V, B[29..28] = [00] 1.35 V, B[29..28] = [01] 1.5 V, B[29..28] = [10] 1.65 V, B[29..28] = [11] Recommended programming [00]
Bit29	VCO_VB_CTRL _1	1	
Bit30	RSV	0	
Bit31	EN_LD_ISOURCE	1	Enable monitoring of LD to turn on Isource when in frac-n mode (EN_FRAC=1). 0 = ISource set by EN_ISOURCE. 1 = ISource set by LD. Recommended programming [0]

7.5.1.1.6 Register 6

Table 24. Register 6

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
Register address					BB DC OFFSET										

Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31
BB DC OFFSET					VREF SEL			TXDIV SEL		LODIV SEL		TXDIV BIAS		LODIV BIAS	

Table 25. Register 6 Field Descriptions

REGISTER 6	NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	1	
Bit2	ADDR_2	1	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	IOFF_0	0	Adjust Iref current used for defining I DC offset. Full range, 2 × Iref, B[12..5] = [1 1111 111] Mid scale, Iref B[12..5] = [1 0000 000]
Bit6	IOFF_1	0	
Bit7	IOFF_2	0	
Bit8	IOFF_3	0	
Bit9	IOFF_4	0	
Bit10	IOFF_5	0	
Bit11	IOFF_6	0	
Bit12	IOFF_7	1	
Bit13	QOFF_0	0	Adjust Iref current used for defining Q DC offset. Full range, 2 × Iref, B[20..13] = [1 1111 111] Mid scale, Iref B[20..13] = [1 0000 000]
Bit14	QOFF_1	0	
Bit15	QOFF_2	0	
Bit16	QOFF_3	0	
Bit17	QOFF_4	0	
Bit18	QOFF_5	0	
Bit19	QOFF_6	0	
Bit20	QOFF_7	1	
Bit21	VREF_SEL_0	0	Adjust Vref in baseband common mode generation circuit. 0.65 V, B[23..21] = [000] 1 V, B[23..21] = [111] Modulator common mode is Vref + Vbe. Recommended programming [100]
Bit22	VREF_SEL_1	0	
Bit23	VREF_SEL_2	1	
Bit24	TX_DIV_SEL_0	0	Adjust Tx path divider. Div1, [B25..24] = [00] Div2, [B25..24] = [01] Div4, [B25..24] = [10] Div8, [B25..24] = [11]
Bit25	TX_DIV_SEL_1	0	
Bit26	LO_DIV_SEL_0	0	Adjust LO path divider Div1, [B28..27] = [00] Div2, [B28..27] = [01] Div4, [B28..27] = [10] Div8, [B28..27] = [11]
Bit27	LO_DIV_SEL_1	0	
Bit28	TX_DIV_BIAS_0	0	TX divider bias reference current 25 µA, [B29..28] = [00] 37.5 µA, [B29..28] = [01] 50 µA, [B29..28] = [10] 62.5 µA, [B29..28] = [11] Bias current varies directly with reference current
Bit29	TX_DIV_BIAS_1	1	
Bit30	LO_DIV_BIAS_0	0	LO divider bias reference current 25 µA, [B29..28] = [00] 37.5 µA, [B29..28] = [01] 50 µA, [B29..28] = [10] 62.5 µA, [B29..28] = [11] Bias current varies directly with reference current
Bit31	LO_DIV_BIAS_1	1	

7.5.1.1.7 Register 7

Table 26. Register 7

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
Register address					VCO CAP ARRAY CONTROL								RSV	VCO test mode	CAL bypass

Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31
MUX CONTROL			ISRC SINK	OFFSET CURRENT ADJUST			LP PD TimeConst		VCM Bias	MIX LO VCM			DC OFF REF		VCO BIAS SEL

Table 27. Register 7 Field Descriptions

REGISTER 7	NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	1	Register address bits
Bit1	ADDR_1	1	
Bit2	ADDR_2	1	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	RSV	0	
Bit6	RSV	0	
Bit7	VCO_TRIM_0	0	VCO capacitor array control bits, used in manual cal mode
Bit8	VCO_TRIM_1	0	
Bit9	VCO_TRIM_2	0	
Bit10	VCO_TRIM_3	0	
Bit11	VCO_TRIM_4	0	
Bit12	VCO_TRIM_5	1	
Bit13	RSV	0	
Bit14	VCO_TEST_MODE	0	Counter mode: measure max/min frequency of each VCO
Bit15	CAL_BYPASS	0	Bypass of VCO auto-calibration. When 1, VCO_TRIM and VCO_SEL bits are used to select the VCO and the cap array setting
Bit16	MUX_CTRL_0	1	Select signal for test output (pin 5, LD). [000] = Ground [001] = Lock detector [010] = NDIV counter output [011] = Ground [100] = RDIV counter output [101] = Ground [110] = A_counter output [111] = Logic high;
Bit17	MUX_CTRL_1	0	
Bit18	MUX_CTRL_2	0	
Bit19	ISOURCE_SINK	0	Charge pump offset current polarity.
Bit20	ISOURCE_TRIM_0	0	Adjust isource bias current in frac-n mode.
Bit21	ISOURCE_TRIM_1	0	
Bit22	ISOURCE_TRIM_2	1	
Bit23	PD_TC_0	0	Time constant control for PWD_OUT_BUFF [00] = Minimum time constant [11] = Maximum time constant
Bit24	PD_TC_1	0	
Bit25	IB_VCM_SEL	0	Select constant/ptat current for Common mode bias generation block 0 = PTAT 1 = const
Bit26	RSV	0	
Bit27	RSV	0	
Bit28	RSV	1	

Table 27. Register 7 Field Descriptions (continued)

REGISTER 7	NAME	RESET VALUE	DESCRIPTION
Bit29	DCOFFSET_I_0	0	Adjust BB input DC offset Iref 50 µA, B[27..26] = [00] 100 µA, B[27..26] = [01] 150 µA, B[27..26] = [10] 200 µA, B[27..26] = [11]
Bit30	DCOFFSET_I_1	1	
Bit31	VCO_BIAS_SEL	0	Select VCO_BIAS trim settings stored in EEPROM 0 = Use EEPROM settings if parity check is 1; otherwise, use SPI settings 1 = Use SPI settings Recommended programming [1]

7.5.1.2 Readback Mode

Register 0 functions as a Readback register. TRF372017 implements the capability to read-back the content of any serial programming interface register by initializing register 0.

Each read-back is composed by two phases: writing followed by the actual reading of the internal data. This is shown in the timing diagram in Figure 2. During the writing phase, a command is sent to TRF372017 register 0 to set it in read-back mode and to specify which register is to be read. In the proper reading phase, at each rising clock edge, the internal data is transferred into the RDBK pin and can be read at the following falling edge (LSB first). The first clock after the LE goes high (end of writing cycle) is idle and the following 32 clocks pulses transfer the internal register content to the RDBK pin.

7.5.1.2.1 Readback From the Internal Registers Banks

TRF372017 integrates 8 registers: Register 0 (000) to Register 7 (111). Registers 1 through 7 are used to set-up and control the TRF372017 functionalities, while register 0 is used for the readback function.

The latter register must be programmed with a specific command that sets TRF372017 in read-back mode and specifies the register to be read:

- Set B[31] to 1 to put TRF372017 in read-back mode.
- Set B[30,28] equal to the address of the register to be read (000 to 111).
- Set B27 to control the VCO frequency counter in VCO test mode.

7.5.1.2.1.1 Register 0 Write

Table 28. Register 0 Write

		NAME	RESET VALUE	DESCRIPTION
ADDRESS BITS	B0	ADDR<0>	0	Register 0 to be programmed to set TRF372017 in readback mode.
	B1	ADDR<1>	0	
	B2	ADDR<2>	0	
	B3	ADDR<3>	1	
	B4	ADDR<4>	0	

Table 28. Register 0 Write (continued)

		NAME	RESET VALUE	DESCRIPTION
DATA FIELD	B5	N/C	0	
	B6	N/C	0	
	B7	N/C	0	
	B8	N/C	0	
	B9	N/C	0	
	B10	N/C	0	
	B11	N/C	0	
	B12	N/C	0	
	B13	N/C	0	
	B14	N/C	0	
	B15	N/C	0	
	B16	N/C	0	
	B17	N/C	0	
	B18	N/C	0	
	B19	N/C	0	
	B20	N/C	0	
	B21	N/C	0	
	B22	N/C	0	
	B23	N/C	0	
	B24	N/C	0	
	B25	N/C	0	
	B26	N/C	0	
	B27	COUNT_MODE_MUX_SEL	0	Select Readback for VCO maximum frequency or minimum frequency. 0 = Max 1 = Min
	B28	RB_REG<0>	X	3 LSB's of the address for the register that is being read Reg 0, B[30..28] = [000] Reg 7, B[30..28] = [111]
	B29	RB_REG<1>	X	
	B30	RB_REG<2>	X	
	B31	RB_ENABLE	1	1 ≥ Put the device in Readback Mode

The contents of any register specified in RB_REG can be read back during the read cycle, including register 0.

Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12
Register address					CHIP_ID	NU						R_SAT_ERR

Bit13	Bit14	Bit15	Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30
COUNT0-7/VCO_TRM								COUNT8-10/VCO_SEL			COUNT11-17						

Bit31
COUNT_MODE-MUX-SEL

REGISTER 0	NAME	RESET VALUE	DESCRIPTION
Bit0	ADDR_0	0	Register address bits
Bit1	ADDR_1	0	
Bit2	ADDR_2	0	
Bit3	ADDR_3	1	
Bit4	ADDR_4	0	
Bit5	CHIP_ID_0	1	
Bit6	CHIP_ID_1	1	
Bit7	NU	x	

REGISTER 0	NAME	RESET VALUE	DESCRIPTION
Bit8	NU	x	
Bit9	NU	x	
Bit10	NU	x	
Bit11	NU	x	
Bit12	R_SAT_ERR	x	Error flag for calibration speed
Bit13	count_0/NU	x	B[30..13] = VCO frequency counter high when COUNT_MODE_MUX_SEL = 0 and VCO_TEST_MODE = 1
Bit14	count_1/NU	x	
Bit15	count_2/VCO_TRIM_0	x	
Bit16	count_3/VCO_TRIM_1	x	
Bit17	count_4/VCO_TRIM_2	x	
Bit18	count_5/VCO_TRIM_3	x	
Bit19	count_6/VCO_TRIM_4	x	
Bit20	count_7/VCO_TRIM_5	x	
Bit21	count_8/NU	x	B[30..13] = VCO frequency counter low when COUNT_MODE_MUX_SEL = 1 and VCO_TEST_MODE = 1
Bit22	count_9/VCO_sel_0	x	
Bit23	count_10/VCO_sel_1	x	
Bit24	count<11>	x	B[20..15] = Autocal results for VCO_TRIM, B[23..22] = Autocal results for VCO_SEL when VCO_TEST_MODE = 0
Bit25	count<12>	x	
Bit26	count<13>	x	
Bit27	count<14>	x	
Bit28	count<15>	x	
Bit29	count<16>	x	
Bit30	count<17>	x	
Bit31	COUNT_MODE_MUX_SEL	x	0 = Minimum frequency 1 = Maximum frequency

8 Application and Implementation

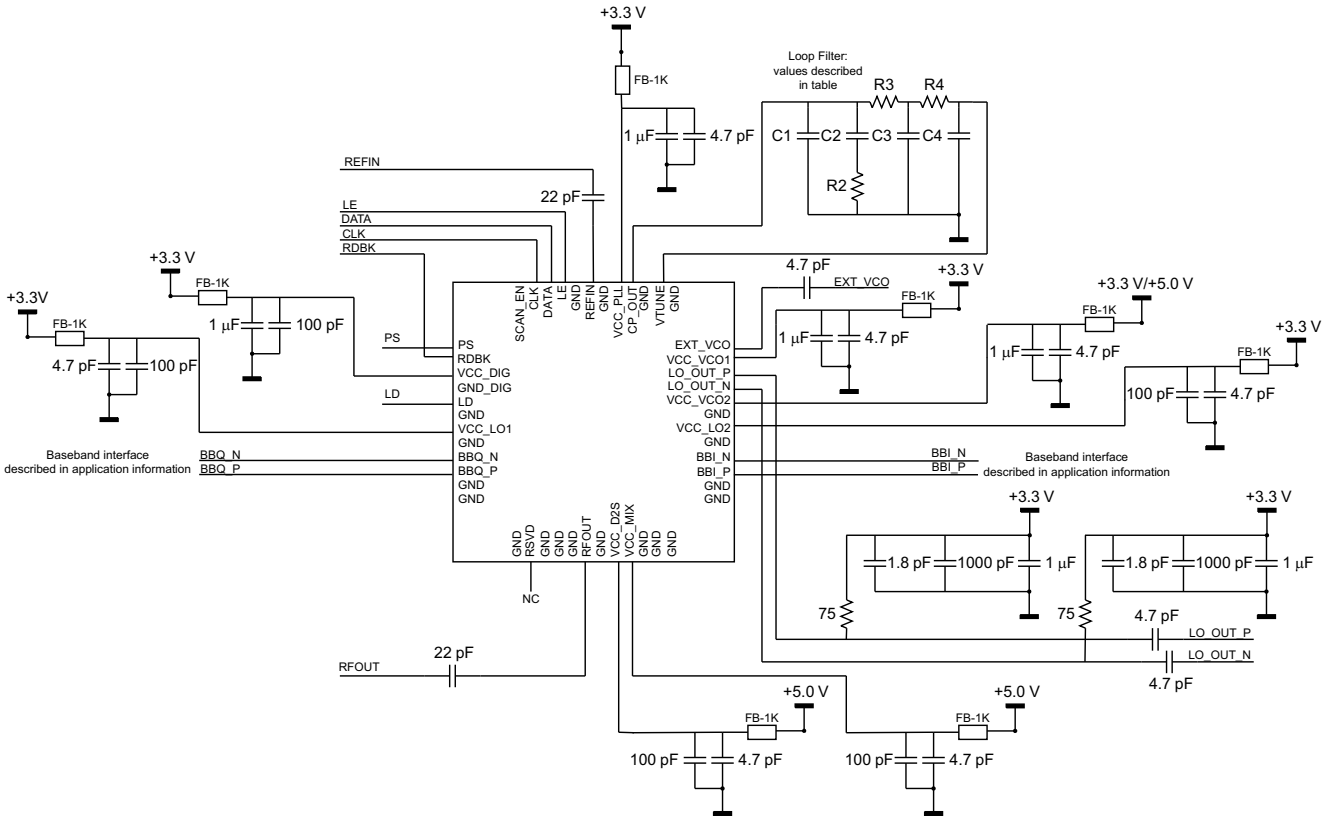
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TRF372017 is suited for quadrature up-conversion applications such as wireless radio transmitters.

8.2 Typical Application



Typical Application (continued)

8.2.1 Design Requirements

Table 29 shows the design requirements for this application.

Table 29. Quadrature Up-Converter Design Requirements for Wireless Transmitter Application

PARAMETER	REQUIREMENT(1)	TRF372017 PERFORMANCE
Gain	–5 to 0 dB	–3.1 dB
Noise figure, NF	<21 dB	19 dB
3rd order intercept (IIP3)	>+20 dBm	+25 dBm
1dB compression (P1dB)	>+10 dBm	+11.5 dBm
ACPR	>70 dBc	75 dBc
RF output frequency range	1500 to 2500 MHz	300 to 4300 MHz
LO input frequency range	1000 to 3000 MHz	300 to 4800 MHz
IF input frequency range	DC - 150 MHz	DC - 1 GHz
LO phase noise	<–130 dBc/Hz, 1 GHz, 1 MHz offset	–137 dBc/Hz, 1 GHz, 1 MHz offset

(1) These requirements represent a hypothetical application and do not reflect the performance of the TRF372017.

8.2.2 Detailed Design Procedure

8.2.2.1 DAC Interfacing With External Baseband Bias Voltage

Common-mode voltage on the baseband inputs can be generated either internally or externally. An external interface must provide 1.7-V DC and any necessary filtering. A typical interface to a DAC device is shown in Figure 86.

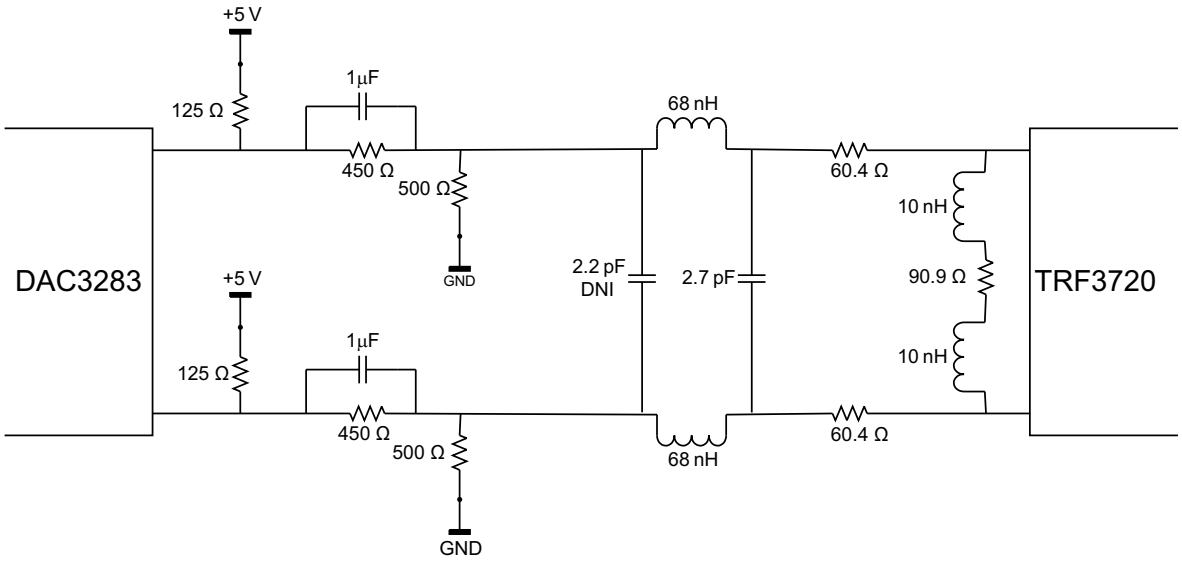


Figure 86. DAC to TRF372017 Interface With External VCM Generation

8.2.2.2 DAC Interface Using Internal VCM Generation

A typical DAC to TRF372017 interface using internal VCM generation is shown in Figure 87.

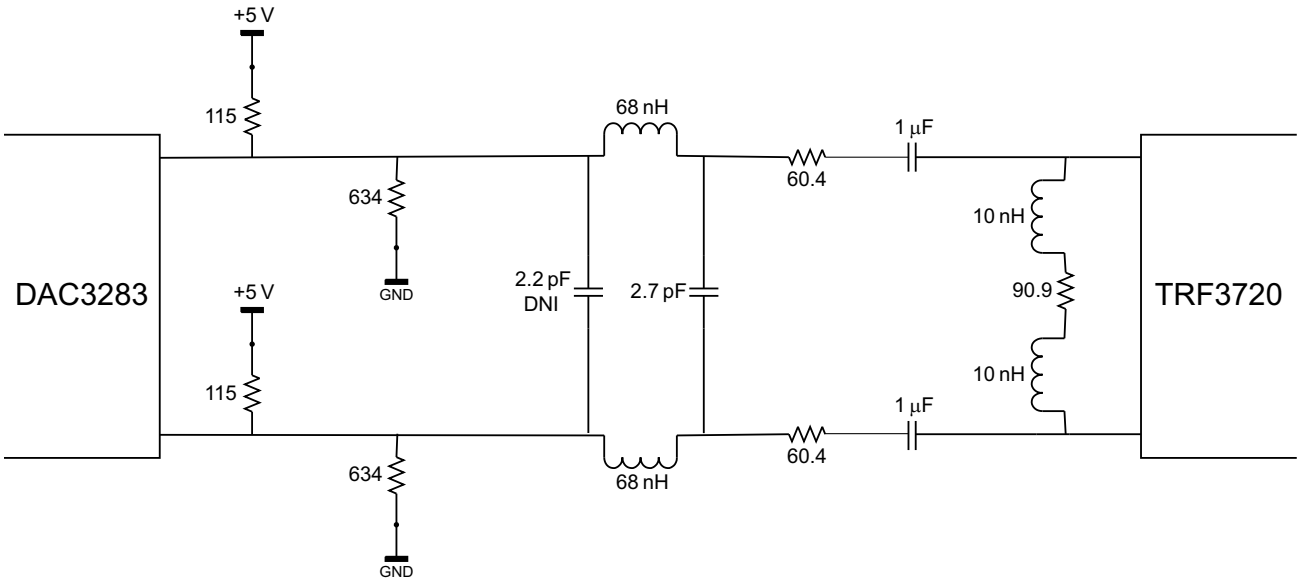


Figure 87. DAC to TRF372017 Interface With Internal VCM Generation

8.2.2.3 LO Outputs

The LO outputs are open collector outputs. They require a pullup to V_{CC}. 75-Ω pullup resistors to V_{CC} with local decoupling provides a good broadband match and is shown in an example circuit in Figure 88. An inductor pullup in parallel with a cap can provide a tuned load for excellent narrowband load matching.

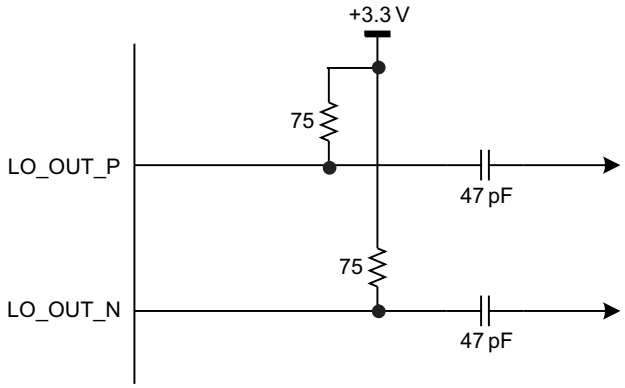


Figure 88. Example LO_OUT Circuit for Broadband Operation

8.2.2.4 Loop Filter

Loop filter design is critical for achieving low closed loop phase noise. Some typical loop filter component values are given in Table 30, referenced to designators in Figure 89. These loop filters are designed using charge pump current of 1.94 mA to minimize noise.

Table 30. Typical Loop Filter Components

f_{PFD} (MHz)	C1 (pF)	C2 (pF)	R2 (kΩ)	C3 (pF)	R3 (kΩ)	C4 (pF)	R4 (kΩ)
40	1000	10000	0.47	39	1.4	1.8	3.3
1.6	47	560	10	4.7	5	open	0
6.4	100	1000	5	20	5	open	0
10	270	4700	1.5	4700	1.5	open	0
30.72	2200	20000	0.47	220	0.475	220	0.475

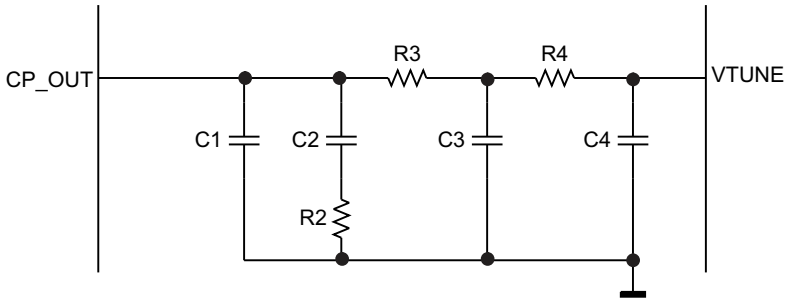


Figure 89. Loop Filter Component Reference Designators

8.2.2.5 ESD Sensitivity

RF devices may be extremely sensitive to electrostatic discharge (ESD) (see). To prevent damage from electrostatic discharge (ESD), devices must be stored and handled in a way that prevents the build up of electrostatic voltages that exceed the rated level. Rated electrostatic discharge (ESD) levels shall also not be exceeded while the device is installed on a printed-circuit board.

8.2.3 Application Curves

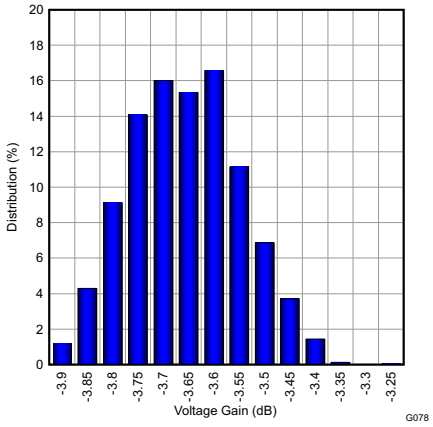


Figure 90. Gain at 2300-MHz Distribution

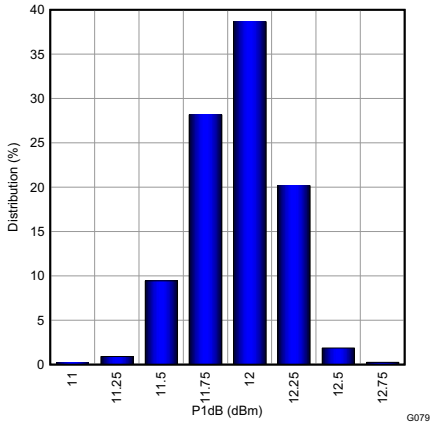


Figure 91. P1dB at 2300-MHz Distribution

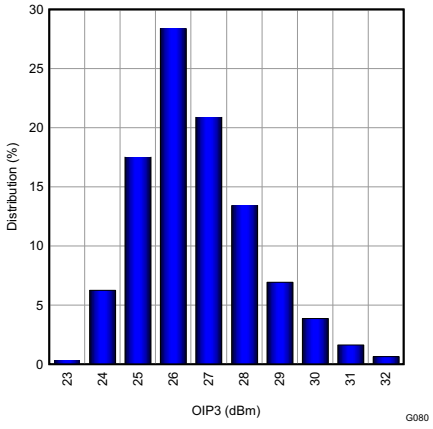


Figure 92. OIP3 at 2300-MHz Distribution

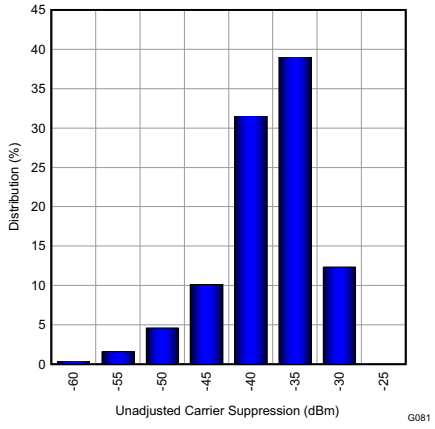


Figure 93. Unadjusted Carrier Suppression at 2300-MHz Distribution

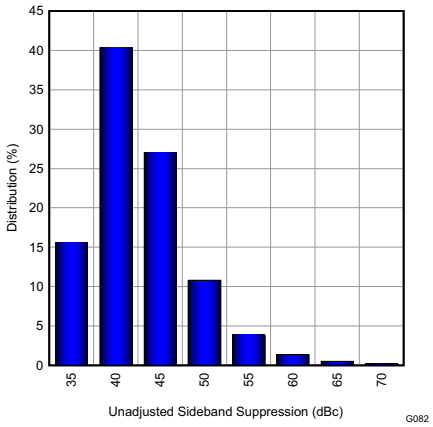


Figure 94. Unadjusted Sideband Suppression at 2300-MHz Distribution

9 Power Supply Recommendations

The TRF372017 must be supplied with a low noise 5-V or 3.3-V supply as required. Each supply pin must generally be isolated from the main power bus with a ferrite or other noise filtering component.

10 Layout

10.1 Layout Guidelines

Layout of the application board significantly impacts the analog performance of the TRF372017 device. Noise and high-speed signals must be prevented from leaking onto power-supply pins or analog signals. Follow these recommendations:

1. Place supply decoupling capacitors physically close to the device, on the same side of the board. Each supply pin must be isolated with a ferrite bead.
2. Maintain a continuous ground plane in the vicinity of the device and as return paths for all high-speed signal lines. Place reference plane vias or decoupling capacitors near any signal line reference transition.
3. The pad on the bottom of the device must be electrically grounded. Connect GND pins directly to the pad on the surface layer. Connect the GND pins and pad directly to surface ground where possible.
4. Power planes must not overlap each other or high-speed signal lines.
5. Isolate REF_IN routing from loop filter lines, control lines, and other high-speed lines.

See Figure 95 for an example of critical component layout (for the top PCB layer).

10.2 Layout Example

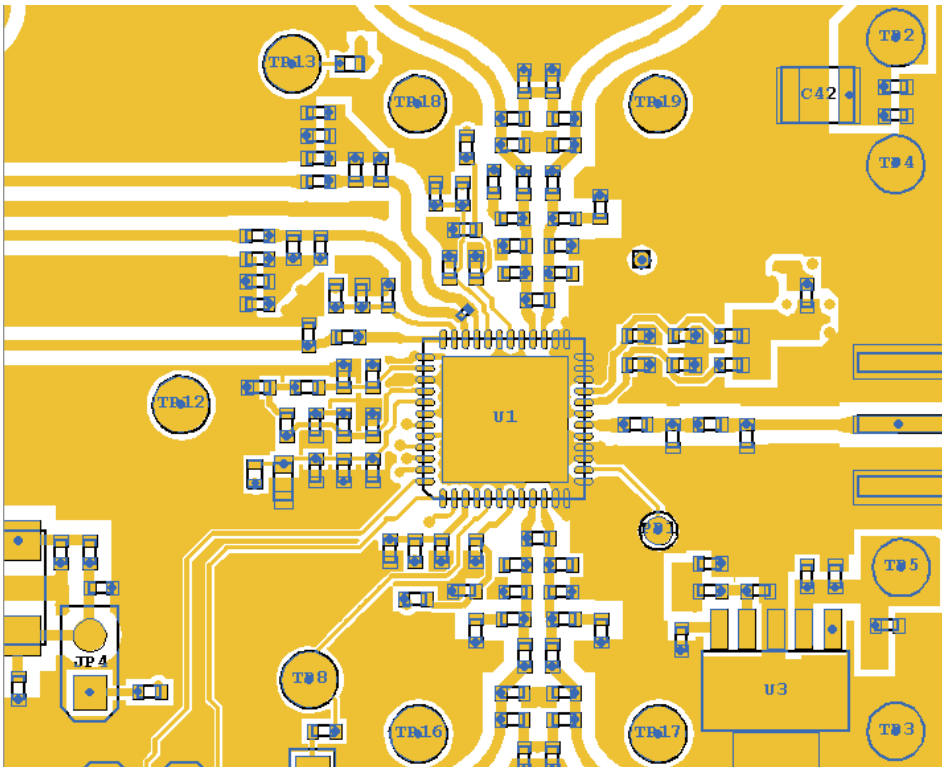


Figure 95. Critical Layout of the TRF372017 EVM Board

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF372017IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TRF372017 IRGZ	Samples
TRF372017IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	TRF372017 IRGZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

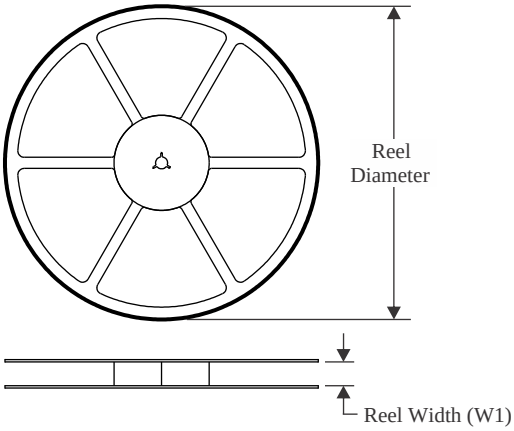
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

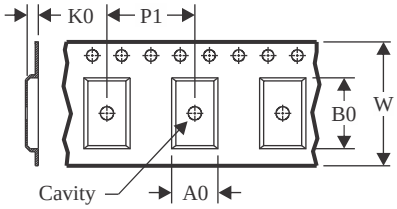
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

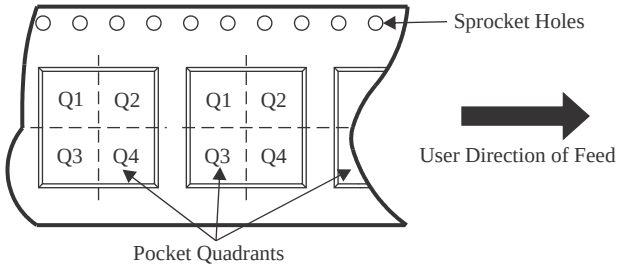


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

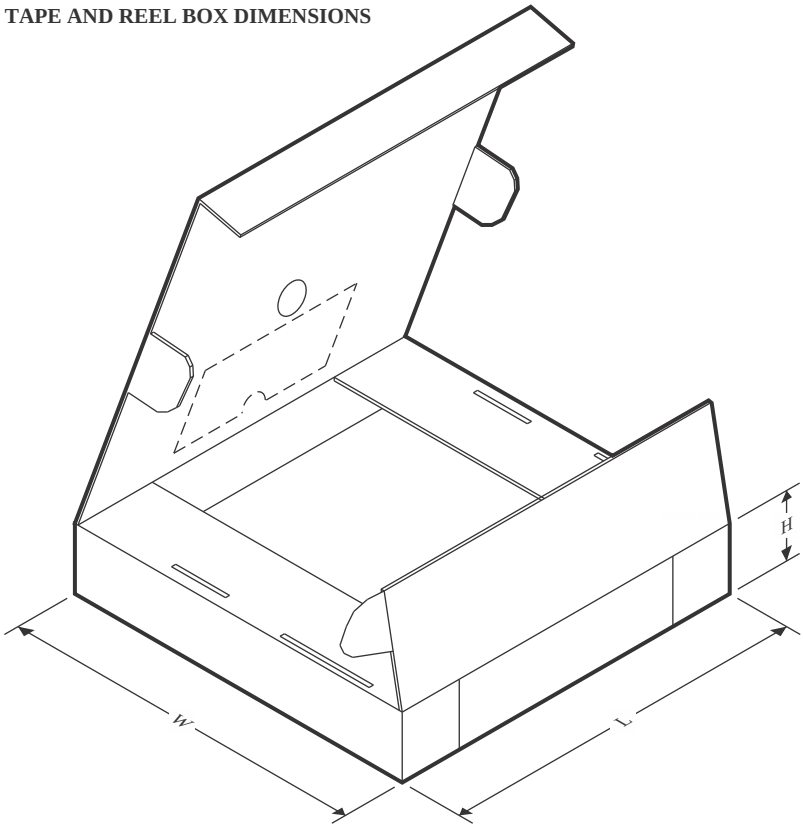
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF372017IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF372017IRGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0

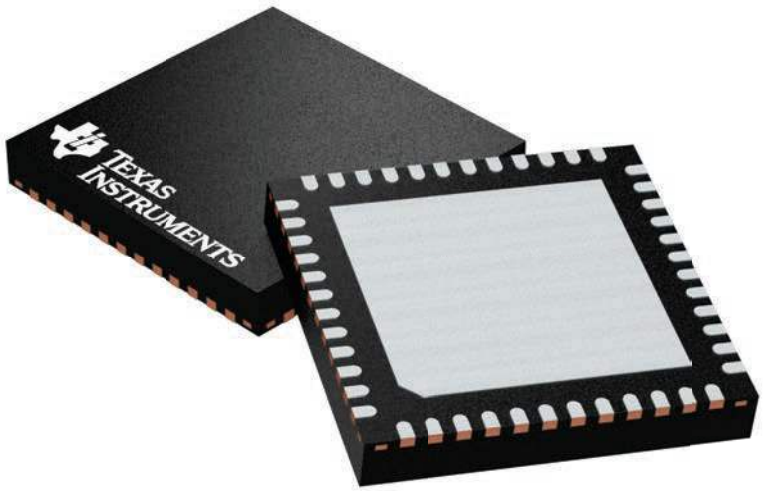
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

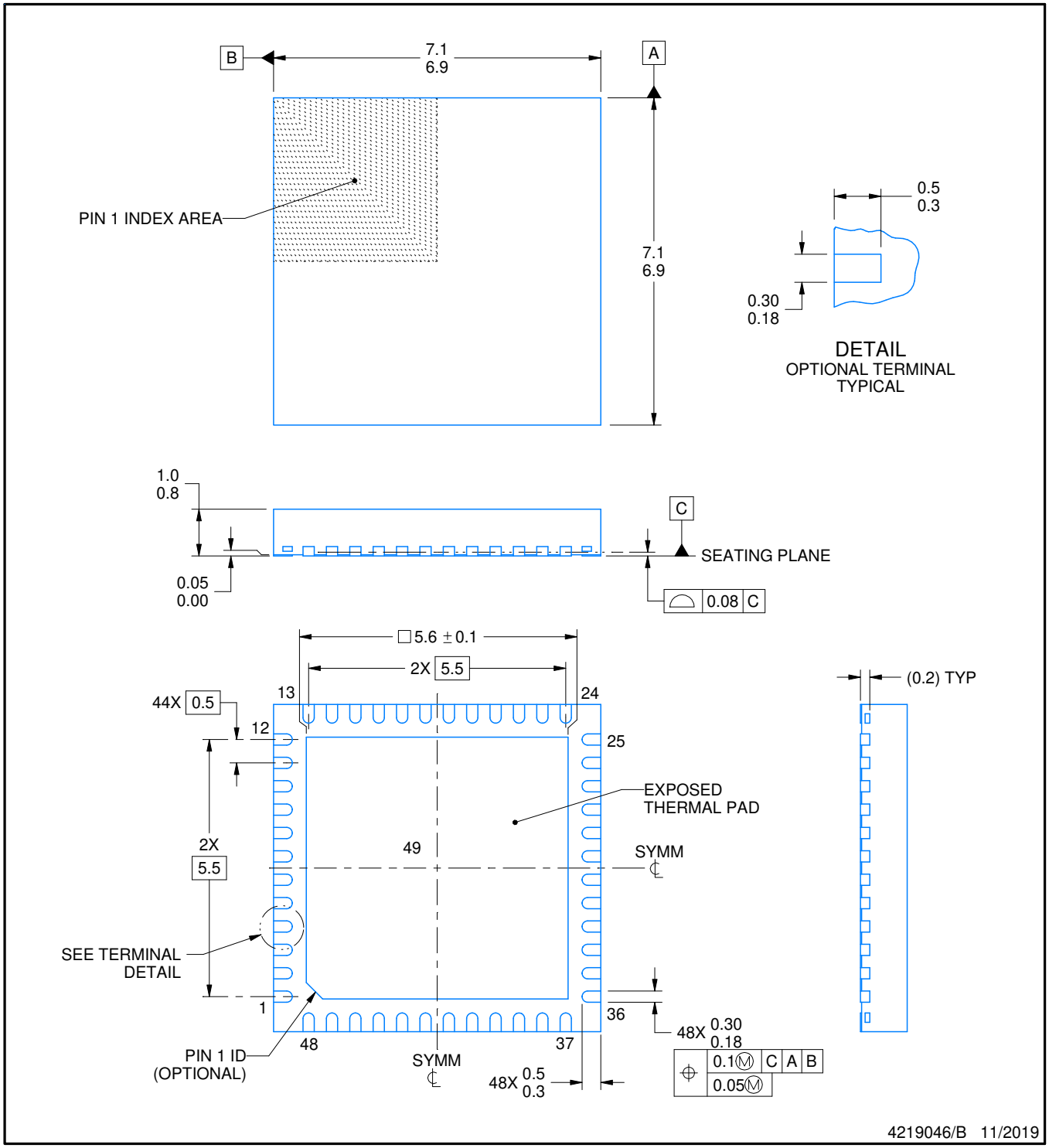
4224671/A

PACKAGE OUTLINE

RGZ0048D

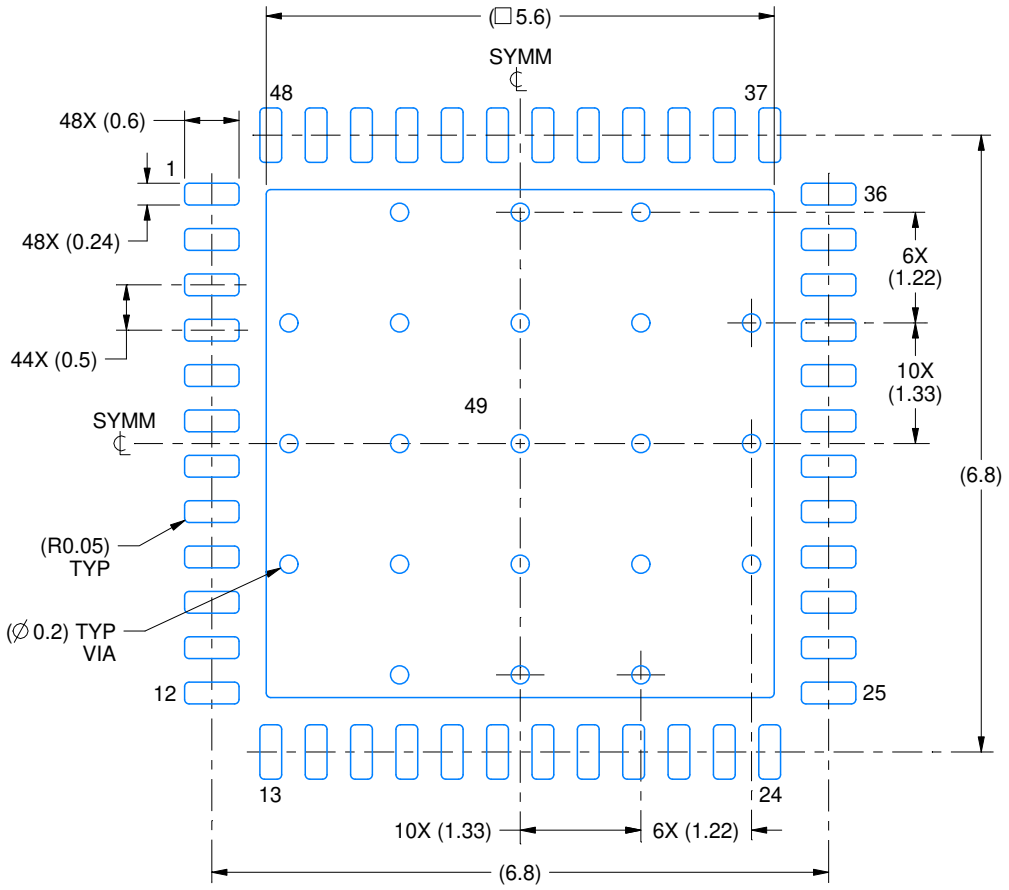
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

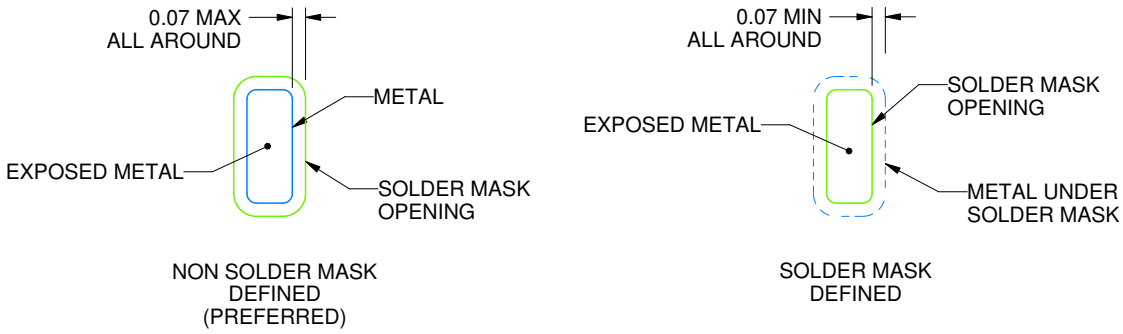


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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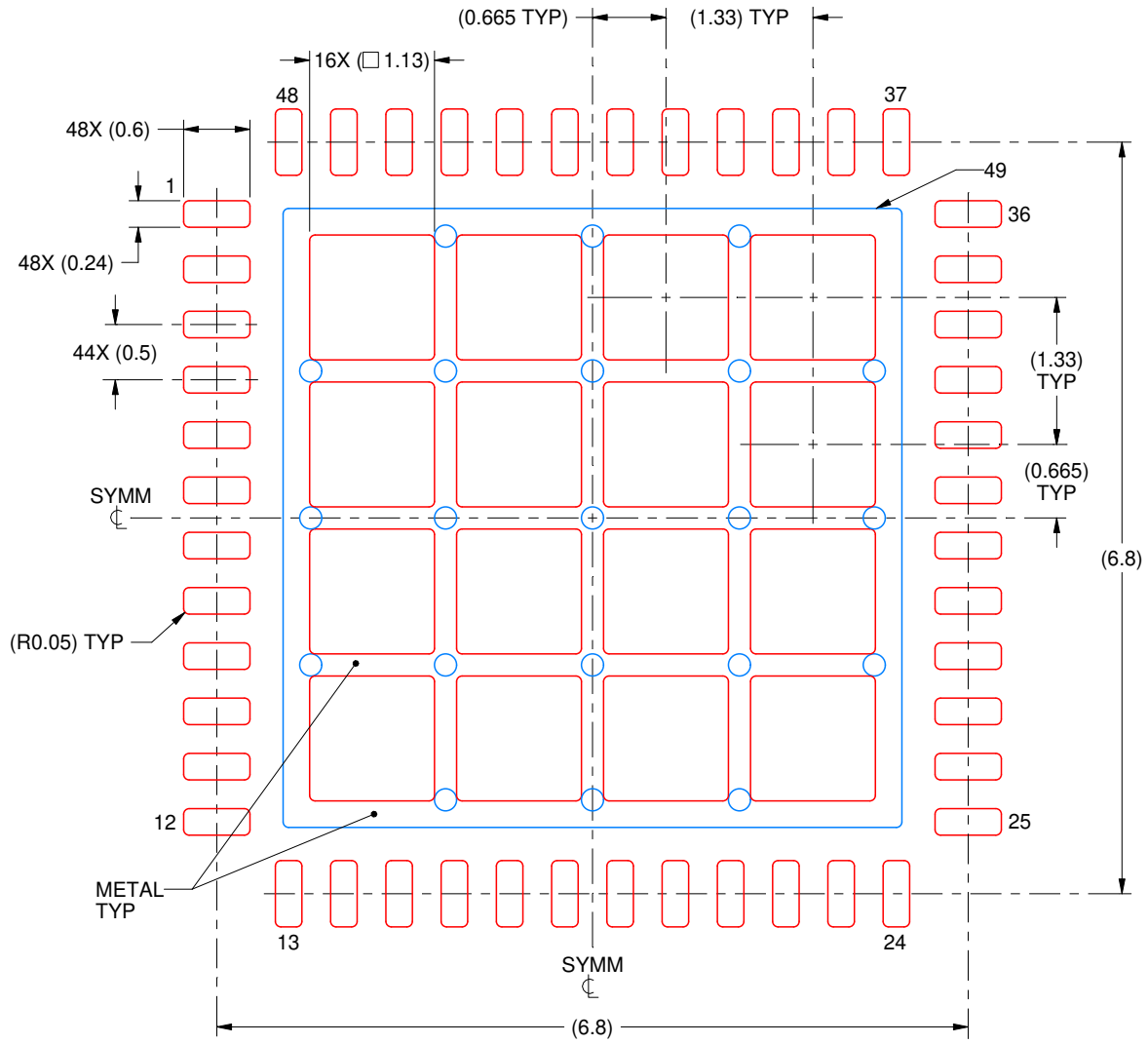
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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