

Features

- I_{off} supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

CY74FCT16823T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) < 1.0V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

CY74FCT162823T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$

Functional Description

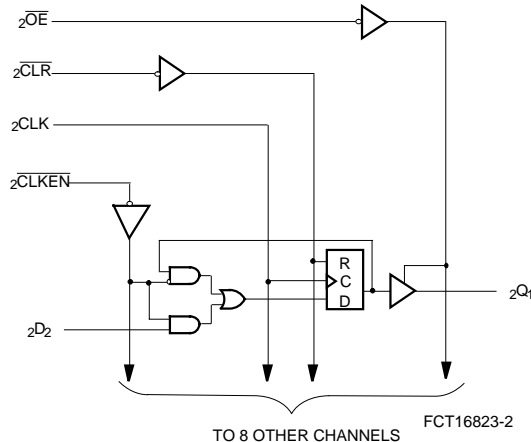
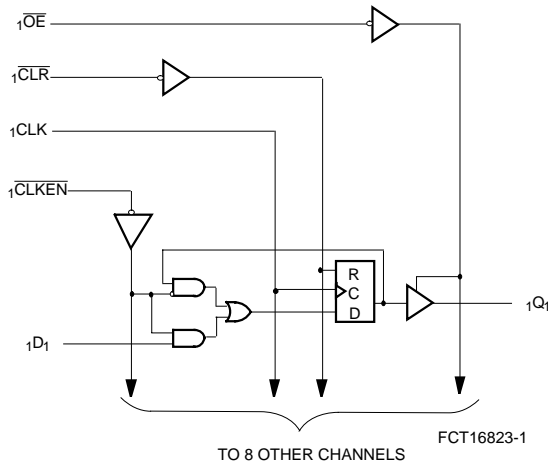
The CY74FCT16823T and the CY74FCT162823T 18-bit bus interface registers are designed for use in high-speed, low-power systems needing wide registers and parity. 18-bit operation is achieved by connecting the control lines of the two 9-bit registers. Flow-through pinout and small shrink packaging aids in simplifying board layout.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16823T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

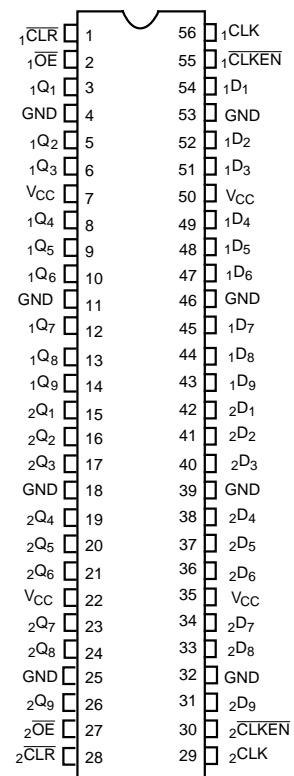
The CY74FCT162823T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162823T is ideal for driving transmission lines.

Logic Block Diagrams



**Pin Configuration
SSOP/TSSOP**

Top View



Pin Description

| Name | Description |
|-------|--|
| D | Data Inputs |
| CLK | Clock Inputs |
| CLKEN | Clock Enable Inputs (Active LOW) |
| CLR | Asynchronous Clear Inputs (Active LOW) |
| OE | Output Enable Inputs (Active LOW) |
| Q | Three-State Outputs |

Function Table^[1]

| Inputs | | | | | | Outputs |
|--------|-----|-------|-----|---|------------------|----------|
| OE | CLR | CLKEN | CLK | D | Q | Function |
| H | X | X | X | X | Z | High Z |
| L | L | X | X | X | L | Clear |
| L | H | H | X | X | Q ^[2] | Hold |
| H | H | L | ┐ | L | Z | Load |
| H | H | L | ┐ | H | Z | |
| L | H | L | ┐ | L | L | |
| L | H | L | ┐ | H | H | |

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|---|-----------------|
| Storage Temperature | -55°C to +125°C |
| Ambient Temperature with Power Applied | -55°C to +125°C |
| DC Input Voltage | -0.5V to +7.0V |
| DC Output Voltage | -0.5V to +7.0V |
| DC Output Current (Maximum Sink Current/Pin) | -60 to +120 mA |

| | |
|---|--------|
| Power Dissipation | 1.0W |
| Static Discharge Voltage..... (per MIL-STD-883, Method 3015) | >2001V |

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Industrial | -40°C to +85°C | 5V ± 10% |

Notes:

- H = HIGH Voltage Level.
L = LOW Voltage Level.
X = Don't Care.
Z = HIGH Impedance.
┐ = LOW-to-HIGH transition.
- Output level before indicated steady-state input conditions were established.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | Min. | Typ. ^[5] | Max. | Unit |
|------------------|---|--|------|---------------------|------|------|
| V _{IH} | Input HIGH Voltage | | 2.0 | | | V |
| V _{IL} | Input LOW Voltage | | | | 0.8 | V |
| V _H | Input Hysteresis ^[6] | | | 100 | | mV |
| V _{IK} | Input Clamp Diode Voltage | V _{CC} =Min., I _{IN} =-18 mA | | -0.7 | -1.2 | V |
| I _{IH} | Input HIGH Current | V _{CC} =Max., V _I =V _{CC} | | | ±1 | μA |
| I _{IL} | Input LOW Current | V _{CC} =Max., V _I =GND | | | ±1 | μA |
| I _{OZH} | High Impedance Output Current (Three-State Output pins) | V _{CC} =Max., V _{OUT} =2.7V | | | ±1 | μA |
| I _{OZL} | High Impedance Output Current (Three-State Output pins) | V _{CC} =Max., V _{OUT} =0.5V | | | ±1 | μA |
| I _{OS} | Short Circuit Current ^[7] | V _{CC} =Max., V _{OUT} =GND | -80 | -140 | -200 | mA |
| I _O | Output Drive Current ^[7] | V _{CC} =Max., V _{OUT} =2.5V | -50 | | -180 | mA |
| I _{OFF} | Power-Off Disable | V _{CC} =0V, V _{OUT} ≤4.5V ^[8] | | | 1 | μA |

Output Drive Characteristics for CY74FCT16823T

| Parameter | Description | Test Conditions | Min. | Typ. ^[5] | Max. | Unit |
|-----------------|---------------------|--|------|---------------------|------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} =Min., I _{OH} =-3 mA | 2.5 | 3.5 | | V |
| | | V _{CC} =Min., I _{OH} =-15 mA | 2.4 | 3.5 | | |
| | | V _{CC} =Min., I _{OH} =-32 mA | 2.0 | 3.0 | | |
| V _{OL} | Output LOW Voltage | V _{CC} =Min., I _{OL} =64 mA | | 0.2 | 0.55 | V |

Output Drive Characteristics for CY74FCT162823T

| Parameter | Description | Test Conditions | Min. | Typ. ^[5] | Max. | Unit |
|------------------|------------------------------------|---|------|---------------------|------|------|
| I _{ODL} | Output LOW Voltage ^[7] | V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V | 60 | 115 | 150 | mA |
| I _{ODH} | Output HIGH Voltage ^[7] | V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V | -60 | -115 | -150 | mA |
| V _{OH} | Output HIGH Voltage | V _{CC} =Min., I _{OH} =-24 mA | 2.4 | 3.3 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} =Min., I _{OL} =24 mA | | 0.3 | 0.55 | V |

Capacitance^[9] (T_A = +25°C, f = 1.0 MHz)

| Parameter | Description | Test Conditions | Typ. ^[5] | Max. | Unit |
|------------------|--------------------|-----------------------|---------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 4.5 | 6.0 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 5.5 | 8.0 | pF |

Notes:

- Typical values are at V_{CC}= 5.0V, T_A= +25°C ambient.
- This input is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Tested at +25°C.
- This parameter is specified but not tested.

Power Supply Characteristics

| Parameter | Description | Test Conditions ^[10] | | Min. | Typ. ^[5] | Max. | Unit |
|-----------------|--|---|---|------|---------------------|----------------------|--------------------------|
| I_{CC} | Quiescent Power Supply Current | $V_{CC}=\text{Max.}$ | $V_{IN}\leq 0.2V$ $V_{IN}\geq V_{CC}-0.2V$ | — | 5 | 500 | μA |
| ΔI_{CC} | Quiescent Power Supply Current (TTL inputs HIGH) | $V_{CC}=\text{Max.}$ | $V_{IN}=3.4V^{[11]}$ | — | 0.5 | 1.5 | mA |
| I_{CCD} | Dynamic Power Supply Current ^[12] | $V_{CC}=\text{Max.}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $OE=\text{CLKEN}=\text{GND}$ | $V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$ | — | 75 | 120 | $\mu\text{A}/\text{MHz}$ |
| I_C | Total Power Supply Current ^[13] | $V_{CC}=\text{Max.}$, $f_0=10\text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling, $OE=\text{CLKEN}=\text{GND}$ at $f_1=5\text{ MHz}$ | $V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$ | — | 0.8 | 1.7 | mA |
| | | | $V_{IN}=3.4V$ or $V_{IN}=\text{GND}$ | — | 1.3 | 3.2 | |
| | | $V_{CC}=\text{Max.}$, at $f_1=2.5\text{ MHz}$, 50% Duty Cycle, Outputs Open, Eighteen Bits Toggling, $OE=\text{CLKEN}=\text{GND}$ $f_0=10\text{ MHz}$ | $V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$ | — | 4.2 | 7.1 ^[14] | |
| | | | $V_{IN}=3.4V$ or $V_{IN}=\text{GND}$ | — | 9.2 | 22.1 ^[14] | |

Notes:

10. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
11. Per TTL driven input ($V_{IN}=3.4V$); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
13. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN}=3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamperes and all frequencies are in megahertz.
14. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[15]

| Parameter | Description | Condition ^[16] | CY74FCT16823AT CY74FCT162823AT | | Unit | Fig.No. ^[16] |
|--------------------------------------|---|--|-----------------------------------|------|------|-------------------------|
| | | | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay CLK to Q | C _L =50 pF R _L =500Ω | 1.5 | 10.0 | ns | 1, 5 |
| | | C _L =300 pF ^[17] R _L =500Ω | 1.5 | 20.0 | | |
| t _{PHL} | Propagation Delay $\overline{\text{CLR}}$ to Q | C _L =50 pF R _L =500Ω | 1.5 | 14.0 | ns | 1, 5 |
| t _{PZH} t _{PZL} | Output Enable Time $\overline{\text{OE}}$ to Q | C _L =50 pF R _L =500Ω | 1.5 | 12.0 | ns | 1, 7, 8 |
| | | C _L =300 pF ^[17] R _L =500Ω | 1.5 | 23.0 | | |
| t _{PHZ} t _{PLZ} | Output Disable Time $\overline{\text{OE}}$ to Q | C _L =5 pF ^[17] R _L =500Ω | 1.5 | 7.0 | ns | 1, 7, 8 |
| | | C _L =50 pF R _L =500Ω | 1.5 | 8.0 | | |
| t _{SU} | Set-Up Time HIGH or LOW, D to CLK | C _L =50 pF R _L =500Ω | 3.0 | — | ns | 4 |
| t _H | Hold Time HIGH or LOW, D to CLK | | 1.5 | — | ns | 4 |
| t _{SU} | Set-Up Time HIGH or LOW, $\overline{\text{CLKEN}}$ to CLK | | 3.0 | — | ns | 9 |
| t _H | Hold Time HIGH or LOW $\overline{\text{CLKEN}}$ to CLK | | 0.0 | — | ns | 9 |
| t _W | CLK Pulse Width HIGH or LOW | | 6.0 | — | ns | 5 |
| t _W | $\overline{\text{CLR}}$ Pulse Width LOW | | 6.0 | — | ns | 5 |
| t _{REM} | Recovery Time $\overline{\text{CLR}}$ to CLK | | 6.0 | — | ns | 6 |
| t _{SK(O)} | Output Skew ^[18] | | — | 0.5 | ns | — |

Switching Characteristics Over the Operating Range^[15]

| Parameter | Description | Condition ^[16] | CY74FCT16823CT CY74FCT162823CT | | Unit | Fig.No. ^[16] |
|--------------------------------------|--|--|-----------------------------------|------|------|-------------------------|
| | | | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay CLK to Q | C _L =50 pF R _L =500Ω | 1.5 | 6.0 | ns | 1, 5 |
| | | C _L =300 pF ^[17] R _L =500Ω | 1.5 | 12.5 | | |
| t _{PHL} | Propagation Delay $\overline{\text{CLR}}$ to Q | C _L =50 pF R _L =500Ω | 1.5 | 6.1 | ns | 1, 5 |
| t _{PZH} t _{PZL} | Output Enable Time $\overline{\text{OE}}$ to Q | C _L =50 pF R _L =500Ω | 1.5 | 5.5 | ns | 1, 7, 8 |
| | | C _L =300 pF ^[17] R _L =500Ω | 1.5 | 12.5 | | |
| t _{PHZ} t _{PLZ} | Output Disable Time $\overline{\text{OE}}$ to Q | C _L =5 pF ^[17] R _L =500Ω | 1.5 | 5.2 | ns | 1, 7, 8 |
| | | C _L =50 pF R _L =500Ω | 1.5 | 6.5 | | |

Switching Characteristics Over the Operating Range^[15] (continued)

| Parameter | Description | Condition ^[16] | CY74FCT16823CT CY74FCT162823CT | | Unit | Fig.No. ^[16] |
|--------------------|--|---|-----------------------------------|------|------|-------------------------|
| | | | Min. | Max. | | |
| t _{SU} | Set-Up Time HIGH or LOW, D to CLK | C _L =50 pF R _L =500Ω | 2.0 | — | ns | 4 |
| t _H | Hold Time HIGH or LOW, D to CLK | | 1.5 | — | ns | 4 |
| t _{SU} | Set-Up Time HIGH or LOW, $\overline{\text{CLKEN}}$ to CLK | | 3.0 | — | ns | 9 |
| t _H | Hold Time HIGH or LOW CLKEN to CLK | | 0.0 | — | ns | 9 |
| t _W | CLK Pulse Width HIGH or LOW | | 3.3 | — | ns | 5 |
| t _W | $\overline{\text{CLR}}$ Pulse Width LOW | | 3.3 | — | ns | 5 |
| t _{REM} | Recovery Time CLR to CLK | | 6.0 | — | ns | 6 |
| t _{SK(O)} | Output Skew ^[18] | | — | 0.5 | ns | — |

Notes:

15. Minimum limits are specified but not tested on Propagation Delays.
16. See "Parameter Measurement Information" in the General Information section.
17. These limits are specified but not tested.
18. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT16823

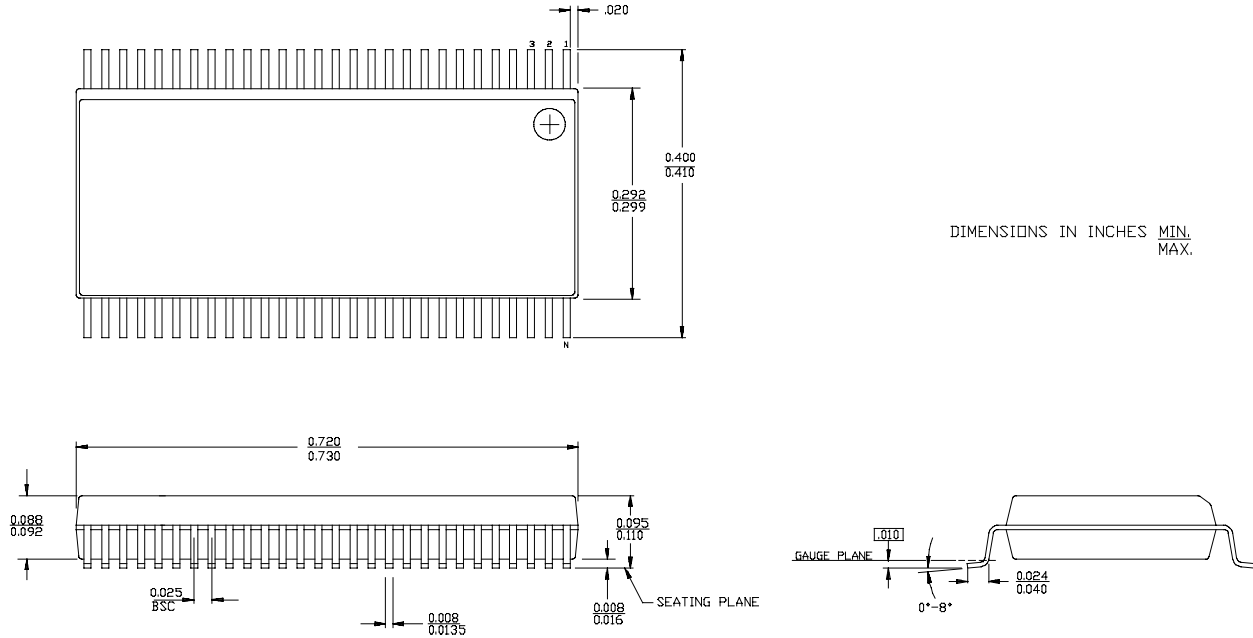
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|------------------------|--------------|-------------------------|-----------------|
| 6.0 | CY74FCT16823CTPACT | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT16823CTPVC/PVCT | O56 | 56-Lead (300-Mil) SSOP | |
| 10.0 | CY74FCT16823ATPACT | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |

Ordering Information CY74FCT162823

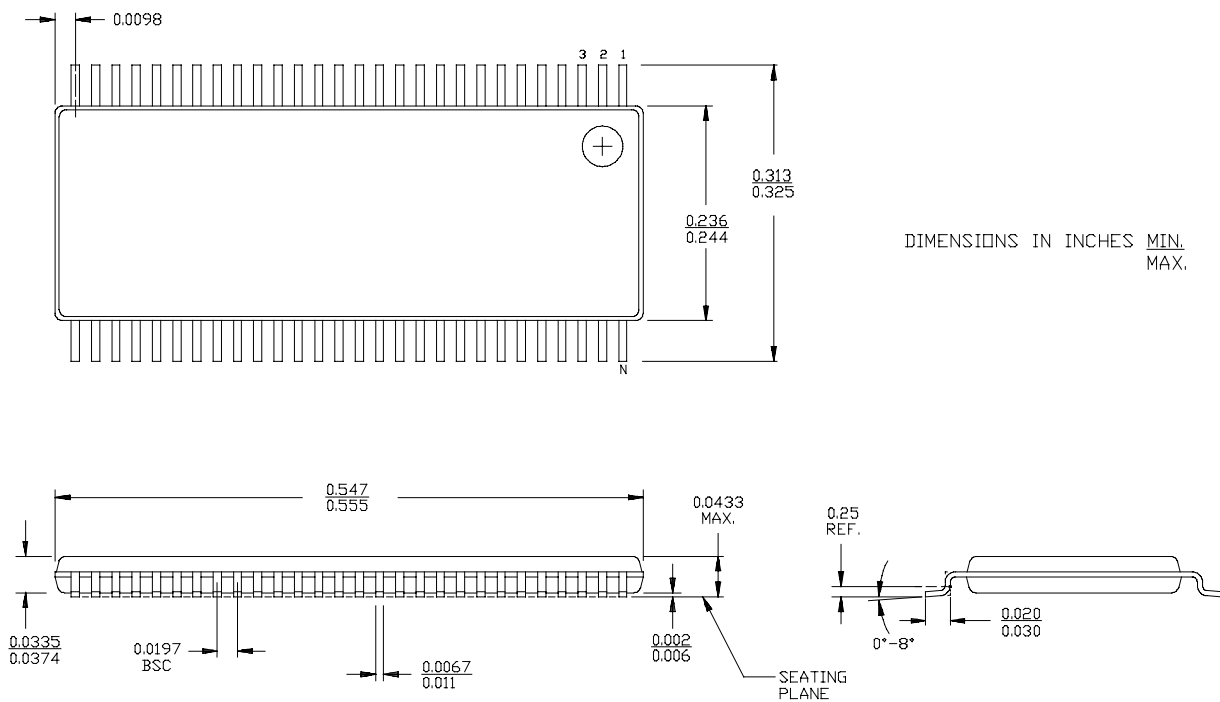
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|--------------------|--------------|-------------------------|-----------------|
| 6.0 | 74FCT162823CTPACT | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162823CTPVC | O56 | 56-Lead (300-Mil) SSOP | |
| | 74FCT162823CTPVCT | O56 | 56-Lead (300-Mil) SSOP | |
| 10.0 | 74FCT162823ATPACT | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |

Package Diagrams

56-Lead Shrunken Small Outline Package O56



56-Lead Thin Shrunken Small Outline Package Z56



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CY74FCT16823ATPACT | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT16823A | Samples |
| CY74FCT16823CTPVC | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT16823C | Samples |
| CY74FCT16823CTPVCT | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT16823C | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

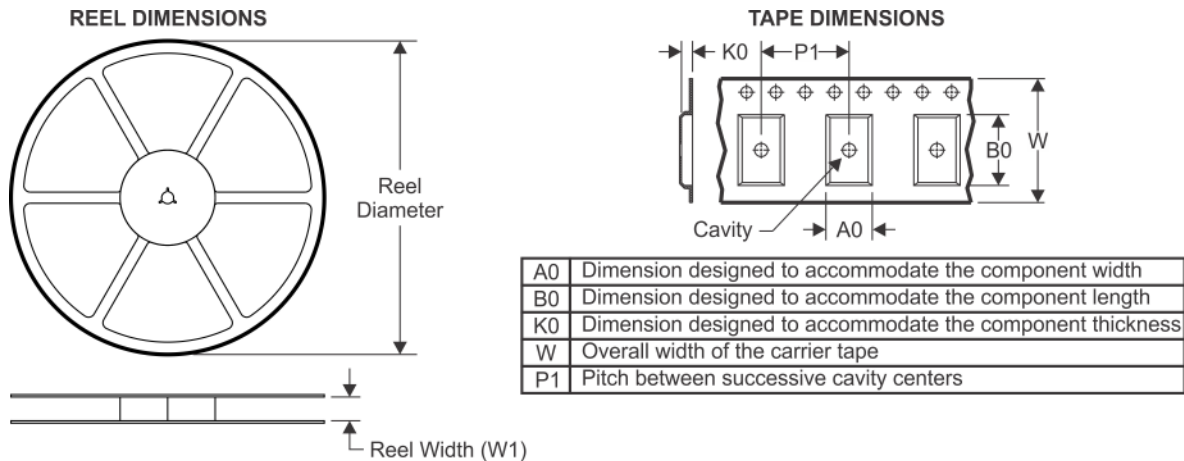
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CY74FCT16823ATPACT | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |
| CY74FCT16823CTPVCT | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

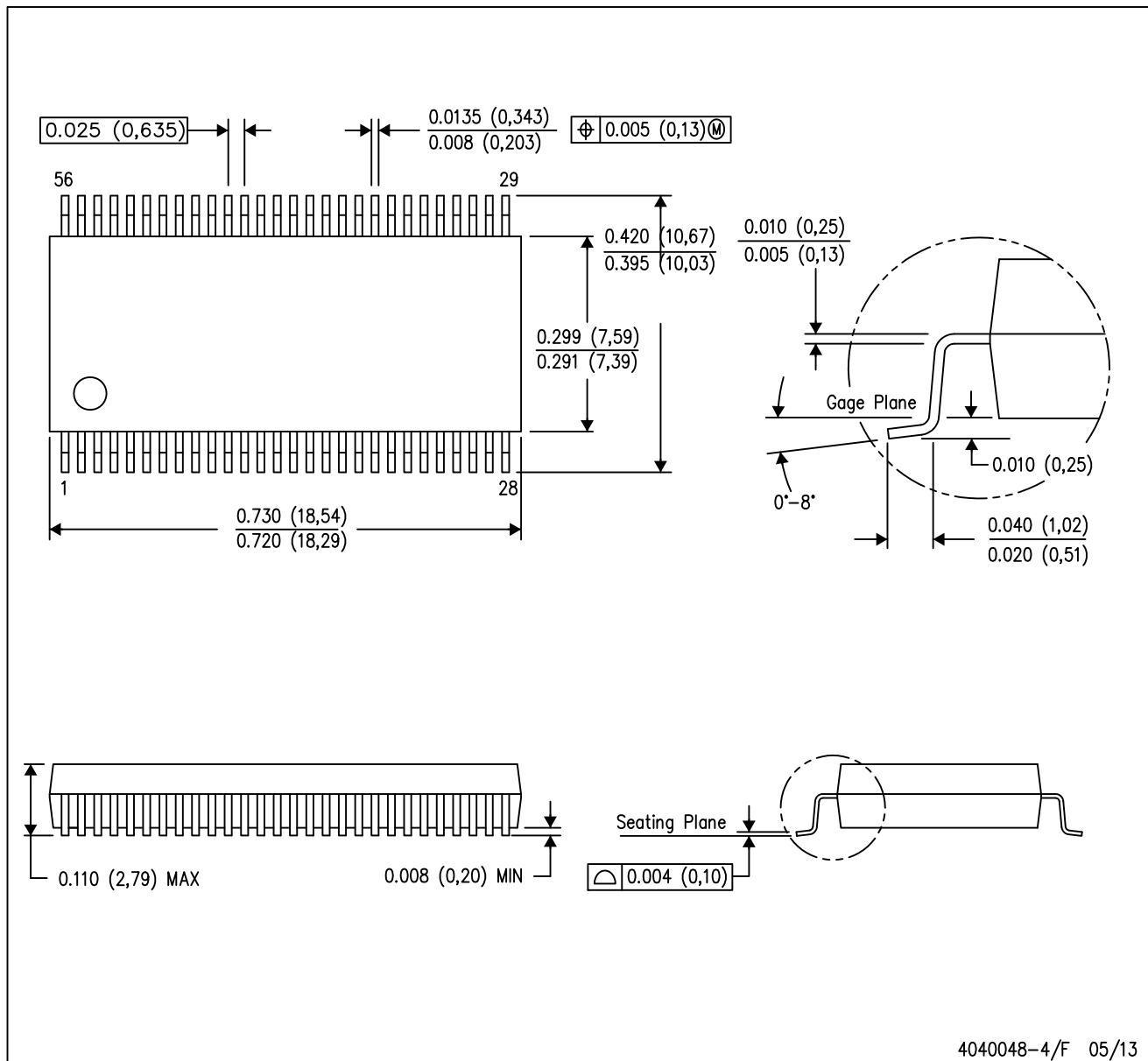

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CY74FCT16823ATPACT | TSSOP | DGG | 56 | 2000 | 367.0 | 367.0 | 45.0 |
| CY74FCT16823CTPVCT | SSOP | DL | 56 | 1000 | 367.0 | 367.0 | 55.0 |

MECHANICAL DATA

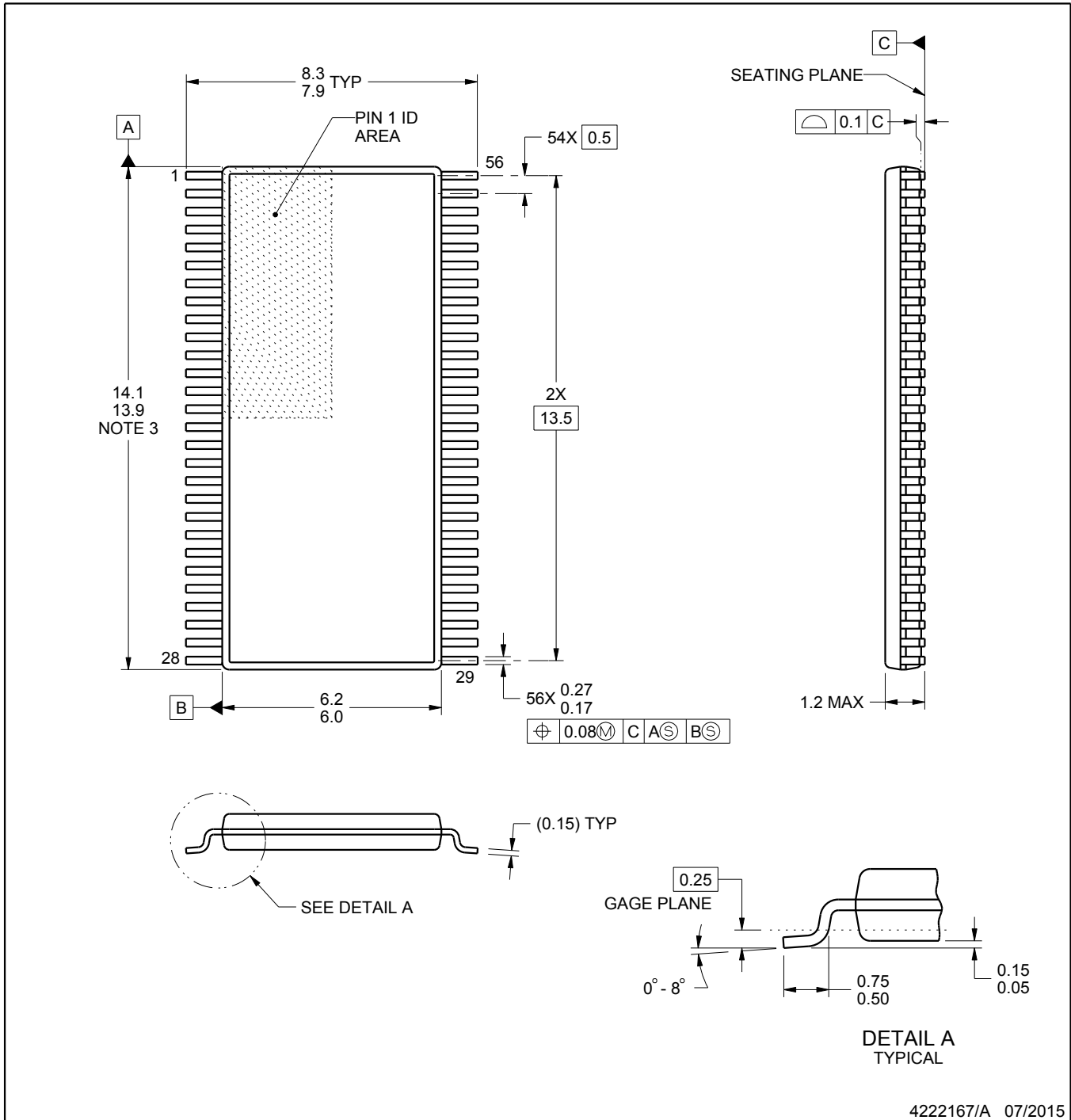
DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



4222167/A 07/2015

NOTES:

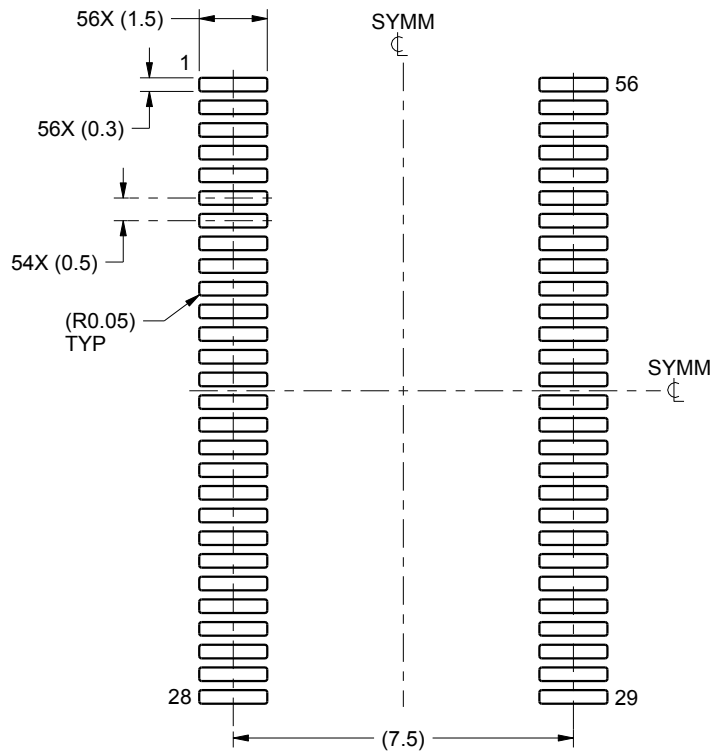
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

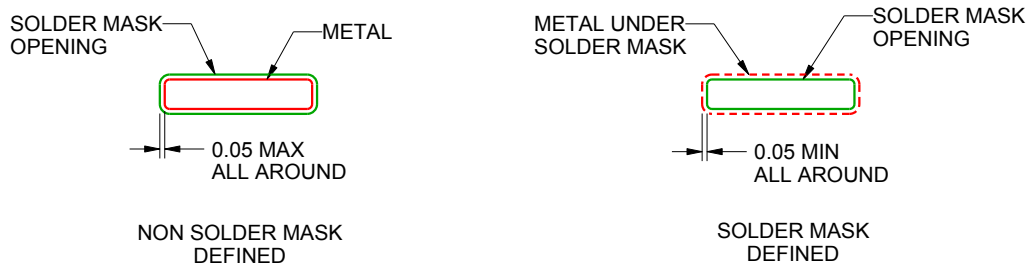
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

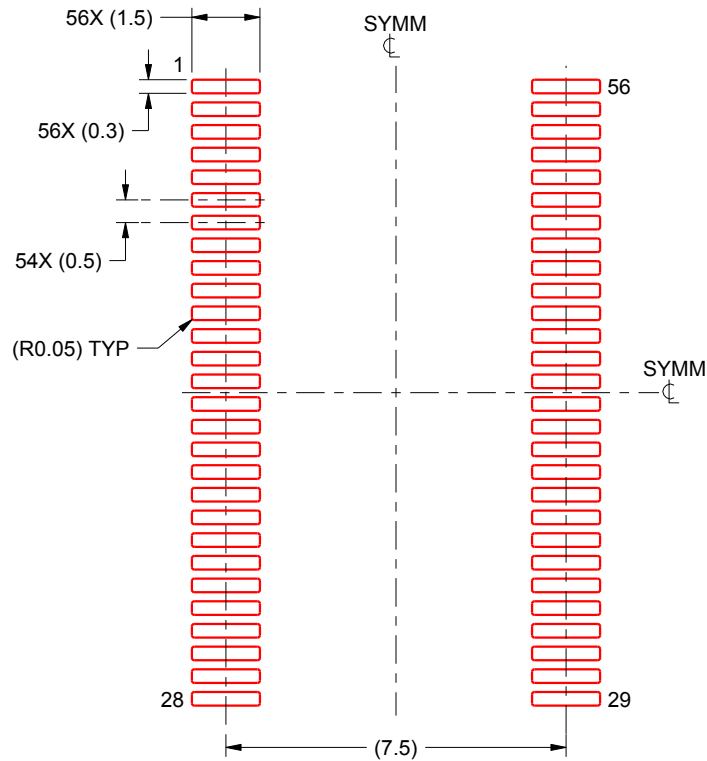
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated