



# TEA6420

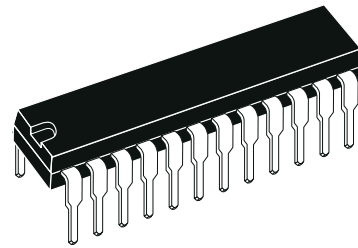
## BUS-CONTROLLED AUDIO MATRIX SWITCH

- 5 Stereo Inputs
- 4 Stereo Outputs
- Gain Control 0/2/4/6dB/Mute for each Output
- cascadable (2 different addresses)
- Serial Bus Controlled
- Very low Noise
- Very low Distorsion

### DESCRIPTION

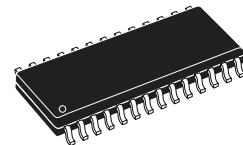
The TEA6420 switches 5 stereo audio inputs on 4 stereo outputs.

All the switching possibilities are changed through the I<sup>2</sup>C bus.



**SHRINK DIP 24  
(Plastic Package)**

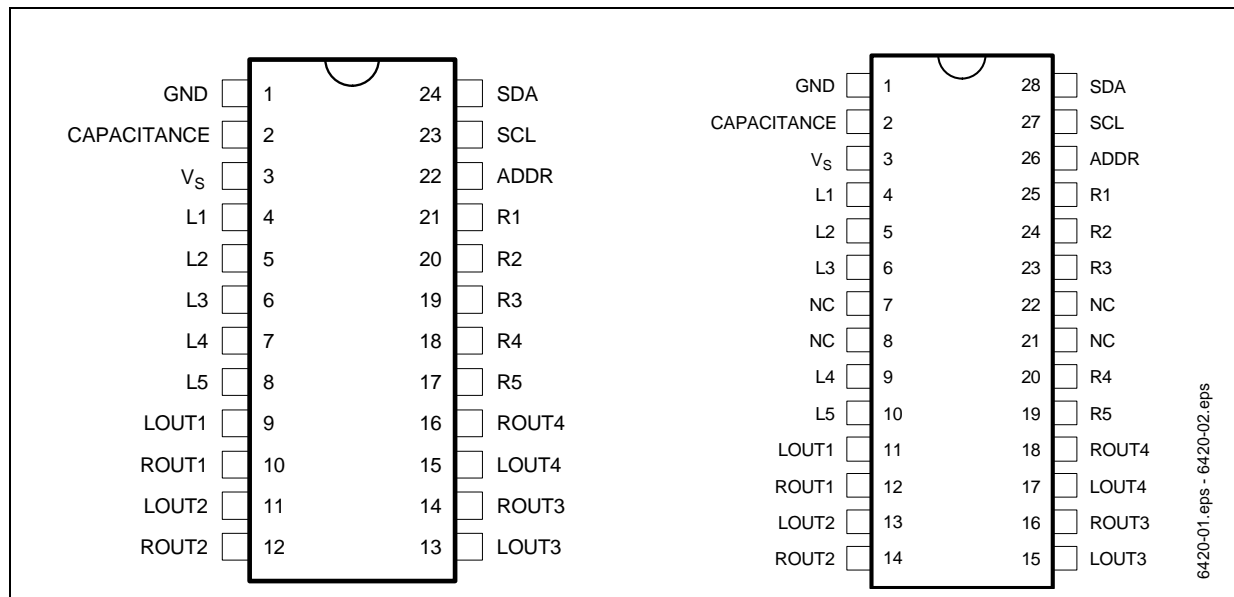
**ORDER CODE: TEA6420**



**SO28  
(Plastic Micropackage)**

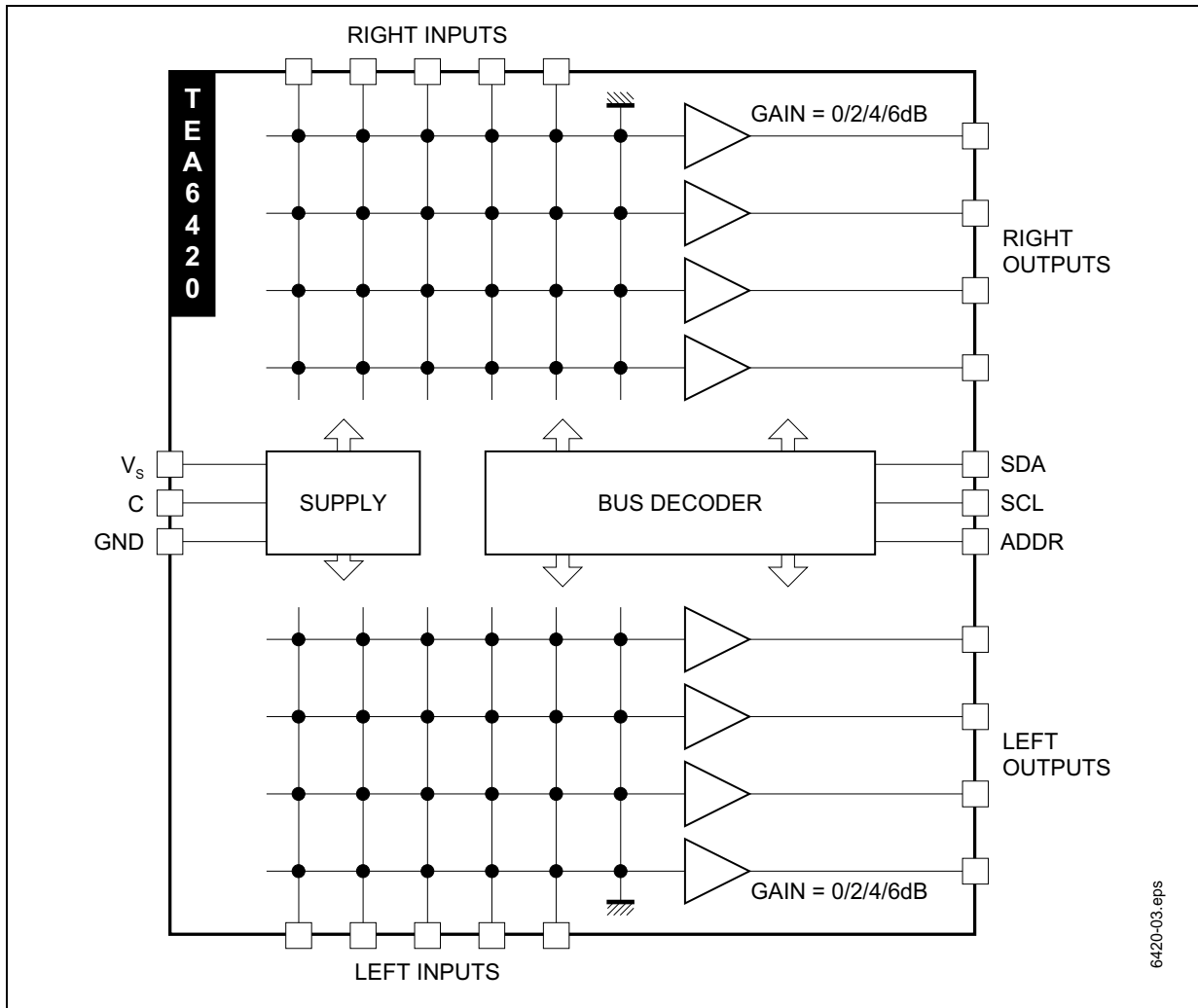
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**Figure 1. PIN CONNECTIONS**



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Figure 2. BLOCK DIAGRAM



6420-03.eps

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage (Pin 9)	12	V
$T_{OPER}$	Operating Ambient Temperature Range	0 to +70	°C
$T_{stg}$	Storage Temperature Range	-20 to +150	°C

**THERMAL DATA**

Symbol	Parameter+	Value	Unit
$R_{th(j-a)}$	Junction-Ambient Thermal Resistance	SDIP24 75 SO28 75	°C/W

**ELECTRICAL CHARACTERISTICS**

$T_A = 25^{\circ}\text{C}$ ,  $V_S = 10\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $R_G = 600\Omega$ ,  $f = 1\text{kHz}$  (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>SUPPLY</b>						
$V_S$	Supply Voltage		8	9	10.2	V
$I_S$	Supply Current			5	8	mA
SVR	Ripple Rejection	$V_{IN} = 500\text{mV}_{RMS}$ , BW = 20 - 20kHz	70	80		dB
<b>MATRIX</b>						
$V_{IN}$	Input DC Level		4.5	5	5.5	V
$R_I$	Input Resistance		30	50	100	k $\Omega$
$C_S$	Channel Separation	$V_{IN} = 2V_{RMS}$ Gain = 0dB $f = 1\text{kHz}$ Gain = 6dB	80 70	90 82		dB dB
<b>OUTPUT BUFFER</b>						
$V_{OUT}$	Output DC Level		4.5	5	5.5	V
$R_{OUT}$	Output Resistance			70	200	W
$e_{NI}$	Input Noise	BW = 20 - 20kHz, flat		3		$\mu\text{V}$
S/N	Signal to Noise Ratio	$V_{IN} = V_{OUT} = 1V_{RMS}$		110		dB
$G_{min}$	Min. Gain		-1	0	+1	dB
$G_{max}$	Max. Gain		5	6	7	dB
d	Distortion	$V_{IN} = V_{OUT} = 1V_{RMS}$		0.01	0.05	%
$V_{CL}$	Clipping Level	$d = 0.3\%$	2	2.5		$V_{RMS}$
$R_L$	Output Load Resistance		2			k $\Omega$
<b>BUS INPUT</b>						
$V_{IL}$	Input Low Voltage				1.5	V
$V_{IH}$	Input High Voltage		3			V
$I_I$	Input Current		-10		10	$\mu\text{A}$
$V_O$	Output Voltage	$I_O = 3\text{mA}$ ; SDA Acknowledge pin			0.4	V
$R_{pu}$	ADDR Pullup Resistor	Note	40	50		k $\Omega$

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## SOFTWARE SPECIFICATION

### 1. Chip address

Address	HEX	ADDR
1001 1000	98	0
1001 1010	9A	1

### 2. Data bytes

Output select								
X	0 0 1 1	0 1 0 1	G <sub>1</sub>	G <sub>0</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	Output 1 Output 2 Output 3 Output 4
Input select								
X	Q <sub>1</sub>	Q <sub>0</sub>	G <sub>1</sub>	G <sub>0</sub>	0 0 0 0 1 1	0 0 1 1 0 0	0 1 0 1 0 1	Input 1 Input 2 Input 3 Input 4 Input 5 Mute
Gain select								
X	Q <sub>1</sub>	Q <sub>0</sub>	0 0 1 1	0 1 0 1	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	Gain = 6 dB Gain = 4 dB Gain = 2 dB Gain = 0 dB

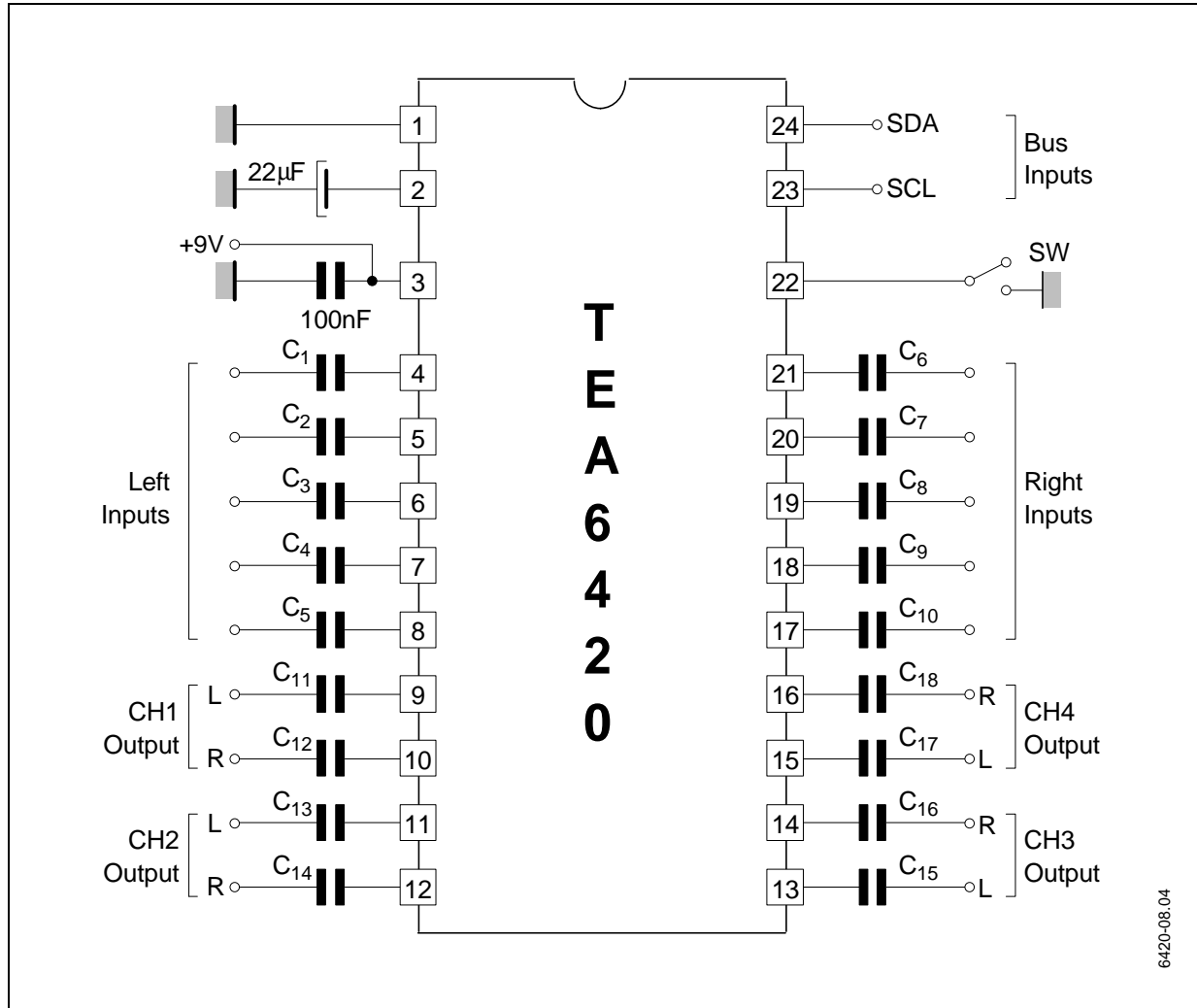
X = don't care - MSB is transmitted first

**Example :** X1001100 connects output 3 with input 5 at a gain of 4dB

The following are selected after power-on reset : input 5 selected for all outputs ; gain = 0dB.

## TYPICAL APPLICATION

Figure 3.

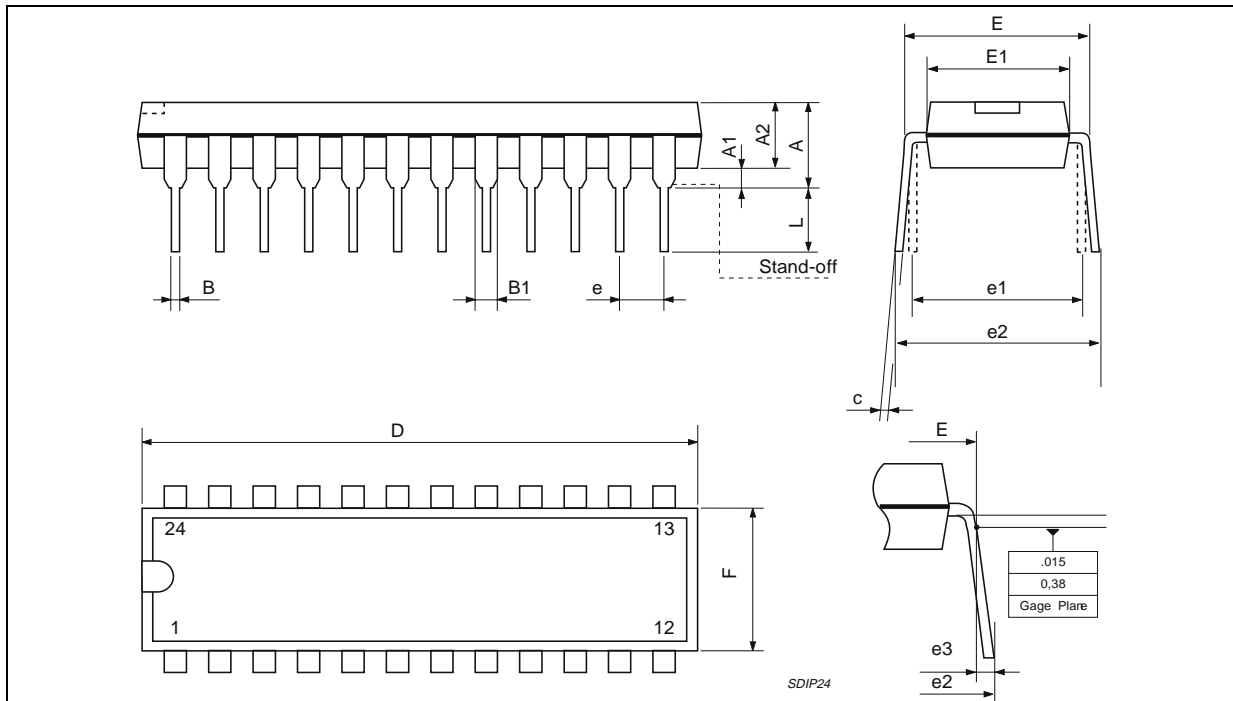


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**PACKAGE MECHANICAL DATA**

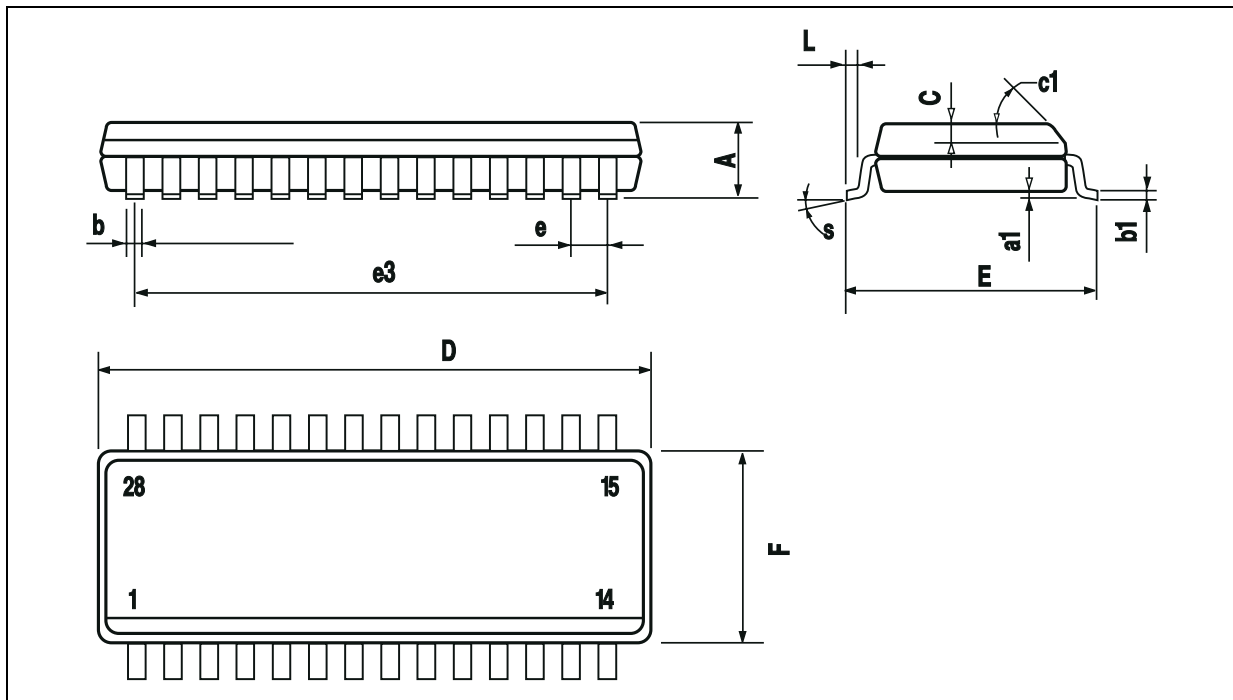
24 PINS - PLASTIC DIP

**Figure 4. 24-Pin Package**



28 PINS - PLASTIC SO

**Figure 5. 28-Pin Package**



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