AMIS-39100

Octal High Side Driver with Protection

ON Semiconductor®

http://onsemi.com

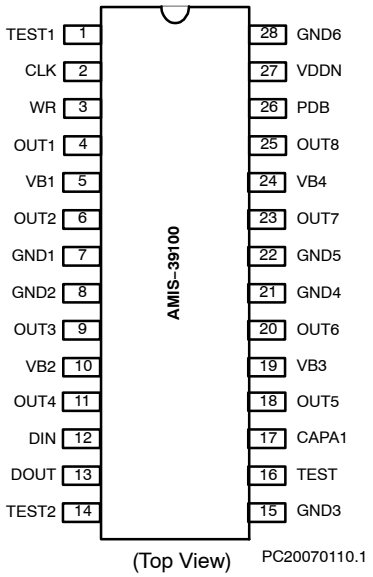
General Description

The AMIS−39100 is a general purpose IC with eight integrated high side (HS) output drivers. The device is designed to control the power of virtually any type of load in a 12 V automotive environment, such as transistor gates, relays, LEDs etc.

Each of the output drivers of the AMIS−39100 is able to drive up to 275 mA continuously when connected to an inductive load of 300 mH. Even higher driver output currents can be obtained as long as the total current of the device is limited. The integrated charge−pump of the AMIS−39100, which uses only one low cost external capacitor, avoids thermal runaways even if the battery voltage is low. The HS drivers withstand short to ground (even when AMIS−39100 has lost its ground connection), short to the battery and has overcurrent limitation. In case of a potential hazardous situation, the drivers are switched off and the diagnostic state of the HS drivers can be read out via serial peripheral interface (SPI). In case of a short to ground, the output driver is deactivated after a de−bounce time.

The AMIS−39100 can be connected to a 3.3 V or 5 V microcontroller by means of a SPI interface. This SPI interface is used to control each of the output drivers individually (on or off) and to read the status of each individual output driver (read−back of possible error conditions). This allows the detection of error situations for each driver individually. Furthermore, the SPI interface can be used to read−back the status of the built−in thermal shutdown protection. The AMIS−39100 has a low−power mode and excellent handling and system ESD characteristics.

PIN ASSIGNMENT



(Top View) PC20070110.1

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

Features

- Eight HS drivers
- Up to 830 mA Continuous Current Per Driver Pair (Resistive Load)
- Charge Pump with One External Capacitor
- Serial peripheral interface (SPI)
- Short−Circuit Protection
- Diagnostic Features
- Powerdown Mode
- Internal Thermal Shutdown
- 3.3 V and 5 V Microcontroller Compliant
- Excellent System ESD
- Automotive Compliant
- SOIC 28 Package with Low R_{thja}
- This is a Pb−Free Device*

Typical Applications

- Automotive Dashboard
- Automotive Load Management
- Actuator Control
- LED Driver Applications
- Relays and Solenoids
- Industrial Process Control

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

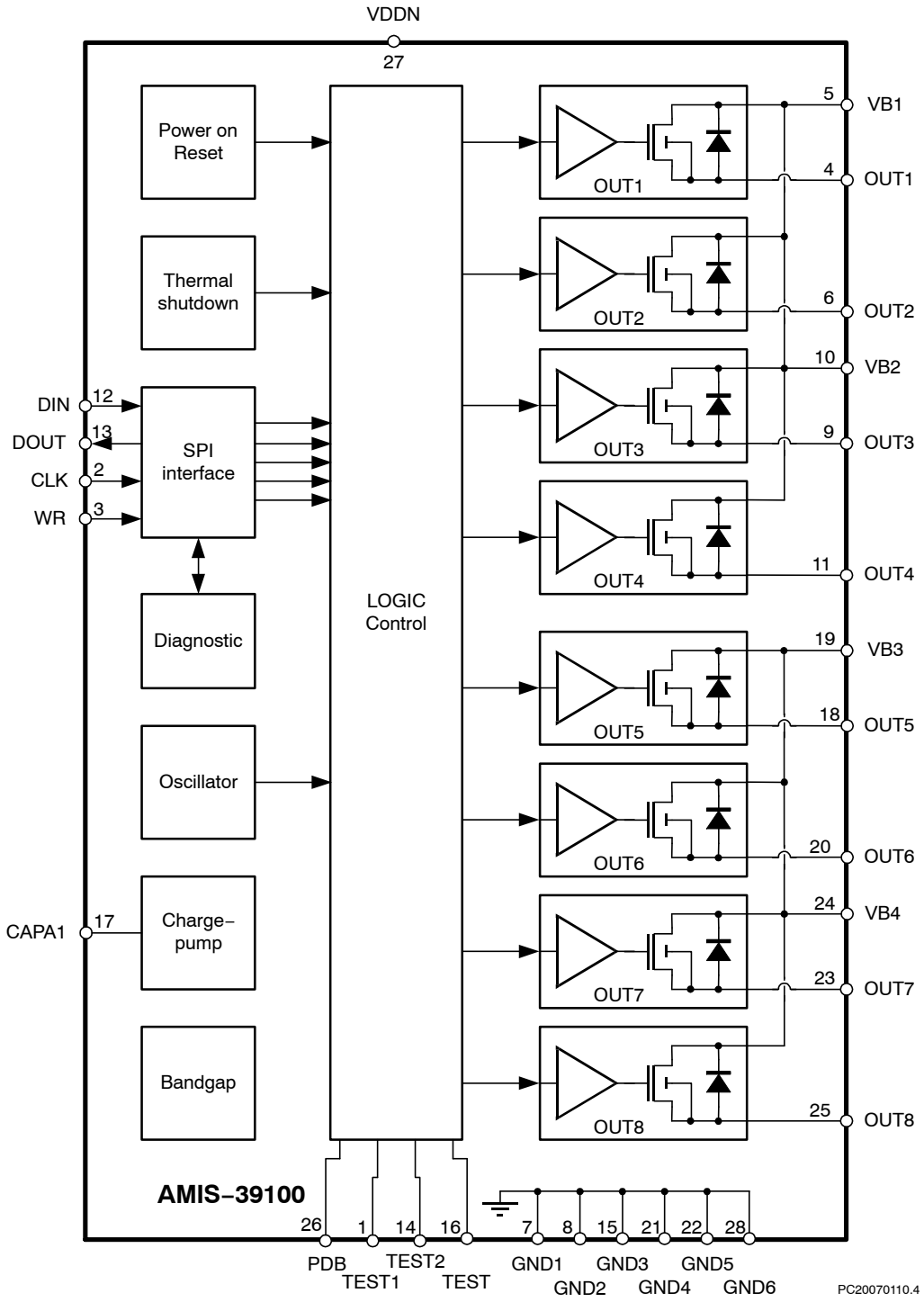


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin	Name	Description
1	TEST1	Connect to GND
2	CLK	Schmitt Trigger SPI CLK Input
3	WR	Schmitt Trigger SPI Write Enable Input
4	OUT1	HS Driver Output
5	VB1	Battery Supply
6	OUT2	HS Driver Output
7	GND1	Power Ground and Thermal Dissipation Path Junction−to−PCB
8	GND2	Power Ground and Thermal Dissipation Path Junction−to−PCB
9	OUT3	HS Driver Output
10	VB2	Battery Supply
11	OUT4	HS Driver Output
12	DIN	SPI Input Pin (Schmitt trigger or CMOS inverter)
13	DOUT	Digital Three State Output for SPI
14	TEST2	Connect to GND
15	GND3	Power Ground and Thermal Dissipation Path Junction−to−PCB
16	TEST	Connect to GND
17	CAPA1	Charge Pump Capacitor Pin
18	OUT5	HS Driver Output
19	VB3	Battery Supply
20	OUT6	HS Driver Output
21	GND4	Power Ground and Thermal Dissipation Path Junction−to−PCB
22	GND5	Power Ground and Thermal Dissipation Path Junction−to−PCB
23	OUT7	HS Driver Output
24	VB4	Battery Supply
25	OUT8	HS Driver Output
26	PDB	Schmitt Trigger Powerdown Input
27	VDDN	Digital Supply
28	GND6	Power Ground and Thermal Dissipation Path Junction−to−PCB

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Unit
VDDN	Power Supply Voltage	GND − 0.3	6	V
VB	DC Battery Supply on Pins VB1 to VB4 Load Dump, Pulse 5b 400 ms	GND − 0.3	35	V
Iout_ON	Maximum Output Current OUTx Pins (Note 1) The HS Driver is Switched On	−3000	350	mA
Iout_OFF	Maximum Output Current OUTx Pins (Note 1) The HS Driver is Switched Off	−350	350	mA
I_OUT_VB	Maximum Output Current VB1, 2, 3, 4 Pins	−700	3750	mA
Vcapa1	DC Voltage on Pins capa1	0	VB + 16.5	V
Vdig_in	Voltage on Digital Inputs CLK, PDB, WR, DIN	−0.3	V_{DDN} + 0.3	V
V_{ESD}	Pins that Connect the Application (Pins VB1 − 8 and Out1 − 8) (Note 2) All Other Pins (Note 2)	−4 −2	+4 +2	kV
V_{ESD}	ESD According Charged Device Model (Note 3)	−750	+750	V
T_J	Junction Temperature (T < 100 hours)	−40	175	°C
Tmr	Ambient Temperature Under Bias	−40	105	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The power dissipation of the chip must be limited not to exceed the maximum junction temperature Tj.
2. According to Human Body Model (HBM) standard MIL−STD−883 method 3015.7
3. According to norm EOS/ESD−STM5.3.1−1999 robotic mode

Table 3. THERMAL CHARACTERISTICS OF THE PACKAGE

Symbol	Description	Conditions	Value	Unit
$R_{th(vj-a)}$	Thermal Resistance from Junction−to−Ambient in Power SOIC 28 Package	In Free Air	145	K/W

Table 4. THERMAL CHARACTERISTICS OF THE AMIS−39100 ON A PCB

PCB Design	Conductivity Top and Bottom Layer	R_{thja} (Note 4)	Unit
Two Layer (35 μm)	Copper Planes According Figure 3 to +25% Popper for the Remaining Areas	24	K/W
Two Layer (35 μm)	Copper Planes According to Figure 3 0% Popper for the Remaining Areas	53	K/W
Four Layer JEDEC: EIA/JESD51−7	25% Copper Coverage	25	K/W
One Layer JEDEC: EIA/JESD51−3	25% Copper Coverage	46	K/W

4. These values are informative only.
   R_{thja} = Thermal Resistance from Junction−to−Ambient

Table 5. OPERATING RANGES

Symbol	Description	Min	Max	Unit
V_{DDN}	Digital Power Supply Voltage	3.1	5.5	V
Vdig_in	Voltage on Digital Inputs CLK, PDB, WR, DIN	−0.3	V_{DDN}	V
VB (Note 5)	DC Battery Supply on Pins VB1 to VB4	3.5	16	V
T_A	Ambient Temperature	−40	105	°C

5. The power dissipation of the chip must be limited not to exceed maximum junction temperature T_J of 130°C.

TYPICAL APPLICATION DIAGRAM

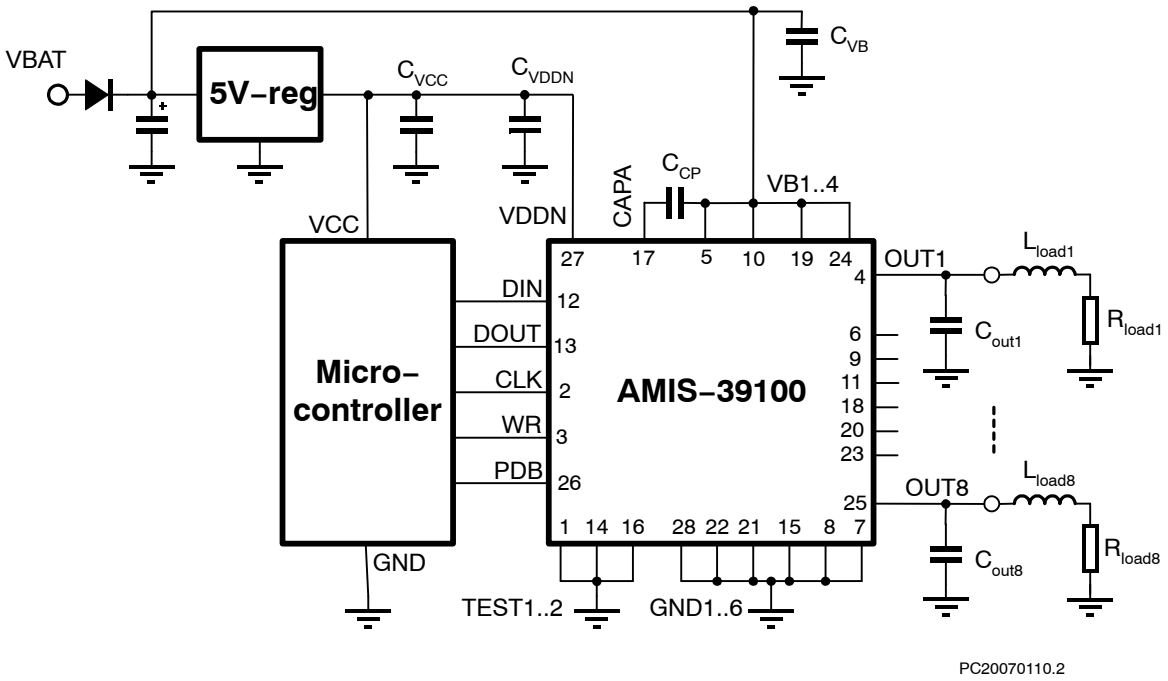


Figure 2. Typical Application Diagram

External Components

It is important to properly decouple the power supplies of the chip with external capacitors that have good high frequency properties.

The VB1, VB2, VB3, and VB4 pins are shorted on the PCB level. Also GND1, GND2, GND3, GND4, GND5, GND6, TEST, TEST1, and TEST2 are shorted on the PCB level.

Table 6. EXTERNAL COMPONENTS

Component	Function	Min	Value	Max	Tol [%]	Unit
C_{VB}	Decoupling Capacitor; X7R	100			±20	nF
C_{charge_pump}	Charge Pump Capacitor (Note 6)	0.47		47		nF
C_{out} (Note 7)	EMC Capacitor on Connector	1				nF
C_{out} (Note 7)	Decoupling Capacitors on OUT 1 to 8; 50 V	22			±20	nF
C_{VDD}	Decoupling Capacitors; 50 V	22			±20	nF
R_{Load}	Load Resistance		65		±10	Ω
L_{Load}	Load Inductance at Maximum Current		300	350		mH

6. The capacitor must be placed close to the AMIS−39100 pins on the PCB.
7. Both capacitors are optional and depend on the final application and board layout.

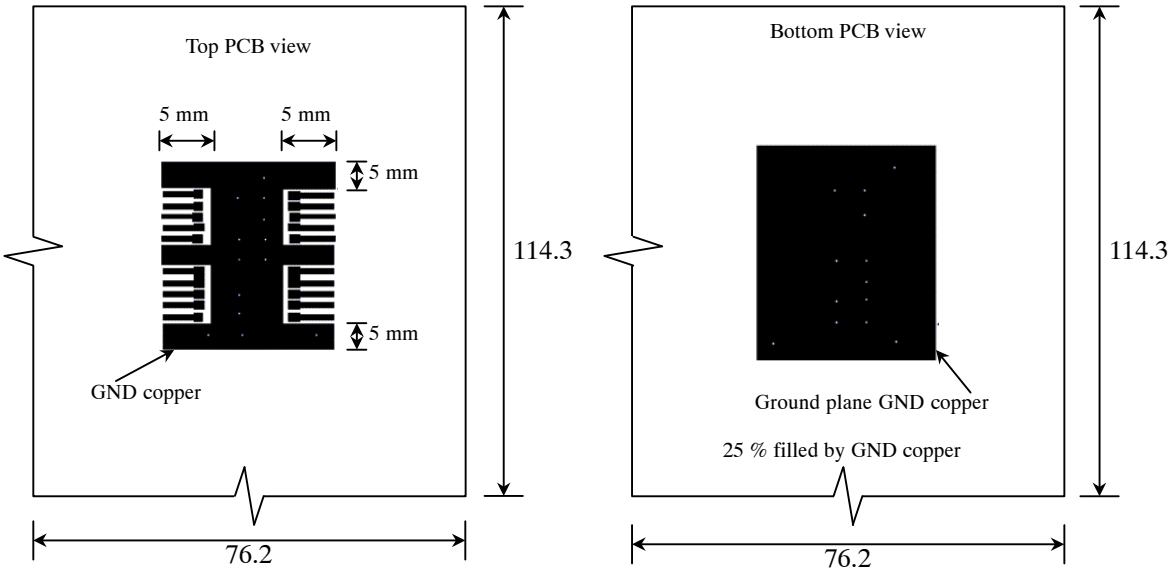


Figure 3. Layout Recommendation for Thermal Characteristics

ELECTRICAL AND ENVIRONMENTAL RATINGS

ELECTRICAL PARAMETERS

Operation outside the operating ranges for extended periods may affect device reliability. Total cumulative dwell time above the maximum operating rating for the power supply or temperature must be less than 100 hours.

The parameters below are independent from load type (see Section “Load Specific Parameters”).

Table 7. ELECTRICAL CHARACTERISTICS

Symbol	Description	Min	Max	Unit
I_VB_norm (Note 8)	Consumption on VB Without Load Currents In Normal Mode of Operation PDB = High		3.5	mA
I_PDB_3.3 (Notes 8 and 9)	Sum of VB and V_{DDN} Consumption in Powerdown Mode of Operation PDB = Low, V_{DDN} 3.3 V, VB = 12 V, 23°C Ambient CLK and WR are at V_{DDN} Voltage		25	μA
I_PDB_5 (Notes 8 and 9)	Sum of VB and V_{DDN} Consumption in Powerdown Mode of Operation PDB = low, V_{DDN} 5 V, VB = 24 V, 23°C Ambient CLK and WR are at V_{DDN} Voltage		40	μA
I_PDB_MAX_VB	VB Consumption in Powerdown Mode of Operation PDB = Low, VB = 16 V		10	μA
I_VDDN_norm (Note 8)	Consumption on V_{DDN} In Normal Mode of Operation PDB = High CLK is 500 kHz, V_{DDN} = 5.5 V, VB = 16 V		1.6	mA
R_on_1 − 8	On Resistance of the Output Drivers 1 through 8 Vb= 16 V (Normal Battery Conditions and T_A = 25°C) Vb = 4.6 V (Worst Case Battery Condition and T_A = 25°C)		 1 3	Ω
I_OUT_lim_x (Note 8)	Internal Overcurrent Limitation of HS Driver Outputs	0.65	2	A
T_shortGND_HSdoff	The Time from Short of HS Driver OUTx Pin to GND and the Driver Deactivation; Driver is Off; Detection Works from VB Minimum of 7 V; VDDN Minimum is 3 V	5.4		μs
TSD_H (Note 8)	High TSD Threshold for Junction Temperature (Temperature Rising)	130	170	°C
TSD_HYST	TSD Hysteresis for Junction Temperature	9	18	°C

8. The power dissipation of the chip must be limited not to exceed maximum junction temperature T_J.
9. The cumulative operation time mentioned above may cause permanent device failure.

LOAD SPECIFIC PARAMETERS

HS driver parameters for specific loads are specified in following categories:

A. Parameters for inductive loads till 350 mH and T_A till 105°C
B. Parameters for inductive loads till 300 mH and T_A till 105°C
C. Parameters for resistive loads and T_A till 85°C

Table 8. LOAD SPECIFIC CHARACTERISTICS

Symbol	Description	Min	Max	Unit
A. INDUCTIVE LOAD TILL 350 mH AND T_A TILL 105°C				
I_OUT_ON_max	Maximum output per HS driver, all eight drivers might be active simultaneously		240	mA
B. INDUCTIVE LOAD TILL 300 mH AND T_A TILL 105°C				
I_OUT_ON_max	Maximum output per HS driver, all eight drivers might be active simultaneously		275	mA
C. RESISTIVE LOAD AND T_A TILL 85°C				
I_OUT_ON_max	Maximum output per HS driver, all eight drivers might be active simultaneously		350	mA
	Maximum output per one HS driver, only one can be active		650	mA
	Maximum output per HS driver, only two HS drivers from a different pair can be active simultaneously		500	mA
	Maximum output per one HS driver pair		830	mA

10. The parameters above are not tested in production but are guaranteed by design. The overall current capability limitations need to be respected at all times.

The maximum current specified in cannot always be obtained. The practically obtainable maximum drive current heavily depends on the thermal design of the application PCB (see Section “Thermal Characteristics”).

The available power in the package is: (TSD_H − T_A) / R_{thja}

With TSD_H = 130°C and R_{thja} according to Table 4.

CHARGE PUMP

The HS drivers use floating NDMOS transistors as power devices**.** To provide the gate voltages for the NDMOS of the HS drivers, a charge pump is integrated. The storage capacitor is an external one. The charge pump oscillator has typical frequency of 4 MHz.

DIAGNOSTICS

Short−Circuit Diagnostics

The diagnostic circuit in the AMIS−39100 monitors the actual output status at the pins of the device and stores the result in the diagnostic register which is then latched in the output register at the rising edge of the WR−pin. Each driver has its corresponding diagnostic bit DIAG_x. By comparing the actual output status (DIAG_x) with the requested driver status (CMD_x) you can diagnose the correct operation of the application according to .

Thermal Shutdown (TSD) Diagnostic

In case of TSD activation, all bits DIAG 1 to DIAG 8 in the SPI output register are set into the fault state and all drivers will be switched off (see).

The TSD error condition is active until it is reset by the next correct communication on SPI interface (i.e. number of clock pulses during WR=0 is divisible by 8), provided that the device has cooled down under the TSD trip point.

Table 9. OUT DIAGNOSTICS

Requested driver status	CMD_x	Actual output status	DIAG_x	Diagnosis
On	1	High	1	Normal State
On	1	Low	0	Short−to−Ground or TSD (Note 12)
Off	0	High	1	Short−to−VB or Missing Load (Note 11) or TSD (Note 12)
Off	0	Low	0	Normal State (Note 11)

11. The correct diagnostic information is available after T_diagnostic_OFF time.
12. All 8 diagnostic bits DIAG_x must be in the fault condition to conclude a TSD diagnostic.

Ground Loss

Due to its design, the AMIS−39100 is protected for withstanding module ground loss and driver output shorted to ground at the same time.

Table 10. POWER LOSS

VDDN	VB	Possible Case	Action
0	0	System stopped	Nothing
0	1	Start case or sleeping mode with missing V_{DDN}	Eight switches in the off−state Power down consumption on VB
1	0	Missing VB supply VDDN normally present	Eight switches in the off−state Normal consumption on VDDN
1	1	System functional	Nominal functionality

SPI INTERFACE

The serial peripheral interface (SPI) is used to allow an external microcontroller (MCU) to communicate with the device. The AMIS−39100 acts always as a slave and it can't initiate any transmission.

SPI Transfer Format and Pin Signals

The SPI block diagram and timing characteristics are shown in and Figures 5 and 6.

During an SPI transfer, data is simultaneously sent to and received from the device. A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DIN and DOUT). DOUT signal is the output from the AMIS−39100 to the external MCU and DIN signal is the input from the MCU to the AMIS−39100. The WR−pin selects the AMIS−39100 for communication and can also be used as a chip select (CS) in a multiple−slave system. The WR−pin is active low. If AMIS−39100 is not selected, DOUT is in high impedance state and it does not interfere with SPI bus activities. Since AMIS−39100 always shifts data out on the rising edge and samples the input data also on the rising edge of the CLK signal, the MCU SPI port must be configured to match this operation. SPI clock idles high between the transferred bytes.

The diagram in Figure 6 represents the SPI timing diagram for 8−bit communication.

Communication starts with a falling edge on the WR−pin which latches the status of the diagnostic register into the SPI output register. Subsequently, the CMD_x bits – representing the newly requested driver status – are shifted into the input register and simultaneously, the DIAG_x bits – representing the actual output status – are shifted out. The bits are shifted with x = 1 first and ending with x = 8.

At the rising edge of the WR−pin, the data in the input register is latched into the command register and all drivers are simultaneously switching to the newly requested status. SPI communication is ended.

In case the SPI master does only support 16−bit communication, then the master must first send 8 clock pulses with dummy DIN data and ignoring the DOUT data. For the next 8 clock pulses the above description can be applied.

The required timing for serial to peripheral interface is shown in Table 11.

Table 11. DIGITAL CHARACTERISTICS

Symbol	Description	Min	Max	Unit
T_CLK	Maximum applied clock frequency on CLK input		500	kHz
T_DATA_ready	Time between falling edge on WR and first bit of data ready on DOUT output (driver going from HZ state to output of first diagnostic bit)		2	μs
T_CLK_first	First clock edge from falling edge on WR	3		μs
T_setup (Note 13)	Setup time on DIN	20		ns
T_hold (Note 13)	Hold time on DIN	20		ns
T_DATA_next	Time between rising edge on CLK and next bit ready on DOUT (capa on DOUT is 30 pF max.)		100	ns
T_SPI_END	Time between last CLK edge and WR rising edge	1		μs
T_risefall	Rise and fall time of all applied signals (maximum loading capacitance is 30 pF)	5	20	ns
T_WR	Time between two rising edge on WR (repetition of the same command)	300		μs

13. Guaranteed by design.

Normal Mode Verification:

- The *command* is the set of eight bits loaded via SPI, which drives the eight HS drivers on or off.
- The *command* is activated with rising edge on WR pin.

Table 12. DIGITAL CHARACTERISTICS

Symbol	Description	Min	Max	Unit
T_command_L_max (Note 14)	Minimum time between two opposite commands for inductive loads and maximum HS driver current of 275 mA	1		s
T_command_R (Note 14)	Minimum time between two opposite commands for resistive loads and maximum HS driver current of 350 mA	2		ms
T_PDB_recov	The time between the rising edge on the PDB input and 90 percent of VB−1V on all HS driver outputs. (all drivers are activated, pure resistive load 35 mA on all outputs)		1	ms

14. Guaranteed by design.

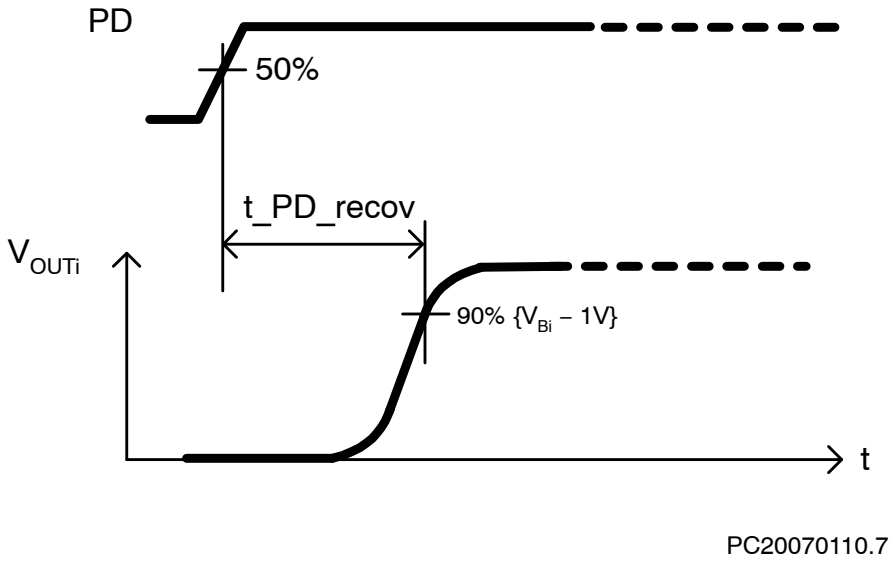


Figure 4. Timing for Powerdown Recovery

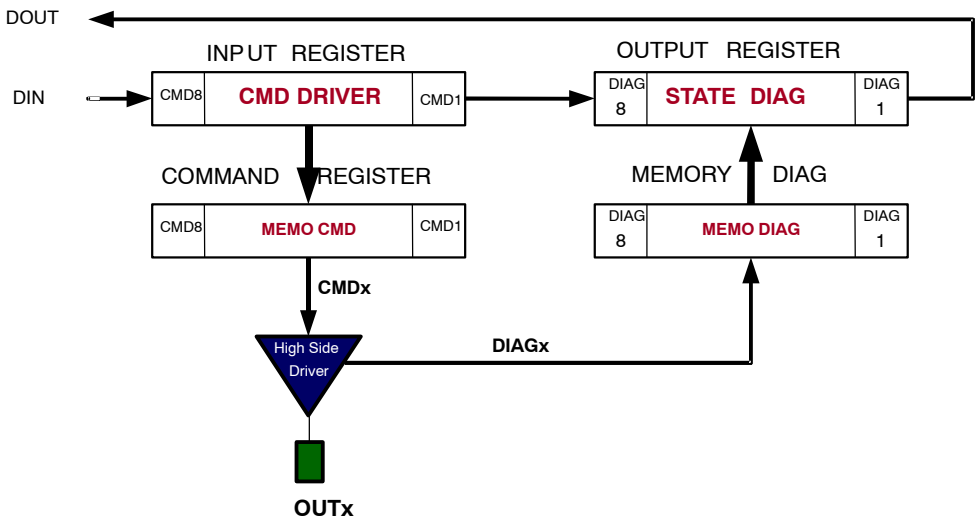


Figure 5. SPI Block Diagram

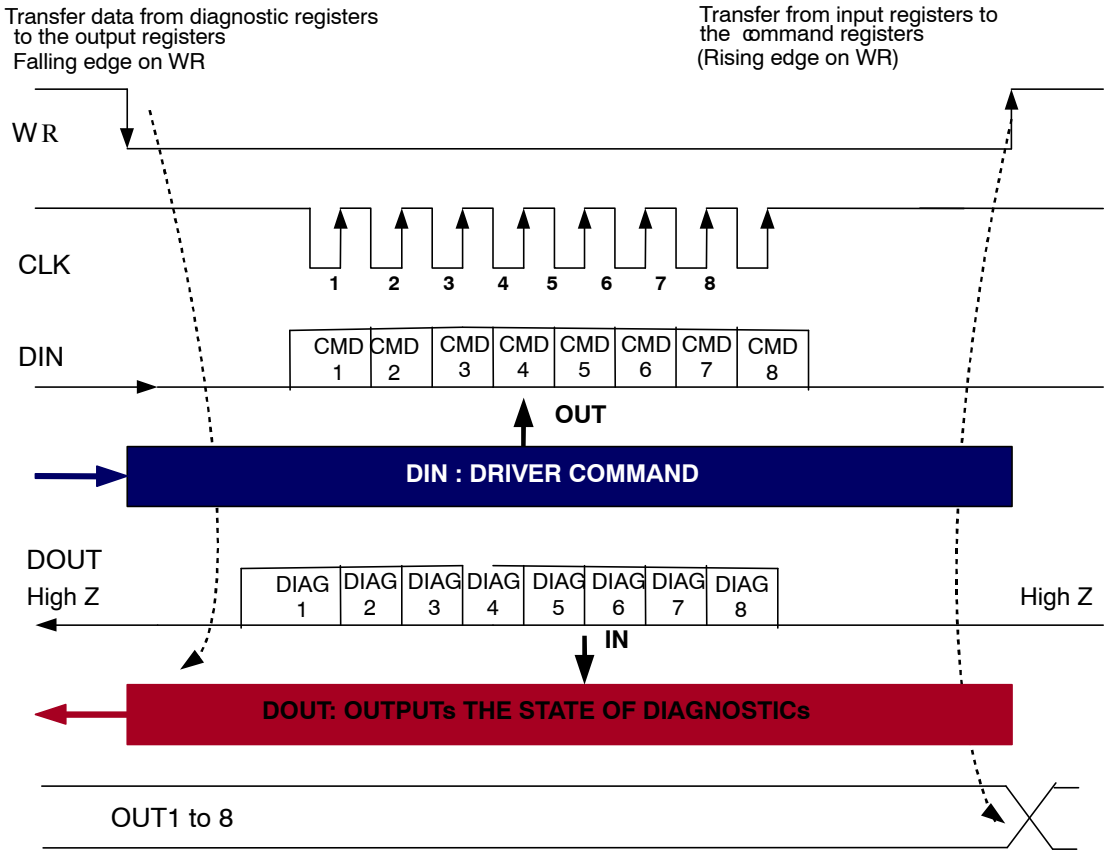


Figure 6. Timing Diagram

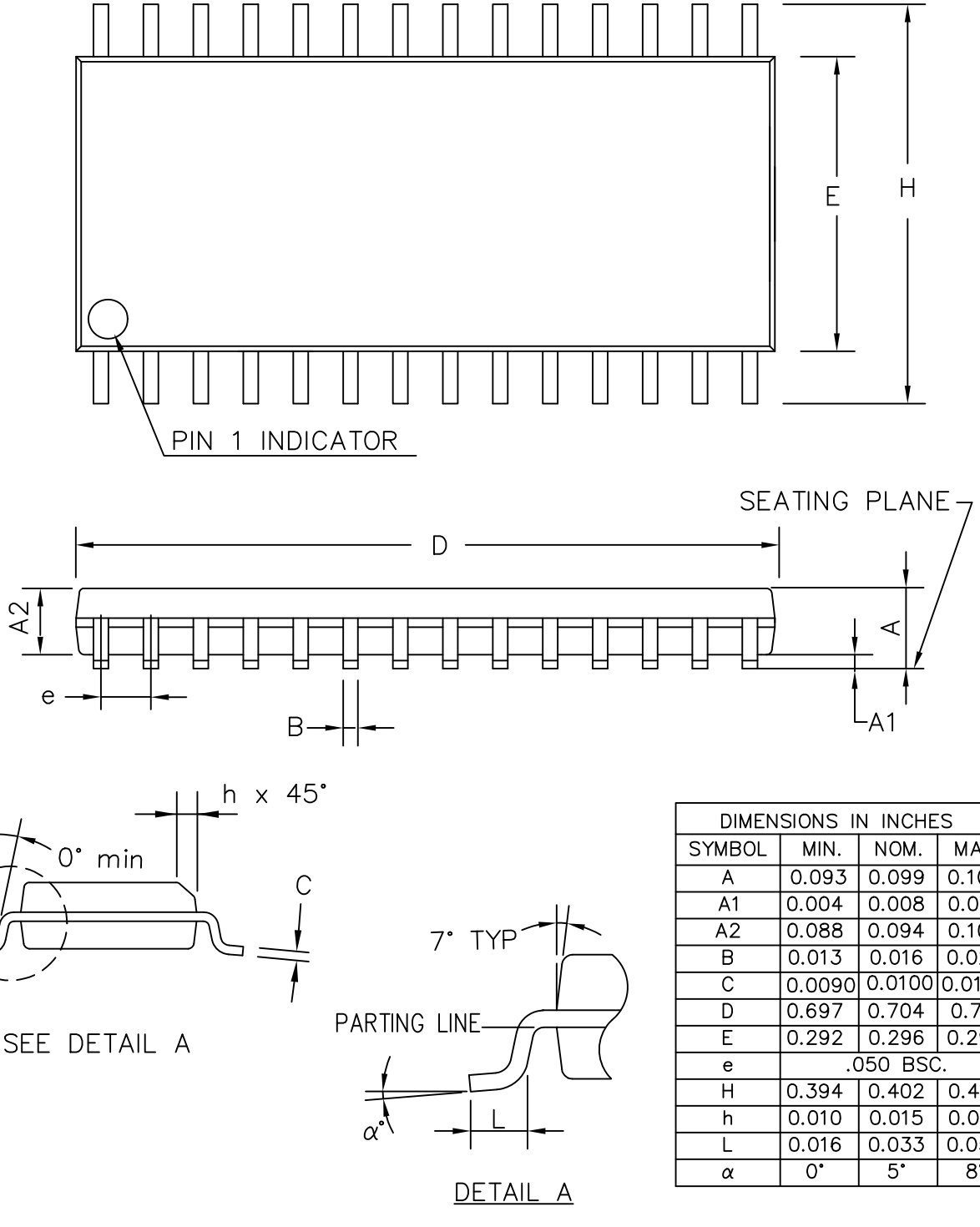
DEVICE ORDERING INFORMATION

Part Number	Temperature Range	Package Type	Shipping†
AMIS39100PNPB3G	−40°C to 105°C	SOIC 28 W (Pb−Free)	26 Units / Rail
AMIS39100PNPB3RG	−40°C to 105°C	SOIC 28 W (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOIC 28 W
CASE 751AR−01
ISSUE O



DIMENSIONS IN INCHES			
SYMBOL	MIN.	NOM.	MAX.
A	0.093	0.099	0.104
A1	0.004	0.008	0.012
A2	0.088	0.094	0.100
B	0.013	0.016	0.020
C	0.0090	0.0100	0.0125
D	0.697	0.704	0.711
E	0.292	0.296	0.299
e	.050 BSC.		
H	0.394	0.402	0.419
h	0.010	0.015	0.019
L	0.016	0.033	0.050
α	0°	5°	8°

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