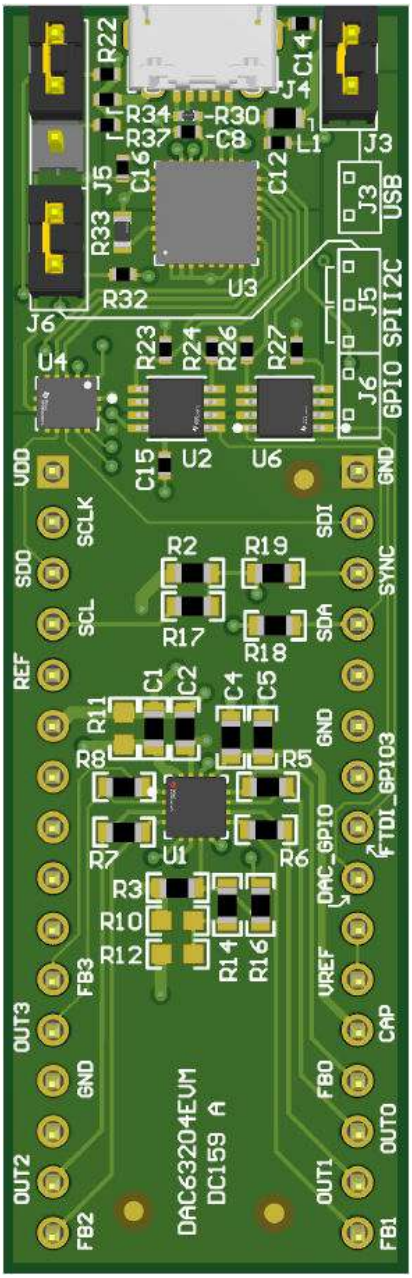
User's Guide

DAC63204EVM User's Guide

ABSTRACT



This user's guide describes the characteristics, operation, and use of the DAC63204EVM evaluation module (EVM). This EVM is designed to evaluate the performance of the DAC63204, DAC53204, and DAC43204 (DACx3204) commercial, buffered voltage output DACs in a variety of configurations. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the DAC63204EVM. This document includes a schematic, printed-circuit board (PCB) layouts, and a complete bill of materials.

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1 Overview

The DAC63204EVM is an easy-to-use platform to evaluate the functionality and performance of the DAC63204, DAC53204, and DAC43204 commercial devices.

The 12-bit DAC63204, 10-bit DAC53204, and 8-bit DAC43204 (DACx3204) are a pin-compatible family of quad-channel, buffered, voltage-output and current-output smart digital-to-analog converters (DACs). The DAC outputs are capable of both voltage and current output. The DACx3204 support Hi-Z power-down mode and Hi-Z output during power-off conditions. The DAC outputs provide a force-sense option for use as a programmable comparator and current sink. The multifunction GPIO, function generation, and nonvolatile memory (NVM) enable these smart DACs for use in applications and design reuse without the need for a processor (*processor-less* operation). These devices also automatically detect I^2C, SPI, and PMBus interfaces, and contain an internal reference.

1.1 Kit Contents

Table 1-1 details the contents of the EVM kit. Contact the nearest TI Product Information Center if any component is missing. Make sure to verify the latest versions of the related software at the Texas Instruments website, www.ti.com.

Table 1-1. Contents of DAC63204EVM Kit

Item	Quantity
DAC63204EVM evaluation board PCB	1
USB micro-B plug to USB-A plug cable	1

Table 1-2. Optional Components Not Included With Kit

Item	Quantity
BOOSTXL-DAC-PORT digital-to-analog converter (DAC) BoosterPack™ plug-in module	1
TM4C1294 Connected LaunchPad™ Evaluation Kit (EK-TM4C1294XL) (In this document, the LaunchPad Evaluation Kit is referred to as TI launchpad)	1

These optional components are available for purchase from the Texas Instruments website at www.ti.com.

1.2 Related Documentation from Texas Instruments

The following document provides information regarding Texas Instruments integrated circuits used in the assembly of the DAC63204EVM. This user's guide is available from the TI web site under literature number SLAU866. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI web site at www.ti.com, or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

Table 1-3. Related Documentation

Document	Literature Number
DAC63204 product page	SLASEX3
DAC53204 product page	
DAC43204 product page	

2 System Setup

2.1 Software Setup

This section provides the procedure for EVM software installation.

2.1.1 Operating Systems

The EVM software is compatible with the Windows™ 10 operating system.

2.1.2 Software Installation

Before software installation, make sure that the DAC63204EVM is not connected to the computer.

The software can be downloaded from the device product folders. After the software is downloaded, navigate to the download folder, and run the DAC63204EVM software installer executable.

When the DAC63204EVM software is launched, an installation dialog window opens and prompts the user to select an installation directory. If left unchanged, the software location defaults to *C:\Program Files (x86)\Texas Instruments\DAC63204EVM* as shown in Figure 2-1.

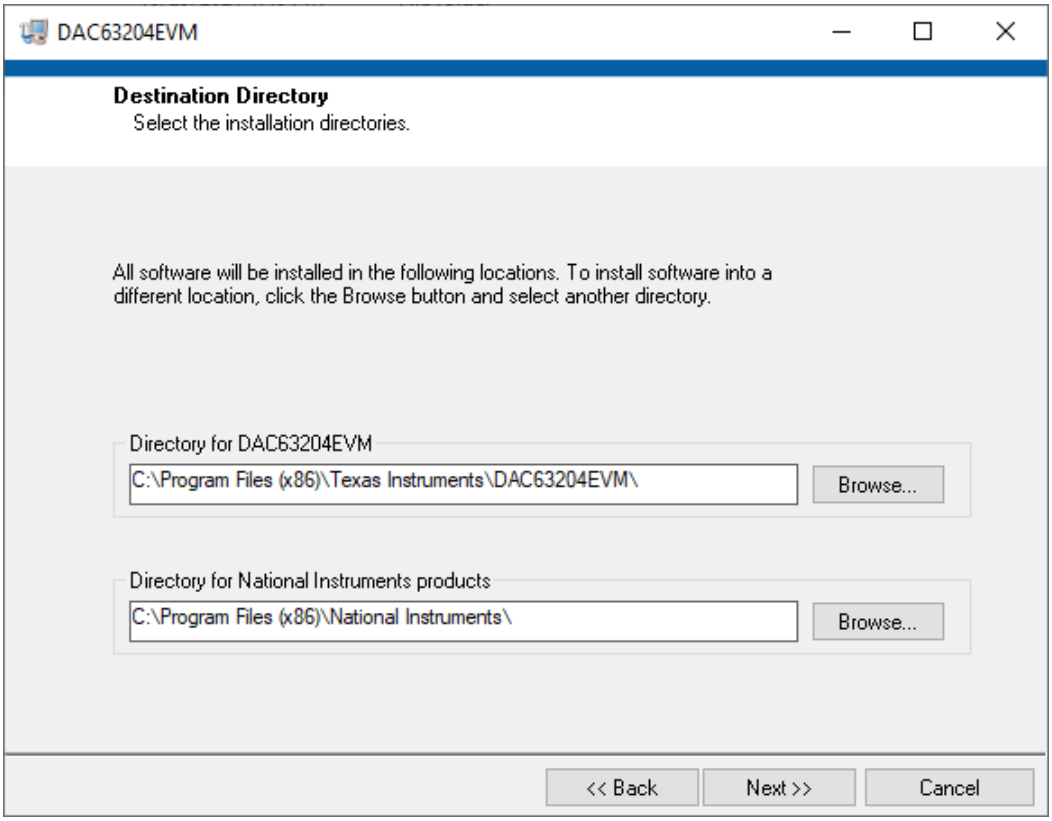

Figure 2-1. Software Installation Path

The software installation also installs the FTDI USB drivers, and automatically copies the required LabVIEW™ software files and drivers to the local machine. The FTDI USB drivers install in a second executable, shown in Figure 2-2, that is automatically launched after the DAC63204EVM software installation is complete.

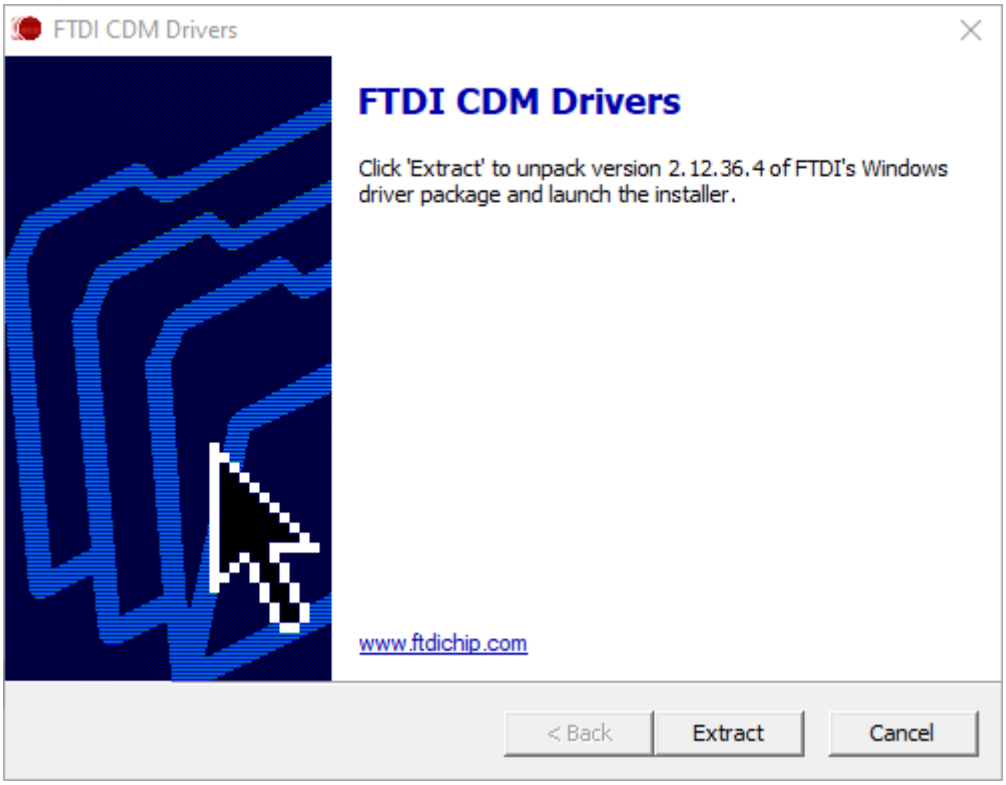

Figure 2-2. FTDI USB Drivers

2.2 Hardware Setup

This section describes the overall system setup for the EVM. A computer runs the software that provides an interface to the DAC63204EVM through the onboard controller.

The USB connection generates 5 V of power for use as the DAC supply voltage (VDD). The onboard controller generates 3.3 V of power for the input/output (IO) signals generated by the controller. These IO signals are level translated to the VDD voltage of the DAC. Figure 2-3 displays the system hardware setup.

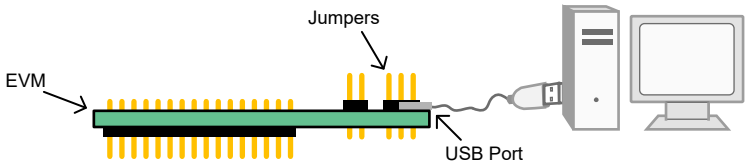

Figure 2-3. Hardware Setup

2.2.1 Electrostatic Discharge Caution

CAUTION

Many of the components on the DAC63204EVM are susceptible to damage by electrostatic discharge (ESD). Observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

2.2.2 Power Configurations and Jumper Settings

The DAC63204EVM provides electrical connections to the device supply pins. The connections are shown in Table 2-1.

Table 2-1. DAC63204EVM Power Supply Inputs

DAC63204EVM Connector	Supply Name	Voltage Range
J2.1	VDD	1.8 V to 5.5 V (5 V available from the USB); remove J3 if applying an external VDD to the DAC.
J1.1	GND	0 V

The jumper settings on the DAC63204EVM are crucial to the proper operation of the EVM. Table 2-2 provides the details of the configurable jumper settings on the EVM. The DAC63204EVM pin numbers are defined in Figure 4-1.

Table 2-2. DAC63204EVM Jumper Settings

Jumper	Default Position	Available Option	Description
J3	Closed: 5-V USB supply connected to DAC VDD	Open: 5-V USB supply disconnected from DAC VDD	External or onboard VDD selection
J5	2-3: I^2C enabled	1-2: SPI enabled	I^2C or SPI selection
J6	Closed: GPIOs enabled	Open: GPIOs disabled	Controller GPIO enable

If an external supply is applied to the DAC VDD pin, remove jumper J3 to disconnect the 5-V USB supply from the DAC VDD pin.

GPIO2 from the onboard controller is connected to the DAC GPIO pin of the DACx3204. This input can be controlled through the graphical user interface (GUI) using the controls for GPIO2. If DAC GPIO is configured as an output, remove J6 to disable the GPIOs from the onboard controller.

GPIO3 from the onboard controller is broken out to J1, pin 8 and is controlled through the GUI using the controls for GPIO3.

To enable the GPIO pins, close jumper J6. To disable the GPIO pins, remove jumper J6.

2.2.3 Connecting the Hardware

After the power and jumper configurations are set up as per Section 2.2.2, connect the USB cable from the DAC63204EVM USB port to the computer.

3 Detailed Description

3.1 Hardware Description

The following sections provide detailed information on the EVM hardware and jumper configuration settings.

3.1.1 Theory of Operation

Figure 3-1 shows a simplified schematic of the DAC63204EVM board. There are two 16-pin connectors that provide access to all of the DAC pins. The GPIO, I^{2}C, and SPI signals from the onboard controller are connected to the DAC through three level translators. Each level translator can be independently disabled to disconnect the onboard controller GPIO, I^{2}C, and SPI signals from the DAC signals while the DAC is running in stand-alone mode.

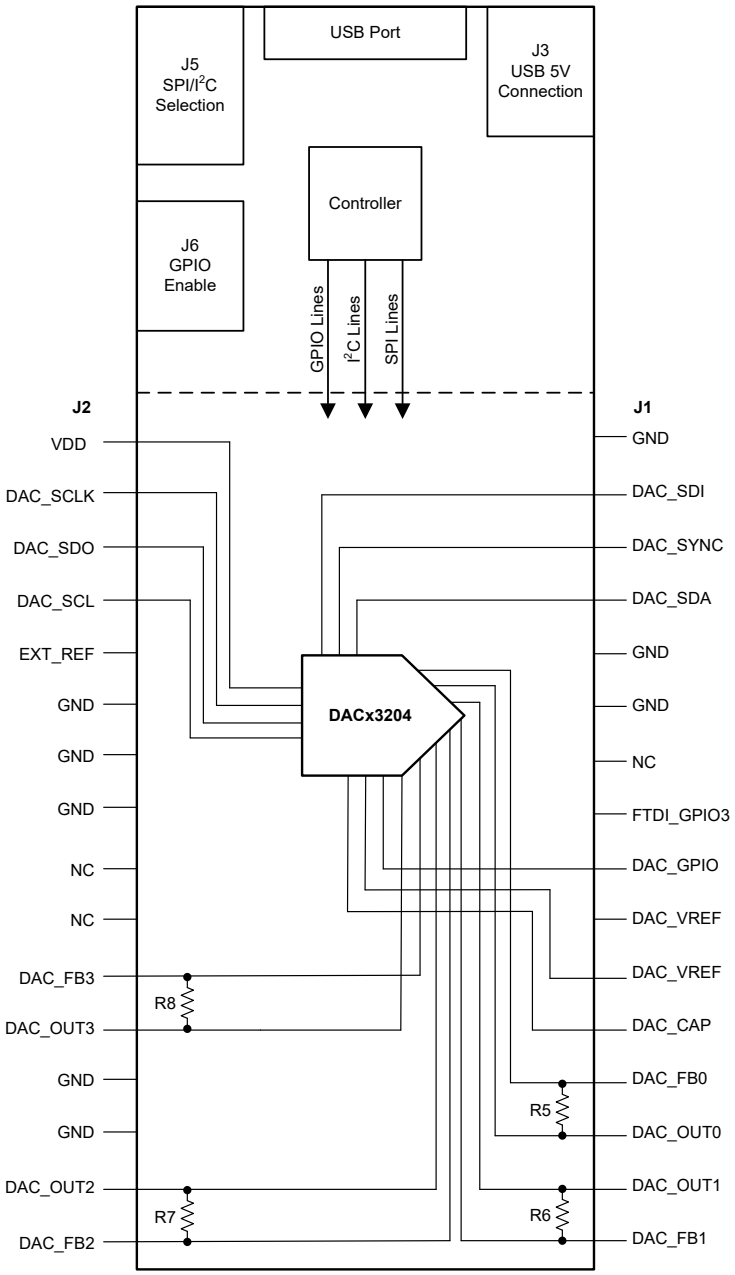

Figure 3-1. DAC63204EVM Hardware Simplified Schematic

3.1.1.1 Signal Definitions

The DAC63204EVM provides access to all DAC pins through connection J1 and J2, as listed in Table 3-1 and Table 3-2.

Table 3-1. DAC63204EVM J1 Pin Definitions

Pin#	Signal	Description
1	GND	Ground
2	DAC_SDI	SPI SDI signal for DAC
3	DAC_SYNC	SPI SYNC signal for DAC
4	DAC_SDA	I^2C SDA
5	GND	Ground
6	GND	Ground
7	NC	Not Connected
8	FTDI_GPIO3	GPIO3 output of the onboard controller
9	DAC_GPIO	GPIO Input for DACx3204
10	DAC_VREF	DAC_VREF
11	DAC_VREF	VREF input to the DAC
12	DAC_CAP	LDO bypass capacitor
13	DAC_FB0	Feedback pin for DAC VOUT0
14	DAC_OUT0	Output pin for DAC VOUT0
15	DAC_OUT1	Output pin for DAC VOUT1
16	DAC_FB1	Feedback pin for DAC VOUT1

Table 3-2. DAC63204EVM J2 Pin Definitions

Pin#	Signal	Description
1	DAC_VDD	VDD power supply for DAC
2	DAC_SCLK	SPI SCLK
3	DAC_SDO	SPI SDO
4	DAC_SCL	I^2C SCL
5	EXT_REF	External Reference input for DAC
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	NC	Not connected
10	NC	Not connected
11	DAC_FB3	Feedback pin for DAC VOUT3
12	DAC_OUT3	Output pin for DAC VOUT3
13	GND	Ground
14	GND	Ground
15	DAC_OUT2	Output pin for DAC VOUT2
16	DAC_FB2	Feedback pin for DAC VOUT2

3.2 Software Description

This section describes the features of the DAC63204EVM software, and discusses how to use these features. The software provides basic control of all the DACx3204 registers and functions.

3.2.1 Starting the Software

To launch the software, locate the Texas Instruments folder in the *All Programs* menu, and select the *DAC63204EVM* icon.

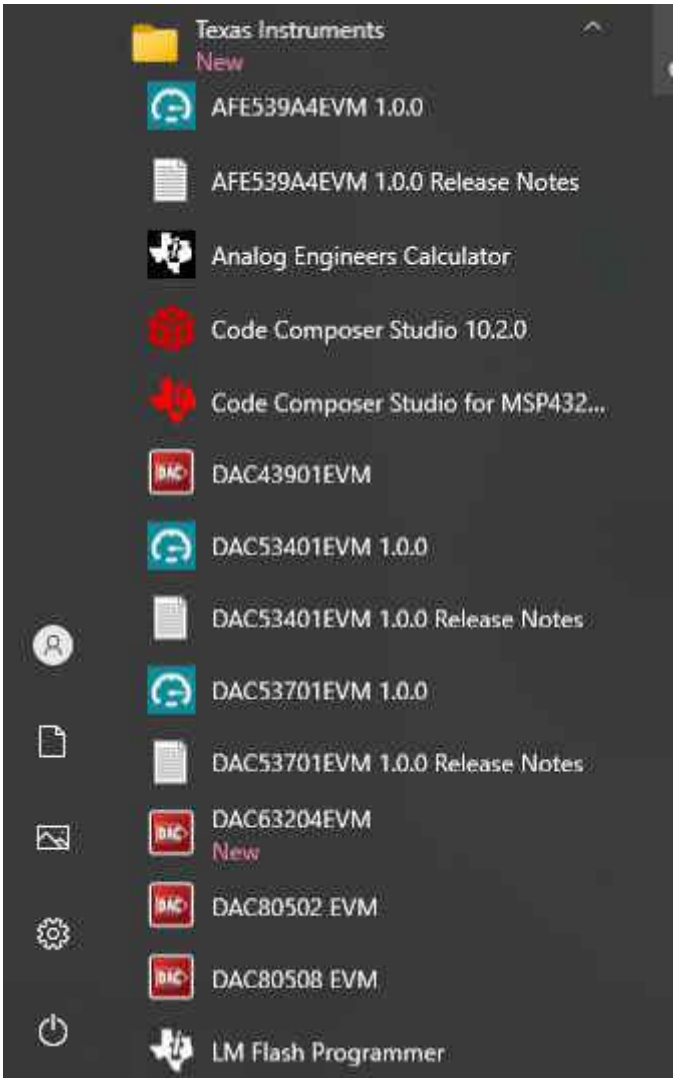

Figure 3-2. DAC63204EVM GUI Location

If the onboard controller is connected correctly, the status bar at the bottom of the screen displays *CONNECTED* as shown in Figure 3-3. If the controller is not properly connected or not connected at all, the status displays *DEMO*. If the GUI is not displaying, the *CONNECTED* status while the EVM is connected, unplug and reconnect the EVM, and then relaunch the GUI software.

Figure 3-3. DAC63204EVM GUI Connection Detection

3.2.2 Software Features

The DAC63204EVM GUI incorporates interactive functions that help configure an individual DACx3204 device using I^2C communication. These functions are built into several GUI pages, as shown in the following subsections. The menu bar on the far left of the GUI allows the user to switch between pages. The menu bar displays the *High Level Configuration* page with *Basic DAC*, *Margining*, and *Function Generation* subpages, *and the Low Level Configuration* page.

Before using the GUI, see the respective device data sheet for detailed DACx3204 programming instructions.

3.2.2.1 High Level Configuration Page

The *High Level Configuration* page, shown in Figure 3-4, provides an interface to quickly configure the parameters and relevant register settings for the respective DACx3204 device. The *High Level Configuration* page consists of the *Basic DAC*, *Margining*, and *Function Generation* subpages.

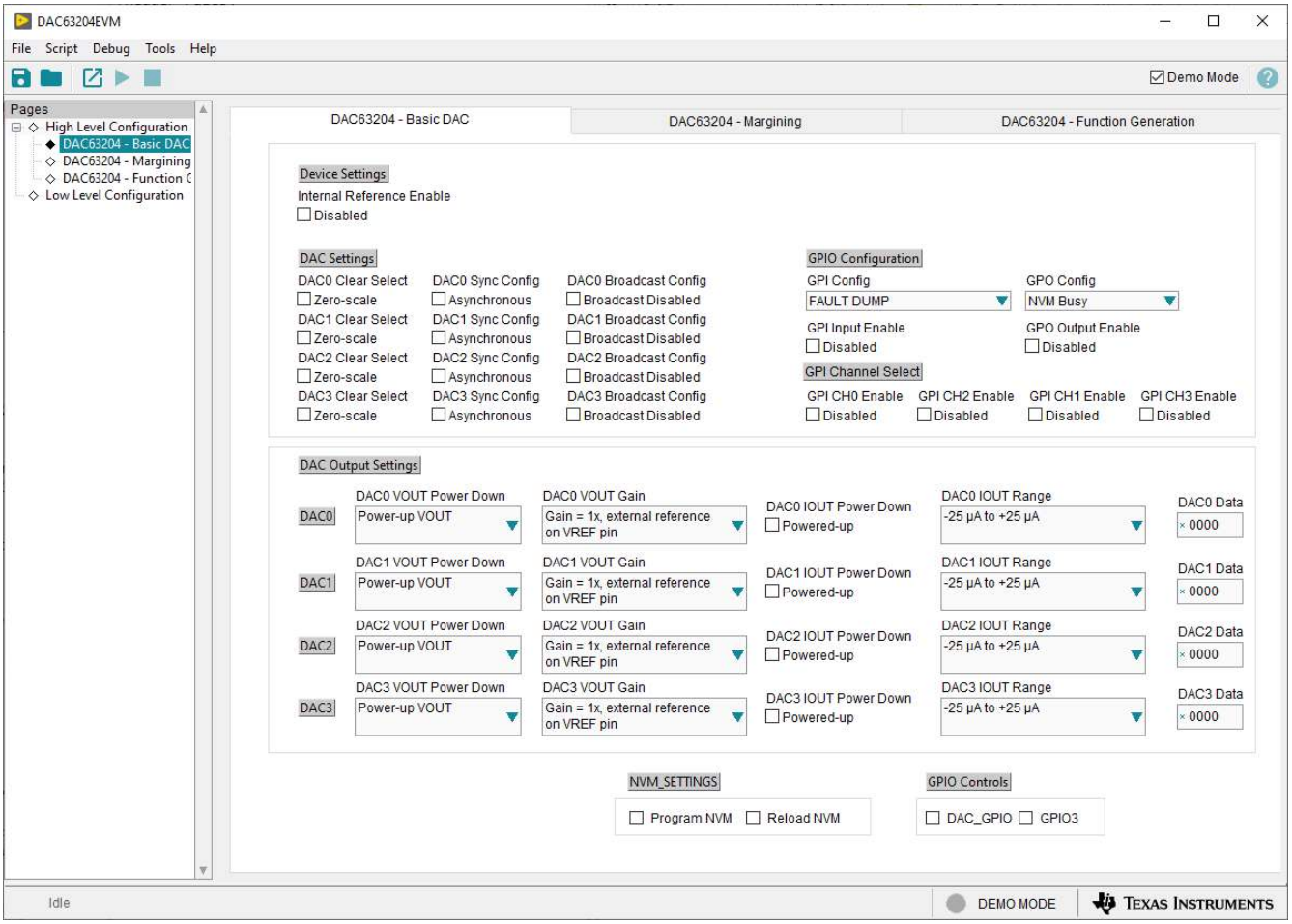

Figure 3-4. High Level Configuration Page

3.2.2.1.1 Basic DAC Subpage

The *Basic DAC* subpage shown in Figure 3-5 provides an interface to quickly power up, select the reference and output span, and program the output voltage or current for the respective DACx3204 device. When VDD is applied, the DACx3204 device starts up in Hi-Z power-down mode by default. The *Basic DAC* subpage also provides controls to configure the GPIO pin on the respective DACx3204 device, and control the two GPIO outputs of the DAC63204EVM onboard controller. The register settings can be programmed or retrieved using the *Program NVM* or *Reload NVM* checkboxes, respectively.

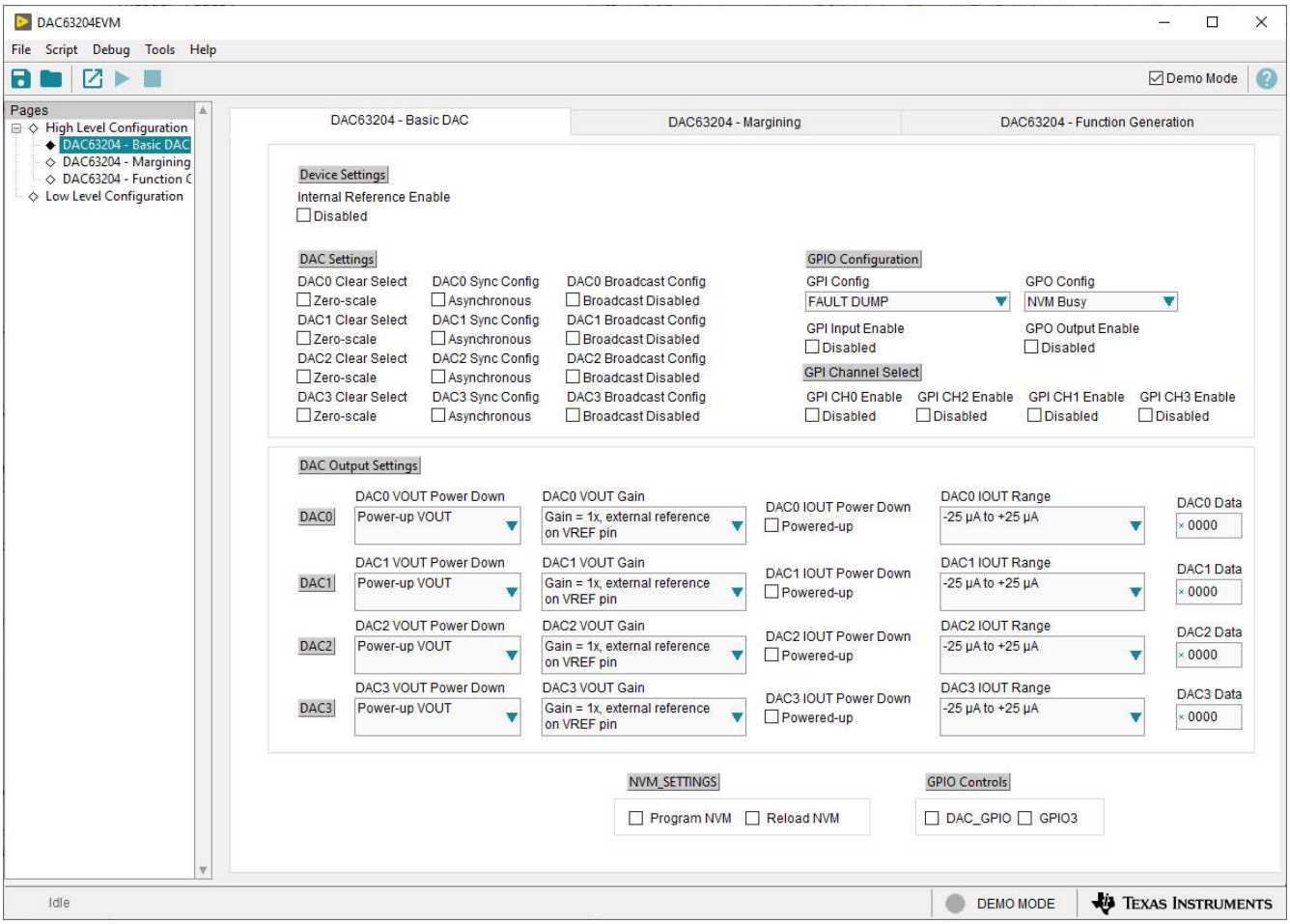

Figure 3-5. Basic DAC Subpage

3.2.2.1.2 Margining Subpage

The *Margining* subpage is shown in Figure 3-6. This subpage provides the settings for the margin-low, margin-high, and nominal DAC outputs. Self-resetting triggers are used to trigger the margin-high and margin-low voltage levels for each DAC channel. The *Code Step* and *Slew Rate* drop-down menu settings are also provided on this page to control the slew of each margin high or low trigger (*Trigger MHx*). The register settings can be programmed or retrieved using the *Program NVM* or *Reload NVM* checkboxes, respectively.

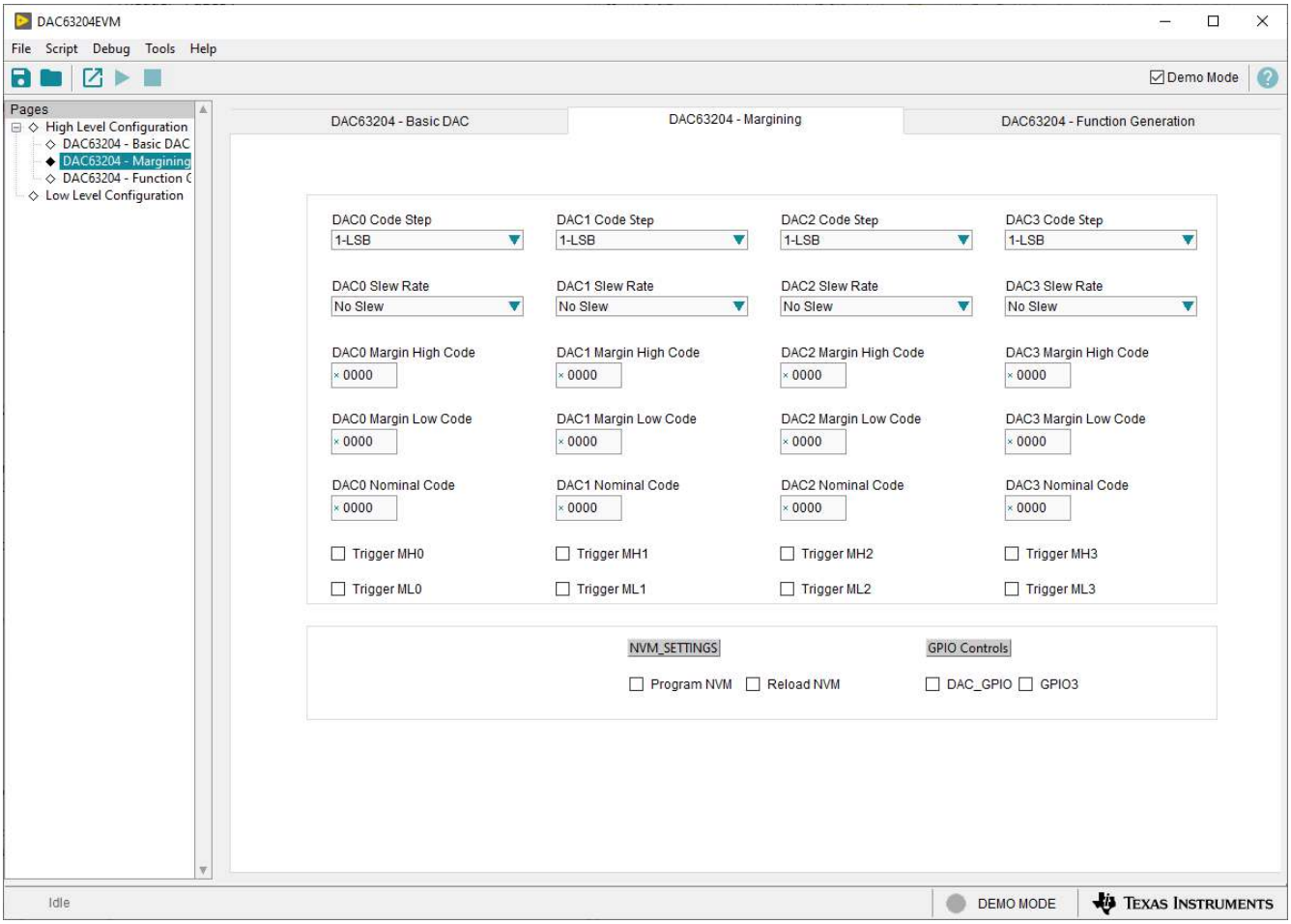

Figure 3-6. Margining Subpage

3.2.2.1.3 Functions Generation Subpage

The *Function Generation* subpage, as shown in Figure 3-7, provides control of the relevant register settings for function generation This subpage provides the ramp programming done through the *Code Step* and *Slew Rate* drop-down menu settings. The DAC waveform drop-down menu selects the waveform to be generated: triangular, saw-tooth, inverse saw-tooth, square, or sine. The *Margin High Code* and *Margin Low Code* settings define the upper and lower bounds of the waveform, respectively. The *Start Function Gen* checkboxes start or stop the defined function generation for each channel. The register settings can be programmed or retrieved using the *Program NVM* or *Reload NVM* checkboxes, respectively.

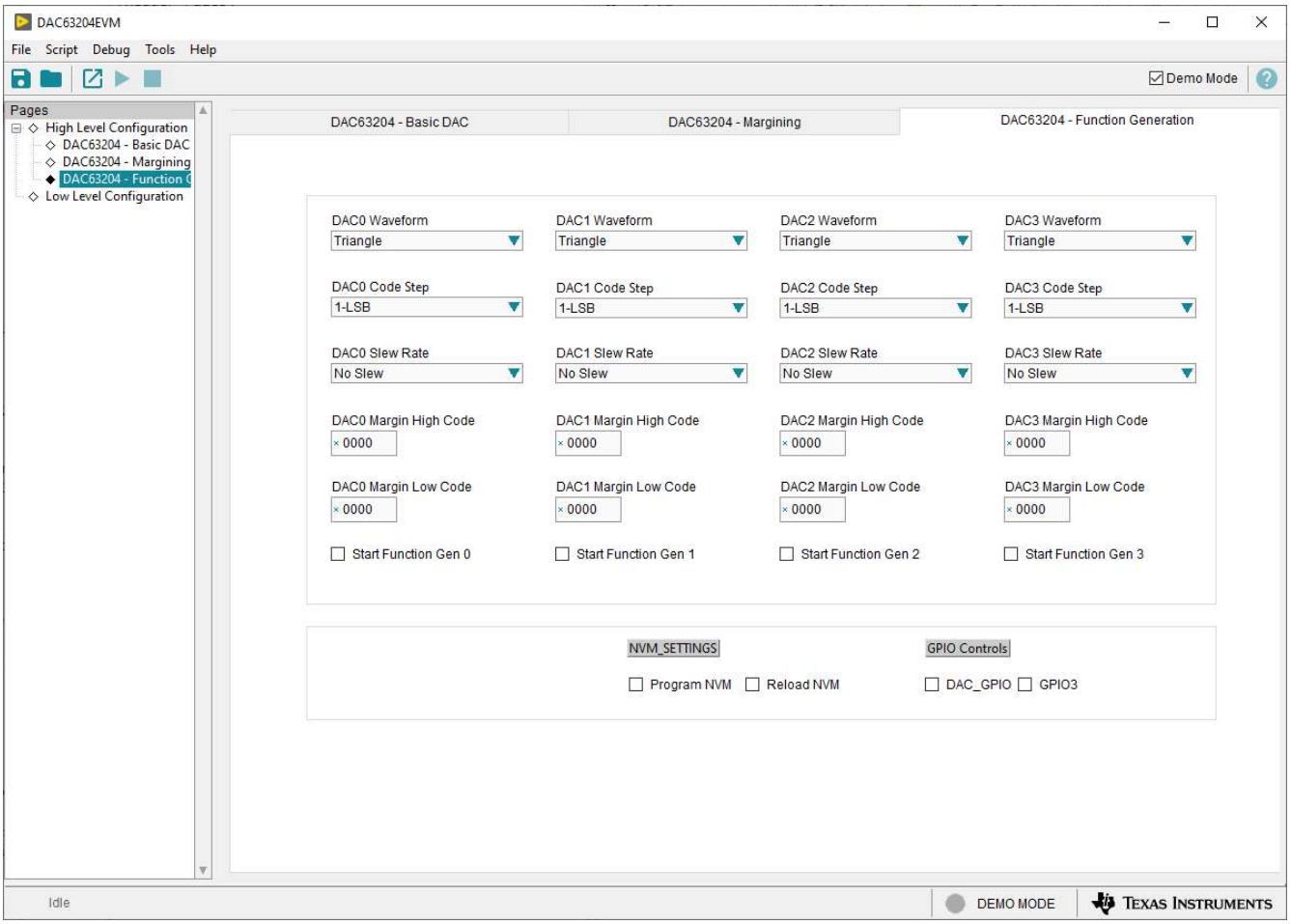

Figure 3-7. Function Generation Subpage

3.2.2.2 Low Level Configuration Page

The *Low Level Configuration* page, shown in Figure 3-8, allows access to low-level communication directly with the respective DACx3204 device registers. Select a register on the *Register Map* list to show a description of the values in that register, as well as information on the register address, default value, size, and current value. Data are written to the registers by entering a value in the value column of the GUI.

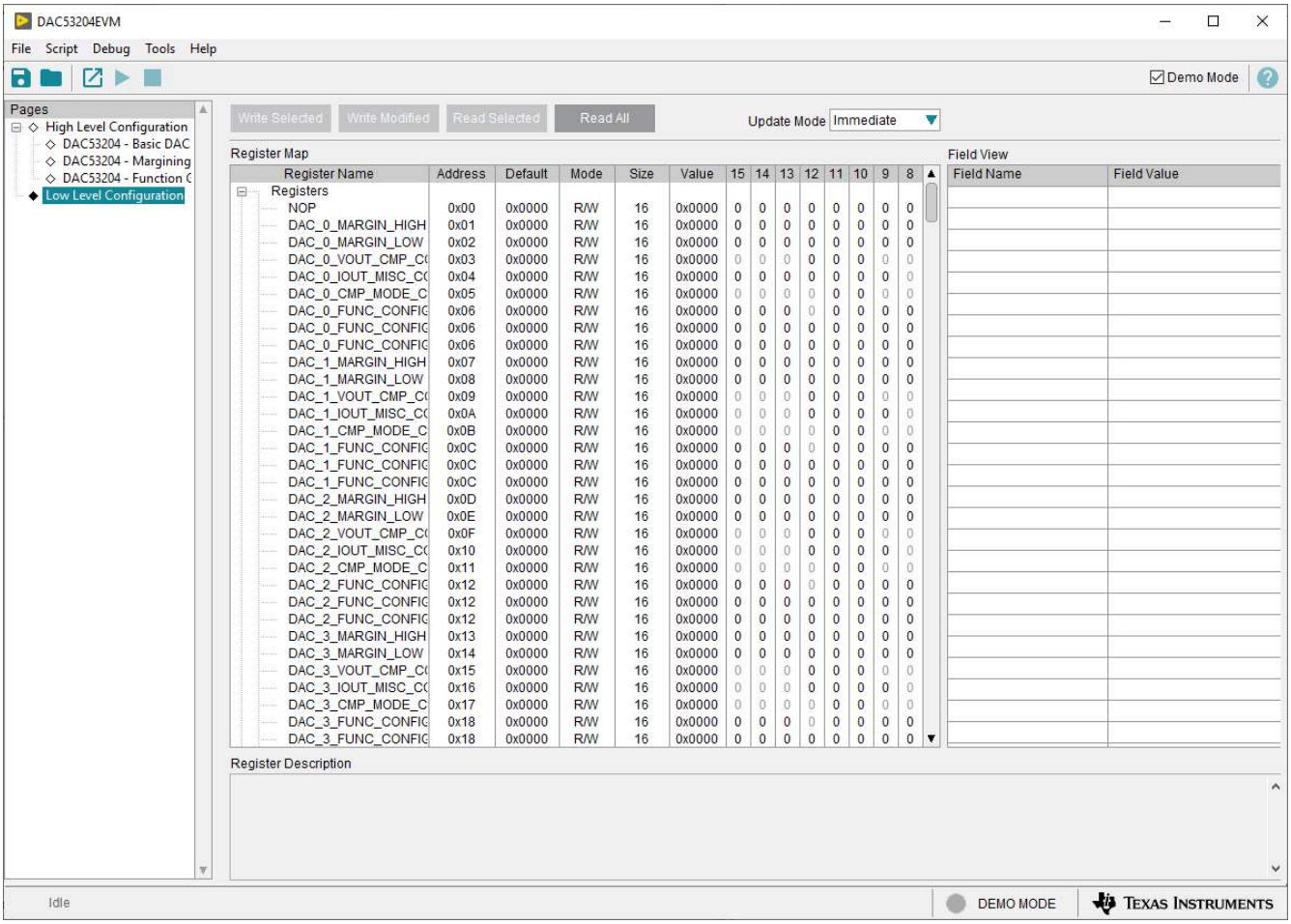

Figure 3-8. Low Level Configuration Page

To store the values of the register map locally, select *Save Configuration* under the *File* menu option. The stored configuration files can be recalled and loaded by selecting *Open Configuration*.

Figure 3-9 shows the four configuration buttons provided on the *Low Level Configuration* page that allow the user to read from and write to the device registers:

- **Write Selected**
- **Write Modified**
- **Read Selected**
- **Read All**

The **Write Modified** button is enabled only in *Deferred Update Mode*. *Deferred Update Mode* initiates a write operation only when the **Write Selected** or **Write Modified** buttons are pressed. By default, *Immediate Update Mode* is selected for the *Low Level Configuration* page write operations.

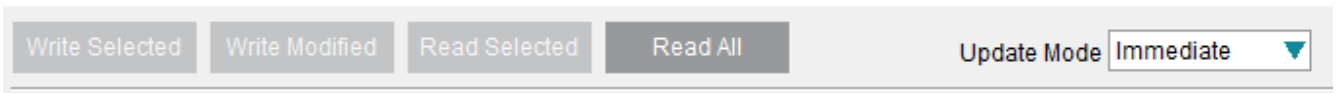

Figure 3-9. Low Level Configuration Page Options

4 Schematic, PCB Layout, and Bill of Materials

This section contains the schematics, printed circuit board (PCB) layout diagrams, and a complete bill of materials for the DAC63204EVM.

4.1 Schematic

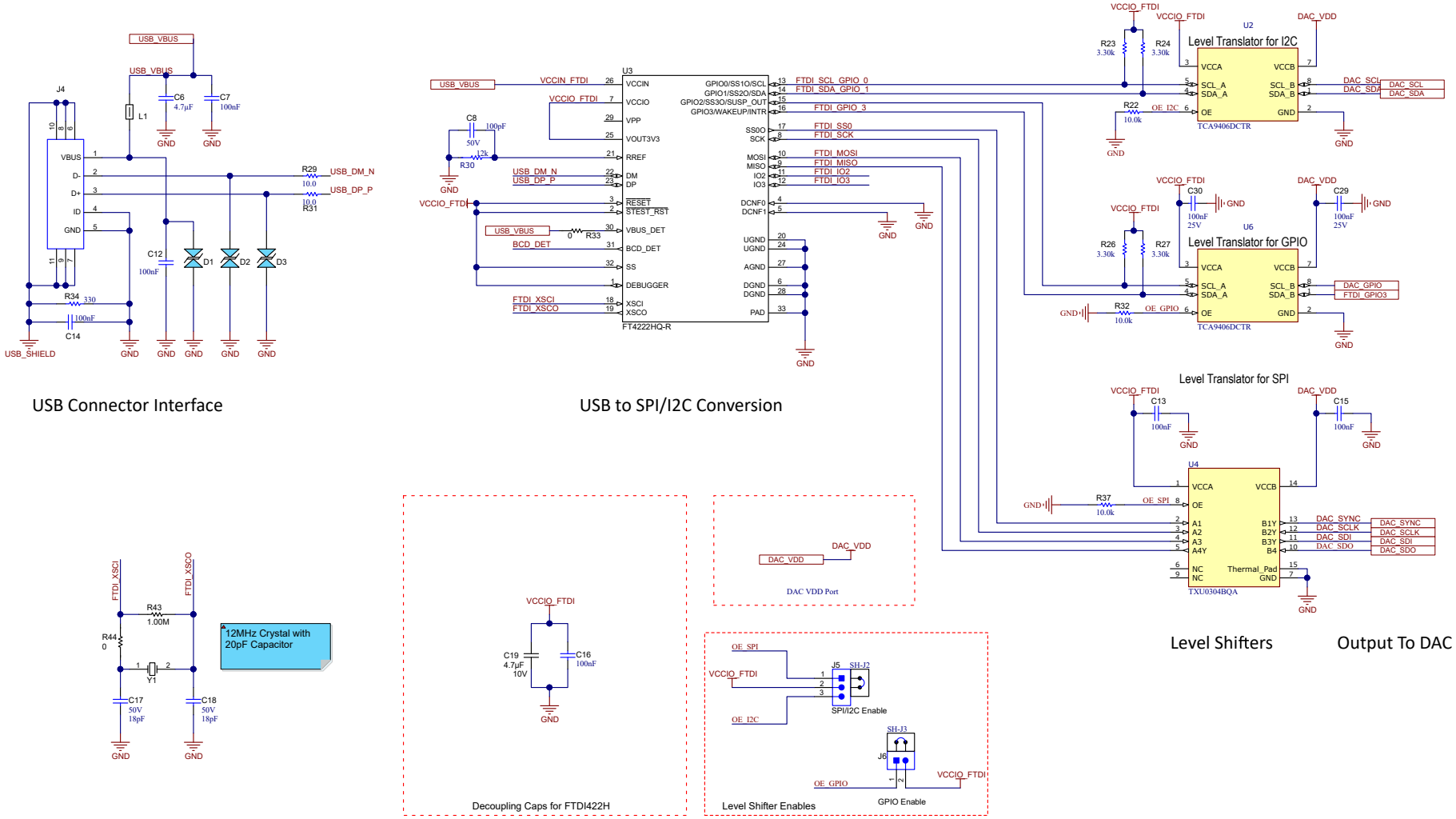

Figure 4-1. DAC63204EVM Schematic Page 1

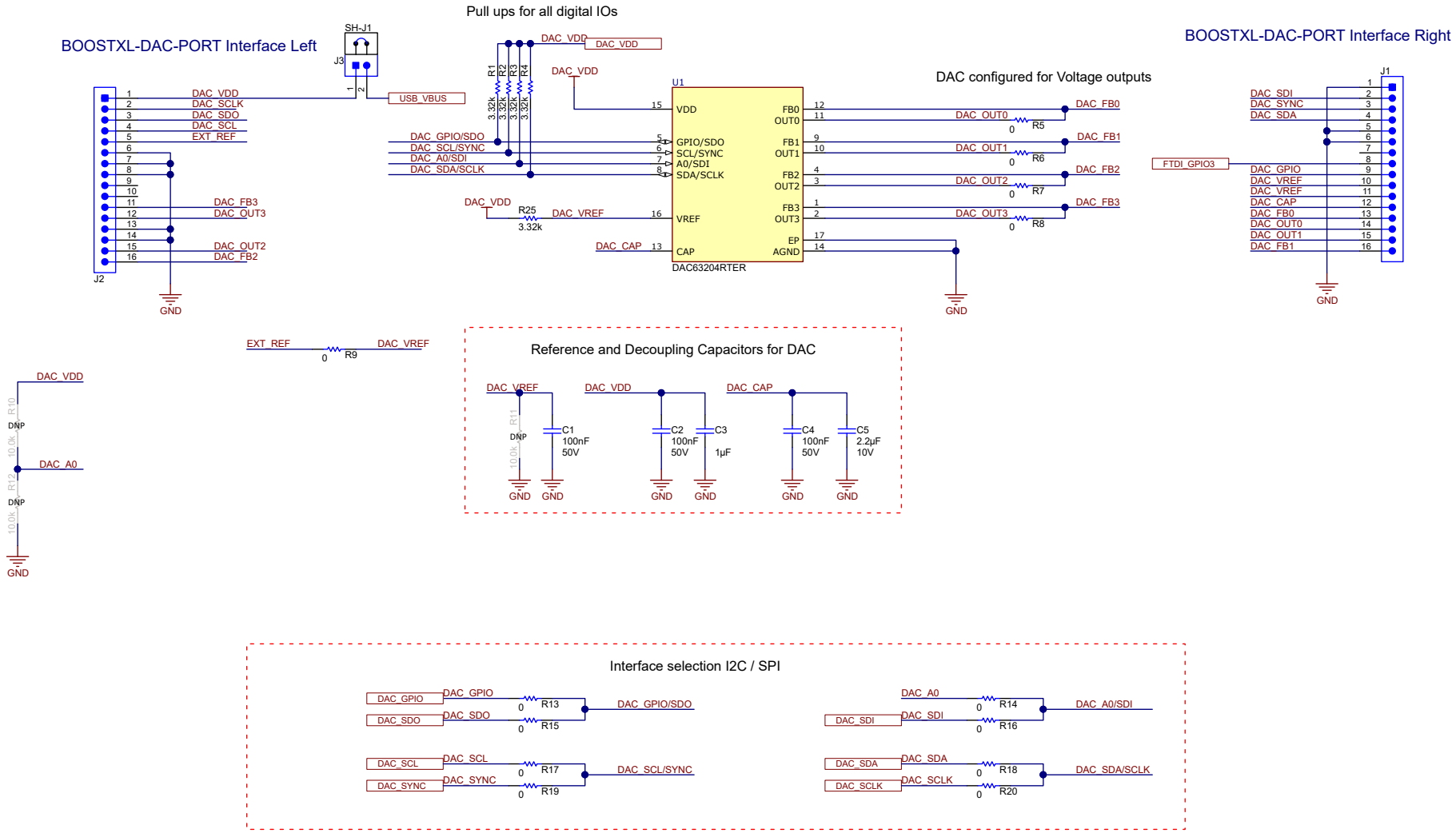

Figure 4-2. DAC63204EVM Schematic Page 2

4.2 PCB Layout

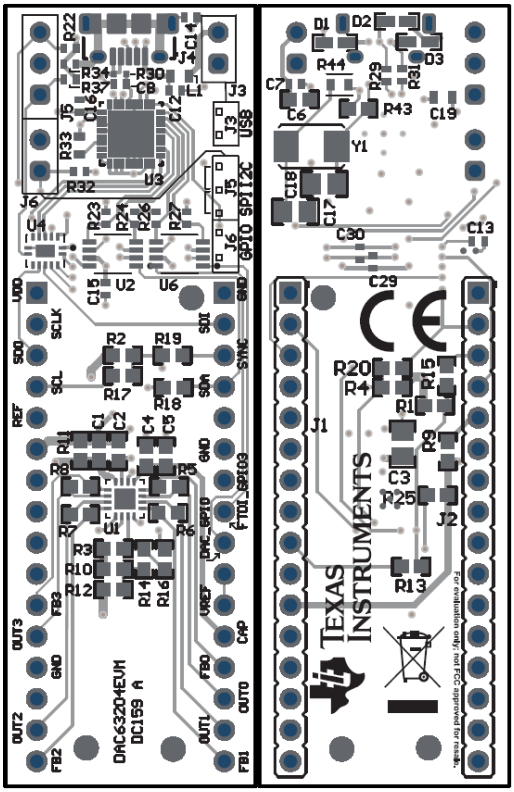

Figure 4-3. DAC63204EVM PCB Components Layout

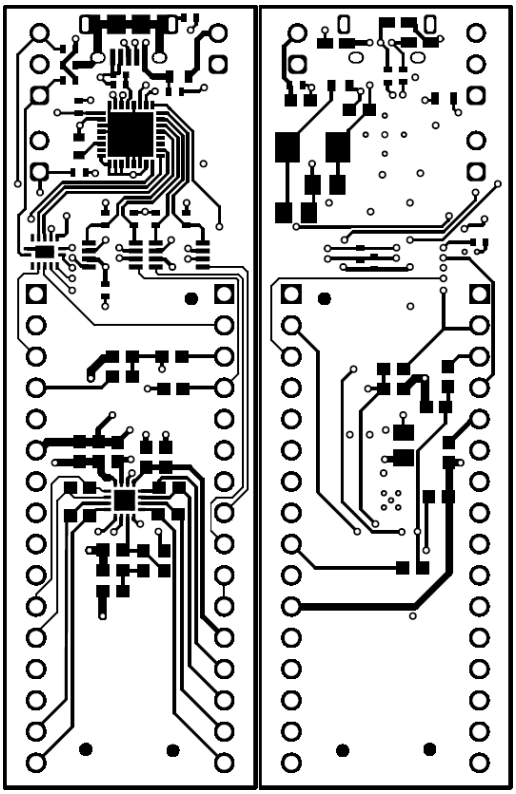

Figure 4-4. DAC63204EVM PCB Layers

4.3 Bill of Materials

Table 4-1. DAC63204EVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB	1		Printed Circuit Board		DC159	Any
C1, C2, C4	3	0.1 µF	CAP, CERM, 0.1 µF, 50 V,+/- 5%, X7R, 0603	0603	06035C104JAT2A	AVX
C3	1	1 µF	CAP, CERM, 1 µF, 50 V,+/- 10%, X7R, 0805	0805	GJ821BR71H105KA12L	MuRata
C5	1	2.2 µF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7R, 0603	0603	GRM188R71A225KE15D	MuRata
C6, C19	2	4.7 µF	CAP, CERM, 4.7 uF, 10 V, +/- 20%, X7R, 0603	0603	GRM188Z71A475ME15D	MuRata
C7, C12, C13, C14, C15, C16, C29, C30	8	0.1 µF	CAP, CERM, 0.1 µF, 25 V,+/- 10%, X7R, 0402	0402	CC0402KRX7R8BB104	Yageo
C8	1	100 pF	CAP, CERM, 100 pF, 50 V, +/- 10%, X7R, 0402	0402	885012205055	Wurth Elektronik
C17, C18	2	18 pF	CAP, CERM, 18 pF, 50 V, +/- 5%, C0G/NP0, 0805	0805	CC0805JRNP09BN180	Yageo America
J1, J2	2		Header, 2.54mm, 16x1, TH	Header, 2.54mm, 16x1, TH	22284160	Molex
J3, J6	2		Header, 2.54mm, 2x1, Tin, TH	Header, 2.54mm, 2x1, TH	TSW-102-23-T-S	Samtec
J4	1		Receptacle, USB 2.0, Micro-USB Type B, R/A, SMT	USB-micro B USB 2.0, 0.65mm, 5 Pos, R/A, SMT	10118194-0001LF	FCI
J5	1		Header, 2.54mm, 3x1, Gold, TH	Header, 2.54mm, 3x1, TH	TSW-103-08-G-S	Samtec
L1	1	600 ohm	Ferrite Bead, 600 ohm @ 100 MHz, 1 A, 0603	0603	782633601	Wurth Elektronik
R1, R2, R3, R4, R25	5	3.32 k	RES, 3.32 k, 1%, 0.1 W, 0603	0603	RC0603FR-073K32L	Yageo America
R5, R6, R7, R8, R9, R13, R14, R15, R16, R17, R18, R19, R20	13	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo America
R10, R11, R12	0	10.0 k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo America
R22, R32, R37	0	10.0 k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RMCF0402FT10K0	Stackpole Electronics Inc
R23, R24, R26, R27	4	3.30k	RES, 3.30 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RK73H1ETTP3301F	KOA Speer
R29, R31	2	10.0	RES, 10.0, 1%, 0.063 W, 0402	0402	RK73H1ETTP10R0F	KOA Speer

Table 4-1. DAC63204EVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R30	1	12 k	12 kOhms ±1% 0.1W, 1/10W Chip Resistor 0402 (1005 Metric) Automotive AEC-Q200 Thick Film	0402	ERJ-2RKF1202X	Panasonic ECG
R33, R44	2	0	0 Ohms Jumper 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	0603	ERJ-3GEY0R00V	Panasonic
R34	1	330	RES, 330, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF3300X	Panasonic
R43	1	1 M	RES, 1.00 M, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M00FKEA	Vishay-Dale
U1	1		Automotive, Smart DACs for Animation and Fault Management With I 2C, SPI, GPIO, and PWM Interface	WQFN16	DAC63204RTER	Texas Instruments
U2, U6	2		Voltage Level Translator Bidirectional 1 Circuit 2 Channel 24Mbps SM8	SSOP8	TCA9406DCTR	Texas Instruments
U3	1		USB2.0 to QuadSPI/I2C Bridge IC, VQFN-32	VQFN-32	FT4222HQ-D-R	FTDI
U4	1		4-Bit Fixed Direction Voltage-Level Translator with Schmitt- Trigger Inputs, and Tri-State Outputs, WQFN14	WQFN14	TXU0304BQA	Texas Instruments
Y1	1		Crystal, 12 MHz, 18pF, SMD	ABM3	ABM3-12.000MHZ-B2-T	Abracon Corporation

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