Product Document

Published by ams OSRAM Group





Datasheet

DS001038



13-Channel Multi-Spectral Sensor

v2-00 • 2022-Aug-12

Content Guide

| General Description 3 |
|---|
| Key Benefits & Features3 Applications4 Block Diagram4 |
| Ordering Information5 |
| Pin Assignment 6 |
| Pin Diagram6 Pin Description6 |
| Absolute Maximum Ratings 8 |
| Electrical Characteristics9 |
| Optical Characteristics 10 |
| Typical Operating Characteristics14 |
| Functional Description15 |
| Device Architecture 16 Sensor Array 17 GPIO 17 Interrupt (INT) 17 LED Driver (LDR) 17 |
| I ² C Interface18 |
| |

| 9.1 9.2 9.3 9.4 9.5 | I ² C Address I ² C Write Transaction I ² C Read Transaction Timing Characteristics Timing Diagrams | 18 19 19 |
|---------------------------------|--|----------------|
| 10 | Register Description | . 21 |
| 10.1 10.2 | Register Overview Detailed Register Description | 21 24 |
| 11 | Application Information | .44 |
| 11.1 11.2 11.3 | Schematic PCB Pad Layout Application Optical Requirements | 44 |
| 12 | Package Drawings & Markings | . 46 |
| 13 | Tape & Reel Information | . 47 |
| 14 | Soldering & Storage Information | n 49 |
| 14.1 | Storage Information | 50 |
| 15 | Revision Information | . 51 |
| 16 | Legal Information | . 52 |
| | | |

1 General Description

The ams OSRAM AS7343L¹ is a 13-channel spectrometer designed for spectral identification of lateral flow particle markers. It is highly versatile sensor targeted to enable new laboratory applications. It is optimized for reflective, transmissive and emissive measurements including lateral flow test applications, fluid or reagent analysis, color matching, and spectral identification in the visible range.

13 individual channels cover the spectral range from approximately 380 nm to 1000 nm. 11 channels are centered in the visible spectrum (VIS), plus one near-infrared (NIR) and a clear channel. Allowing a full spectral re-construction of the incoming light.

AS7343L integrates high-precision optical filters onto standard CMOS silicon via deposited interference filter technology. A built-in aperture controls the light entering the sensor array to increase accuracy. A programmable digital GPIO and LED driver enable light source and trigger/sync control. Device control and spectral data access is implemented through a serial I²C interface. The device is available in an ultra-low profile package with dimensions of 3.1 mm x 2 mm x 1 mm.

1.1 Key Benefits & Features

The benefits and features of AS7343L, 13-Channel Multi-Spectral Sensor, are listed below:

Figure 1:

Added Value of Using AS7343L

| Benefits | Features |
|--|--|
| Highly versatile spectral sensor | 13 channels between 380 nm and 1000 nm Reflective, transmissive and emissive applications Fluorescence and luminescence measurements Spectral re-construction |
| Highest sensitivity | Enables ultra-low light operation (e.g. chemiluminescence applications) Enables operation behind additional external filters |
| Low power consumption and minimum I ² C traffic | 1.8 V VDD operationConfigurable sleep modeInterrupt-driven device |
| Ultra-high integration | On chip interference filter technology Integrated LED driver and 6 integrated ADCs 3.1 mm x 2 mm x 1 mm package outline |

¹ L = Lateral flow

| Benefits | Features |
|-------------------------------------|---|
| Electronic shutter/external trigger | GPIO can be configured to function as external |
| functionality | trigger input to enable fluorescence measurements |

1.2 Applications

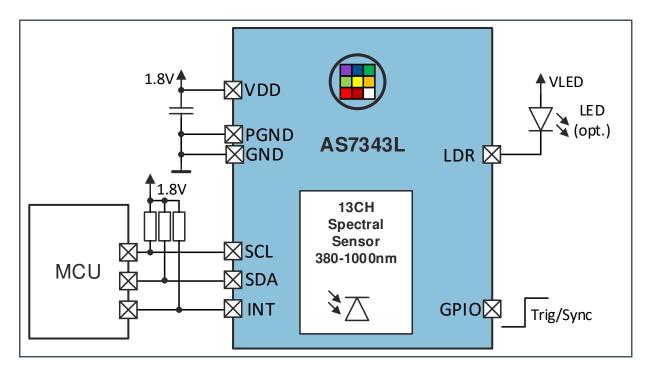
- Multi-analyte detection
- Fluorescent-based measurement applications
- Luminescence-based measurement applications
- Reflection- or transmissivity-based color detection (e.g. lateral flow strips)

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2:

Functional Blocks of AS7343L



2 Ordering Information

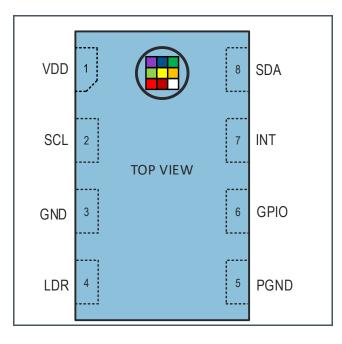
| Ordering Code | Package | Delivery Form | Delivery Quantity |
|---------------|---------|----------------------|-------------------|
| AS7343L-DLGT | OLGA-8 | Tape & Reel 13-inch | 5000 pcs/reel |
| AS7343L-DLGM | OLGA-8 | Tape & Reel 7-inch | 500 pcs/reel |

3 Pin Assignment

3.1 Pin Diagram

Figure 3:

Pin Assignment of AS7343L (TOP VIEW)



3.2 Pin Description

Pin Description of AS7343L

| Pin Number | Pin Name | Pin Type ⁽¹⁾ | Description |
|------------|----------|-------------------------|--|
| 1 | VDD | Р | Positive supply voltage terminal |
| 2 | SCL | DI | Serial interface clock signal line for I ² C interface. Connect pull up resistor to 1.8 V. |
| 3 | GND | Р | Ground. All voltages referenced to GND |
| 4 | LDR | A_I/O | LED current sink input. If not used leave pin unconnected. |
| 5 | PGND | Р | Ground. All voltages referenced to GND |
| 6 | GPIO | D_I/O | General purpose input/output. Default output open drain. If not used leave pin unconnected. |
| 7 | INT | DO_OD | Interrupt. Open drain output active low. Connect pull up resistor to 1.8 V. If not used leave pin unconnected. |

Figure 4:

| Pin | Number | Pin Name | Pin Type ⁽¹⁾ | Description |
|-----|-------------------|--|-------------------------|---|
| 8 | | SDA | D_I/O | Serial interface data signal line for I ² C interface. Connect pull up resistor to 1.8 V. |
| (1) | Explanatior DI | n of abbreviations: Digital Input | | |
| | D_I/O DO OD | Digital Input/Outpu Digital Output, ope | | |
| | P A_I/O | Power pin Analog pin | | |

4 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. All voltages with respect to GND/PGND. Device parameters are guaranteed at V_{DD}=1.8 V and T_A=25 °C unless otherwise noted.

Figure 5:

Absolute Maximum Ratings of AS7343L

| Symbol | Parameter | Min | Мах | Unit | Comments |
|------------------------------------|--|------|------|------|---|
| Electrical Pa | arameters | | | | |
| V_{DD} / V_{GND} | Supply Voltage to Ground | -0.3 | 1.98 | V | Applicable for pin VDD |
| V _{ANA_MAX} | Analog Pins | -0.3 | 3.6 | V | Applicable for pin LDR |
| V _{DIG_MAX} | Digital Pins | -0.3 | 3.6 | V | Applicable for pins SCL,SDA,GPIO and INT |
| I _{SCR} | Input Current (latch-up immunity) | ÷. | 100 | mA | AEC-Q100-004E |
| lo | Output Terminal Current | -1 | 20 | mA | |
| Electrostatio | : Discharge | | | | |
| ESD _{HBM} | Electrostatic Discharge HBM | ± 2 | 000 | V | JS-001-2017 |
| ESD _{CDM} | Electrostatic Discharge CDM | ± { | 500 | V | JS-002-2018 |
| Temperature | e Ranges and Storage Conditions | | | | |
| T _A | Operating Ambient Temperature | -30 | 85 | °C | |
| T _{STRG} | Storage Temperature Range | -40 | 85 | °C | |
| TBODY | Package Body Temperature | | 260 | °C | IPC/JEDEC J-STD-020 ⁽¹⁾ |
| RH _{NC} | Relative Humidity (non- condensing) | 5 | 85 | % | |
| MSL | Moisture Sensitivity Level | | 3 | | Maximum floor life time of 168h |

The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020
 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn)

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages with respect to GND/PGND. Device parameters are guaranteed at VDD=1.8 V and $T_A=25$ °C unless otherwise noted.

Figure 6:

Electrical Characteristics of AS7343L

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|--------------|---|--|------|-----|------|------|
| VDD | Supply Voltage | | 1.7 | 1.8 | 1.98 | V |
| ТА | Operating free-air temperature ⁽¹⁾ | | -30 | 25 | 85 | °C |
| Power Consur | nption | | | | | |
| IDD | | VDD=1.8 V; T _A =25 °C Active mode ⁽³⁾ | | 210 | 280 | μΑ |
| | Supply Current ⁽²⁾ | VDD=1.8 V; T _A =25 °C Idle mode ⁽⁴⁾ | | 40 | 60 | μA |
| | | VDD=1.8 V; T _A =25 °C Sleep mode ⁽⁵⁾ | | 0.7 | 5 | μΑ |
| Digital Pins | | | | | | |
| VIH | SCL,SDA input high voltage | | 1.26 | | | V |
| VIL | SCL,SDA input low voltage | | | | 0.54 | V |
| VOL | INT, SDA output low voltage | 6 mA sink current | | | 0.4 | V |
| CI | Input pin capacitance | | | | 10 | pF |
| lleak | Leakage current into SCL,SDA,INT pins | | -5 | | 5 | μΑ |
| GPIO | | | | | | |
| CLOAD | Maximum capacitive load GPIO | | | | 20 | pF |
| LED Driver | | | | | | |
| | | I_LDR= 4 mA ; LED_HALF = "0" | | | 240 | m)/ |
| | | I_LDR= 4 mA ; LED_HALF = "1" | _ | | 130 | – mV |
| V_LDR | LDR compliance voltage | I LDR 134 mA ; LED_HALF = "0" | | | 280 | |
| | | I LDR 134 mA ; LED_HALF = "1" | _ | | m | – mV |

(1) While the device is operational across the temperature range, functionality will vary with temperature.

(2) Supply current values are shown at the VDD pin and do not include current through pin LDR.

(3) Active state occurs during active integration. (PON = "1"; SP_EN = "1") If wait is enabled (WEN = "1"), supply current is lower during the wait period

(4) Idle state occurs when PON = "1" and all functions are disabled

(5) Sleep state occurs when PON = "0" and I²C bus is idle. If I²C traffic is active device automatically enters idle mode.

6 Optical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages with respect to GND/PGND. Device parameters are guaranteed at VDD=1.8 V and $T_A=25$ °C unless otherwise noted.

Figure 7:

AS7343L Optical Channel Summary

| Channel | Peak | Wavelength [ni | Full Width Half Maximum [nm] | |
|---------|-------|----------------|------------------------------|-------|
| Channel | (min) | λp (typ) | (max) | (typ) |
| F1 | 395 | 405 | 415 | 30 |
| F2 | 415 | 425 | 435 | 22 |
| FZ | 440 | 450 | 460 | 55 |
| F3 | 465 | 475 | 485 | 30 |
| F4 | 505 | 515 | 525 | 40 |
| FY | 545 | 555 | 565 | 100 |
| F5 | 540 | 550 | 560 | 35 |
| FXL | 590 | 600 | 610 | 80 |
| F6 | 630 | 640 | 650 | 50 |
| F7 | 680 | 690 | 700 | 55 |
| F8 | 735 | 745 | 755 | 60 |
| NIR | 845 | 855 | 865 | 54 |

(1) Parameter measured on a production ongoing sample bases on glass using diffused light. The table above is valid for full sensor response including diffuser, package and photodiode response.

(2) Peak Wavelength is validated by smoothed/averaged monochromator measurement data

Figure 8:

Optical Characteristics of Spectral Channels, AGAIN: 1024x, Integration Time: 27.8 ms

| Symbol | Parameter | Conditions | Min | Тур | Мах | Unit |
|--------------------|---|--|------|-------|-------|--------|
| Re_F1 | Irradiance responsivity channel F1 | LED_396nm ; Ee= 155 mW/m² LED_408nm ; Ee= 155 mW/m² | 4311 | 5749 | 7186 | counts |
| R _{e_F2} | Irradiance responsivity channel F2 | LED_408nm ; Ee= 155 mW/m² LED_448nm ; Ee= 155 mW/m² | 1317 | 1756 | 2196 | counts |
| R _{e_FZ} | Irradiance responsivity channel FZ | LED_428nm ; Ee= 155 mW/m² LED_480nm ; Ee= 155 mW/m² | 1627 | 2169 | 2711 | counts |
| R _{e_F3} | Irradiance responsivity channel F3 | LED_448nm ; Ee= 155 mW/m² LED_500nm ; Ee= 155 mW/m² | 577 | 770 | 962 | counts |
| R _{e_F4} | Irradiance responsivity channel F4 | LED_500nm ; Ee= 155 mW/m² LED_534nm ; Ee= 155 mW/m² | 2356 | 3141 | 3926 | counts |
| R _{e_FY} | Irradiance responsivity channel FY | LED_534nm ; Ee= 155 mW/m² LED_593nm ; Ee= 155 mW/m² | 2810 | 3747 | 4684 | counts |
| R _{e_F5} | Irradiance responsivity channel F5 | LED_531nm ; Ee= 155 mW/m² LED_594nm ; Ee= 155 mW/m² | 1180 | 1574 | 1967 | counts |
| R _{e_FXL} | Irradiance responsivity channel FXL | LED_593nm ; Ee= 155 mW/m² LED_628nm ; Ee= 155 mW/m² | 3582 | 4776 | 5970 | counts |
| R _{e_F6} | Irradiance responsivity channel F6 | LED_618nm ; Ee= 155 mW/m² LED_665nm ; Ee= 155 mW/m² | 2502 | 3336 | 4170 | counts |
| R _{e_F7} | Irradiance responsivity channel F7 | LED_685nm ; Ee= 155 mW/m² LED_715nm ; Ee= 155 mW/m² | 4095 | 5435 | 6774 | counts |
| R _{e_F8} | Irradiance responsivity channel F8 | LED_715nm ; Ee= 155 mW/m² LED_766nm ; Ee= 155 mW/m² | 648 | 864 | 1080 | counts |
| R _{e_NIR} | Irradiance responsivity channel NIR | LED_849nm ; Ee= 155 mW/m² LED_903nm ; Ee= 155 mW/m² | 7936 | 10581 | 13226 | counts |



Figure 9:

Optical Characteristics of Broadband Channels, AGAIN: 1024x, FD_GAIN: 64x, Integration Time: 27.8 ms

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|--------|---|--|------|------|------|--------|
| Re_FD | Irradiance responsivity channel Flicker | LED_593nm ; Ee= 155 mW/m² LED_766nm ; Ee= 155 mW/m² FD_GAIN=64x | 3233 | 4311 | 5389 | counts |
| Re_vis | Irradiance responsivity channel VIS | LED_396nm ; Ee= 155 mW/m ² LED_766nm ; Ee= 155 mW/m ² 2 VIS PDs read-out | 749 | 999 | 1248 | counts |



Figure 10:

Optical Characteristics of AS7343L, AGAIN: 128x, Integration Time: 11 ms (unless otherwise noted)

| | | | | | Мах | Unit |
|-------------------------------|-------------------|--|-------|-------|-------|---------------------|
| valu | k ADC count le | Ee = 0 μW/cm ² AGAIN: 512x Integration time: 98 ms | | 0 | 5 | counts |
| | | AGAIN: 0.5x | 7.49 | 7.9 | 8.28 | |
| | _ | AGAIN: 1x | 15 | 15.8 | 16.5 | |
| | | AGAIN: 2x | 30 | 31.6 | 33.2 | See |
| | _ | AGAIN: 4x | 61 | 64 | 67 | note ⁽³⁾ |
| | _ | AGAIN: 8x | 117 | 124 | 130 | |
| o Onti | ical gain ratios, | AGAIN: 16x | 235 | 247 | 259 | |
| relation relation | tive to 64x gain | AGAIN: 32x | 0.475 | 0.5 | 0.525 | |
| setti | ing | AGAIN: 64x | | 1 | | |
| | _ | AGAIN: 128x | 1.9 | 2 | 2.1 | |
| | _ | AGAIN: 256x | 3.9 | 4.1 | 4.3 | |
| | _ | AGAIN: 512x | 8.1 | 8.6 | 9.1 | |
| | _ | AGAIN: 1024x | 15.2 | 16.9 | 18.6 | |
| | _ | AGAIN: 2048x | 28.2 | 34.75 | 41.3 | |
| ADC noise ⁽⁴⁾ | | White LED, 2700 K Integration time: 100 ms | | 0.05 | | % full scale |
| t _{int} Typi time | ical integration | ASTEP = 599 ATIME = 29 | | 50 | | ms |
| t _{ASTEP} Integ | gration time step | ASTEP = 999 | | 2.78 | | ms |
| h _{ca} Half | f cone angle | On the sensor | | 40 | | deg |

(1) The typical 3-sigma distribution is between 0 and 1 counts for AGAIN setting of 16x.

(2) The gain ratios are relative to 64x gain setting and are calculated relative to the response with integration time: 11 ms and AGAIN: 128x.

(3) ADC noise is calculated as the standard deviation of relative to full scale.

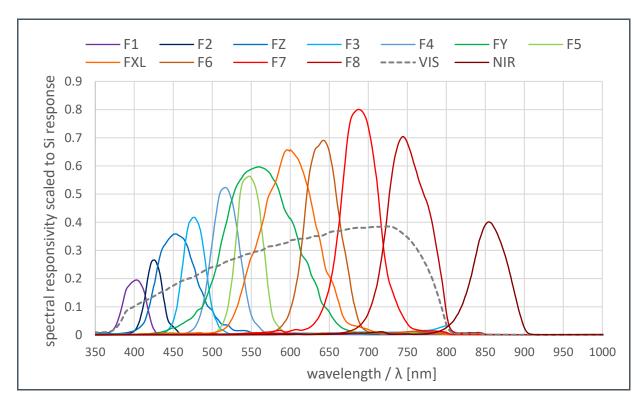
(4) Integration time, in milliseconds, is equal to: (ATIME + 1) x (ASTEP + 1) x 2.78 μs

(5) AGAIN ratio 0.5x to 16x is multiplied by 1000 for easier readability

7 Typical Operating Characteristics

Figure 11:

Typical Spectral Responsivity

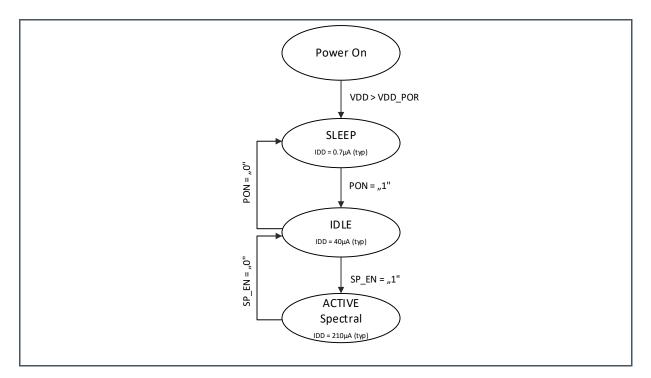


8 **Functional Description**

Upon power-up (POR), the device initializes. During initialization (typically 200 µs), the device will deterministically send NAK on I²C and cannot accept I²C transactions. All communication with the device must be delayed and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state, the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I²C transaction occurs during this state, the I²C core wakes up temporarily to service the communication. Once the Power ON bit, "PON", is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. Whenever the spectral measurement is enabled (SP_EN = "1") the device enters the ACTIVE state. If the spectral measurement is disabled (SP_EN = "0") the device returns to the IDLE state. The figure below describes a simplified state diagram and the typical supply currents in each state.

If Sleep after Interrupt is enabled (SAI = "1" in register 0xAC), the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP does not automatically change any of the register settings (e.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the SAI_ACTIVE bit is cleared (the status bit is in register 0xA7 and the clear status bit is in register 0xFA).

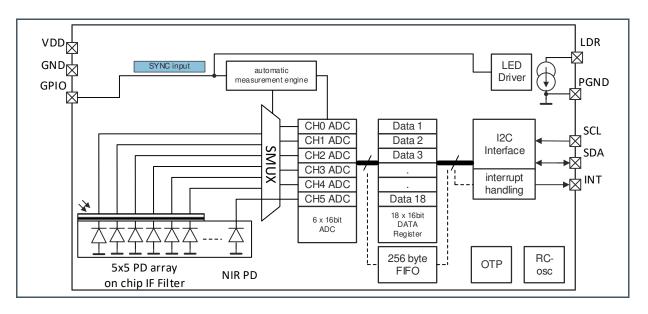
Figure 12: Simplified State Diagram



8.1 Device Architecture

The device features six independent 16-bit ADCs. Gain and integration time of the six ADCs can be adjusted with the I²C interface. A wait time can be programed to automatically set a delay between two consecutive spectral measurements and to reduce overall power consumption. Once a measurement is started, the device is automatically processing the channels and storing the measurement data on chip in the corresponding data registers.

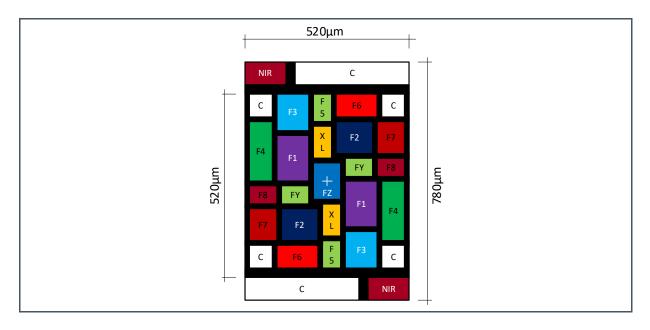
Figure 13: Simplified Block Diagram



8.2 Sensor Array

The device features a 5x5-photodiode array and two near- infrared response ("NIR") sense fields and two large clear photodiodes ("C").

Figure 14: Sensor Array



8.3 GPIO

The GPIO can be used synchronization input to start/stop the spectral measurement. It also allows synchronizing the LED driver (LDR) with an external start/stop signal. Default state of the GPIO is "output".

8.4 Interrupt (INT)

The interrupt (INT) can be used to define thresholds and read-out the device only when the channel threshold has been reached. The pin is active low.

8.5 LED Driver (LDR)

The LED driver is programmable and can be used to drive external LEDs. It is also possible to synchronize the LED driver with an external start/stop signal via pin GPIO.

9 I²C Interface

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1. All 16-bit fields have a latching scheme for reading and writing. In general, it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

9.1 I²C Address

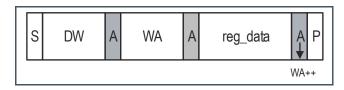
Figure 15: AS7343L I²C Slave Address

| Device | I ² C Address |
|---------|--------------------------|
| AS7343L | 0x39 |
| | |

9.2 I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP (P). Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (A/N) on the bus. If the slave transmits N, the master may issue a STOP.

Figure 16: I²C Byte Write

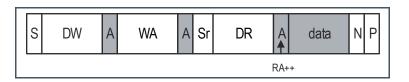




9.3 I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Figure 17: I²C Read



9.4 Timing Characteristics

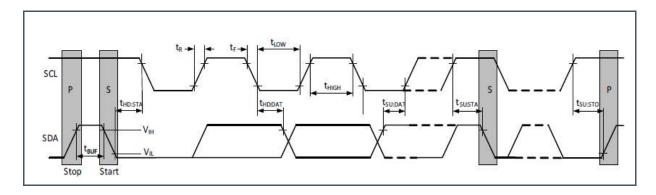
Figure 18:

I²C Timing Characteristics

| Symbol | Parameter | Min | Тур | Max | Unit |
|------------------|---|-----|-----|-----|------|
| f _{SCL} | I ² C clock frequency | | | 1 | MHz |
| tbuf | Bus free time between start and stop condition | 1.3 | | | |
| ths;sta | Hold time after (repeated) start condition. After this period, the first clock is generated. | 0.6 | | | |
| tsu;sta | Repeated start condition setup time | 0.6 | | | μs |
| tsu;sto | Stop condition setup time | 0.6 | | | |
| tLOW | SCL clock low period | 1.3 | | | |
| tніgн | SCL clock high period | 0.6 | | | |
| thd;dat | Data hold time | 0 | | | |
| tsu;dat | Data setup time | 100 | | | 20 |
| t⊧ | Clock/data fall time | | | 300 | ns |
| tR | Clock/data rise time | | | 300 | |

9.5 Timing Diagrams

Figure 19: I²C Slave Timing Diagram



10 Register Description

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide device control functions and can be read to determine device status and acquire device data.

The register set is summarized below. The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. Two-byte fields are always latched with the low byte followed by the high byte. The "Name" column illustrates the purpose of each register by highlighting the function associated to each bit. The bits are shown from MSB (D7) to LSB (D0). GRAY fields are reserved and their values must not be changed at any time.

In order to access registers from 0x60 to 0x74 bit REG_BANK in register CFG0 (0xA9) needs to be set to "1".

10.1 Register Overview

Figure 20: Register Overview

| Addr | Name | <d7></d7> | <d6></d6> | <d5></d5> | <d4></d4> | <d3></d3> | <d2></d2> | <d1></d1> | <d0></d0> |
|------|-----------|-----------------|----------------|-----------|-----------|------------|-----------|-------------|-----------|
| 0x58 | AUXID | | | | | | AUXID | [3:0] | |
| 0x59 | REVID | | | | | | | REVID [2:0] | |
| 0x5A | ID | | | | ID [| 7:0] | | | |
| 0x66 | CFG12 | | | | | | S | P_TH_CH [| 2:0] |
| 0x80 | ENABLE | | | | SMUXEN | WEN | | SP_EN | PON |
| 0x81 | ATIME | | | | ATIME | E [7:0] | | | |
| 0x83 | WTIME | | | | WTIMI | E [7:0] | | | |
| 0x84 | | | | | SP_TH_L | _LSB [7:0] | | | |
| 0x85 | - SP_TH_L | | | | SP_TH_L | MSB [7:0] | | | |
| 0x86 | | | | | SP_TH_H | _LSB [7:0] | | | |
| 0x87 | - SP_TH_H | | | | SP_TH_H_ | _MSB [7:0] | | | |
| 0x93 | STATUS | ASAT | | | | AINT | FINT | | SINT |
| 0x94 | ASTATUS | ASAT_ STATUS | | | | | AGAIN_STA | TUS [3:0] | |
| 0x95 | | | DATA_0_L [7:0] | | | | | | |
| 0x96 | - DATA_0 | | DATA_0_H [7:0] | | | | | | |
| 0x97 | | | DATA_1_L [7:0] | | | | | | |
| 0x98 | – DATA_1 | DATA_1_H [7:0] | | | | | | | |
| 0x99 | - DATA 2 | | | | DATA_2 | 2_L [7:0] | | | |
| 0x9A | DATA_2 | | | | DATA_2 | _H [7:0] | | | |

| $ \begin{array}{ c c c c } 0ATA,3 & OATA,3 L(7.0) & \\ \hline DATA,3 L(7.0) & \\ \hline DATA,4 L(7.0) & \\ \hline DATA,5 L(7.0) & \\ \hline DATA,5 L(7.0) & \\ \hline DATA,5 L(7.0) & \\ \hline DATA,6 & \\ \hline DATA,7 L(7.0) & \\ \hline DATA,7 L(7.0) & \\ \hline DATA,7 L(7.0) & \\ \hline DATA,8 & \\ \hline DATA,8 & \\ \hline DATA,8 & \\ \hline DATA,9 & \\ \hline DATA,11 & \\ \hline DATA,11 & \\ \hline DATA,11 & \\ \hline DATA,11 & \\ \hline DATA,12 & \\ \hline DATA,12 & \\ \hline DATA,12 & \\ \hline DATA,13 & \\ \hline DATA,13 & \\ \hline DATA,14 & \\ \hline DATA,14 & \\ \hline DATA,14 & \\ \hline DATA,15 & \\ \hline DATA,15 & \\ \hline DATA,16 & \\ \hline DATA,16 & \\ \hline DATA,17 & \\ \hline DATA,17 & \\ \hline DATA,17 & \\ \hline DATA,11 & \\ \hline DATA,12 & \\ \hline DATA,13 & \\ \hline DATA,13 & \\ \hline DATA,13 & \\ \hline DATA,13 & \\ \hline DATA,14 & \\ \hline DATA,13 & \\ \hline DATA,15 & \\ \hline DATA,16 & \\ \hline DATA,16 & \\ \hline \hline DATA,17 & \\ \hline DATA,18 & \\ \hline DATA,19 & \\ \hline DATA,19 & \\ \hline DATA,10 & \\ \hline DATA,10 & \\ \hline DATA,10 & \\ \hline DATA & \\ \hline DATA,10 & \\ \hline DATA & \\ $ | Addr | Name | <d7></d7> | <d6></d6> | <d5></d5> | <d4></d4> | <d3></d3> | <d2></d2> | <d1></d1> | <d0></d0> | |
|--|------|------------|-----------|-----------|-----------|----------------|-----------|-----------|-----------|-----------|--|
| $ \begin{array}{ c c c c } 0.473 &$ | 0x9B | | | | | DATA_3 | 8_L [7:0] | | | | |
| Ox9E DATA, 4 IP 20 0x96 DATA, 5 DATA, 5.L [7:0] DATA, 5.L [7:0] 0xA1 DATA, 5.L [7:0] DATA, 6.L [7:0] OATA, 6.L [7:0] 0xA2 DATA, 6.L [7:0] DATA, 6.L [7:0] OATA, 6.L [7:0] 0xA2 DATA, 7.L [7:0] DATA, 6.L [7:0] OATA, 7.L [7:0] 0xA4 DATA, 7.L [7:0] DATA, 7.L [7:0] OATA, 7.L [7:0] 0xA4 DATA, 9.L [7:0] DATA, 8.L [7:0] OATA, 8.L [7:0] 0xA7 DATA, 8.L [7:0] DATA, 8.L [7:0] OATA, 9.L [7:0] 0xA7 DATA, 9.L [7:0] DATA, 9.L [7:0] OATA, 9.L [7:0] 0xA7 DATA, 10.L [7:0] DATA, 10.L [7:0] OATA, 11.L [7:0] 0xA8 DATA, 12 DATA, 12.L [7:0] OATA, 12.L [7:0] 0xA8 DATA, 13 DATA, 14.L [7:0] OATA, 14.L [7:0] 0xA9 DATA, 14 DATA, 13.L [7:0] OATA, 14.L [7:0] 0xA8 DATA, 14 DATA, 14.L [7:0] OATA, 14.L [7:0] 0xA9 DATA, 14 DATA, 14.L [7:0] OATA, 14.L [7:0] 0xA9 | 0x9C | - DATA_3 | | | | DATA_3 | _H [7:0] | | | | |
| 0x96 DATA_4.H [7:0] 0x40 DATA_5.L [7:0] 0x41 DATA_6.H [7:0] 0x42 DATA_6.L [7:0] 0x43 DATA_7.L [7:0] 0x44 DATA_7.H [7:0] 0x45 DATA_7.H [7:0] 0x46 DATA_7.H [7:0] 0x47 DATA_8.H [7:0] 0x48 DATA_9.H [7:0] 0x47 DATA_9.H [7:0] 0x48 DATA_9.H [7:0] 0x49 DATA_9.H [7:0] 0x40 DATA_9.H [7:0] 0x41 DATA_9.H [7:0] 0x42 DATA_9.H [7:0] 0x44 DATA_9.H [7:0] 0x45 DATA_9.H [7:0] 0x46 DATA_10.L [7:0] 0x47 DATA_11.H [7:0] 0x48 DATA_11 0x41 DATA_11.H [7:0] 0x42 DATA_12.L [7:0] 0x44 DATA_12.H [7:0] 0x45 DATA_14.H [7:0] 0x46 DATA_14.H [7:0] 0x47 DATA_15.L [7:0] 0x48 DATA_14.H [7:0] 0x41 DATA_15.L [7:0] 0x42 DATA_15.H [7:0] 0x41 DATA_15.L [7:0] 0x41 DATA_15.H [7:0] 0x41 DATA_15.H [7:0] 0x42 | 0x9D | | | | | DATA_4 | L [7:0] | | | | |
| $ \begin{array}{ c c c c c } \hline DATA_5 & DATA_5 H(7:0) & \\ \hline DATA_6 & DATA_6 H(7:0) & \\ \hline DATA_7 L(7:0) & \\ \hline DATA_7 L(7:0) & \\ \hline DATA_7 L(7:0) & \\ \hline DATA_8 L(7:0) & \\ \hline DATA_9 & \\ \hline DATA_9 & \\ \hline DATA_9 H(7:0) & \\ \hline DATA_10 L(7:0) & \\ \hline DATA_111 L(7:0) & \\ \hline DATA_112 & \\ \hline DATA_12 L(7:0) & \\ \hline DATA_12 L(7:0) & \\ \hline DATA_12 H(7:0) & \\ \hline DATA_12 L(7:0) & \\ \hline DATA_13 & \\ \hline DATA_13 & \\ \hline DATA_13 & \\ \hline DATA_13 & \\ \hline DATA_14 & \\ \hline DATA_14 L(7:0) & \\ \hline DATA_15 L(7:0) & \\ \hline DATA_15 L(7:0) & \\ \hline DATA_15 L(7:0) & \\ \hline DATA_16 L(7:0) & \\ \hline DATA_16 H(7:0) & \\ \hline DATA_16 H(7:0) & \\ \hline DATA_17 & \\ \hline DATA_18 H(7:0) & \\ \hline CASS & CFG 0 & \\ \hline F & \\ CFG 0 & \\ \hline CV & \hline OV & \\ \hline CV & \hline POWER & \\ \hline REG & \\ \hline POWER & \\ \hline POWER & \\ \hline POWER & \\ \hline AAVLID & \\ \hline CASS & CFG 1 & \\ \hline \hline CV & \hline DATA & \\ \hline DA$ | 0x9E | - DATA_4 | | | | DATA_4_H [7:0] | | | | | |
| 0xA0 DATA_5_H[7:0] 0xA2 DATA_6_L[7:0] 0xA2 DATA_6_L[7:0] 0xA3 DATA_7 0xA4 DATA_7_L[7:0] 0xA5 DATA_8_H[7:0] 0xA6 DATA_8_H[7:0] 0xA7 DATA_8_H[7:0] 0xA8 DATA_9 0xA7 DATA_9_H[7:0] 0xA8 DATA_9_H[7:0] 0xA8 DATA_9_H[7:0] 0xA8 DATA_9_H[7:0] 0xA8 DATA_10_H[7:0] 0xA8 DATA_10_H[7:0] 0xA8 DATA_11_H[7:0] 0xA8 DATA_12_H[7:0] 0xA8 DATA_12_H[7:0] 0xA8 DATA_12_H[7:0] 0xA8 DATA_12_H[7:0] 0xA9 DATA_12_H[7:0] 0xA11_1_H[7:0] DATA_13_H[7:0] 0xA8 DATA_12_H[7:0] 0xA9 DATA_13_H[7:0] 0xA11_12_H[7:0] DATA_14_H[7:0] 0xA11_2_H[7:0] DATA_15_H[7:0] 0xB1 DATA_15_H[7:0] 0xB2 DATA_15_H[7:0] </td <td>0x9F</td> <td></td> <td></td> <td></td> <td></td> <td>DATA_5</td> <td>5_L [7:0]</td> <td></td> <td></td> <td></td> | 0x9F | | | | | DATA_5 | 5_L [7:0] | | | | |
| DATA_6 DATA_6, H [7:0] DATA_7, L [7:0] DATA_7, L [7:0] DATA_7, L [7:0] DATA_7, L [7:0] DATA_8 DATA_8, L [7:0] DATA_8 DATA_8, L [7:0] DATA DATA_8, L [7:0] DATA DATA_8, L [7:0] DATA DATA_8, L [7:0] DATA DATA_9, L [7:0] DATA DATA_9, L [7:0] DATA DATA_10, L [7:0] DAAA DATA_10, L [7:0] DATA_11 DATA_11, L [7:0] DAAA DATA_12, L [7:0] DATA_12 DATA_12, L [7:0] DATA_13 DATA_12, L [7:0] DATA_14 DATA_12, L [7:0] DATA DATA_12, L [7:0] DATA DATA_13, L [7:0] DATA DATA_13, L [7:0] DATA_13 DATA_14, L [7:0] DATA_14 DATA_14, H [7:0] DATA_15 DATA_15, L [7:0] DATA_14 DATA_15, L [7:0] DATA_15 DATA_16, L [7:0] DATA_16 DATA_16, L [7:0] DATA_16 <tdd< td=""><td>0xA0</td><td>- DATA_5</td><td></td><td></td><td></td><td>DATA_5</td><td>_H [7:0]</td><td></td><td></td><td></td></tdd<> | 0xA0 | - DATA_5 | | | | DATA_5 | _H [7:0] | | | | |
| 0xA2 DATA_6.H [7:0] 0xA3 DATA_7 DATA_7.L [7:0] 0xA4 DATA_7.H [7:0] | 0xA1 | | | | | DATA_6 | 6_L [7:0] | | | | |
| DATA_7 DATA_7, H(7.0) 0xA6 DATA_8 DATA_8, L(7.0) 0xA7 DATA_9 DATA_8, L(7.0) 0xA7 DATA_9 DATA_9, L(7.0) 0xA8 DATA_9, L(7.0) OATA_9, L(7.0) 0xA8 DATA_10 DATA_9, H(7.0) 0xA8 DATA_10, L(7.0) OATA_10, L(7.0) 0xA8 DATA_11 DATA_10, L(7.0) 0xA0 DATA_11 DATA_11, L(7.0) 0xA0 DATA_12 DATA_12, L(7.0) 0xA0 DATA_12 DATA_13, L(7.0) 0xA0 DATA_13 DATA_13, L(7.0) 0xA10 DATA_13, L(7.0) OATA_13, L(7.0) 0xA11 DATA_14 DATA_14, L(7.0) 0xA11 DATA_14, L(7.0) OATA_14, L(7.0) 0xA11 DATA_15, L(7.0) OATA_14, L(7.0) 0xA11 DATA_16, L(7.0) OATA_14, L(7.0) 0xA11 DATA_16, L(7.0) OATA_16, L(7.0) 0xA11 DATA_16, L(7.0) OATA_14, L(7.0) 0xA11 DATA_16, L(7.0) OATA_14, L(7.0) | 0xA2 | - DATA_6 | | | | DATA_6 | _H [7:0] | | | | |
| $ \begin{array}{ c c c c } 0xA4 & & & & & & & & & & & & & & & & & & &$ | 0xA3 | | | | | DATA_7 | ′_L [7:0] | | | | |
| DATA_8 DATA_8_H[7:0] DATA_9 DATA_8_H[7:0] DATA_9_L[7:0] DATA_9_L[7:0] DATA_0 DATA_9_L[7:0] DATA_10 DATA_9_L[7:0] DATA_10_L[7:0] DATA_10_L[7:0] DATA_11 DATA_11_L[7:0] DATA_11 DATA_11_L[7:0] DATA_12 DATA_12_L[7:0] DATA_13 DATA_13_L[7:0] DATA_13 DATA_13_L[7:0] DATA_14 DATA_14_L[7:0] DATA_14 DATA_14_L[7:0] DATA_14 DATA_14_L[7:0] DATA_14 DATA_14_L[7:0] DATA_15 DATA_14_L[7:0] OxAB DATA_14_L[7:0] OxB2 DATA_15_L[7:0] OxAB DATA_16_L[7:0] OxAB DATA_16_L[7:0] OxAB DATA_16_L[7:0] OxAB DATA_16_L[7:0] OxAB DATA_16_L[7:0] OxAB | 0xA4 | - DATA_/ | | | | DATA_7 | ′_H [7:0] | | | | |
| 0xA6 DATA_B_H[7:0] 0xA7 DATA_9 0xA8 DATA_9 0xA8 DATA_10 0xAA DATA_10_L[7:0] 0xAA DATA_10_L[7:0] 0xAA DATA_10_L[7:0] 0xAA DATA_10_H[7:0] 0xAA DATA_11_L[7:0] 0xAA DATA_12_H[7:0] 0xAA DATA_12_L[7:0] 0xAA DATA_12_H[7:0] 0xAA DATA_13_L[7:0] 0xAA DATA_14_14_[7:0] 0xAB DATA_14_14_[7:0] 0xB0 DATA_14 0xB1 DATA_15_H[7:0] 0xB2 DATA_14_14_[7:0] 0xB3 DATA_15_H[7:0] 0xB4 DATA_15_H[7:0] 0xB5 DATA_16_H[7:0] 0xB4 DATA_15_H[7:0] 0xB5 DATA_16_H[7:0] 0xB6 DATA_16_H[7:0] 0xB7 DATA_16_H[7:0] 0xB8 DATA_16_H[7:0] 0xB8 DATA_16_H[7:0] 0xB7 DATA_16_H[7:0] 0xB8 | 0xA5 | | | | | DATA_8 | B_L [7:0] | | | | |
| OxA8 DATA_9 DATA_9 H[7:0] 0xA9 DATA_10 IC7:0] IC7:0] 0xA8 DATA_11 IC7:0] IC7:0] 0xA8 DATA_11 IC7:0] IC7:0] 0xA0 DATA_11 IC7:0] IC7:0] 0xA8 DATA_11 IC7:0] IC7:0] 0xA0 DATA_12 IC7:0] IC7:0] 0xA8 DATA_12 IC7:0] IC7:0] 0xA8 DATA_13 IC7:0] IC7:0] 0xA8 DATA_14 IC7:0] IC7:0] 0xA9 DATA_15 IC7:0] IC7:0] 0xB1 DATA_15 IC7:0] IC7:0] 0xB2 DATA_15 IC7:0] IC7:0] 0xB3 DATA_15 IC7:0] IC7:0] 0xB4 DATA_16 IC7:0] IC7:0] 0xB6 DATA_16 IC7:0] IC7:0] 0xB6 DATA_16 IC7:0] IC7:0] 0xB7 DATA_17:1[7:0] IC7:0] IC7:0] | 0xA6 | - DATA_8 | | | | DATA_8 | _H [7:0] | | | | |
| 0xA8 DATA_9,H[7:0] 0xA9 DATA_10 DATA_10_L[7:0] 0xAA DATA_10_H[7:0] DATA_10_H[7:0] 0xAB DATA_11 DATA_11_L[7:0] DATA_11_L[7:0] 0xAC DATA_12 DATA_11_L[7:0] DATA_12_L[7:0] 0xAC DATA_12 DATA_12_L[7:0] TOTA_12_L[7:0] 0xAB DATA_13 DATA_13_L[7:0] TOTA_13_L[7:0] 0xAB DATA_14 DATA_14_L[7:0] TOTA_15_L[7:0] 0xB1 DATA_15 DATA_15_L[7:0] TOTA_15_L[7:0] 0xB2 DATA_15 DATA_15_L[7:0] TOTA_16_L[7:0] 0xB3 DATA_16 DATA_15_L[7:0] TOTA_16_L[7:0] 0xB4 DATA_15 DATA_16_L[7:0] TOTA_16_L[7:0] 0xB5 DATA_16 DATA_16_L[7:0] TOTA_16_L[7:0] 0xB6 DATA_16 DATA_17_L[7:0] TOTA_16_L[7:0] 0xB7 DATA_16_L[7:0] TOTA_16_L[7:0] TOTA_16_L[7:0] 0xB8 DATA_16 MAA_17_L[7:0] TOTA_16_L[7:0] 0xB8 STATUS 2 AVAL | 0xA7 | | | | | DATA_9 | 9_L [7:0] | | | | |
| OKAA DATA_10 DATA_10_H [7:0] 0xAA DATA_10_H [7:0] OATA_11_L [7:0] 0xAB DATA_11_L [7:0] DATA_11_L [7:0] 0xAC DATA_12 DATA_11_L [7:0] OATA_11_L [7:0] 0xAB DATA_12 DATA_12_L [7:0] OATA_13_L [7:0] 0xAB DATA_13 DATA_13_L [7:0] OATA_13_L [7:0] 0xAB DATA_14 DATA_14_L [7:0] OATA_15_L [7:0] 0xB1 DATA_15 DATA_15_L [7:0] OATA_15_L [7:0] 0xB2 DATA_15 DATA_15_L [7:0] OATA_15_L [7:0] 0xB3 DATA_15 DATA_16_L [7:0] OATA_16_L [7:0] 0xB4 DATA_16 DATA_16_L [7:0] OATA_16_L [7:0] 0xB5 DATA_17 DATA_16_L [7:0] OATA_16_L [7:0] 0xB6 DATA_17 DATA_17_L [7:0] OATA_17_L [7:0] 0x88 DATA_15 INT_SP_L SINT 0x90 STATUS 2 AVALID ASAT_ ASAT_ DIG ANA SINT 0x88 STATUS 3 INT_SP_H INT_SP_L SINT 0x | 0xA8 | - DATA_9 | | | | DATA_9 | _H [7:0] | | | | |
| DATA_10_H[7:0] DATA_11_[F:0] 0xAR DATA_11 [7:0] | 0xA9 | | | | | DATA_1 | 0_L [7:0] | | | | |
| OXAC DATA_11 TOTA_11 H [7:0] 0xAC DATA_12 DATA_12 L [7:0] DATA_12 H [7:0] 0xAE DATA_13 L [7:0] DATA_13 L [7:0] DATA_13 L [7:0] 0xB0 DATA_14 DATA_13 H [7:0] DATA_13 H [7:0] 0xB1 DATA_14 DATA_14_14 [7:0] DATA_14_14 [7:0] 0xB2 DATA_15 DATA_15_L [7:0] DATA_15_L [7:0] 0xB3 DATA_15 DATA_15_L [7:0] DATA_16_L [7:0] 0xB4 DATA_16_L [7:0] DATA_16_L [7:0] DATA_16_L [7:0] 0xB5 DATA_16 DATA_17_L [7:0] DATA_17_L [7:0] 0xB8 DATA_17 DATA_17_L [7:0] DATA_17_L [7:0] 0xB8 DATA_17 DATA_17_L [7:0] DATA_17_L [7:0] 0xB7 DATA_17 DATA_17_L [7:0] DATA_117_L [7:0] 0xB8 STATUS 2 AVALID ASAT_ASAT_DIG SINT_SMUX 0x90 STATUS 3 INT_SP_L SINT_SMUX SINT_SMUX 0x88 STATUS 4 FIFO_OV OVTEMP SP_TRIG SAI ACT | 0xAA | - DATA_10 | | | | DATA_1 | 0_H [7:0] | | | | |
| $ \begin{array}{c c c c c c } \hline 0xAC & DATA_11_{-}H[7:0] & \\ \hline DATA_12_{-}H[7:0] & \\ \hline DATA_12_{-}H[7:0] & \\ \hline DATA_12_{-}H[7:0] & \\ \hline DATA_13_{-}H[7:0] & \\ \hline DATA_13_{-}H[7:0] & \\ \hline DATA_13_{-}H[7:0] & \\ \hline DATA_14_{-}H[7:0] & \\ \hline DATA_14_{-}H[7:0] & \\ \hline DATA_14_{-}H[7:0] & \\ \hline DATA_15_{-}H[7:0] & \\ \hline DATA_15_{-}H[7:0] & \\ \hline DATA_15_{-}H[7:0] & \\ \hline DATA_16_{-}H[7:0] & \\ \hline DA$ | 0xAB | 5474 44 | | | | DATA_1 | 1_L [7:0] | | | | |
| OARE DATA_12 IT INT_SP_H INT_SP_H INT_SP_H INT_SP_L SINT_SMUX INT_BUS INT_BUS <th< td=""><td>0xAC</td><td>- DATA_11</td><td></td><td></td><td></td><td>DATA_1</td><td>1_H [7:0]</td><td></td><td></td><td></td></th<> | 0xAC | - DATA_11 | | | | DATA_1 | 1_H [7:0] | | | | |
| DATA_12_H [7:0] DATA_13_L DATA_13_L [7:0] 0x80 DATA_13_L [7:0] DATA_13_L [7:0] 0x80 DATA_13_H [7:0] DATA_13_H [7:0] 0x81 DATA_14_L [7:0] DATA_14_L [7:0] 0x82 DATA_14 DATA_14_H [7:0] DATA_14_H [7:0] 0x83 DATA_15 DATA_15_L [7:0] DATA_15_L [7:0] 0x84 DATA_16 DATA_16_L [7:0] DATA_16_L [7:0] 0x85 DATA_16 DATA_16_L [7:0] DATA_16_L [7:0] 0x86 DATA_16 DATA_17_L [7:0] DATA_17_L [7:0] 0x87 DATA_17_L [7:0] DATA_17_L [7:0] DATA_17_L [7:0] 0x88 DATA_17 DATA_17_L [7:0] DATA_17_L [7:0] 0x89 STATUS 2 AVALID ASAT_ ASAT_ DIG ANA SNIT 0x90 STATUS 3 INT_SP_H INT_SP_L V V 0x88 STATUS 4 FIFO_ OV OVTEMP SP_TRIG ACT INT_BUS ACT 0x88 STATUS 4 FIFO_ OV OVTEMP SP_TRIG ACT INT_BUS ACT 0x88 | 0xAD | | | | | DATA_1 | 2_L [7:0] | | | | |
| $ \begin{array}{c c c c c c c c } \hline DATA_13 & & & & & & & & & & & & & & & & & & &$ | 0xAE | - DATA_12 | | | | DATA_1 | 2_H [7:0] | | | | |
| OxB0 DATA_13_H [7:0] OxB1 DATA_14 [7:0] OxB2 DATA_14_L [7:0] DATA_14_L [7:0] OxB3 DATA_15 [7:0] OxB4 DATA_15_L [7:0] DATA_15_L [7:0] OxB5 DATA_16 [7:0] OxB6 DATA_16_L [7:0] Image: Comparison of the state of t | 0xAF | | | | | DATA_1 | 3_L [7:0] | | | | |
| DATA_14 DATA_14_H [7:0] 0xB3 DATA_15 DATA_15_L [7:0] 0xB4 DATA_15 DATA_15_L [7:0] 0xB5 DATA_16 DATA_16_L [7:0] 0xB6 DATA_16_L [7:0] DATA_16_L [7:0] 0xB7 DATA_16_H [7:0] DATA_16_H [7:0] 0x88 DATA_17_L [7:0] DATA_17_L [7:0] 0x90 STATUS 2 AVALID ASAT ASAT DIG ANA 0x91 STATUS 3 INT_SP_H INT_SP_L 0xB8 STATUS 5 SINTSMUX SINTSMUX 0xBC STATUS 4 FIFOOV OVTEMP SP_TRIG SAI INT_BUSY 0xBF CFG 0 LOW POWER REG BANK WLONG WLONG VLONG | 0xB0 | - DATA_13 | | | | DATA_1 | 3_H [7:0] | | | | |
| $\begin{array}{c c c c c c c c } \hline OXB2 & DATA_14 \ H \ [7:0] \\ \hline OXB3 \\ OXB4 \\ \hline DATA_15 \\ \hline OXB4 \\ \hline DATA_15 \\ \hline OXB5 \\ OXB6 \\ \hline DATA_16 \\ \hline DATA_16 \ H \ [7:0] \\ \hline DATA_17 \ H \ [7:0$ | 0xB1 | 5474 44 | | | | DATA_1 | 4_L [7:0] | | | | |
| OxB4 DATA_15 DATA_15_H [7:0] 0xB5 DATA_16 DATA_15_H [7:0] 0xB6 DATA_16 DATA_16_L [7:0] 0xB7 DATA_17_L [7:0] DATA_17_L [7:0] 0xB8 DATA_17 DATA_17_L [7:0] 0x90 STATUS 2 AVALID ASATASATASAT 0x91 STATUS 3 INT_SP_H INT_SP_L 0x88 STATUS 5 INT_SP_H INT_SP_L 0x88 STATUS 4 FIFO | 0xB2 | - DATA_14 | | | | DATA_1 | 4_H [7:0] | | | | |
| OxB4 DATA_15_H [7:0] OxB5 DATA_16 L [7:0] OxB6 DATA_16 L [7:0] OxB7 DATA_17 DATA_16_H [7:0] OxB8 DATA_17 DATA_17_L [7:0] OxB8 DATA_17 DATA_17_L [7:0] Ox90 STATUS 2 AVALID ASAT_ ASAT_ DIG ANA Ox91 STATUS 3 INT_SP_H INT_SP_L Ox88 STATUS 5 SINT _SMUX Ox88 STATUS 4 FIFO_ OV Ox87 OVTEMP REG_ BANK Ox88 CFG 0 UND POWER Ox66 CFG1 INT_SP_K | 0xB3 | D.4.7.4.7 | | | | DATA_1 | 5_L [7:0] | | | | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | 0xB4 | - DATA_15 | | | | DATA_1 | 5_H [7:0] | | | | |
| Ox86 DATA_16_H [7:0] Ox87 DATA_17 Ox88 DATA_17 Ox88 DATA_17_H [7:0] Ox90 STATUS 2 AVALID ASATASATDIGANA Ox91 STATUS 3 INT_SP_H INT_SP_L Ox88 STATUS 5 INT_SP_H INT_SP_L Ox88 STATUS 4 FIFO | 0xB5 | | | | | DATA_1 | 6_L [7:0] | | | | |
| DATA_17 DATA_17 DATA_17_H [7:0] 0x88 STATUS 2 AVALID ASAT_ ASAT_ DIG ANA 0x90 STATUS 3 INT_SP_H INT_SP_L 0x8B STATUS 5 INT_SP_H INT_SP_L 0x8C STATUS 4 FIFO_ OV OVTEMP SP_TRIG SAI_ ACT INT_BUS Y 0x8F CFG 0 Image: Status 4 Image: Status 4 Image: Status 4 REG_ POWER BANK WLONG Image: Status 4 0x66 CFG1 Image: Status 4 | 0xB6 | - DATA_16 | | | | DATA_1 | 6_H [7:0] | | | | |
| Ox88 DATA_17_H [7:0] Ox90 STATUS 2 AVALID ASAT_DIG ASAT_ANA Ox91 STATUS 3 INT_SP_H INT_SP_L INT_SP_L Ox88 STATUS 5 INT_SP_H INT_SP_L SINT_SMUX Ox88 STATUS 4 FIFO_OV OVTEMP SP_TRIG SAL_ACT INT_BUS Ox86 STATUS 4 FIFO_OV OVTEMP REG_BANK WLONG INT_BUS Ox86 CFG 0 Image: Status 4 FIFO_OV SP_TRIG SAL_ACT INT_BUS Ox86 CFG 1 Image: Status 4 STATUS 5 < | 0xB7 | D.4.7.4 (- | | | | DATA_1 | 7_L [7:0] | | | | |
| OX90 STATUS 2 AVALID DIG ANA OX91 STATUS 3 INT_SP_H INT_SP_L OXBB STATUS 5 INT_SP_H INT_SP_L OxBC STATUS 4 FIFO_ OV OVTEMP INT_SP_H OxBF CFG 0 INT_SP_H REG_ POWER SAL OxC6 CFG1 INT_SP_H INT_SP_L | 0xB8 | - DATA_1/ | | | | DATA_1 | 7_H [7:0] | | | | |
| 0xBB STATUS 5 0xBC STATUS 4 FIFO_ OV OVTEMP 0xBF CFG 0 0xC6 CFG1 | 0x90 | STATUS 2 | | AVALID | | | | | | | |
| 0xBB STATUS 5 | 0x91 | STATUS 3 | | | INT_SP_H | INT_SP_L | | | | | |
| OXBC STATUS 4 OV OVTEMP SP_TRIG ACT Y 0xBF CFG 0 LOW_ POWER REG_ BANK WLONG V 0xC6 CFG1 V ACT Y | 0xBB | STATUS 5 | | | | | | | | | |
| OXBF CFG 0 POWER BANK WLONG 0xC6 CFG1 AGAIN[4:0] | 0xBC | STATUS 4 | | | OVTEMP | | | SP_TRIG | | | |
| | 0xBF | CFG 0 | | | | | | WLONG | | | |
| 0xC7 CFG3 SAI | 0xC6 | CFG1 | | | | | AC | GAIN[4:0] | | | |
| | 0xC7 | CFG3 | | | | SAI | | | | | |

| Addr | Name | <d7></d7> | <d6></d6> | <d5></d5> | <d4></d4> | <d3></d3> | <d2></d2> | <d1></d1> | <d0></d0> |
|------|------------------|-------------|-----------|--------------|---------------|-----------------|----------------|--------------|-------------------|
| 0xF5 | CFG6 | | | | | MUX_ ID[4:3] | | | |
| 0xC9 | CFG8 | FIFO_TH [| 7:6] | | | | | | |
| 0xCA | CFG9 | | | | SIEN _SMUX | | | | |
| 0x65 | CFG10 | | | | | | | | |
| 0xCF | PERS | | | | | | APERS | [3:0] | |
| 0x6B | GPIO | | | | | GPIO_ INV | GPIO_ IN_EN | GPIO_ OUT | GPIO_ IN |
| 0xD4 | ACTED | | | | ASTE | P [7:0] | | | |
| 0xD5 | ASTEP | | | | ASTEI | P [15:8] | | | |
| 0xD6 | CFG20 | | auto | _SMUX | | | | | |
| 0xCD | LED | LED_AC T | | | LE | D_DRIVE [6:0] | | | |
| 0xD7 | AGC_GAIN_ MAX | | AGC_FD_ | GAIN_MAX [7: | 4] | | | | |
| 0xDE | AZ_CONFIG | | | | AT_NTH_ITE | RATION [7:0] | | | |
| 0xF9 | INTENAB | ASIEN | | | | SP_IEN | FIEN | | SIEN |
| 0xFA | CONTROL | | | | | SW_ RESET | SP_MAN _AZ | FIFO_ CLR | CLEAR_ SAI_ACT |
| 0xFC | FIFO_MAP | | F | FIFO_WRITE_C | CH5_DATA – F | IFO_WRITE_CH | 10_DATA [6:1 |] | ASTATU S |
| 0xFD | FIFO_LVL | | | | FIFO_L | .VL [7:0] | | | |
| 0xFE | - FDATA | | | | FDATA | _L[7:0] | | | |
| 0xFF | | | | | FDATA | _H [15:8] | | | |



10.2 Detailed Register Description

For easier readability, the detailed register description is done in groups of registers related to dedicated device functions. This is not necessarily related to its register address.

Explanation of register access abbreviations: RW = read or write R = read only W = write only SC = self-clearing after access

10.2.1 Enable and Configuration Registers

The following registers are needed to power up and configure the device. To operate the device set bit PON = "1" first (register 0x80) after that configure the device and enable interrupts before setting $SP_EN = "1"$. Changing configuration while $SP_EN = "1"$ may result in invalid results.

ENABLE Register (Address 0x80)

Figure 21: ENABLE Register

| Addr: | 0x80 | ENABLE | ENABLE | | | |
|-------|----------|---------|--------|---|--|--|
| Bit | Bit Name | Default | Access | Bit Description | | |
| 7:5 | Reserved | 0 | RW | Reserved | | |
| 4 | SMUXEN | 0 | RW | SMUX Enable. 1: Starts SMUX command Note: This bit gets cleared automatically as soon as SMUX operation is finished | | |
| 3 | WEN | 0 | RW | Wait Enable. 0: Wait time between two consecutive spectral measurements disabled 1: Wait time between two consecutive spectral measurements enabled | | |
| 2 | Reserved | 0 | RW | Reserved | | |
| 1 | SP_EN | 0 | RW | Spectral Measurement Enable. 0: Spectral Measurement Disabled 1: Spectral Measurement Enabled | | |
| 0 | PON | 0 | RW | Power ON. 0: AS7343L disabled 1: AS7343L enabled Note: When bit is set, internal oscillator is activated, allowing timers and ADC channels to operate. | | |



GPIO Register (Address 0x6B)

Figure 22: GPIO Register

| Addr: | 0x6B | GPIO | GPIO | | |
|-------|------------|---------|--------|--|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:4 | Reserved | 0 | | Reserved | |
| 3 | GPIO_INV | 0 | RW | GPIO Invert. If set, the GPIO output is inverted. | |
| 2 | GPIO_IN_EN | 0 | RW | GPIO Input Enable. If set, the GPIO pin accepts a non-floating input. | |
| 1 | GPIO_OUT | 1 | RW | GPIO Output. If set, the output state of the GPIO is active directly. | |
| 0 | GPIO_IN | 0 | R | GPIO Input. Indicates the status of the GPIO input if GPIO_IN_EN is set. | |

LED Register (Address 0xCD)

Figure 23: LED Register

| Addr: 0xCD | | LED | LED | | |
|------------|-----------|----------|--------|---|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7 | LED_ACT | 0 | RW | LED Control. 0: External LED connected to pin LDR off 1: External LED connected to pin LDR on | |
| 6:0 | LED_DRIVE | 000 0100 | RW | LED Driving Strength. 000 0000: 4 mA 000 0001: 6 mA 000 0010: 8 mA 000 0011: 10 mA 000 0100: 12 mA 111 1110: 256 mA 111 1111: 258 mA | |



INTENAB Register (Address 0xF9)

Figure 24:

INTENAB Register

| Addr: | 0xF9 | INTENAB | INTENAB | | |
|-------|----------|---------|---------|--|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7 | | 0 | BW | Spectral and Flicker Detect Saturation Interrupt Enable. | |
| 7 | ASIEN | 0 | | When asserted permits saturation interrupts to be generated. | |
| 6:4 | Reserved | | | Reserved | |
| | | | | Spectral Interrupt Enable. | |
| 3 | SP_IEN | 0 | RW | When asserted permits interrupts to be generated, subject to the spectral thresholds and persistence filter. Bit is mirrored in the ENABLE register. | |
| | | | | FIFO Buffer Interrupt Enable. | |
| 2 | F_IEN | 0 | RW | When asserted permits interrupt to be generated when FIFO_LVL exceeds the FIFO threshold condition. | |
| 1 | Reserved | 0 | | Reserved | |
| | | | | System Interrupt Enable. | |
| 0 | SIEN | | RW | When asserted permits system interrupts to be generated. Indicates that flicker detection status has changed or SMUX operation has finished. | |

CONTROL Register (Address 0xFA)

Figure 25: CONTROL Register

| Addr: | 0xFA | CONTROL | | |
|-------|---------------|---------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:4 | Reserved | 0 | | Reserved |
| 3 | SW_RESET | 0 | RW | Software Reset. When set the device will force a power on reset. |
| 2 | SP_MAN_AZ | 0 | RW | Spectral Engine Manual Autozero. Starts a manual autozero of the spectral engines. Set SP_EN = 0 before starting a manual autozero for it to work. |
| 1 | FIFO_CLR | 0 | RW | FIFO Buffer Clear. Clears all FIFO data, FINT, FIFO_OV, and FIFO_LVL. |
| 0 | CLEAR_SAI_ACT | 0 | RW | Clear Sleep-After-Interrupt Active. Clears SAI_ACTIVE, ends sleep, and restarts device operation. |

10.2.2 ADC Timing Configuration / Integration Time

The integration time is set using the ATIME (0x81) and ASTEP (0xD4, 0xD5) registers. The integration time, in milliseconds, is equal to:

Equation 1: Setting the integration time

 $t_{int} = (ATIME + 1) \times (ASTEP + 1) \times 2.78 \mu s$

It is not allowed that both settings -ATIME and ASTEP - are set to "0".

The integration time also defines the full-scale ADC value, which is equal to:

Equation 2: ADC full scale value²

 $ADC_{fullscale} = (ATIME + 1) \times (ASTEP + 1)$

ATIME Register (Address 0x81)

Figure 26: ATIME Register

| Addr: | 0x81 | ATIME | | | |
|-------|----------|---------|--------|-------------------------------------|-------------------------------------|
| Bit | Bit Name | Default | Access | Bit Description | on |
| | | | | Integration Time Sets the number | of integration steps from 1 to 255. |
| | | | | Value | Integration Time |
| 7:0 | ATIME | 0x00 | RW | 0 | ASTEP |
| | | | | n | ASTEP x (n+1) |
| | | | | 255 | ASTEP x 256 |

² The maximum ADC count is 65535. Any ATIME/ASTEP field setting resulting in higher ADC full-scale values would result in a full-scale of 65535.



ASTEP Register (Address 0xD4, 0xD5)

Figure 27: ASTEP Register

| Addr: 0xD4, 0xD5 | | ASTEP | ASTEP | | | | |
|------------------|------------|---------|--------|---|----------------------|--|--|
| Bit | Bit Name | Default | Access | Bit Descriptio | on | | |
| | | | RW | Integration Time Step Size. Sets the integration time per step in increments of $2.78 \ \mu s$. The default value is 999. | | | |
| 7:0 | ASTEP 0xCA | | | VALUE | STEP SIZE | | |
| | | | | 0 | 2.78 μs | | |
| | | 999 | | n | 2.78 μs x (n+1) | | |
| | | | | 599 | 1.67 ms | | |
| | | | | 999 | 2.78 ms | | |
| 15:8 | ASTEP 0xCB | | | 17999 | 50 ms | | |
| | | | | 65534 | 182 ms | | |
| | | | | 65535 | Reserved, do not use | | |

WTIME Register (Address 0x83)

If wait is enabled (WEN = "1" register 0x80), each new measurement is started based on WTIME. It is necessary for WTIME to be sufficiently long for spectral integration and any other functions to be completed within the period. The device will warn the user if the timing is configured incorrectly. If WTIME is too short, then SP_TRIG in register STATUS6 (ADDR: 0xA7) will be set to "1".

Figure 28: WTIME Register

| Addr: 0x83 WTIME | | | | | | |
|------------------|----------|---------|--------|---------------|---|-----------------|
| Bit | Bit Name | Default | Access | Bit Dese | cription | |
| | | | | 8-bit value t | easurement Wait Tir o specify the delay be spectral measureme | etween two |
| | | 0×00 | RW | Value | Wait Cycles | Wait Time |
| 7:0 | WTIME | | | 0x00 | 1 | 2.78 ms |
| | | | | 0x01 | 2 | 5.56 ms |
| | | | | n | n | 2.78 ms x (n+1) |
| | | | | 0xff | 256 | 711 ms |



10.2.3 ADC Configuration

The following registers provide configuration for the 6 integrated ADCs (CH0 to CH5). It is possible to adjust the gain and setup the auto zero compensation for the ADCs.

CFG1 Register (Address 0xC6)

Figure 29: CFG1 Register

| Addr: 0xC6 | | CFG1 | CFG1 | | | | |
|------------|----------|---------|--------|--------------------------------------|-------|--|--|
| Bit | Bit Name | Default | Access | Bit Description | on | | |
| 7:5 | Reserved | 0 | | Reserved | | | |
| | | | | Spectral Engine Sets the spectral | | | |
| | | | | VALUE | GAIN | | |
| | | | | 0 | 0.5x | | |
| | | | | 1 | 1x | | |
| | | | | 2 | 2x | | |
| | | | | 3 | 4x | | |
| | | | 514 | 4 | 8x | | |
| 4:0 | AGAIN | 9 | RW | 5 | 16x | | |
| | | | | 6 | 32x | | |
| | | | | 7 | 64x | | |
| | | | | 8 | 128x | | |
| | | | | 9 | 256x | | |
| | | | 10 | 512x | | | |
| | | | | 11 | 1024x | | |
| | | | | 12 | 2048x | | |

AZ_CONFIG Register (Address 0xDE)

The following register configures how often the spectral engine offsets are reset (auto zero) to compensate for changes of the device temperature. The typical time auto zero needs to be completed is 15 ms.



Figure 30:

AZ_CONFIG Register

| Addr: 0xDE | | AZ_CONFIG | | | |
|------------|------------------|-----------|--------|---------------|--|
| Bit | Bit Name | Default | Access | Bit Desc | ription |
| | | 255 | | Sets the free | D FREQUENCY. quency at which the device performs auto spectral engines. |
| | | | RW | VALUE | AUTOZERO FREQUENCY |
| | | | | 0 | Never (not recommended) |
| 7:0 | AZ_NTH_ITERATION | | | 1 | Every integration cycle |
| | | | | 2 | Every 2 cycles |
| | | | | | Every "AZ_NTH_ITERATION" cycle |
| | | | | 254 | Every 254 cycles |
| | | | | 255 | Only before first measurement cycle |

CFG8 Register (Address 0xC9)

Figure 31: CFG8 Register

| Addr: 0xC9 | | CFG8 | CFG8 | | | |
|------------|----------|---------|--|----------------|----------|--|
| Bit | Bit Name | Default | Access | Bit Descriptio | n | |
| | | | FIFO Threshold. Sets a threshold on the FIFO level that triggers the first FIFO buffer interrupt (FINT). | | | |
| | | | 2 RW | VALUE | FIFO_LVL | |
| 7:6 | FIFO_TH | 2 | | 0 | 1 | |
| | | | | 1 | 4 | |
| | | | | 2 | 8 | |
| | | | | 3 | 16 | |
| 5:0 | Reserved | 0 | | Reserved | | |



10.2.4 Device Identification

The following registers provided device identification. Device ID, revision ID and auxiliary ID are read only.

AUXID Register (Address 0x58)

Figure 32: AUXID Register

| Addr: (| 0x58 | AUXID | | |
|---------|----------|---------|--------|---------------------------|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:4 | Reserved | | | Reserved |
| 3:0 | AUXID | 0000 | R | Auxiliary Identification. |

REVID Register (Address 0x59)

Figure 33: REVID Register

| Addr: 0x59 | | REVID | | |
|------------|----------|---------|--------|---------------------------------|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:3 | Reserved | | | Reserved |
| 2:0 | REV_ID | 000 | R | Revision Number Identification. |

ID Register (Address 0x5A)

Figure 34: ID Register

| Addr: 0x5A | | ID | | |
|------------|----------|----------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | ID | 10000001 | R | Part Number Identification. Value 10000001 |





10.2.5 Spectral Interrupt Configuration

The spectral interrupt threshold registers provide 16-bit values to be used as the high and low thresholds for comparison to the 16-bit CH0_DATA values (ADC CH0). If SP_IEN (register 0xF9) is enabled and CH0_DATA is not between the two thresholds for the number of consecutive measurements specified in APERS (register 0xBD) an interrupt is set.

SP_TH_L_LSB Register (Address 0x84)

Figure 35: SP_TH_L_LSB Register

| Addr: 0x84 | | SP_TH_L_ | SP_TH_L_LSB | | |
|------------|-------------|----------|-------------|---|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:0 | SP_TH_L_LSB | 0x00 | RW | Spectral Low Threshold LSB. This register provides the low byte of the low interrupt threshold (CH0). | |

SP_TH_L_MSB Register (Address 0x85)

Figure 36: SP_TH_L_MSB Register

| Addr: 0x85 | | SP_TH_L_MSB | | |
|------------|-------------|-------------|--------|--|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | SP_TH_L_MSB | 0x00 | RW | Spectral Low Threshold MSB. This register provides the high byte of the low interrupt threshold (CH0). Both SP_TH_L registers are combined to a 16-bit threshold. If the value captured by channel 0 is below the low threshold and the APERS value is reached the bit SP_IEN is set and an interrupt is generated. There is an 8-bit data latch implemented that stores the written low byte until the high byte is written. Both bytes will be applied at the same time to avoid an invalid threshold. Note: The LSB register cannot be changed without writing to the MSB register. It is recommended to write to SP_TH_L_SB and SP_TH_L_MSB within one I²C command. |



SP_TH_H_LSB Register (Address 0x86)

Figure 37:

SP_TH_H_LSB Register

| Addr: 0x86 | | SP_TH_H_ | SP_TH_H_LSB | | |
|------------|-------------|----------|-------------|---|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:0 | SP_TH_H_LSB | 0x00 | RW | Spectral High Threshold LSB. This register provides the low byte of the high interrupt threshold (CH0). | |

SP_TH_H_MSB Register (Address 0x87)

Figure 38:

SP_TH_H_MSB Register

| Addr: 0x87 | | SP_TH_H_ | SP_TH_H_MSB | | |
|------------|-------------|----------|-------------|---|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| | | | | Spectral High Threshold MSB. This register provides the high byte of the high interrupt threshold (CH0). | |
| 7:0 | SP_TH_H_MSB | 0x00 | RW | Both SP_TH_H registers are combined to a 16-bit threshold. If the value captured by channel 0 is above the high threshold and the APERS value is reached the bit SP_IEN is set and an interrupt is generated. | |

CFG12 Register (Address 0x66)

Figure 39: CFG12 Register

| Addr: 0x66 | | CFG12 | CFG12 | | | |
|------------|----------|---------|--------|---|---------|--|
| Bit | Bit Name | Default | Access | Bit Descriptio | 'n | |
| 7:3 | Reserved | 0 | | Reserved | | |
| | | | | Spectral Threshold Channel. Sets the channel used for interrupts and persister if enabled, to determine device status and gain settings. | | |
| 2:0 | SP_TH_CH | 0 | RW | VALUE | CHANNEL | |
| | | | | 0 | CH0 | |
| | | | | 1 | CH1 | |
| | | | | 2 | CH2 | |



| Addr: 0x66 | | CFG12 | | | | |
|------------|----------|---------|--------|-----------------|-----|--|
| Bit | Bit Name | Default | Access | Bit Description | on | |
| | | | | 3 | CH3 | |
| | | | | 4 | CH4 | |
| | | | | 5 | CH5 | |

10.2.6 Device Status Registers

The following registers provide status of the device and indicate details about saturation, interrupts, over temperature, device execution and ambient light flicker detection.

STATUS Register (Address 0x93)

The primary status register for AS7343L indicates if there are saturation or interrupt events that need to be handled by the user. This register is self-clearing, meaning that writing a "1" to any bit in the register clears that status bit. In this way, the user should read the STATUS register, handle all indicated event(s) and then write the register value back to STATUS to clear the handled events. Writing "0" will not clear those bits if they have a value of "1", which means that new events that occurred since the last read of the STATUS register will not be accidentally cleared. In case channel saturation has happened (ASAT) it is recommended to discard the measurement results and reconfigure device configuration such as AGAIN and Integration Time to avoid saturation.

Figure 40: STATUS Register

| Addr: 0x93 | | STATUS | STATUS | | |
|------------|----------|---------|--------|--|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7 | ASAT | 0 | R, SC | Spectral and Flicker Detect Saturation. If ASIEN is set, indicates Spectral saturation. Check STATUS2 register to distinguish between analog or digital saturation. | |
| 6:4 | Reserved | 0 | R | Reserved | |
| 3 | AINT | 0 | R, SC | Spectral Channel Interrupt. If SP_IEN is set, indicates that a spectral event that met the programmed thresholds and persistence (APERS) occurred. | |
| 2 | FINT | 0 | R, SC | FIFO Buffer Interrupt. If FIEN is set, indicates that the FIFO_LVL fulfills the threshold condition. If cleared by writing 1, the interrupt will be asserted again as more data is collected. To fully clear this interrupt, all data must be read from the FIFO buffer. | |
| 1 | Reserved | 0 | R | Reserved | |
| 0 | SINT | 0 | R, SC | System Interrupt. | |

| Addr: 0x93 | | STATUS | STATUS | | |
|------------|----------|---------|--------------------------------|---|--|
| Bit | Bit Name | Default | Default Access Bit Description | | |
| | | | | If SIEN is set, indicates that system interrupt is set. Refer to Status5 register. | |

STATUS 2 Register (Address 0x90)

Figure 41: STATUS 2 Register

| Addr: 0x90 | | STATUS 2 | STATUS 2 | | |
|------------|--------------|----------|----------|--|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7 | Reserved | 0 | | Reserved | |
| 6 | AVALID | 0 | R | Spectral Valid. Indicates that the spectral measurement has been completed | |
| 5 | Reserved | 0 | | Reserved | |
| 4 | ASAT_DIGITAL | 0 | R | Digital Saturation . Indicates that the maximum counter value has been reached. Maximum counter value depends on integration time set in the ATIME register. | |
| 3 | ASAT_ANALOG | 0 | R | Analog Saturation. Indicates that the intensity of ambient light has exceeded the maximum integration level for the spectral analog circuit. | |
| 2:0 | Reserved | 0 | R | Reserved | |

STATUS 3 Register (Address 0x91)

Figure 42: STATUS 3 Register

| Addr: 0x91 | | STATUS 3 | STATUS 3 | | |
|------------|----------|----------|----------|---|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:6 | Reserved | 0 | | Reserved | |
| 5 | INT_SP_H | 0 | R | Spectral Interrupt High. Indicates that a spectral interrupt occurred because the data exceeded the high threshold. | |
| 4 | INT_SP_L | 0 | R | Spectral Interrupt Low. Indicates that a spectral interrupt occurred because the data is below the low threshold. | |
| 3:0 | Reserved | 0 | | Reserved | |



STATUS 5 Register (Address 0xBB)

Figure 43:

STATUS 5 Register

| Addr: 0xBB | | STATUS 5 | STATUS 5 | | | |
|------------|-----------|----------|----------|--|--|--|
| Bit | Bit Name | Default | Access | Bit Description | | |
| 7:3 | Reserved | 0 | | Reserved | | |
| 2 | SINT_SMUX | 0 | R | SMUX Operation Interrupt. Indicates that SMUX command execution has finished. | | |
| 1:0 | Reserved | 0 | | Reserved | | |

STATUS 4 Register (Address 0xBC)

Figure 44: STATUS 4 Register

| Addr: 0xBC | | STATUS 4 | STATUS 4 | | |
|------------|------------|----------|------------------------------|---|--|
| Bit | Bit Name | Default | fault Access Bit Description | | |
| 7 | FIFO_OV | 0 | R | FIFO Buffer Overflow. Indicates that the FIFO buffer overflowed and information has been lost. Bit is automatically cleared when the FIFO buffer is read | |
| 6 | Reserved | 0 | R | Reserved | |
| 5 | OVTEMP | 0 | R | Over Temperature Detected. Indicates the device temperature is too high. Write 1 to clear this bit. | |
| 4:3 | Reserved | 0 | | Reserved | |
| 2 | SP_TRIG | 0 | R | Spectral Trigger Error. Indicates that there is a timing error. The WTIME is too short for the selected ATIME. | |
| 1 | SAI_ACTIVE | 0 | R | Sleep after Interrupt Active. Indicates that the device is in SLEEP due to an interrupt. To exit SLEEP mode, clear this bit. | |
| 0 | INT_BUSY | 0 | R | Initialization Busy. Indicates that the device is initializing. This bit will remain 1 for about 300 μ s after power on. Do not interact with the device until initialization is complete. | |



10.2.7 Spectral Data and Status

The ASTATUS register provides saturation and gain status associated to each set of spectral data. Reading the ASTATUS register (0x94) latches all 36 spectral data bytes to that status read. Reading these bytes consecutively (0x94 to 0xB8) ensures that the data is concurrent. All spectral data are stored as 16-bit values. The ASTATUS and spectral data registers are read only.

ASTATUS Register (Address 0x94)

Figure 45: ASTATUS Register

| Addr: 0x94 | | ASTATUS | | |
|------------|--------------|---------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | ASAT_STATUS | 0 | R, SC | Saturation Status. Indicates if the latched data is affected by analog or digital saturation. |
| 6:4 | Reserved | 0 | R | Reserved |
| 3:0 | AGAIN_STATUS | 0 | R, SC | Gain Status. Indicates the gain applied for the spectral data latched to this ASTATUS read. |

DATA Register (Address 0x95/0xB8)

Figure 46: DATA_L Register

| Addr: (|)x95/97/99B7 | DATA_N_L | | |
|---------|--------------|----------|--------|--------------------------|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | DATA_L | 0 | R | Spectral Data – low byte |

Figure 47: DATA_H Register

| Addr: 0 | x96/98/9AB8 | DATA_N_H | | |
|---------|-------------|----------|--------|---------------------------|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | DATA_H | 0 | R | Spectral Data – high byte |



10.2.8 Miscellaneous Configuration

CFG0 Register (Address 0xBF)

Figure 48: CFG 0 Register

| Addr: | 0xBF | CFG0 | CFG0 | | |
|-------|-----------|---------|--------|--|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:6 | Reserved | 0 | | Reserved | |
| | | | | Low Power Idle. | |
| 5 | LOW_POWER | 0 | RW | When asserted, the device will automatically run in a low power mode whenever all functions are in wait states or disabled. | |
| | | | | Register Bank Access. | |
| | | | | 0: Register access to register 0x80 and above | |
| 4 | REG BANK | 0 | RW | 1: Register access to register 0x20 to 0x7F | |
| | | C C | | Note: Bit needs to be set to access registers 0x20 to 0x7F. If registers 0x80 and above needs to be accessed bit needs to be set to "0". | |
| 3 | Reserved | 0 | | Reserved | |
| 0 | WI ONC | 0 | | Trigger Long. | |
| 2 | WLONG | 0 | RW | Increases the WTIME setting by a factor of 16. | |
| 1:0 | Reserved | 0 | | Reserved | |
| | | | | | |

CFG3 Register (Address 0xC7)

Figure 49: CFG 3 Register

| Addr: 0xC7 | | CFG3 | CFG3 | | |
|------------|----------|---------|--------|--|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:5 | Reserved | 0 | | Reserved | |
| 4 | SAI | 0 | RW | Sleep After Interrupt. If set, the oscillator is turned off whenever an interrupt is active. SAI_ACTIVE is set in this event. To activate the oscillator again, clear all interrupts and clear the SAI_ACTIVE bit. | |
| 3:0 | Reserved | 0xC | | Reserved | |



CFG6 Register (Address 0xF5)

Figure 50:

CFG6 Register

| Addr: 0xF5 | | CFG6 | CFG6 | | | |
|------------|----------|---------|--------------------------------|----------|--|--|
| Bit | Bit Name | Default | Default Access Bit Description | | | |
| | | | | SMUX Com | nand. | |
| | | | | | MUX command to execute when KEN gets set. Do not change during JX operation. | |
| | | | | VALUE | SMUX_CMD | |
| 4:3 | SMUX_CMD | 2 | RW | 0 | ROM code initialization of SMUX | |
| | | | | 1 | Read SMUX configuration to RAM from SMUX chain | |
| | | | | 2 | Write SMUX configuration from RAM to SMUX chain | |
| | | | | 3 | Reserved, do not use | |

CFG9 Register (Address 0xCA)

Figure 51: CFG9 Register

| Addr: 0xCA | | CFG9 | CFG9 | | |
|------------|-----------|---------|--------|--|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:5 | Reserved | 0 | | Reserved | |
| | | | | System Interrupt SMUX Operation. | |
| 4 | SIEN_SMUX | 0 | RW | Enables system interrupt when SMUX command has finished | |
| 3:0 | Reserved | | | Reserved | |
| | | | | | |

CFG20 Register (Address 0xD6)

Figure 52: CFG20 Register

| Addr: 0xD6 CFG20 | | | | |
|------------------|----------|---------|------------------------|----------|
| Bit | Bit Name | Default | Access Bit Description | |
| 7 | Reserved | | | Reserved |

| Addr: | 0xD6 | CFG20 | CFG20 | | |
|-------|-----------|---------|--------------------------------|---|--|
| Bit | Bit Name | Default | Default Access Bit Description | | |
| 6:5 | auto_smux | 0 | RW | Automatic Channel Read-Out. 0: 6 Channel FZ, FY, FXL, NIR, 2xVIS, Clear 1: Reserved 2: Automatic 12 channel Cycle 1: FZ, FY, FXL, NIR, 2xVIS, Clear Cycle 2: F2, F3, F4, F6, 2xVIS, Clear 3: Automatic 18 channel Cycle 1: FZ, FY, FXL, NIR, 2xVIS, Clear Cycle 2: F2, F3, F4, F6, 2xVIS, Clear Cycle 2: F2, F3, F4, F6, 2xVIS, Clear Cycle 3: F1, F5, F7, F8, 2xVIS, Clear Cycle 3: F1, F5, F7, F8, 2xVIS, Clear Note: The bit "auto_smux" should only be changed before a measurement is started. Once a measurement is started the device is automatically processing the channels as per definition above and storing the measurement results in the eighteen data registers. 2xVIS: Per default the "Top Left" and "Bot Right" VIS/CLEAR PD is read-out | |
| 4:0 | Reserved | | | Reserved | |

PERS Register (Address 0xCF)

Figure 53: PERS Register

| Addr: 0xCF | | PERS | | | |
|------------|----------|----------------|------------|--|--|
| Bit | Bit Name | Default Access | | Bit Des | cription |
| 7:4 | Reserved | 0 | 0 Reserved | | I |
| | | | | Defines a occurrent the thresh SP_TH_H spectral c is set by S | Interrupt Persistence. filter for the number of consecutive ces that spectral data must remain outside hold range between SP_TH_L and d before an interrupt is generated. The data channel used for the persistence filter SP_TH_CHANNEL. Any sample that is e threshold range resets the counter to 0. |
| | | | | VALUE | CHANNEL |
| 3:0 | APERS | 0 | RW | 0 | Every spectral cycle generates an interrupt |
| | | | | 1 | 1 |
| | | | | 2 | 2 |
| | | | | 3 | 3 |
| | | | | 4 | 5 |
| | | | | 5 | 10 |

| Addr: 0xCF | | PERS | | | |
|------------|----------|---------|--------|--------|-----------------|
| Bit | Bit Name | Default | Access | Bit De | escription |
| | | | | | 5 x (APERS – 3) |
| | | | | 14 | 55 |
| | | | | 15 | 60 |



10.2.9 FIFO Buffer Data and Status

The FIFO buffer is used to poll spectral data with fewer I²C read and write transactions. The FIFO buffer is 256 bytes of RAM containing 128 two-byte datasets. If the FIFO overflows (i.e. 129 datasets before host reads data from the FIFO buffer), an overflow flag will be set and new data will be lost. The Host acquires data by reading addresses: 0xFE - 0xFF. The register address pointer automatically wraps from 0xFF to 0xFE as data are read. Data can be read one byte at a time or in blocks, (there is no block-read length limit). When reading single bytes, the internal FIFO read pointer and the FIFO Buffer Level, FIFO_LVL, are updated each time register 0xFF is read. For block-reads, the internal FIFO read pointer and the FIFO Buffer Level, FIFO_LVL = 0, the device will return 0 for all data. The FINT interrupt indicates when there is valid data in the FIFO buffer. The amount of unread data is indicated by the FIFO_LVL.

FIFO_MAP Register (Address 0xFC)

Figure 54: FIFO_MAP Register

| Addr: 0xFC | | FIFO_MAP | | |
|------------|---------------------|----------|--------|---|
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | Reserved | 0 | | Reserved |
| 6 | FIFO_WRITE_CH5_DATA | 0 | RW | FIFO Write CH5 Data. If set, CH5 data is written to the FIFO Buffer. (two bytes per sample) |
| 5 | FIFO_WRITE_CH4_DATA | 0 | RW | FIFO Write CH4 Data. If set, CH4 data is written to the FIFO Buffer. (two bytes per sample) |
| 4 | FIFO_WRITE_CH3_DATA | 0 | RW | FIFO Write CH3 Data. If set, CH3 data is written to the FIFO Buffer. (two bytes per sample) |
| 3 | FIFO_WRITE_CH2_DATA | 0 | RW | FIFO Write CH2 Data. If set, CH2 data is written to the FIFO Buffer. (two bytes per sample) |
| 2 | FIFO_WRITE_CH1_DATA | 0 | RW | FIFO Write CH1 Data. If set, CH1 data is written to the FIFO Buffer. (two bytes per sample) |
| 1 | FIFO_WRITE_CH0_DATA | 0 | RW | FIFO Write CH0 Data. If set, CH0 data is written to the FIFO Buffer. (two bytes per sample) |
| 0 | FIFO_WRITE_ASTATUS | 0 | RW | FIFO Write Status. If set, ASTATUS (one byte per sample) is written to the FIFO Buffer. |



FIFO_LVL Register (Address 0xFD)

Figure 55:

FIFO_LVL Register

| Addr: 0xFD | | FIFO_LVL | FIFO_LVL | | |
|------------|----------|----------|----------|---|--|
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:0 | FIFO_LVL | 0 | R | FIFO Buffer Level. Indicates the number of entries (each are 2 bytes) available in the FIFO buffer waiting for readout. The FIFO RAM is 256byte, the FIFO_LVL range is from 0 entries to 128 entries. | |

FDATA Register (Address 0xFE and 0xFF)

Figure 56: FDATA_L Register

| Addr: 0xFE | | FDATA_L | | |
|------------|----------|---------|--------|------------------|
| Bit | Bit Name | Default | Access | Bit Description |
| 7:0 | FDATA | 0 | R | FIFO Buffer Data |

Figure 57:

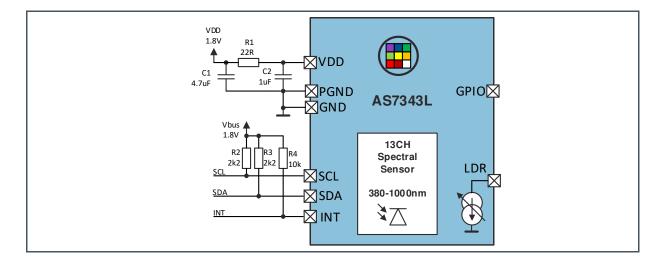
FDATA_H Register

| Addr: 0xFF | | FDATA_H | | |
|------------|----------|---------|--------|------------------|
| Bit | Bit Name | Default | Access | Bit Description |
| 15:8 | FDATA | 0 | R | FIFO Buffer Data |

11 Application Information

11.1 Schematic

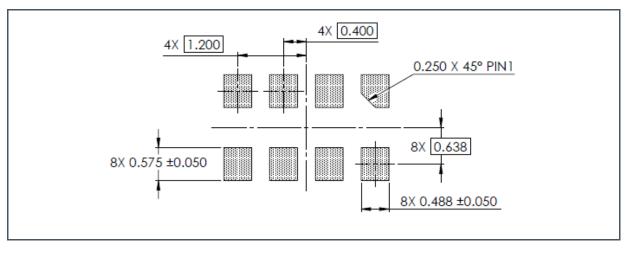
Figure 58: Application Example



11.2 PCB Pad Layout

Figure 59:

Recommended PCB Pad Layout



(1) All dimensions are in millimeters.

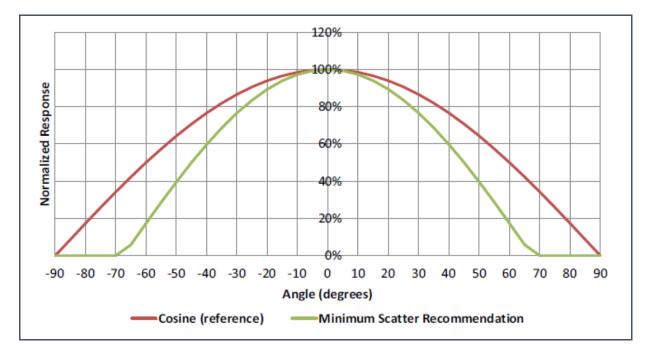
(2) Dimension tolerances are 0.05 mm unless otherwise noted.

(3) This drawing is subject to change without notice.

11.3 Application Optical Requirements

For optimal performance, an achromatic diffuser shall be placed above the device aperture. The recommended solution is a bulk diffuser that meets the minimum recommended scattering characteristic shown below. For more details refer to the optical design guide or contact ams OSRAM.

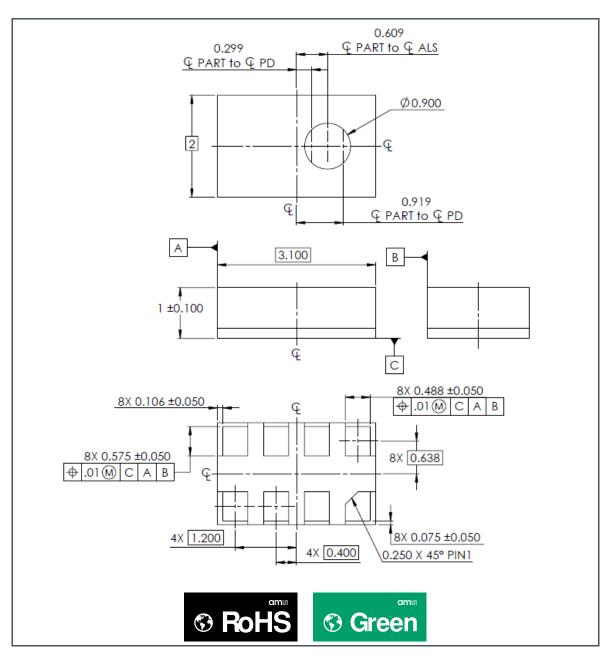
Figure 60: Diffuser Characteristics



12 Package Drawings & Markings

Figure 61:

OLGA8 Package Outline Drawing

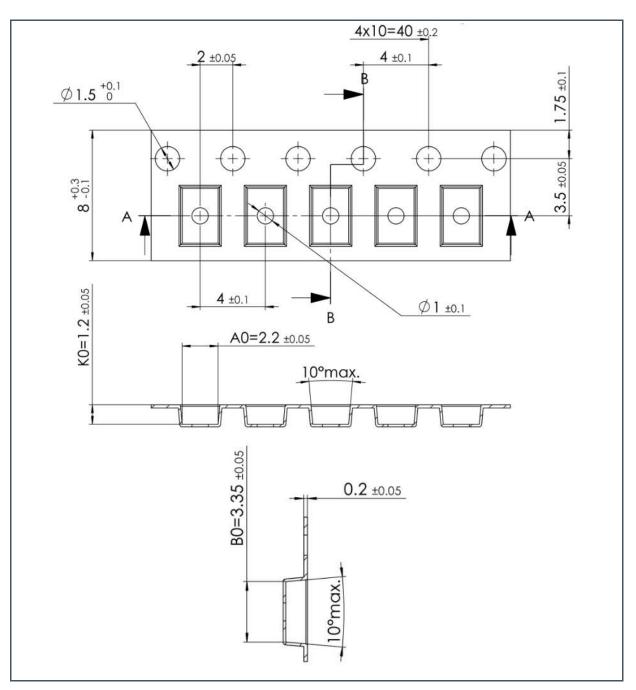


- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Dimensioning and tolerance conform to ASME Y14.5M-1994.
- (3) This package contains no lead (Pb).
- (4) This drawing is subject to change without notice.

13 Tape & Reel Information

Figure 62:

AS7343L OLGA8 Tape Dimensions

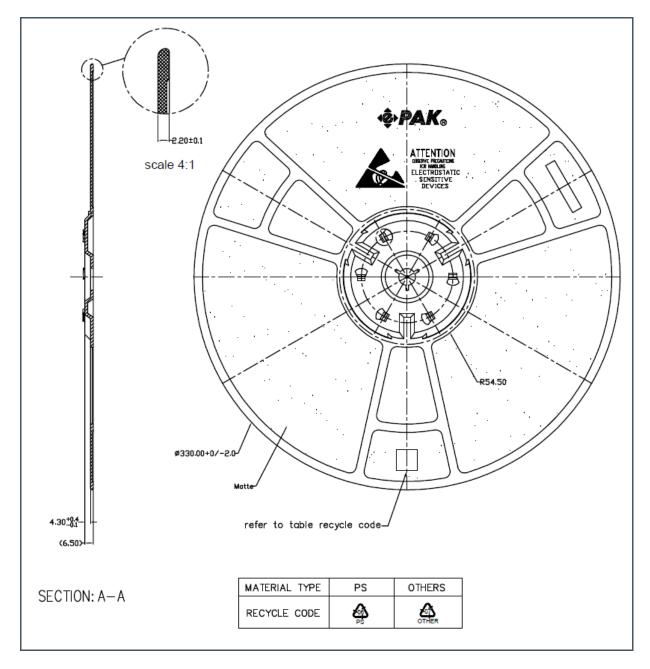


(1) All dimensions are in millimeters. Angles in degrees.

(2) This drawing is subject to change without notice.



Figure 63: AS7343L OLGA8 Reel Dimensions



(1) All dimensions are in millimeters. Angles in degrees.

(2) This drawing is subject to change without notice.

14 Soldering & Storage Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 64: Solder Reflow Profile Graph

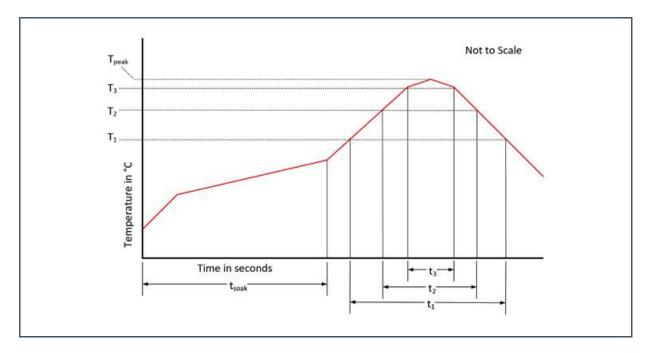


Figure 65: Solder Reflow Profile

| Parameter | Reference | Device |
|--|-------------------|----------------|
| Average temperature gradient in preheating | | 2.5 °C/s |
| Soak time | t _{soak} | 2 to 3 minutes |
| Time above 217 °C (T1) | t1 | Max 60 s |
| Time above 230 °C (T2) | t2 | Max 50 s |
| Time above T _{peak} – 10 °C (T3) | t3 | Max 10 s |
| Peak temperature in reflow | T _{peak} | 260 °C |
| Temperature gradient in cooling | | Max −5 °C/s |



14.1 Storage Information

14.1.1 Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package.

To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

14.1.2 Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40 °C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

14.1.3 Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

14.1.4 Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50 °C for 12 hours.

15 Revision Information

| Document Status | Product Status | Definition |
|-----------------------------|-----------------|--|
| Product Preview | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice |
| Preliminary Datasheet | Pre-Production | Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice |
| Datasheet | Production | Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade |
| Datasheet (discontinued) | Discontinued | Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs |

Changes from previous version to current revision v2-00

Page

Document security class is updated to "Public" in the footer

• Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.

Correction of typographical errors is not explicitly mentioned.

16 Legal Information

Copyrights & Disclaimer

Copyright ams-OSRAM AG, Tobelbader Strasse 30, 8141 Premstaetten, Austria-Europe. Trademarks Registered. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

Devices sold by ams-OSRAM AG are covered by the warranty and patent indemnification provisions appearing in its General Terms of Trade. ams-OSRAM AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein. ams-OSRAM AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with ams-OSRAM AG for current information. This product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by ams-OSRAM AG for each application. This product is provided by ams-OSRAM AG "AS IS" and any express or implied warranties, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose are disclaimed.

ams-OSRAM AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of ams-OSRAM AG rendering of technical or other services.

RoHS Compliant & ams Green Statement

RoHS Compliant: The term RoHS compliant means that ams-OSRAM AG products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories plus additional 4 substance categories (per amendment EU 2015/863), including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ams Green (RoHS compliant and no Sb/Br/Cl): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material) and do not contain Chlorine (Cl not exceed 0.1% by weight in homogeneous material).

Important Information: The information provided in this statement represents ams-OSRAM AG knowledge and belief as of the date that it is provided. ams-OSRAM AG bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. ams-OSRAM AG has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams-OSRAM AG and ams-OSRAM AG suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

| Headquarters | Please visit our website at www.ams.com |
|-------------------------|---|
| ams-OSRAM AG | Buy our products or get free samples online at www.ams.com/Products |
| Tobelbader Strasse 30 | Technical Support is available at www.ams.com/Technical-Support |
| 8141 Premstaetten | Provide feedback about this document at www.ams.com/Document-Feedback |
| Austria, Europe | For sales offices, distributors and representatives go to www.ams.com/Contact |
| Tel: +43 (0) 3136 500 0 | For further information and requests, e-mail us at ams_sales@ams.com |
| | |