

# 74F30

## 8-Input NAND Gate

### General Description

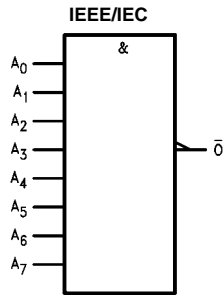
This device contains a single gate, which performs the logic NAND function.

### Ordering Code:

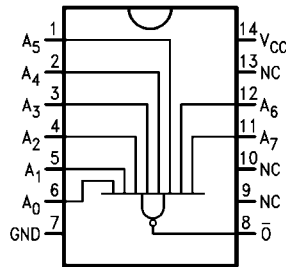
Order Number	Package Number	Package Description
74F30SC (Note 1)	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F30SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F30PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

**Note 1:** Devices also available in Tape and Reel. Specify by appending the letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Unit Loading/Fan Out

Pin Names	Description	U.L.	Input $I_{IH}/I_{IL}$
		HIGH/LOW	Output $I_{OH}/I_{OL}$
$A_0$ - $A_7$	Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$\bar{O}$	Output	50/33.3	-1 mA/20 mA

### Function Table

Inputs								Output
$A_0$	$A_1$	$A_2$	$A_3$	$A_4$	$A_5$	$A_6$	$A_7$	$\bar{O}$
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

**Absolute Maximum Ratings** (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

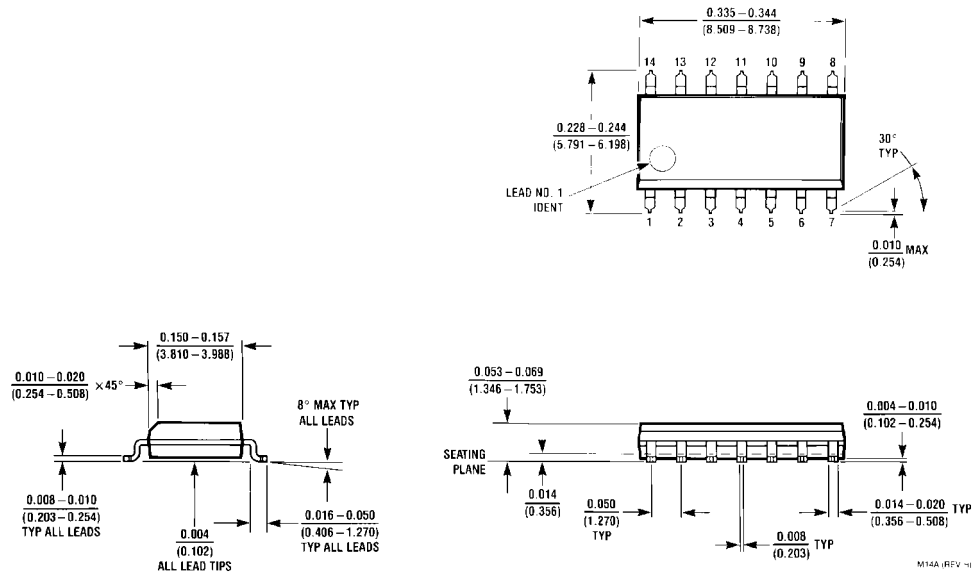
**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCH</sub>	Power Supply Current		0.5	1.5	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			4.5	mA	Max	V <sub>O</sub> = LOW

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	1.0	3.7	5.0	1.0	5.5	ns
t <sub>PHL</sub>	A <sub>n</sub> to $\bar{O}$	1.5	2.8	5.0	1.5	5.5	

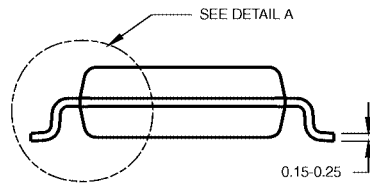
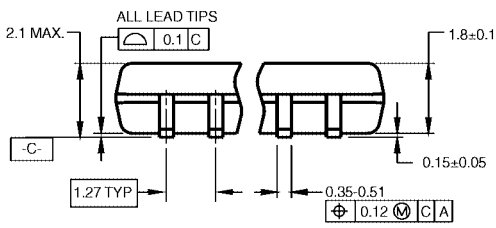
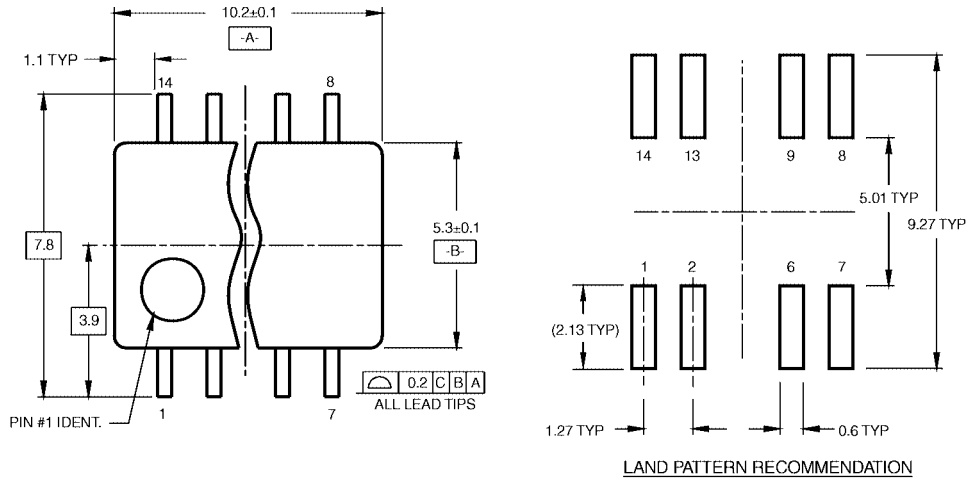
**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M14A**

M14A (REV. 1)

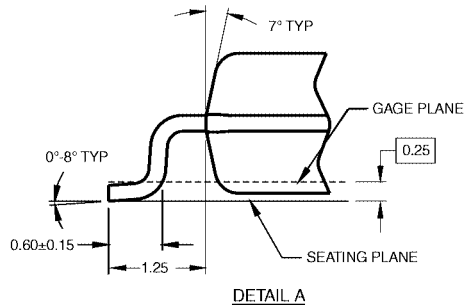
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

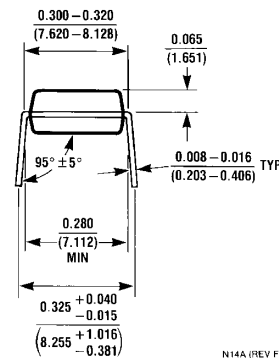
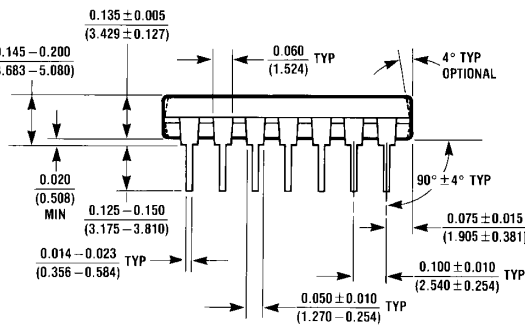
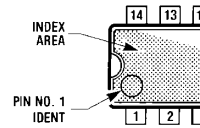
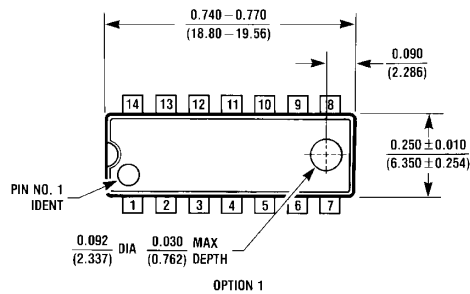
- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
 Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



N14A (REV F)

**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)

Home >> Find products >>

## 74F30

8-Input NAND Gate

### Contents

- [General description](#)
- [Product status/pricing/packageing](#)
- [Order Samples](#)
- [Qualification Support](#)


### General description

This device contains a single gate, which performs the logic NAND function.

[back to top](#)

### Product status/pricing/packageing

**BUY**

Product	Product status	Pb-free Status	Package type	Leads	Packing method	Package Marking Convention**
74F30SCX_NL	Not recommended for new designs		<a href="#">SOIC</a>	14	TAPE REEL	Line 1: \$Y (Fairchild logo) &Z (Asm. Plant Code) &2 (2-Digit Date Code) &T (Die Trace Code) Line 2: 74F30



Indicates product with Pb-free second-level interconnect. For more information [click here](#).

Package marking information for product 74F30 is available. [Click here for more information](#).

[back to top](#)

### Qualification Support

Click on a product for detailed qualification data

**BUY**

### Datasheet

[Download this datasheet](#)



[e-mail this datasheet](#)



### This page

[Print version](#)

### Related Links

[Request samples](#)

[How to order products](#)

[Product Change Notices \(PCNs\)](#)

[Support](#)

[Sales support](#)

[Quality and reliability](#)

[Design center](#)

<b>Product</b>
----------------

<a href="#">74F30SCX_NL</a>
-----------------------------

[back to top](#)

© 2007 Fairchild Semiconductor



[Products](#) | [Design Center](#) | [Support](#) | [Company News](#) | [Investors](#) | [My Fairchild](#) | [Contact Us](#) | [Site Index](#) | [Privacy Policy](#) | [Site Terms & Conditions](#) | [Standard Terms & Conditions](#) | [Contact Us](#)