



EMIF06-10006F2

IPAD™

6 line EMI filter and ESD protection

Main product characteristics

Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Computers, printers and MCU Boards

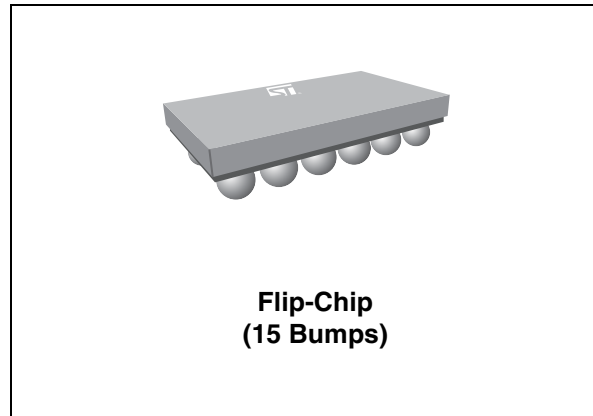
Description

The EMIF06-10006F2 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The EMIF06 Flip-Chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents damage to the application when subjected to ESD surges up to 15 kV. This device includes 6 EMIF filters.

Benefits

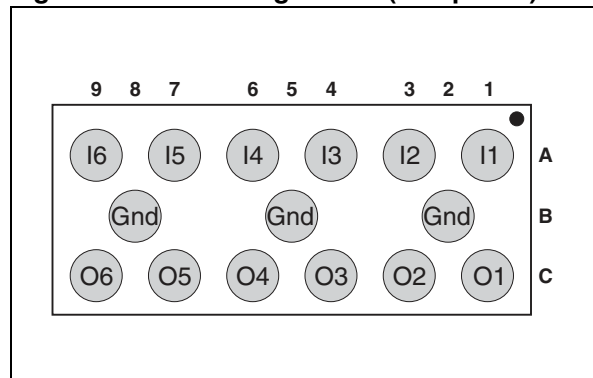
- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead free package
- Very low PCB space consumption
2.92 mm x 1.29 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
(IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging



Order code

Part Number	Marking
EMIF06-10006F2	FT

Figure 1. Pin configuration (bump side)



Complies with the following standards:

IEC 61000-4-2 level 4:

15 kV (air discharge)

8 kV (contact discharge)

MIL STD 883E - Method 3015-6 Class 3: 30 kV

TM: IPAD is a trademark of STMicroelectronics

1 Characteristics

Figure 2. Basic cell configuration

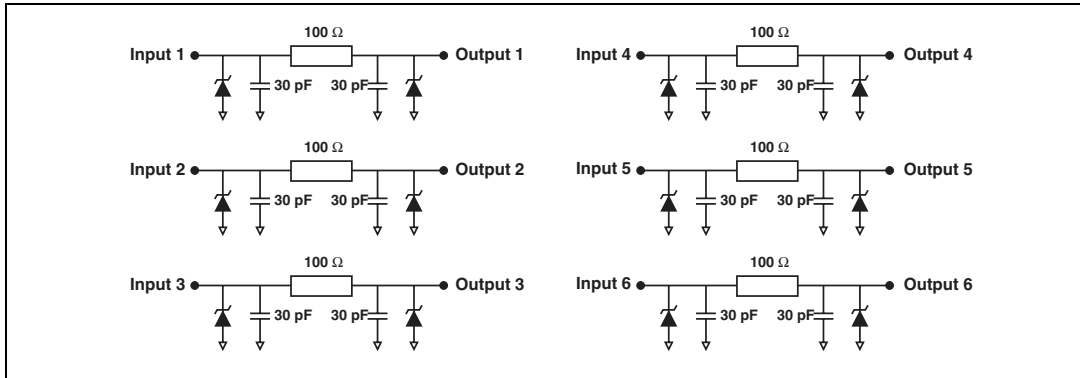


Table 1. Absolute Ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
P_R	DC power per resistance	0.1	W
P_T	Total DC power per package	0.6	W
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	125	°C

Table 2. Electrical Characteristics ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input and output
C_{line}	Capacitance per line

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	5.5	7	9	V
I_{RM}	$V_{RM} = 3.3\text{ V per line}$			500	nA
$R_{I/O}$	$I = 10\text{ mA}$	80	100	120	Ω
C_{line}	$V_R = 2.5\text{ V}, F = 1\text{ MHz}, 30\text{ mV (on filter cells)}$	50	60	70	pF

Figure 3. S21 (db) attenuation measurements and Aplac simulation **Figure 4. Analog crosstalk measurements**

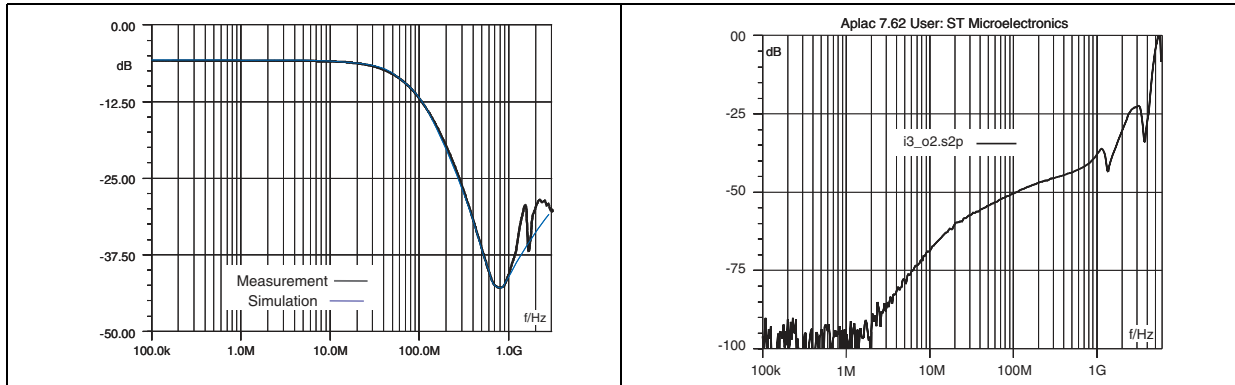


Figure 5. Digital crosstalk measurements **Figure 6. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{in}) and one output (V_{out})**

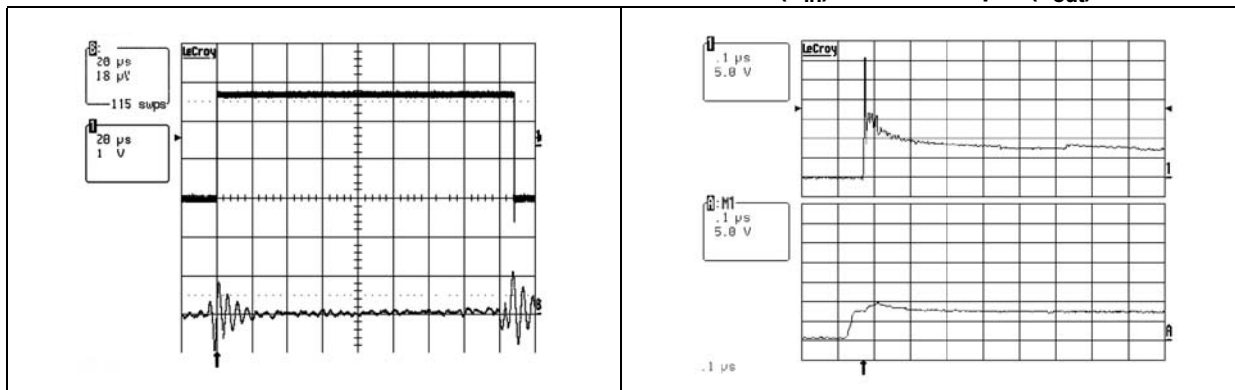


Figure 7. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (V_{in}) and one output (V_{out}) **Figure 8. Line capacitance versus applied voltage for filter**

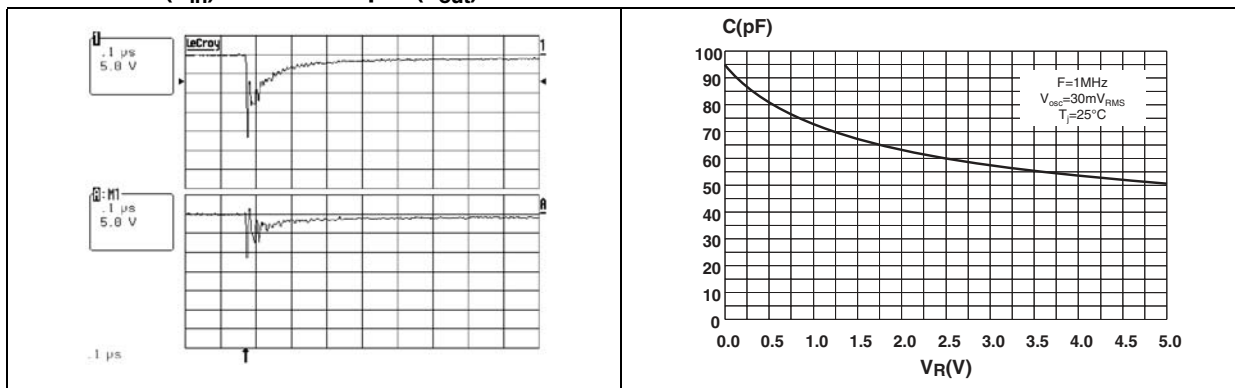


Figure 9. Aplac model

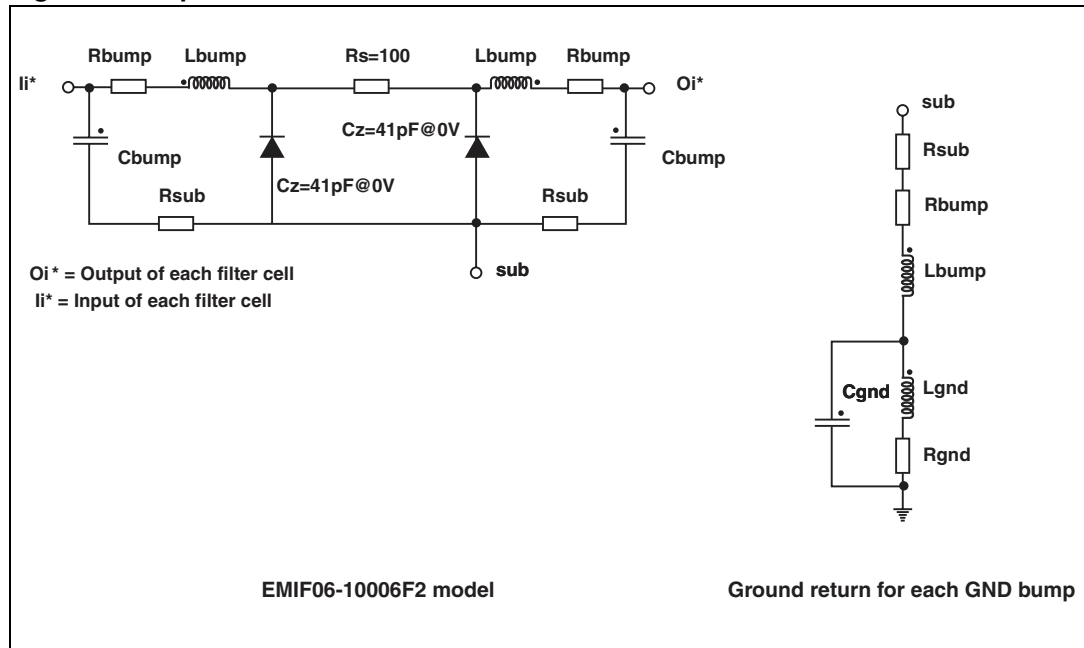
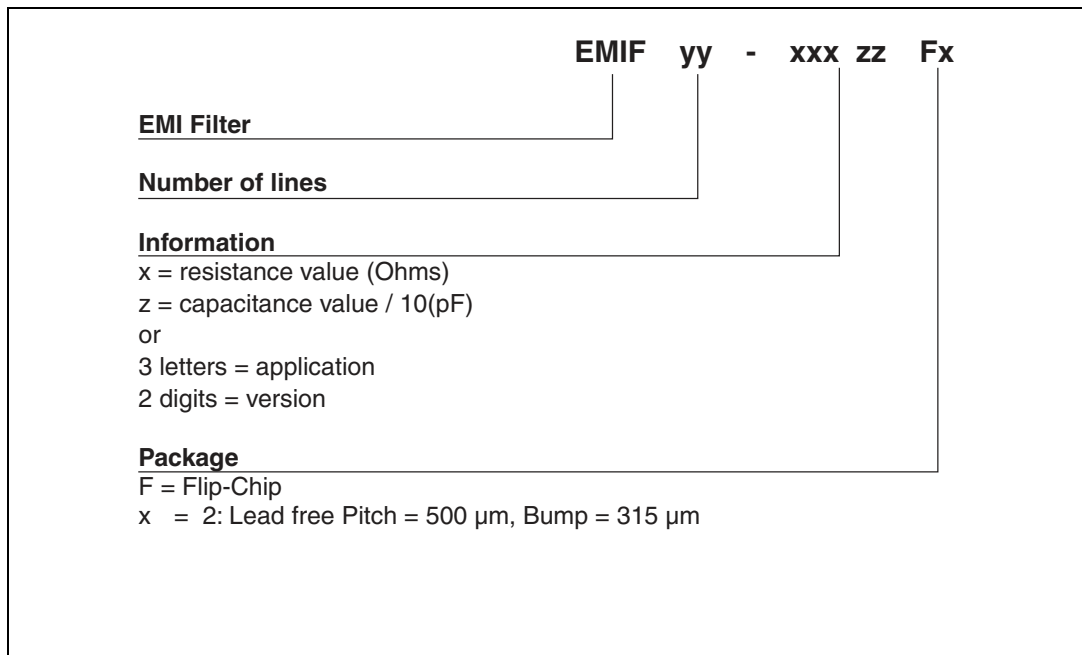


Figure 10. Figure 10: Aplac parameters

aplacvar RS	100Ω
aplacvar Cz	41 pF
aplacvar Lbump	50 pH
aplacvar Rbump	20 m
aplacvar Cbump	1.2 pF
aplacvar Rsub	100 m
aplacvar Rgnd	100 m
aplacvar Lgnd	100 pH
aplacvar Cgnd	0.15 pF

2 Ordering Information Scheme



3 Package information

Figure 11. Flip-Chip Package dimensions

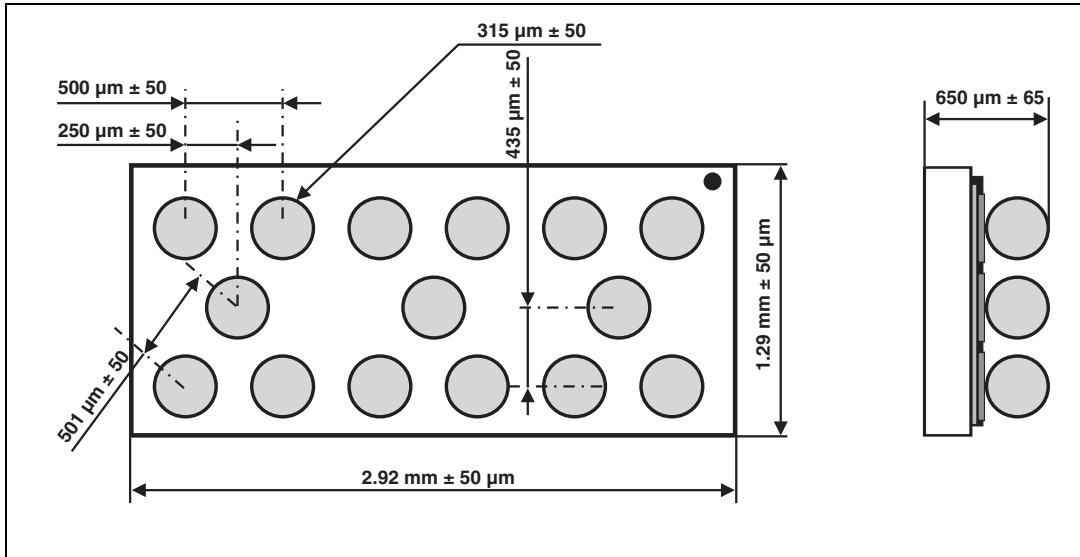


Figure 12. Foot print recommendations Figure 13. Marking

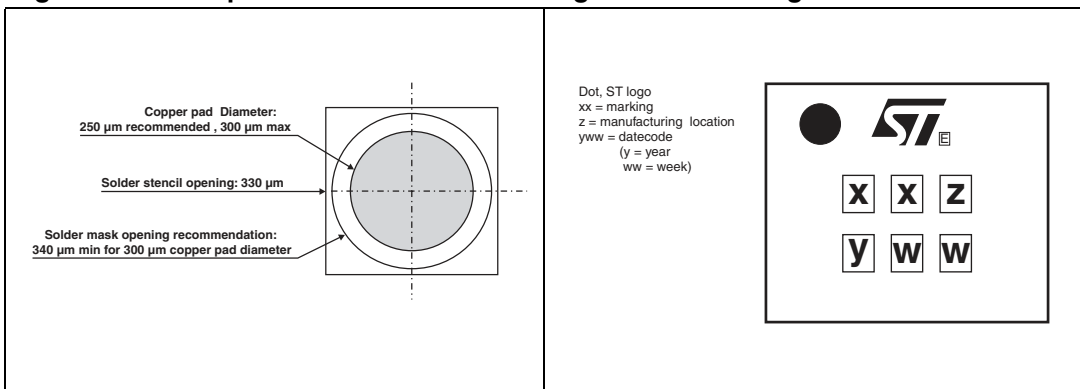
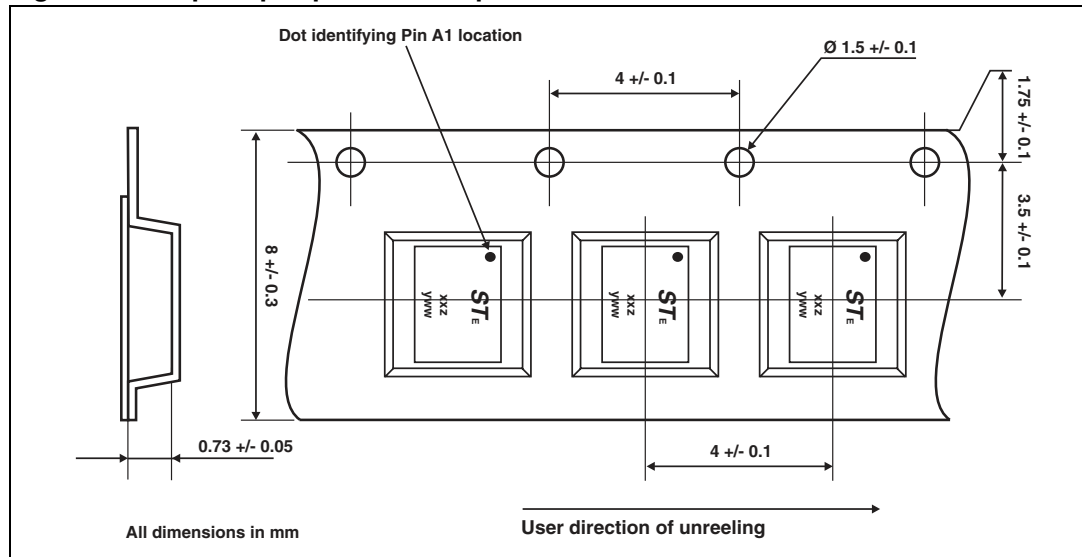


Figure 14. Flip-Chip Tape and reel specification



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Note:

Note: More packing information is available in the application notes:

AN1235: "Flip-Chip: Package description and recommendations for use"

AN1751: "EMI Filters: Recommendations and measurements"

4 Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-10006F2	FT	Flip-Chip	5.4 mg	5000	Tape and reel 7"

5 Revision History

Date	Revision	Description of Changes
Sep-2004	1	First issue
19-Nov-2004	2	Figure 2 on page 2: Basic cell configuration corrected for I/O5 and I/O6.
11-Apr-2006	3	Reformatted to current standard. Marking corrected in ordering information.
17-Nov-2006	4	Ordering code in ordering information corrected.

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