Rail-to-Rail Output, High Quality Audio, Dual Operational Amplifier

■ GENERAL DESCRIPTION

The MUSES8832 is a Rail-to-Rail output High quality audio operational amplifier, which is optimized for high-end audio and portable audio applications.

The MUSES8832 features 2.1nV/√Hz low noise, 10MHz wide gain bandwidth, 0.0009% low distortion, 600Ω drive capability, -40°C to +125°C operating temperature range, and various reliabilities and conveniences are improved.

It is the best for audio preamplifiers, active filters, microphone amplifiers, and line amplifiers with excellent sound.

■ PACKAGE OUTLINE

MUSES8832E
(SOP8 JEDEC 150 mil (EMP8))

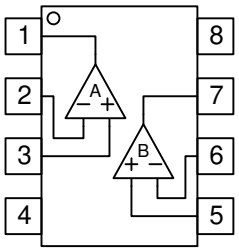
MUSES8832KW1
(DFN8-W1 (ESON8-W1))

■ FEATURES

● Operating Voltage	+2.7V to +14V ±1.35V to ±7.0V
● Low Noise	2.1nV/√Hz typ. at f=1kHz 0.3μVrms typ. (20Hz to 20kHz)
● Output Current	32mA typ. (Capability of driving 600Ω loads)
● GBW	10MHz typ.
● Low Distortion	0.0009% typ. at V+=+5V, Vo=1.3Vrms
● Slew Rate	1V/μs typ.
● Bipolar Technology	
● Package Outline	SOP8 JEDEC 150 mil DFN8-W1 (ESON8-W1) (3.0mm x 3.0mm)
● Operating Temperature Range	-40 to +125°C

■ PIN CONFIGLATION

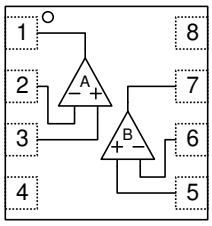
SOP8 JEDEC 150 mil



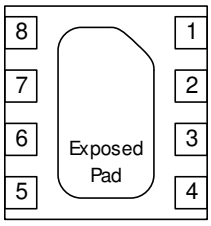
1. A OUTPUT
2. A -INPUT
3. A +INPUT
4. V-
5. B +INPUT
6. B -INPUT
7. B OUTPUT
8. V+

DFN8-W1 (ESON8-W1)

Top View



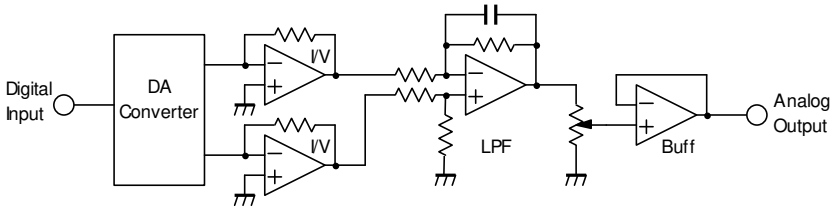
Bottom View



About Exposed Pad
Connect the Exposed Pad on the GND.

■ APPLICATIONS

- Portable Audio
- Home Audio
- PC Audio
- Car Audio



DAC Output I/V converter + LPF circuit

■ **ABSOLUTE MAXIMUM RATINGS** (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+ (V^+/V^-)	+15 (±7.5)	V
Input Voltage	V_{IN}	+15 (1)	V
Differential Input Voltage	V_{ID}	±15	V
Power Dissipation	P_D	SOP8 JEDEC 150 mil: 800 (2) DFN8-W1: 650 (3) / 2100 (4)	mW
Operating Temperature Range	T_{opr}	-40 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(Note1) For supply Voltages less than +15 V, the maximum input voltage is equal to the Supply Voltage.
(Note2) EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 2layers, FR-4) mounting.
(Note3) EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 2layers, FR-4) mounting. The PAD connecting to GND in the center part on the back
(Note4) EIA/JEDEC STANDARD Test board (76.2 x 114.3 x 1.6mm, 4layers, FR-4, Applying a thermal via hole to a board based on JEDEC standard JESD51-5) mounting. The PAD connecting to GND in the center part on the back

■ **RECOMMENDED OPERATING CONDITION** (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+		+2.7	-	+14.0	V
	V^+/V^-		±1.35	-	±7.0	V

■ **ELECTRIC CHARACTERISTICS**

V^+= +5V, V^-=0V, Ta=25°C, R_L to V^+/2, unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	I_{CC}	No Signal, R_L=∞	-	7.5	10	mA
Input Offset Voltage	V_{IO}	Rs=50Ω	-	0.1	0.5	mV
Input Bias Current	I_B		-	4	6.5	μA
Input Offset Current	I_{IO}		-	100	500	nA
Open-Loop Voltage Gain	A_V	R_L=10kΩ to V+/2, V_O=0.5 to 4.5V	90	115	-	dB
Common Mode Input Voltage Range	V_{ICM}	CMR≥90dB	0.5	-	3.7	V
Common Mode Rejection Ratio	CMR	R_S=50Ω	90	110	-	dB
Supply Voltage Rejection Ratio	SVR	R_S=50Ω	90	105	-	dB
Maximum Output Voltage 1	V_{OH1}	R_L=10kΩ to 0V	4.9	4.95	-	V
	V_{OL1}	R_L=10kΩ to 0V	-	0.05	0.1	V
Maximum Output Voltage 2	V_{OH2}	R_L=600Ω to V^+/2	4.8	4.9	-	V
	V_{OL2}	R_L=600Ω to V^+/2	-	0.1	0.2	V
Output Source Current	I_{SOURCE}	V_O=V^+-0.5V	10	32	-	mA
Output Sink Current	I_{SINK}	V_O=0.5V	10	20	-	mA
Gain Bandwidth Product	GBW	f=10kHz	-	10	-	MHz
Slew Rate	SR	R_L=2kΩ	-	1	-	V/μs
Total Harmonic Distortion + Noise	THD+N	A_V=10,V_O=1.3Vrms,R_L=2kΩ,f=1kHz	-	0.0009	-	%
Channel Separation	CS	A_V=100, R_S=1kΩ, R_L=10kΩ, f=1kHz	-	140	-	dB
Input Noise Voltage1	e_n	f=1kHz	-	2.1	-	nV/√Hz
Input Noise Voltage2	V_n	f=20Hz to 20kHz	-	0.30	-	μVrms

■ **NOTE**

1. The closed gain should be 6dB or higher to prevent the oscillation. Unity gain follower application may cause the oscillation.
2. Minimize the load capacitor for the better performance. A large load capacitor CL reduces the frequency response and causes oscillation or ringing.
3. Be careful to the circuit of high impedance. Input bias current influences an input noise and output offset voltage.

■ **POWER DISSIPATION vs. AMBIENT TEMPERATURE**

IC is heated by own operation and possibly gets damage when the junction power exceeds the acceptable value called Power Dissipation P_D. The dependence of the MUSES8832 P_D on ambient temperature is shown in Fig 1. The plots are depended on following two points. The first is P_D on ambient temperature 25ºC, which is the maximum power dissipation. The second is 0W, which means that the IC cannot radiate any more. Conforming the maximum junction temperature Tjmax to the storage temperature Tstg derives this point. Fig.1 is drawn by connecting those points and conforming the P_D lower than 25ºC to it on 25ºC. The P_D is shown following formula as a function of the ambient temperature between those points.

$$\text{Dissipation Power} \quad P_D = \frac{Tjmax - Ta}{\theta ja} \ [W] \ (Ta=25ºC \text{ to } Ta=150ºC)$$

Where, θja is heat thermal resistance which depends on parameters such as package material, frame material and so on. Therefore, P_D is different in each package.

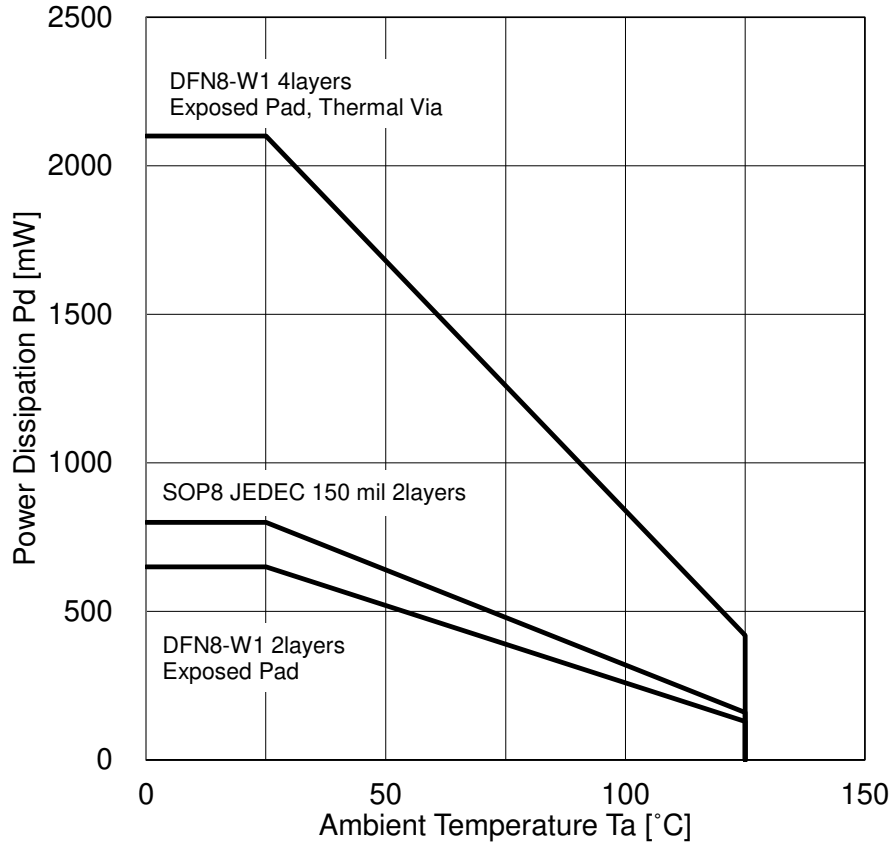
While, the actual measurement of dissipation power on MUSES8832 is obtained using following equation.

(Actual Dissipation Power) = (Supply Current Icc) X (Supply Voltage $V^+ - V-$) – (Output Power Po)

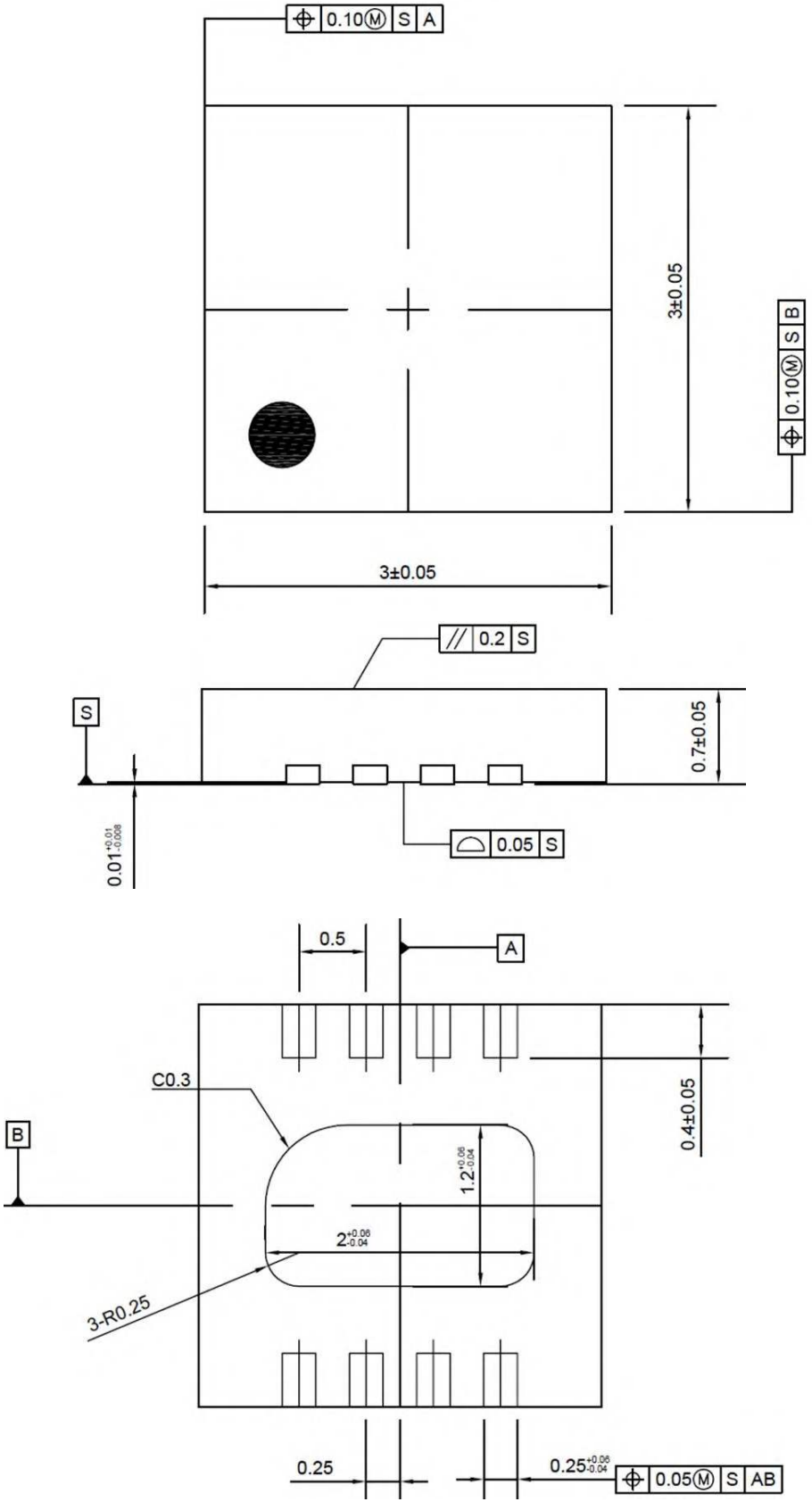
The MUSES8832 should be operated in lower than P_D of the actual dissipation power.

To sustain the steady state operation, take account of the Dissipation Power and thermal design.

Fig 1

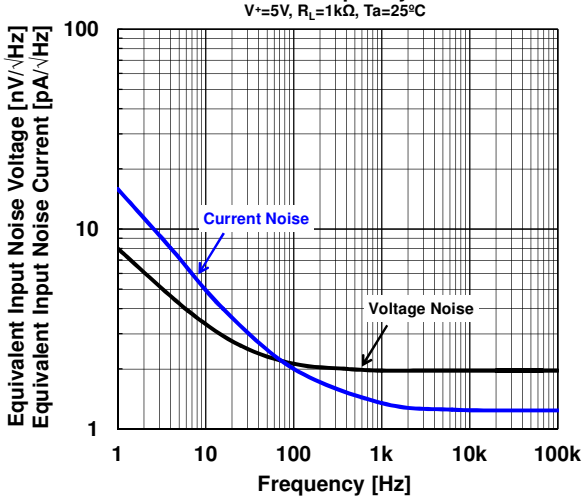


■ **PACKAGE OUTLINE (ESON8-W1)**

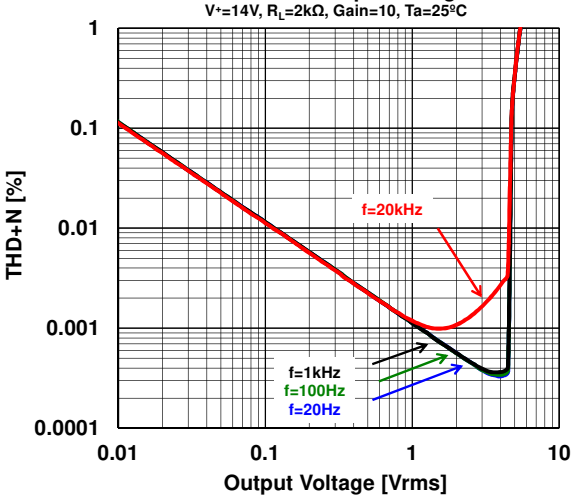


■ **TYPICAL CHARACTERISTICS** (V^-=0V, V_{CM}=V^+/2, unless otherwise specified)

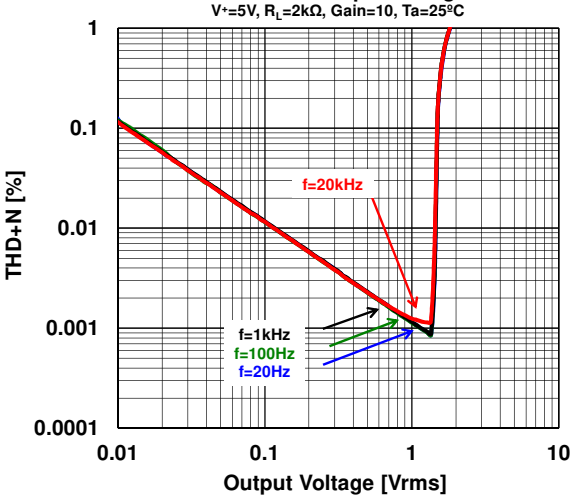
Voltage Noise Density / Current Noise Density vs. Frequency
V^+=5V, R_L=1kΩ, Ta=25ºC



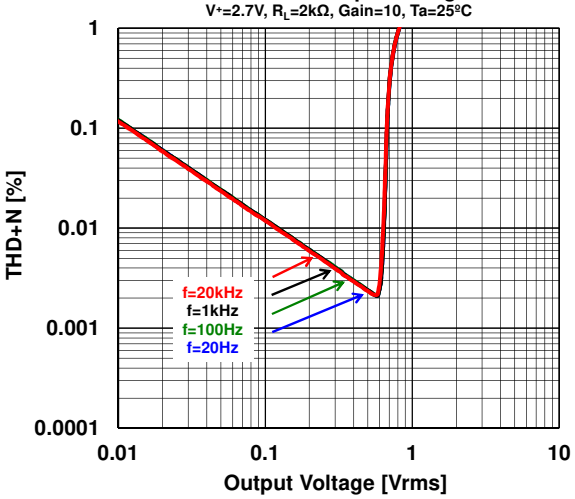
THD+N vs. Output Voltage
V^+=14V, R_L=2kΩ, Gain=10, Ta=25ºC



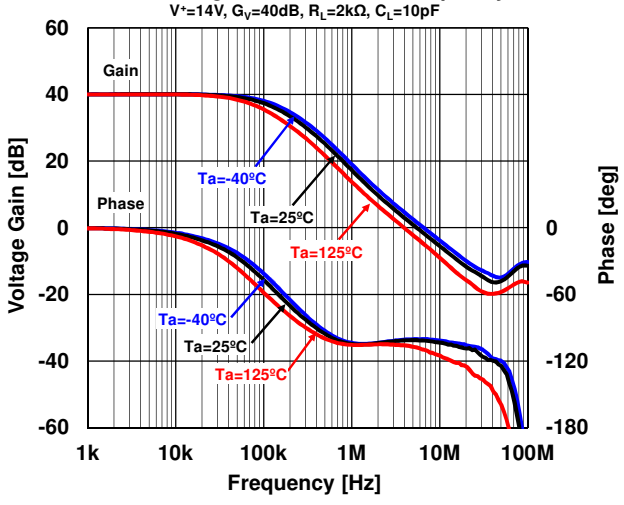
THD+N vs. Output Voltage
V^+=5V, R_L=2kΩ, Gain=10, Ta=25ºC



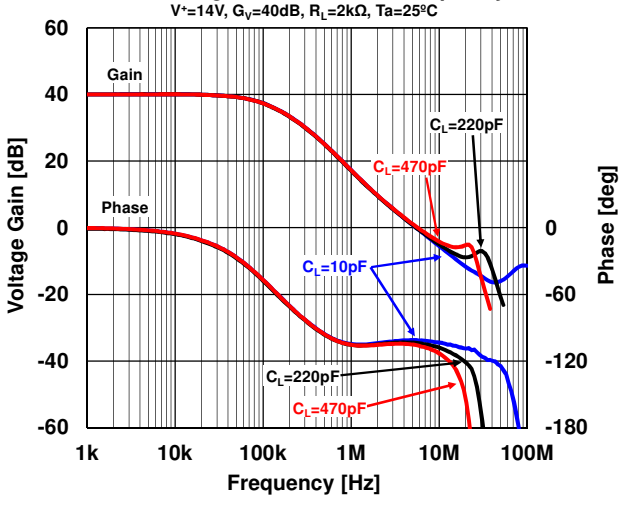
THD+N vs. Output Voltage
V^+=2.7V, R_L=2kΩ, Gain=10, Ta=25ºC



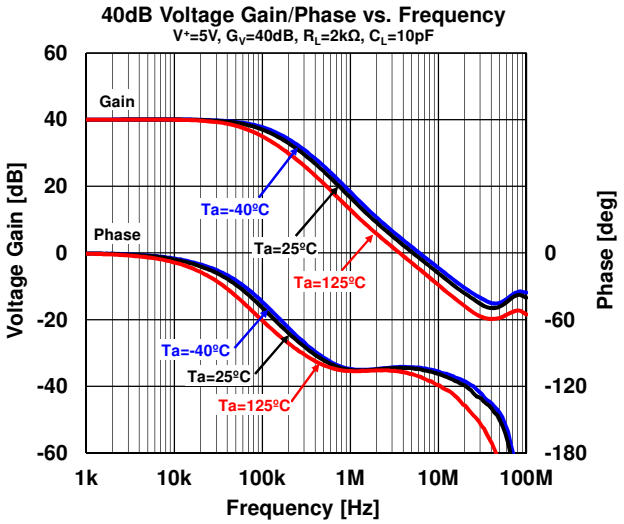
40dB Voltage Gain/Phase vs. Frequency
V^+=14V, G_V=40dB, R_L=2kΩ, C_L=10pF

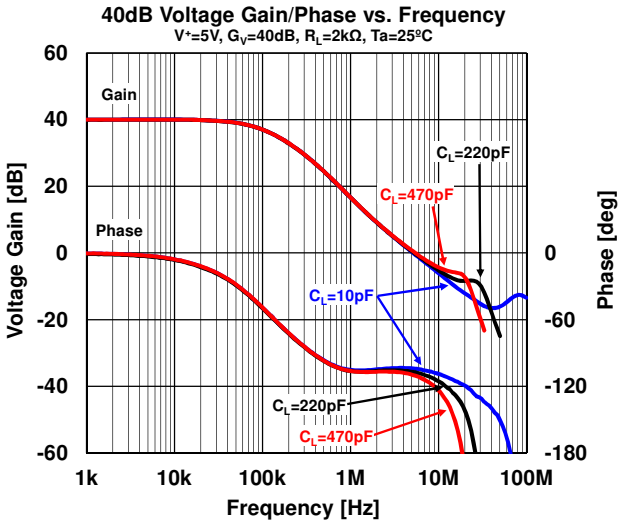


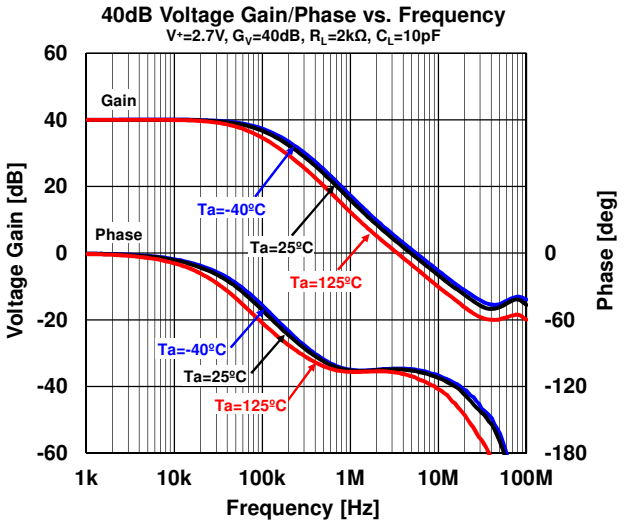
40dB Voltage Gain/Phase vs. Frequency
V^+=14V, G_V=40dB, R_L=2kΩ, Ta=25ºC

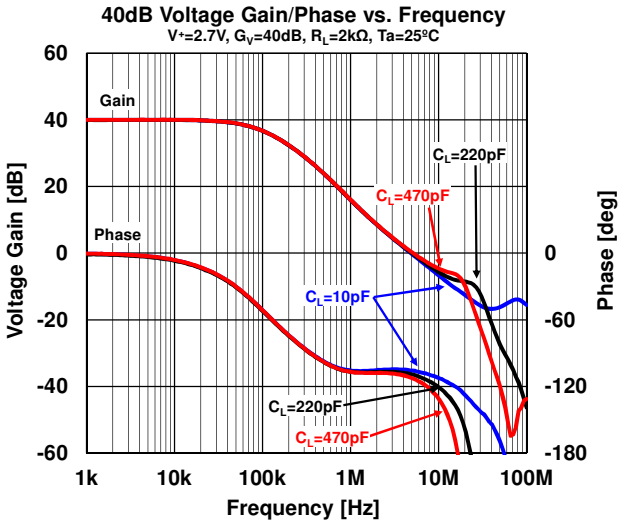


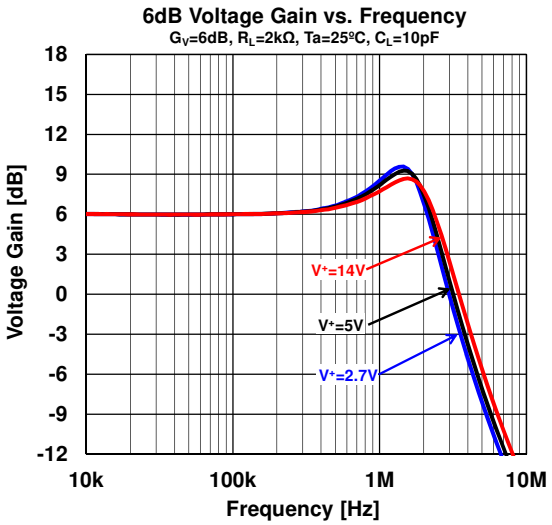
■ **TYPICAL CHARACTERISTICS** (V^-=0V, V_{CM}=V^+/2, unless otherwise specified)

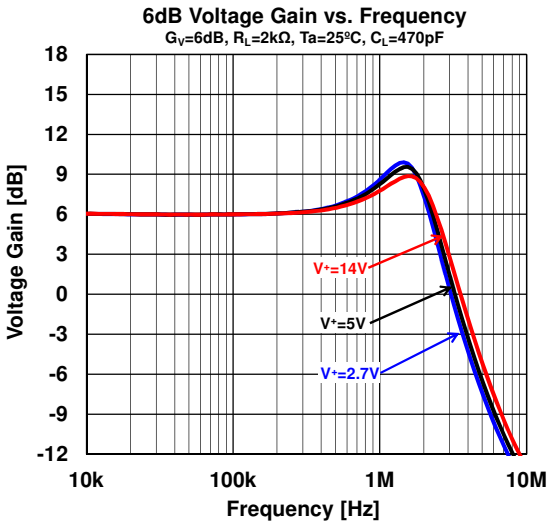












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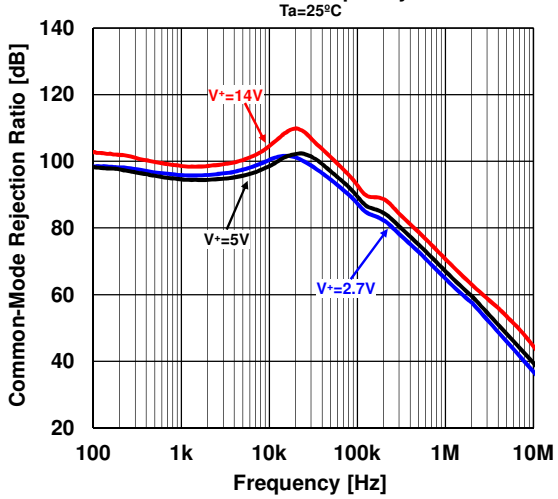
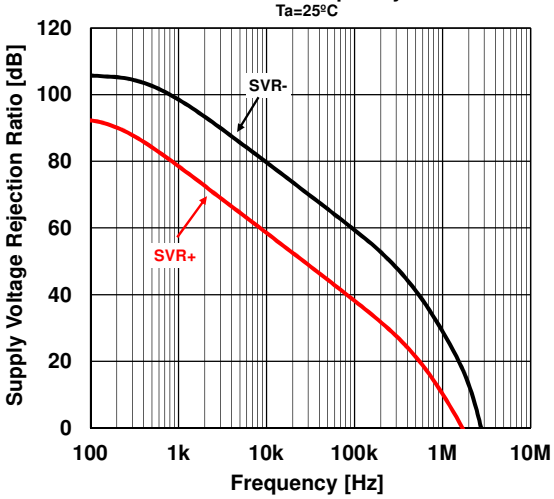
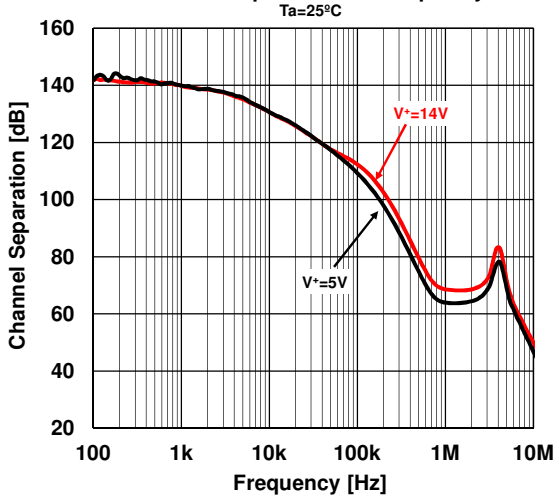
CMR vs. Frequency
Ta=25ºC



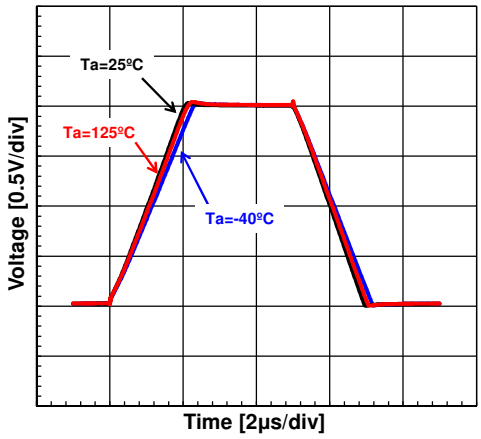
SVR vs. Frequency
Ta=25ºC



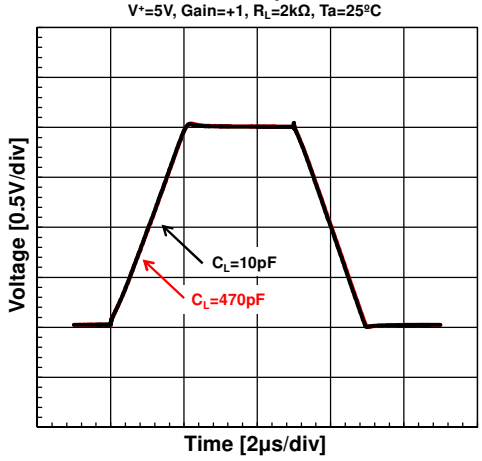
Channel Separation vs. Frequency
Ta=25ºC



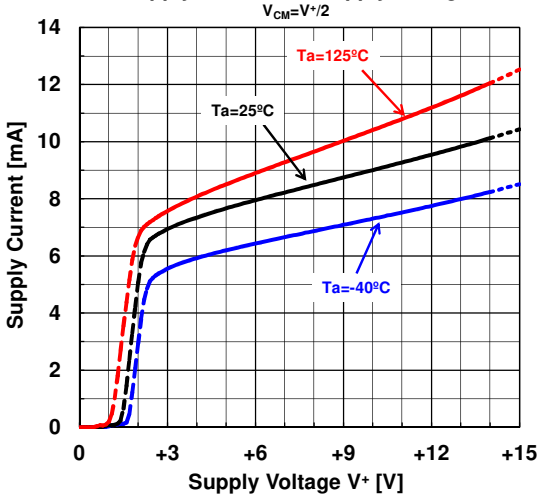
Pulse Response
V^+=5V, Gain=+1, R_L=2kΩ, C_L=10pF



Pulse Response
V^+=5V, Gain=+1, R_L=2kΩ, Ta=25ºC

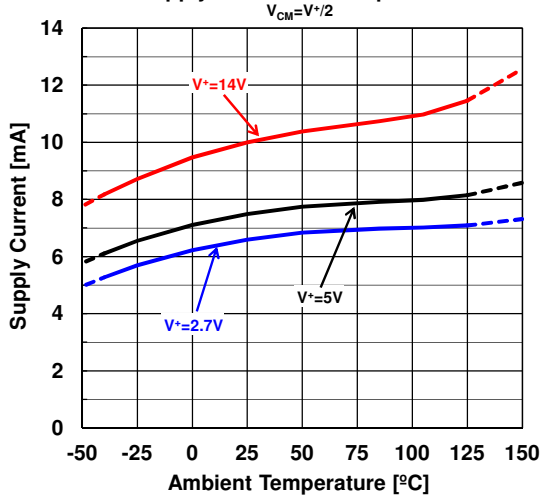


Supply Current vs. Supply Voltage
V_{CM}=V^+/2

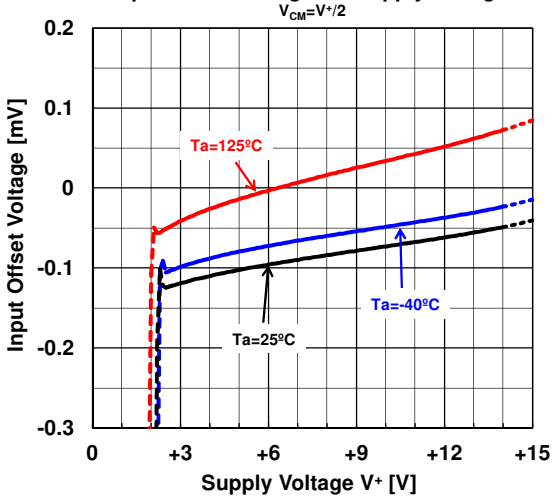


■ **TYPICAL CHARACTERISTICS** (V^-=0V, V_{CM}=V^+/2, unless otherwise specified)

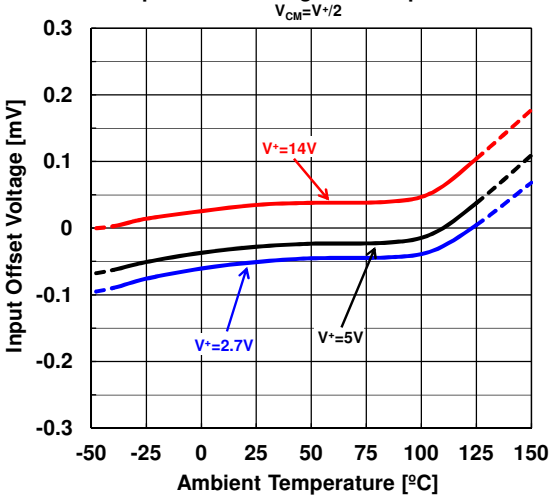
Supply Current vs. Temperature
V_{CM}=V^+/2



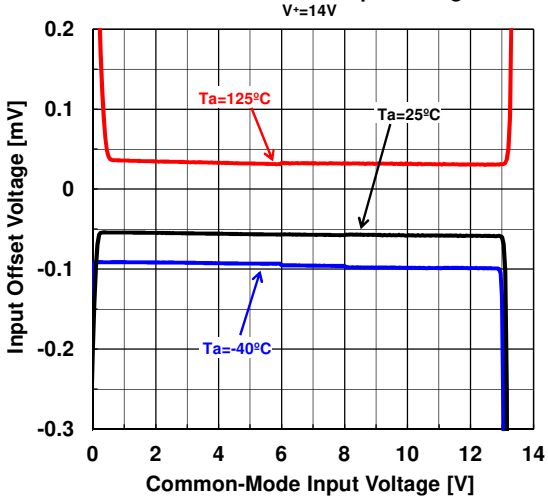
Input Offset Voltage vs. Supply Voltage
V_{CM}=V^+/2



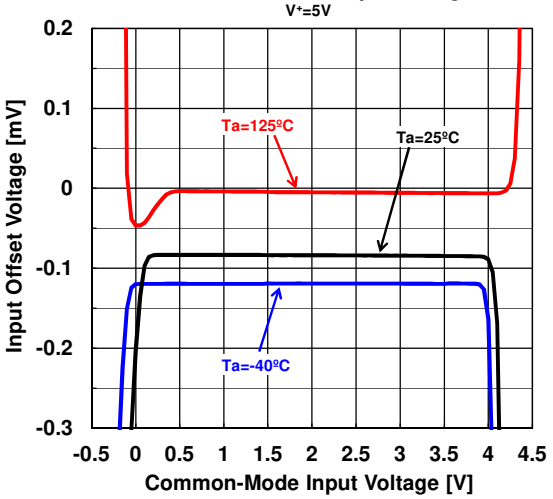
Input Offset Voltage vs. Temperature
V_{CM}=V^+/2



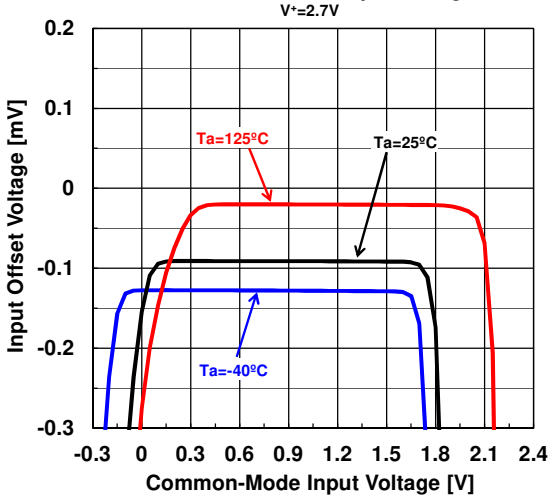
Input Offset Voltage
vs. Common-Mode Input Voltage
V^+=14V



Input Offset Voltage
vs. Common-Mode Input Voltage
V^+=5V

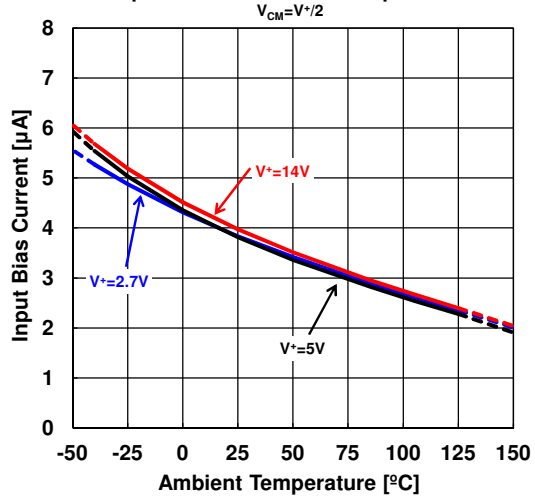


Input Offset Voltage
vs. Common-Mode Input Voltage
V^+=2.7V

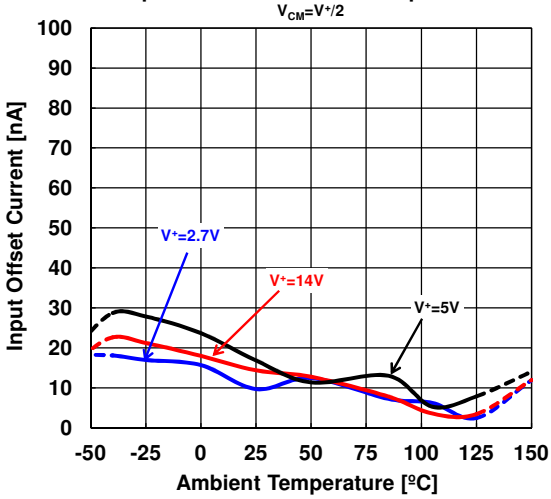


■ **TYPICAL CHARACTERISTICS** (V^-=0V, V_{CM}=V^+/2, unless otherwise specified)

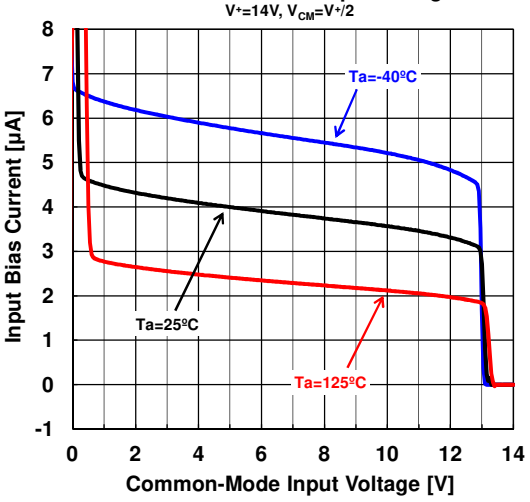
Input Bias Current vs. Temperature
V_{CM}=V^+/2



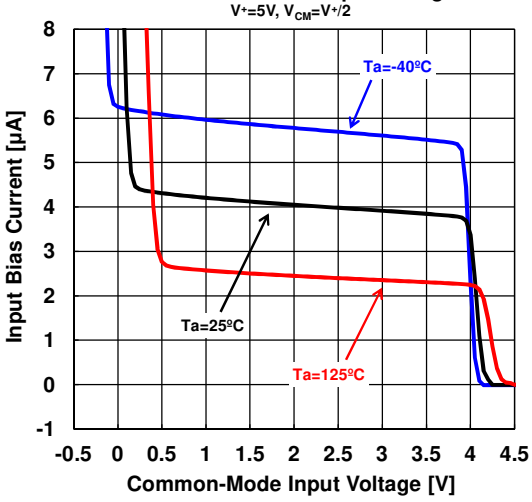
Input Offset Current vs. Temperature
V_{CM}=V^+/2



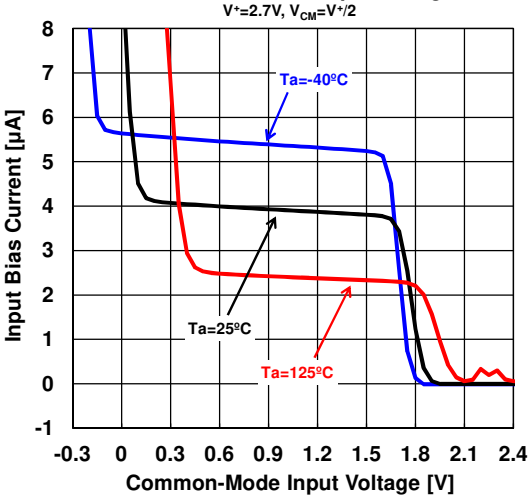
Input Bias Current vs. Common-Mode Input Voltage
V^+=14V, V_{CM}=V^+/2



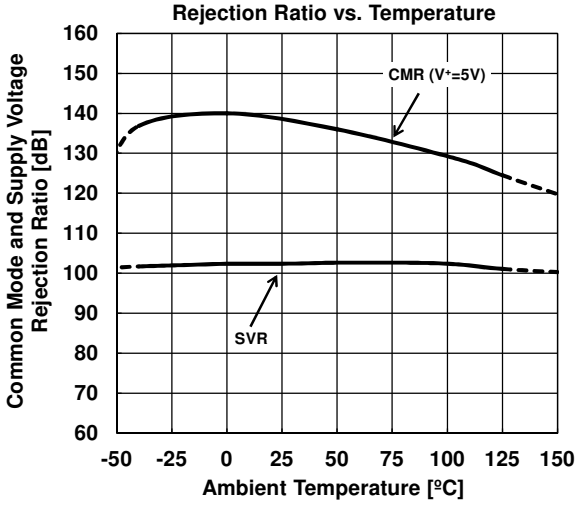
Input Bias Current vs. Common-Mode Input Voltage
V^+=5V, V_{CM}=V^+/2



Input Bias Current vs. Common-Mode Input Voltage
V^+=2.7V, V_{CM}=V^+/2

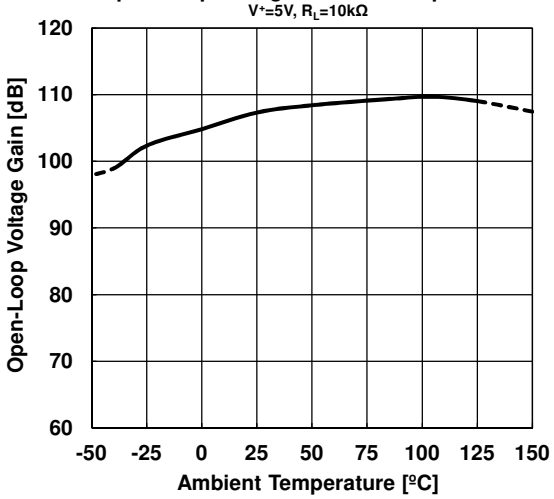


Common Mode and Supply Volrage Rejection Ratio vs. Temperature

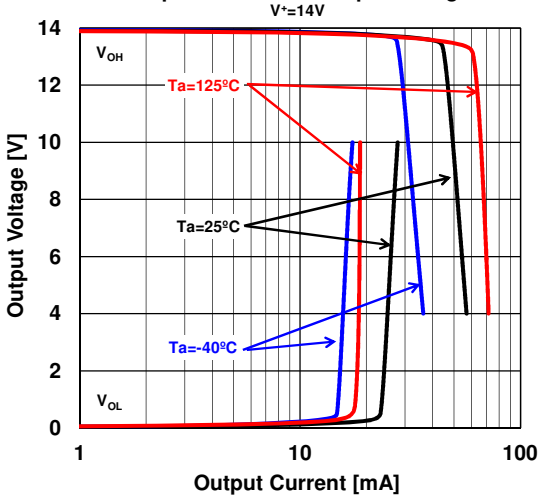


■ **TYPICAL CHARACTERISTICS** (V^-=0V, V_{CM}=V^+/2, unless otherwise specified)

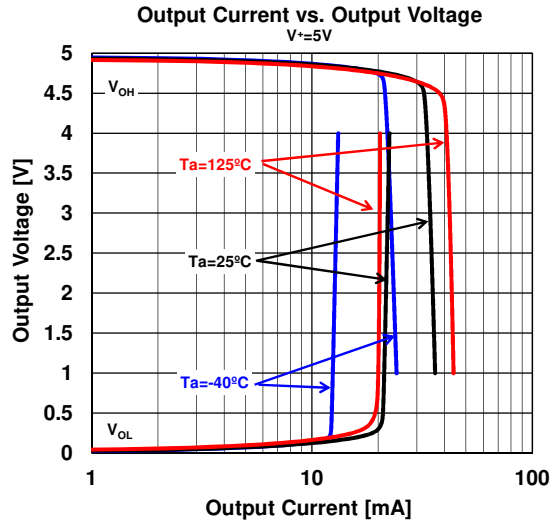
Open-Loop Voltage Gain vs. Temperature



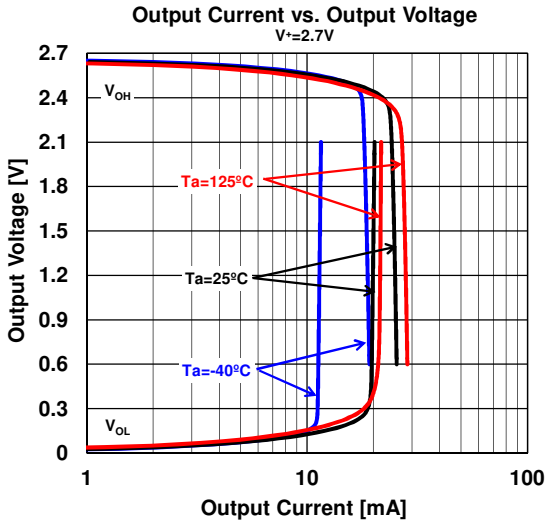
Output Current vs. Output Voltage



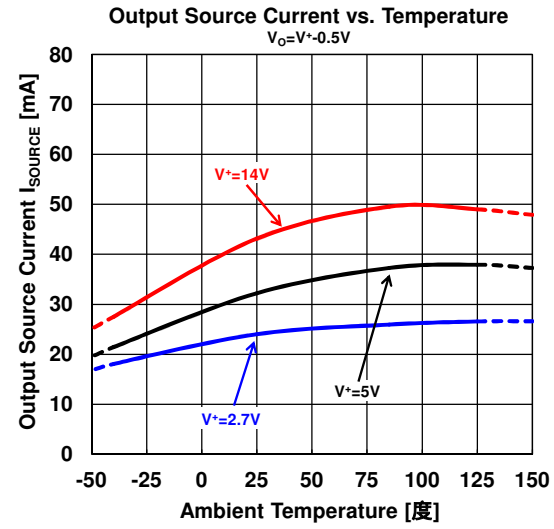
Output Current vs. Output Voltage



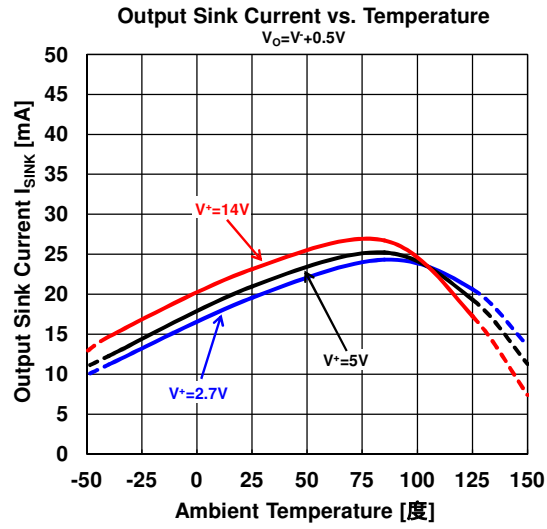
Output Current vs. Output Voltage



Output Source Current vs. Temperature

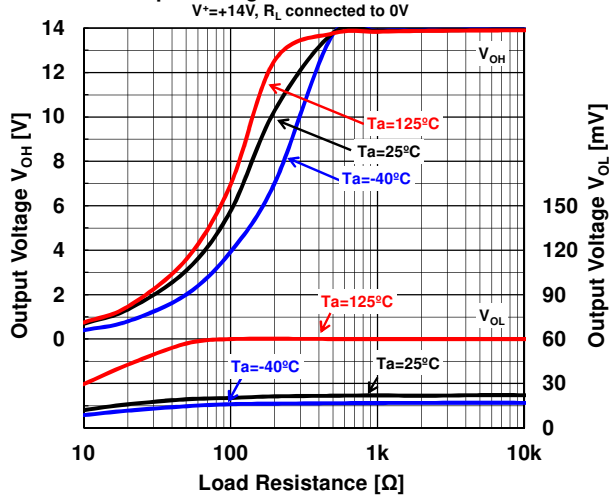


Output Sink Current vs. Temperature

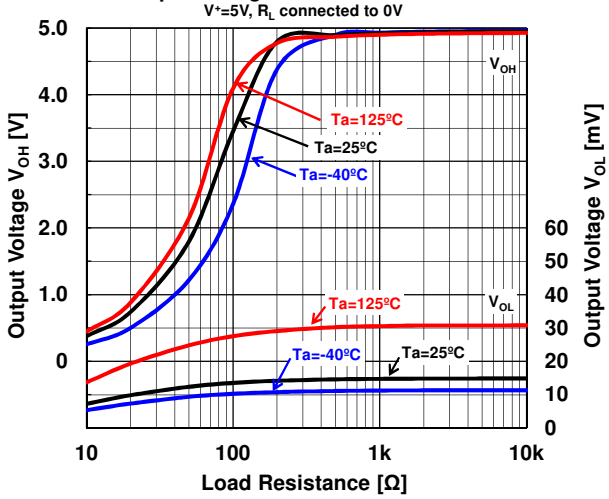


■ **TYPICAL CHARACTERISTICS** (V^-=0V, V_{CM}=V^+/2, unless otherwise specified)

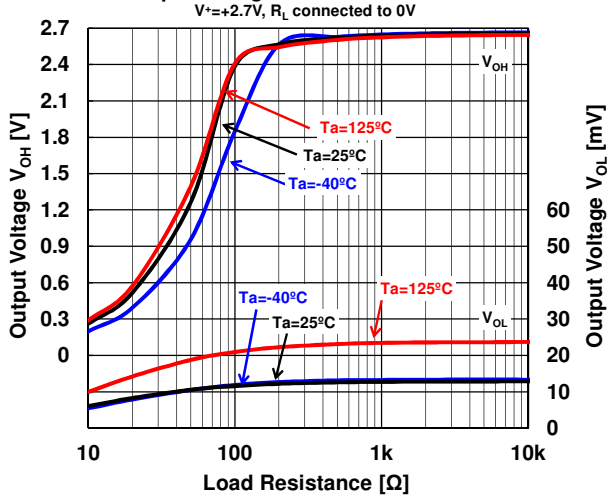
Output Voltage vs. Load Resistance
V^+=+14V, R_L connected to 0V



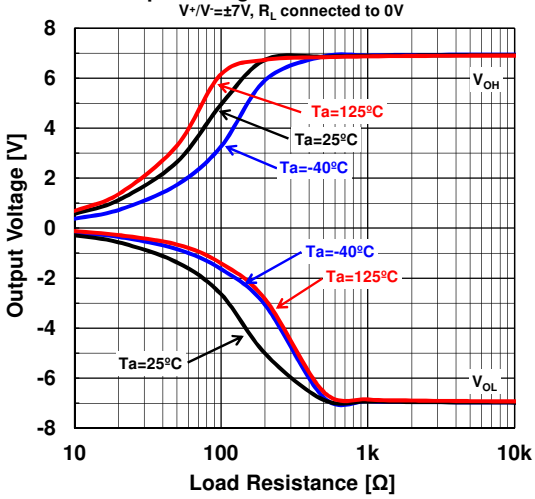
Output Voltage vs. Load Resistance
V^+=5V, R_L connected to 0V



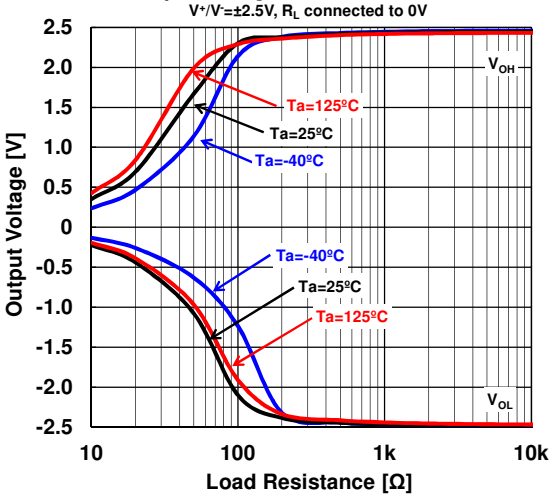
Output Voltage vs. Load Resistance
V^+=+2.7V, R_L connected to 0V



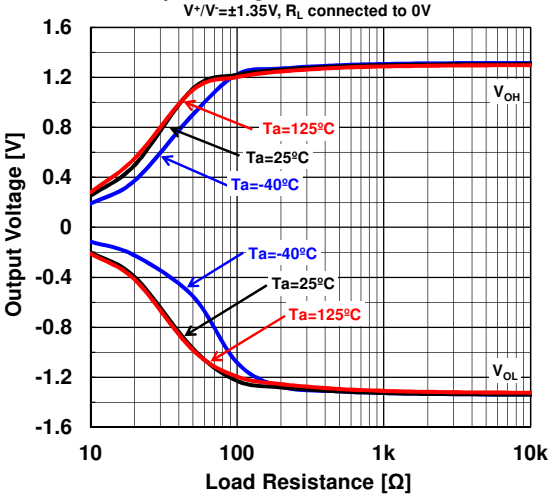
Output Voltage vs. Load Resistance
V^+/V^-=±7V, R_L connected to 0V



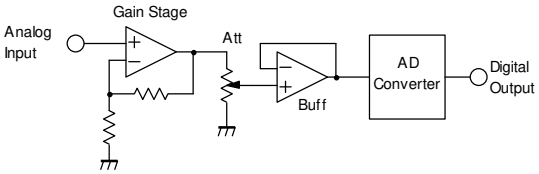
Output Voltage vs. Load Resistance
V^+/V^-=±2.5V, R_L connected to 0V



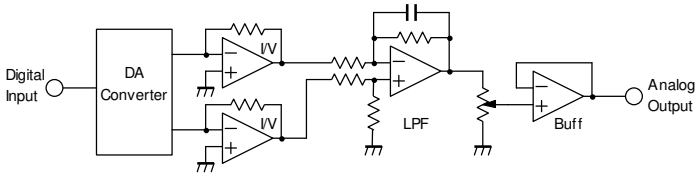
Output Voltage vs. Load Resistance
V^+/V^-=±1.35V, R_L connected to 0V



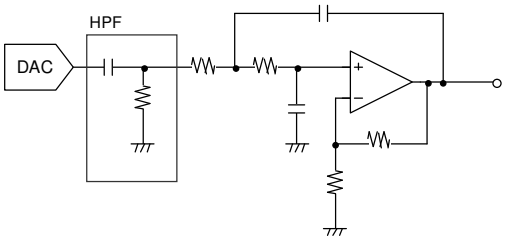
■ APPLICATION CIRCUIT



(Fig.1: ADC Input)



(Fig.2:DAC Output)



(Fig.3:DAC LPF Circuit)

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