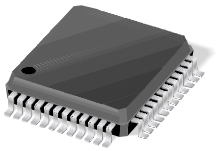


SLAS351B – OCTOBER 2001 – REVISED DECEMBER 2001

1.8-V ANALOG SUPPLY, 10-BIT, 65/40 MSPS ANALOG-TO-DIGITAL CONVERTERS WITH INTERNAL REFERENCE

FEATURES

- **ADS5102 (65 MSPS) ADS5103 (40 MSPS)**
- **Differential Input**
- **1.8 V Analog/Digital Supply**
- **Digital Outputs Compatible With 1.8 V or 3.3 V Logic**
- **Signal-to-Noise: 58 dB at 20 MHz (ADS5103)**
- **Spurious Free Dynamic Range: 71 dB at 20 MHz (ADS5102)**
- **105-mW Power Dissipation (ADS5103)**
- **336 μW Power-Down Mode**

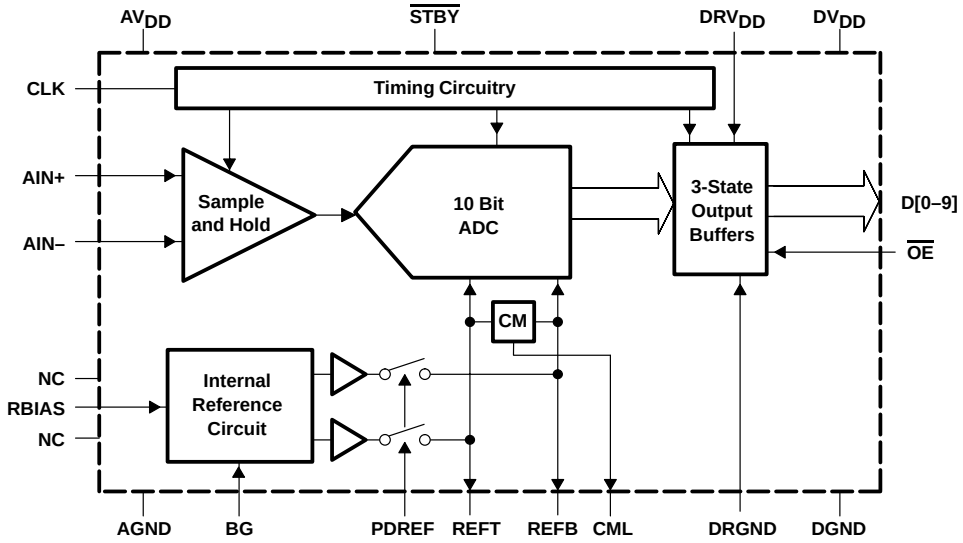
APPLICATIONS

- **Ultrasound**
- **Digital Cameras**
- **Imaging**
- **Communications**
- **Baseband Digitization**

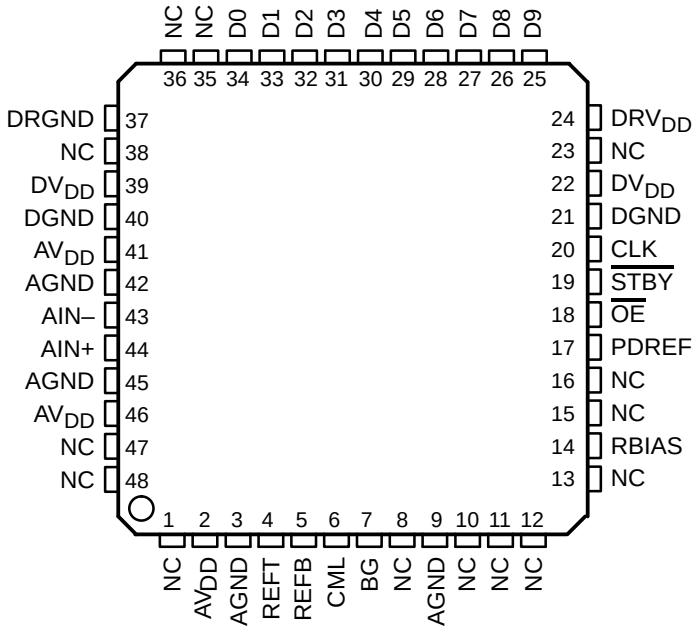
DESCRIPTION

The ADS5102/3 are low-power CMOS, 10-bit, analog-to-digital converters (ADC) that operate from a single 1.8-V supply. The internal reference can be bypassed to use an external reference to suit the dc accuracy and temperature drift requirements of the application. A 10-bit parallel output data bus is provided with 3-state outputs. For power sensitive systems, a standby mode is provided which reduces power consumption to 336 μW. Also, if using external voltage reference, then the internal VREF circuit can be powered down. The analog input is differential, which provides excellent common-mode noise rejection as well as superior performance from the ADS5102/3.

FUNCTIONAL BLOCK DIAGRAM



PFB PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	48-TQFP (PFB) Tape and Reel	48-TQFP (PFB) Tray	48-TQFP (PFB) Tape and Reel	48-TQFP (PFB) Tray
	40 MSPS	40 MSPS	65 MSPS	65 MSPS
0°C to 70°C	ADS5103CPFBR	ADS5103CPFB	ADS5102CPFBR	ADS5102CPFB
–40°C to 85°C	ADS5103IPFBR	ADS5103IPFB	ADS5102IPFBR	ADS5102IPFB
Evaluation module	ADS5103EVM	ADS5103EVM	ADS5102EVM	ADS5102EVM

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{DD}	2, 41, 46	I	Analog supply, 1.8V ±5%
AGND	3, 9, 42, 45	I	Analog ground
REFT	4	I/O	Reference top
REFB	5	I/O	Reference bottom
CML	6	O	Common mode level output—nominally 1.0 V
BG	7	O	Band-gap decoupling—decouple with 1 μF to GND and 100 kΩ to AV_{DD} (refer to Figure 30)
PDREF	17	I	Powerdown reference when using external voltage reference 0 = internal VREF, 1 = external VREF. In external VREF mode, connect pins BG and REFT together.
RBIAS	14	O	Connect a resistor between this pin and AGND. This resistor value is determined by speed grade selected and is used to set amplifier internal bias currents. (see Table 2)
$\overline{OE}$	18	I	1 = 3-state the data outputs , 0 = data bus enable
$\overline{STBY}$	19	I	0 = power down mode, 1 = normal operation mode
CLK	20	I	Clock Input
DGND	21, 40	I	Digital ground
DV_{DD}	22, 39	I	Digital supply—1.8 V nominally
DRV_{DD}	24	I	Driver digital supply—1.8 V or 3.3 V nominally
D9	25	O	Digital Bit 9 (MSB)
D8	26	O	Digital Bit 8
D7	27	O	Digital Bit 7
D6	28	O	Digital Bit 6
D5	29	O	Digital Bit 5
D4	30	O	Digital Bit 4
D3	31	O	Digital Bit 3
D2	32	O	Digital Bit 2
D1	33	O	Digital Bit 1
D0	34	O	Digital Bit 0 (LSB)
DRGND	37	I	Driver digital ground
AIN+	44	I	Positive analog input
AIN–	43	I	Negative analog input
NC	1,8,10,11,12, 13,15,16,23,35, 36, 38,47,48	NA	No internal connection on this pin

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage: V_{DD} to AGND, DV_{DD} to DGND . . . . . –0.3 V to 2.2 V
DRV_{DD} to DRGND . . . . . –0.3 V to 4 V
AGND to DGND . . . . . –0.3 V to 0.3 V
AV_{DD} to DV_{DD} . . . . . –2.2 V to 2.2 V
Reference voltage input range REFT, REFB, to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
CML, analog input voltage range AIN to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Clock input CLK to DRGND . . . . . –0.3 V to DRV_{DD} + 0.3 V
Digital inputs to DRGND . . . . . –0.3 V to DRV_{DD} + 0.3 V
Digital outputs to DRGND . . . . . –0.3 V to DRV_{DD} + 0.3 V
Operating junction temperature range, T_J . . . . . 0°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Analog Inputs					
Analog input voltage (AIN+, AIN–)		REFB		REFT	V
Input voltage, differential full scale			1		V_{pp}
Input common-mode voltage, (REFT+REFB)/2		0.8		1.1	V
Input capacitance (C_i), measured to ground			5		pF
Overvoltage recovery time, 1.8-V input voltage			10		ns
Analog input bandwidth			950		MHz
Input impedance (switch capacitor)	ADS5102		38.5		kΩ
	ADS5103		62.5		
Supplies and References					
Operating free-air temperature, T_A		–40		85	°C
Analog supply voltage, AV_{DD}		1.65	1.80	2.00	V
Digital supply voltage, DV_{DD}		1.65	1.80	2.00	V
Digital driver supply voltage, DRV_{DD}		1.65	1.80	3.6	V
Reference top voltage, VREFT		1.30	1.34	1.39	V
Reference bottom voltage, VREFB		0.78	0.81	0.84	V
Common-mode voltage, VCML		0.85	1.05	1.15	V
Bandgap voltage, VBG		1.22	1.27	1.32	V
Clock Inputs CLK					
Sampling rate	ADS5102	1		65	MSPS
	ADS5103	1		40	

electrical characteristics over recommended operating conditions, AV_{DD} = DV_{DD} = 1.8 V, DRV_{DD} = 3.3 V, F_S = 40, 65 MSPS (as appropriate)/50% duty cycle, –1 dBFS input span, C_L = 10 pF at D0–D9, internal reference, $T_{(min)}$ to $T_{(max)}$, typical data at 25°C (unless otherwise noted)

internal reference voltages

PARAMETER		MIN	TYP	MAX	UNIT
VREFT	Reference top voltage	1.30	1.34	1.39	V
VREFB	Reference bottom voltage	0.78	0.81	0.84	V
VCML	Common-mode voltage	0.85	1.05	1.15	V
VBG	Bandgap voltage	1.22	1.27	1.32	V

external reference voltages

PARAMETER		MIN	TYP	MAX	UNIT
REFT	Reference input voltage (top)	1.15	1.25	1.35	V
REFB	Reference input voltage (bottom)	0.70	0.75	0.85	V
REFT–REFB	Differential input	0.45	0.50	0.55	V
	Input resistance		200		Ω

digital outputs

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 50 μA	DRV_{DD} = 1.8 V	DRV_{DD} – 0.1			V
			DRV_{DD} = 3.3 V	DRV_{DD} – 0.2			
V_{OL}	Low-level output voltage	I_{OL} = 50 μA	DRV_{DD} = 1.8 V			0.1	V
			DRV_{DD} = 3.3 V			0.2	
C_L	External load capacitance				15		pF

digital inputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	DRV_{DD} = 1.8 V	0.8 × DRV_{DD}			V
		DRV_{DD} = 3.3 V	0.8 × DRV_{DD}			
V_{IL}	Low-level input voltage	DRV_{DD} = 1.8 V			0.2 × DRV_{DD}	V
		DRV_{DD} = 3.3 V			0.2 × DRV_{DD}	
I_{IH}	High-level input current	V_{IH} = DRV_{DD}			±5	μA
I_{IL}	Low-level input current	V_{IL} = 0 V			±5	μA

dc accuracy

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
(INL)	Integral nonlinearity	ADS5102			±1	±2.5	LSB
		ADS5103			±0.5	±1.5	LSB
(DNL)	Differential nonlinearity	ADS5102			±0.5	±1	LSB
		ADS5103			±0.4	±0.8	LSB
	Missing code			No missing code assured			
	Offset error		REFT = 1.25 V, REFB = 0.75 V		±0.4	±1.5	%FSR
	Gain error		REFT = 1.25 V, REFB = 0.75 V		±1.4	±2	%FSR

electrical characteristics over recommended operating conditions, AV_{DD} = DV_{DD} = 1.8 V, DRV_{DD} = 3.3 V, F_S = 40, 65 MSPS (as appropriate)/50% duty cycle, –1 dBFS input span, C_L = 10 pF at D0–D9, internal reference, $T_{(min)}$ to $T_{(max)}$, typical data at 25°C (unless otherwise noted) (continued)

dynamic performance

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	ADS5102	f = 3.5 MHz	8.7	9.2		Bits
			f = 20 MHz		9		
		ADS5103	f = 3.5 MHz	9.0	9.3		Bits
			f = 20 MHz		9.2		
SFDR	Spurious free dynamic range	ADS5102	f = 3.5 MHz	58	73		dBc
			f = 20 MHz		71		
		ADS5103	f = 3.5 MHz	64	69		dBc
			f = 20 MHz		66		
THD	Total harmonic distortion	ADS5102	f = 3.5 MHz		–71	–55	dBc
			f = 20 MHz		–71		
		ADS5103	f = 3.5 MHz		–65	–62	dBc
			f = 20 MHz		–68		
SNR	Signal-to-noise ratio	ADS5102	f = 3.5 MHz	56	58		dBc
			f = 20 MHz		57		
		ADS5103	f = 3.5 MHz	57	59		dBc
			f = 20 MHz		58		
SINAD	Signal-to-noise and distortion	ADS5102	f = 3.5 MHz	54	58		dBc
			f = 20 MHz		57		
		ADS5103	f = 3.5 MHz	56	58		dBc
			f = 20 MHz		57		

power supply†

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Operating voltage	AV_{DD}		1.65	1.8	2	V
		DV_{DD}		1.65	1.8	2	
		DRV_{DD}		1.65	1.8	3.6	
$I(AV_{DD})$	Analog supply current	ADS5102	AV_{DD} = DV_{DD} = 1.8 V, DRV_{DD} = 3.3 V		70	80	mA
		ADS5103			45	53	
$I(DV_{DD})$	Digital supply current	ADS5102	AV_{DD} = DV_{DD}= 1.8 V, DRV_{DD} = 3.3 V		8	9	mA
		ADS5103			5	7	
$I(DRV_{DD})$	Output driver supply current	ADS5102	AV_{DD} = DV_{DD} = 1.8 V, DRV_{DD} = 3.3 V		6.5	8	mA
		ADS5103			4.8	5.5	
$I_{(TOTAL)}$	Total current consumption	ADS5102	AV_{DD} = DV_{DD} = 1.8 V, DRV_{DD} = 3.3 V		84	97	mA
		ADS5103			54	66	
P_D	Power dissipation	ADS5102	AV_{DD} = DV_{DD} = 1.8 V, DRV_{DD} = 3.3 V		160	188	mW
		ADS5103			105	126	
	Standby power		CLK running		336	390	µW
	Power supply rejection				0.25		%FS

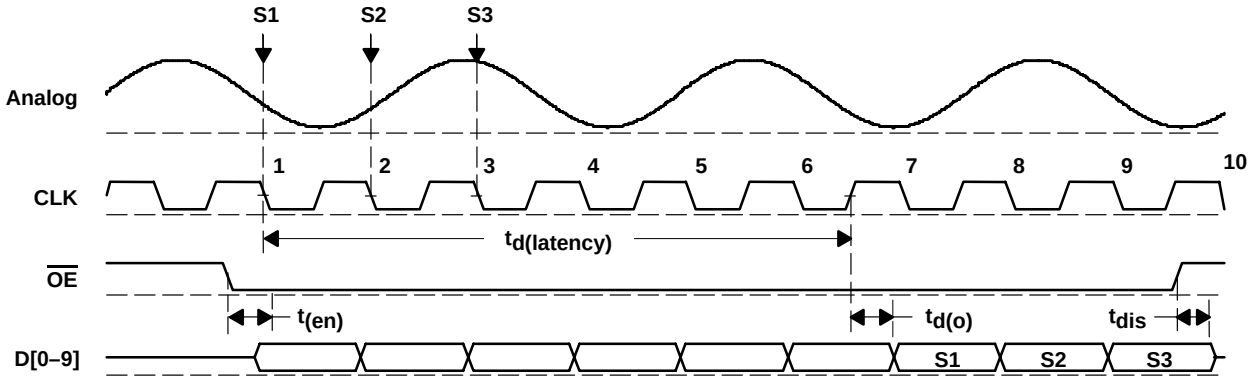
† Sinewave input, f_i = 3.5 MHz, –1 dBFS input span

electrical characteristics over recommended operating conditions, AV_{DD} = DV_{DD} = 1.8 V, DRV_{DD} = 3.3 V, F_S = 40, 65 MSPS (as appropriate)/50% duty cycle, –1 dBFS input span, C_L = 10 pF at D0–D9, internal reference, $T_{(min)}$ to $T_{(max)}$, typical data at 25°C (unless otherwise noted) (continued)

timing characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Clock duty cycle			50 ±10		%
$t_{d(o)}$	Output propagation delay			9	12	ns
$t_{(en)}$	$\overline{OE}$ ↓ to outputs enabled time			6		ns
t_{dis}	$\overline{OE}$ ↑ rising to outputs 3-state disable time			10		ns
$t_{d(latency)}$	Pipeline latency			5.5		cyc
$t_{d(ap)}$	Aperture delay			1		ns
	Aperture uncertainty			2		ps rms

timing diagram



TYPICAL CHARACTERISTICS

ADS5102
ANALOG SUPPLY CURRENT
vs
TEMPERATURE

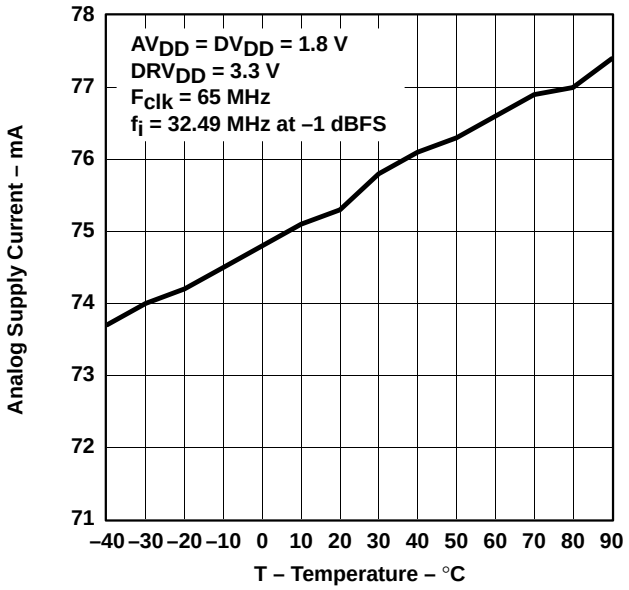


Figure 1

ADS5103
ANALOG SUPPLY CURRENT
vs
TEMPERATURE

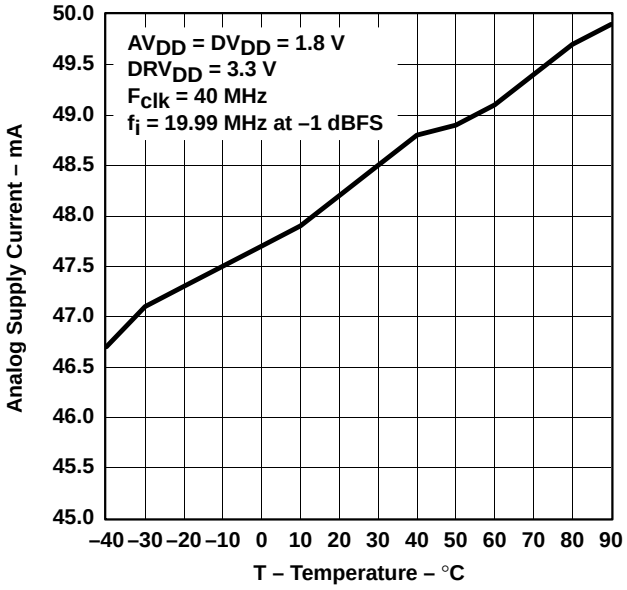


Figure 2

ADS5102
DIGITAL SUPPLY CURRENT
vs
TEMPERATURE

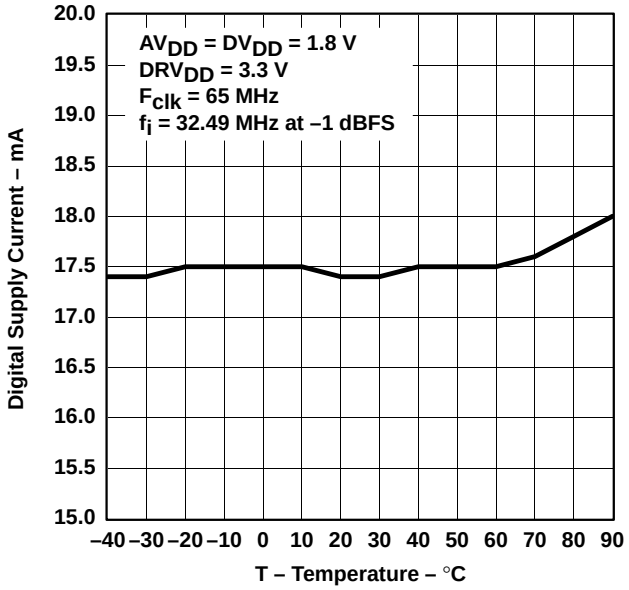


Figure 3

ADS5103
DIGITAL SUPPLY CURRENT
vs
TEMPERATURE

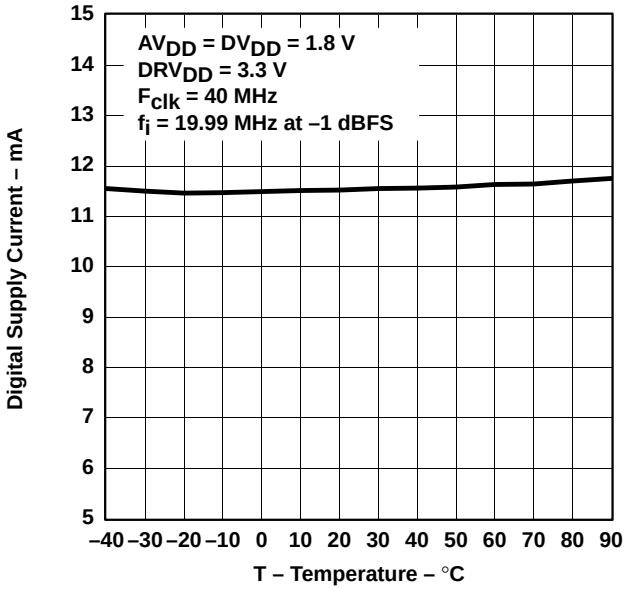


Figure 4

TYPICAL CHARACTERISTICS

ADS5102
INTEGRAL NONLINEARITY
vs
TEMPERATURE

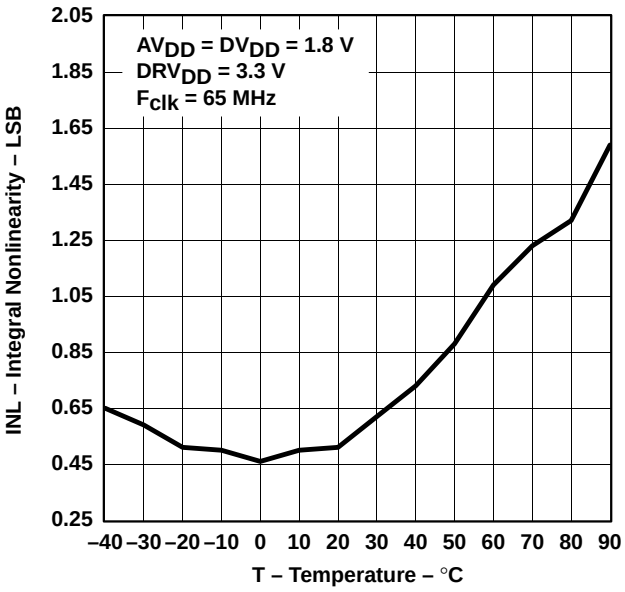


Figure 5

ADS5103
INTEGRAL NONLINEARITY
vs
TEMPERATURE

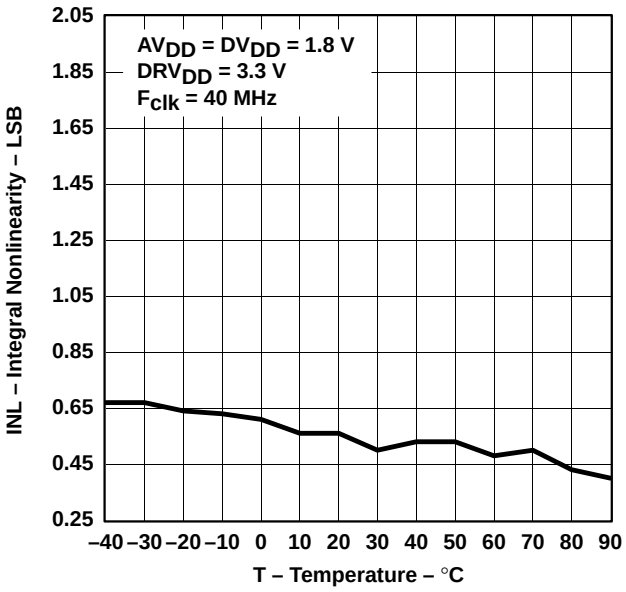


Figure 6

ADS5102
DIFFERENTIAL NONLINEARITY

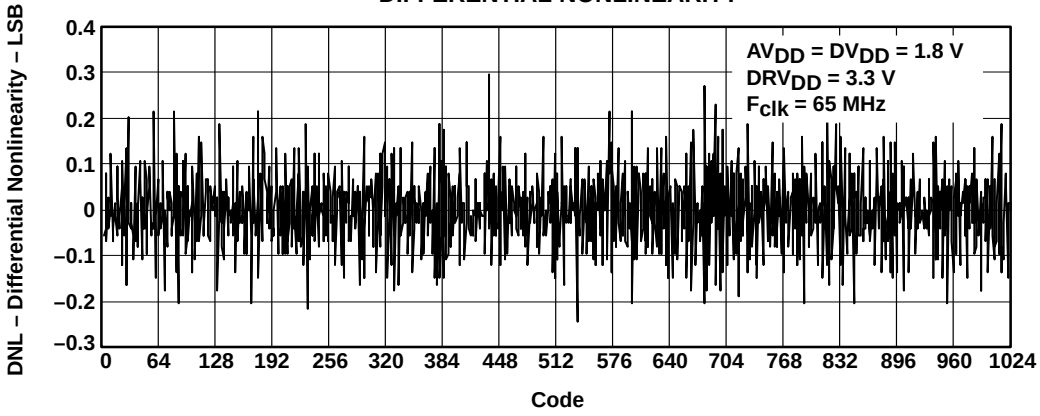


Figure 7

TYPICAL CHARACTERISTICS

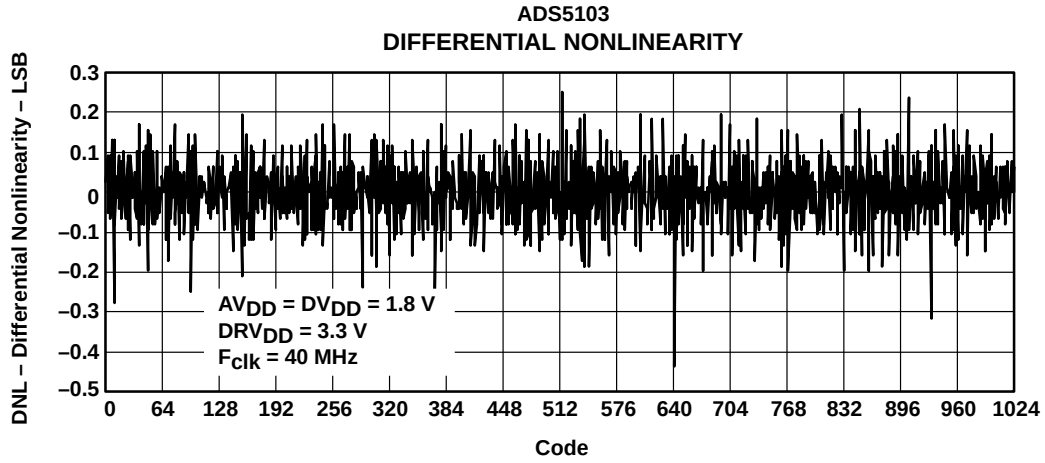


Figure 8

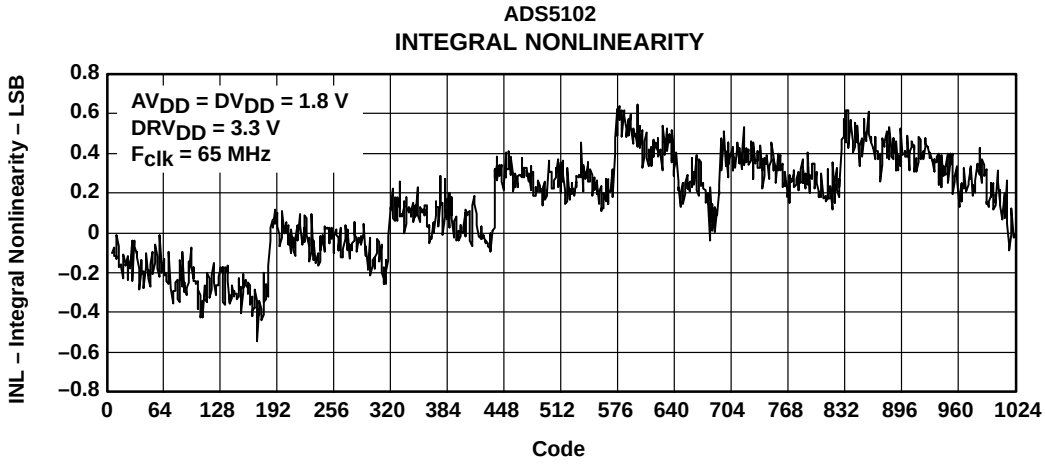


Figure 9

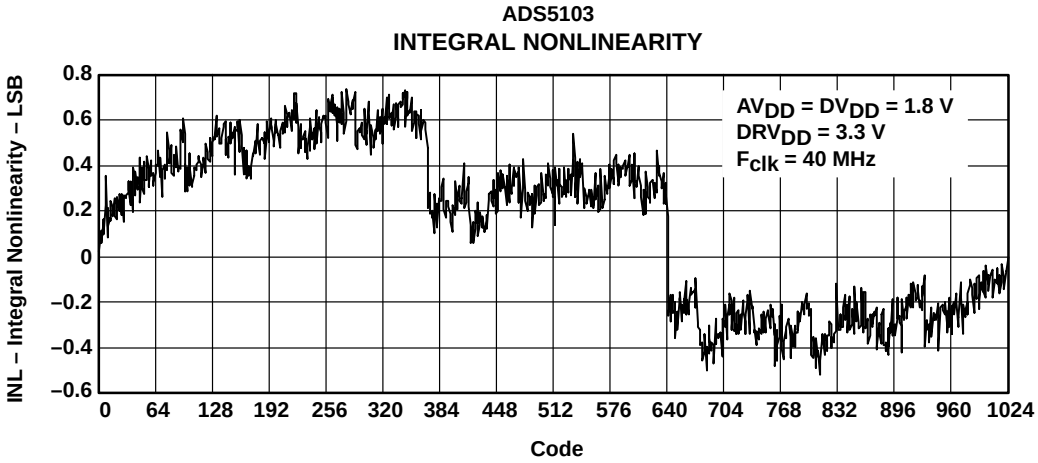


Figure 10

TYPICAL CHARACTERISTICS

ADS5102
INTERNAL VREF VALUES
vs
ANALOG SUPPLY VOLTAGE

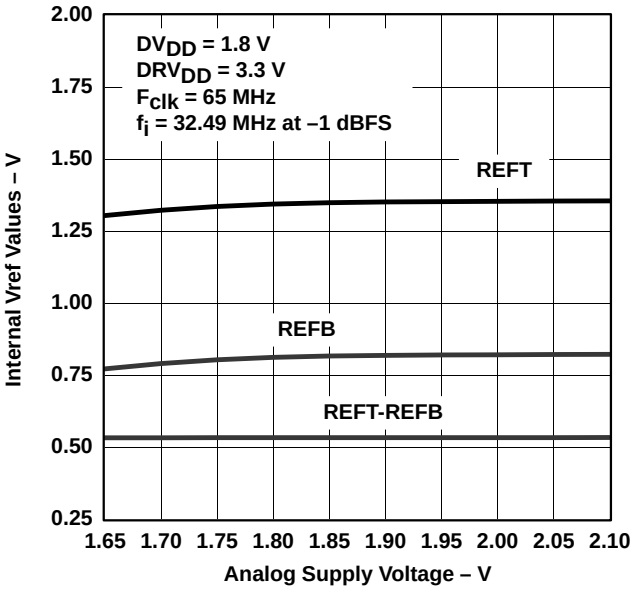


Figure 11

ADS5102
INTERNAL VREF VALUES
vs
TEMPERATURE

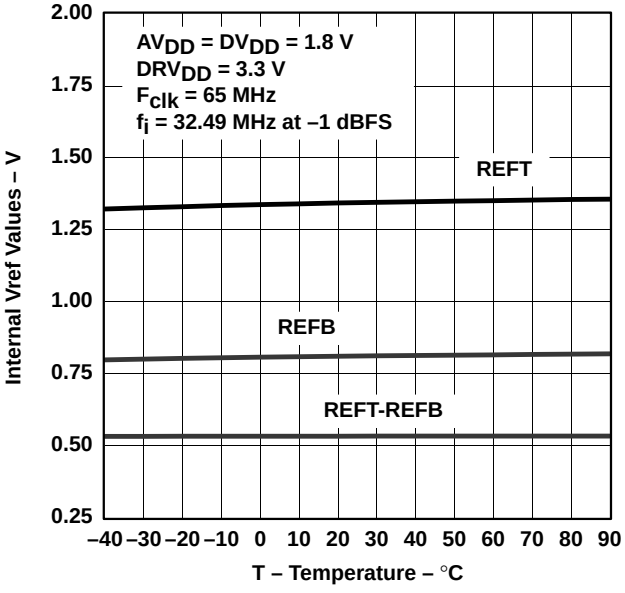


Figure 12

ADS5102
SPURIOUS FREE DYNAMIC RANGE
vs
ANALOG INPUT LEVEL

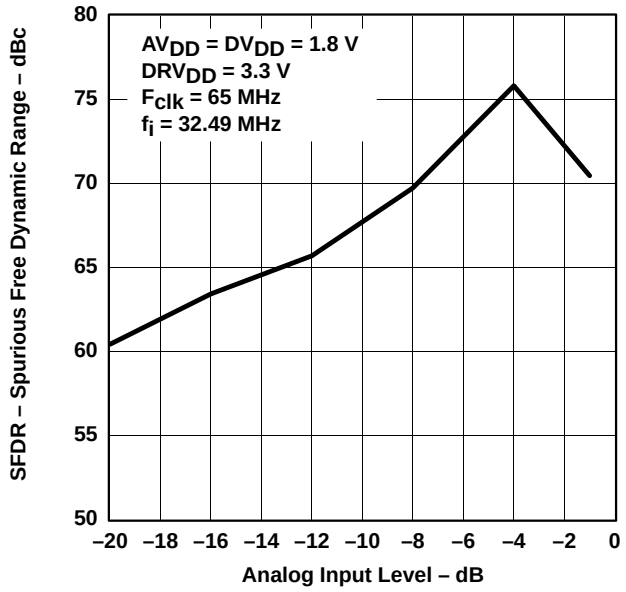


Figure 13

ADS5103
SPURIOUS FREE DYNAMIC RANGE
vs
ANALOG INPUT LEVEL

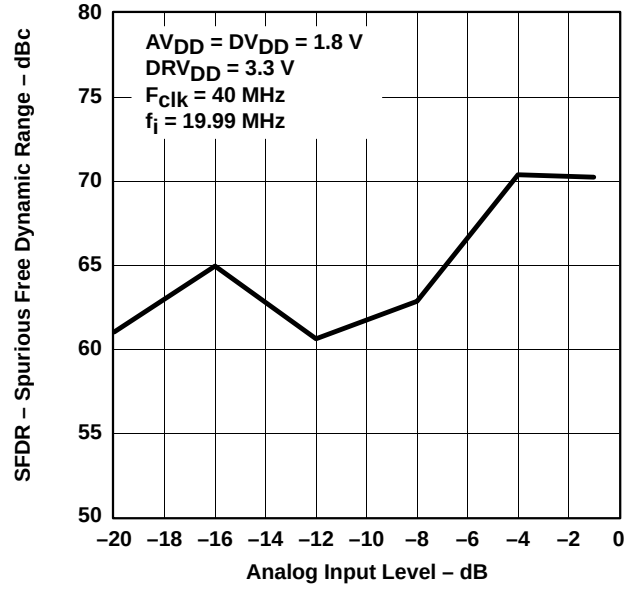


Figure 14

TYPICAL CHARACTERISTICS

ADS5102
TOTAL HARMONIC DISTORTION
vs
ANALOG INPUT FREQUENCY

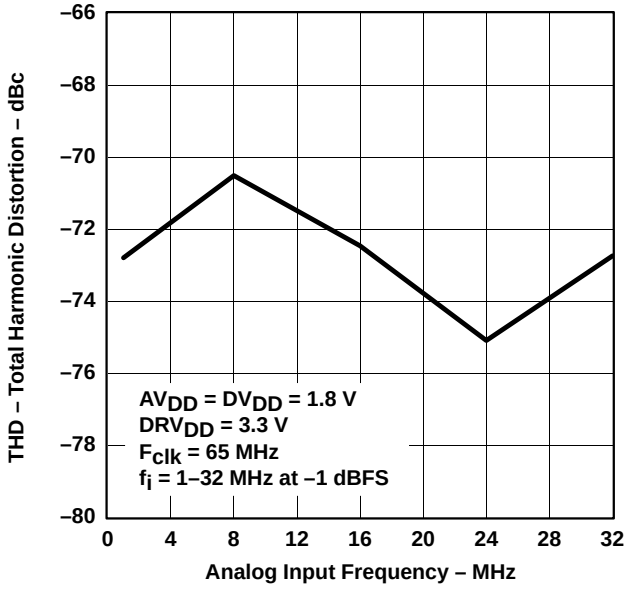


Figure 15

ADS5103
TOTAL HARMONIC DISTORTION
vs
ANALOG INPUT FREQUENCY

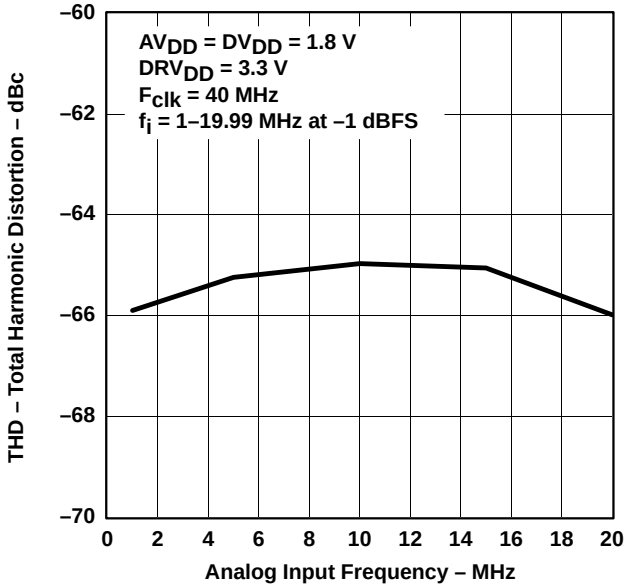


Figure 16

ADS5102
SIGNAL-TO-NOISE RATIO
vs
ANALOG INPUT FREQUENCY

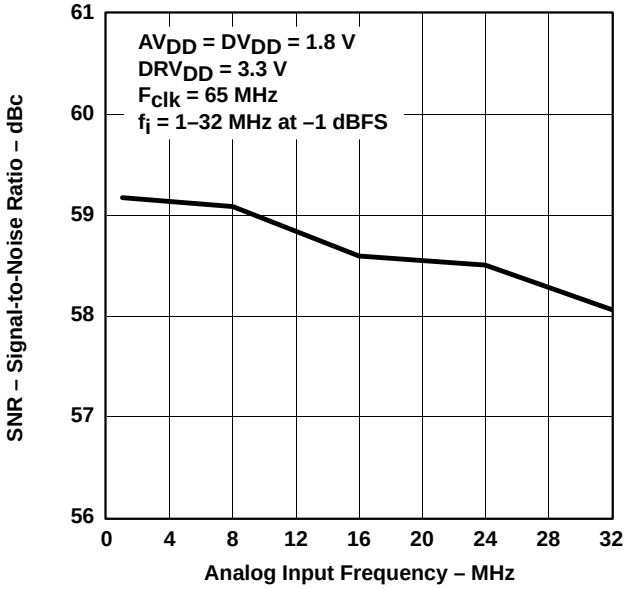


Figure 17

ADS5103
SIGNAL-TO-NOISE RATIO
vs
ANALOG INPUT FREQUENCY

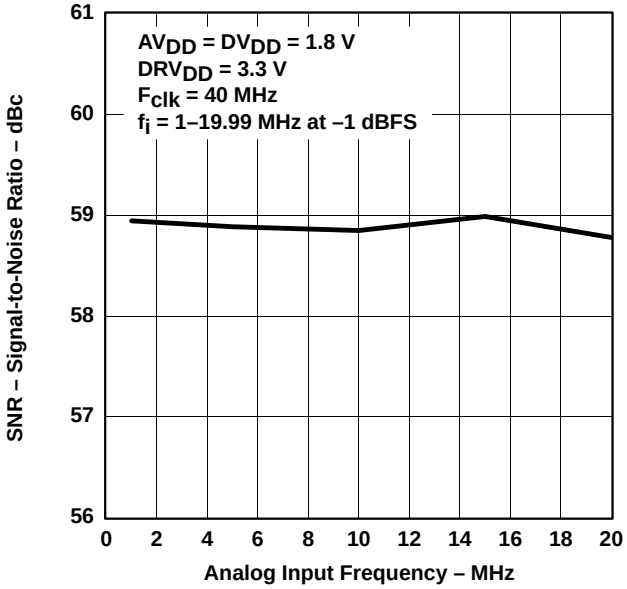


Figure 18

TYPICAL CHARACTERISTICS

ADS5102
SIGNAL-TO-NOISE RATIO and DISTORTION
vs
ANALOG INPUT FREQUENCY

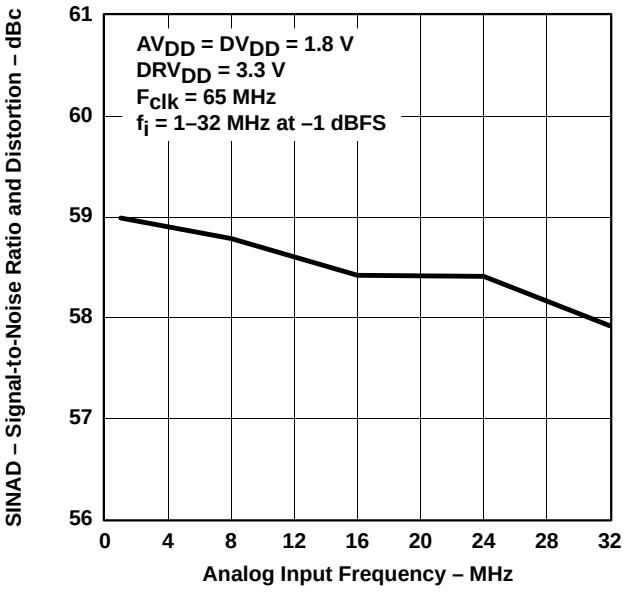


Figure 19

ADS5103
SIGNAL-TO-NOISE RATIO and DISTORTION
vs
ANALOG INPUT FREQUENCY

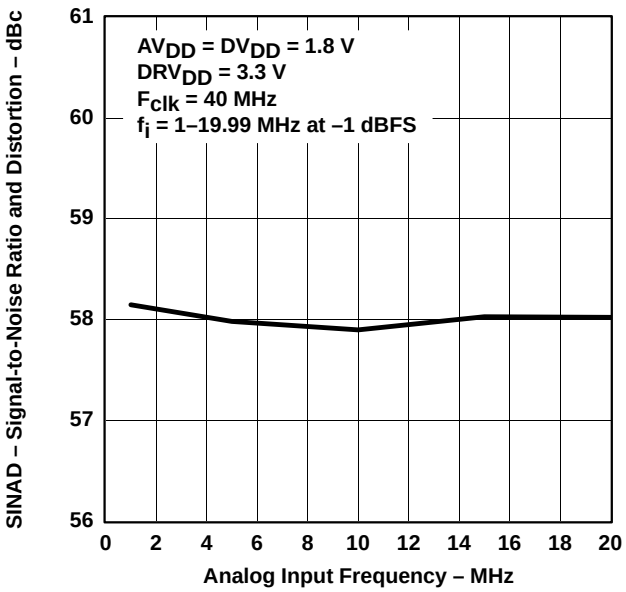


Figure 20

ADS5102
EFFECTIVE NUMBER OF BITS
vs
ANALOG INPUT FREQUENCY

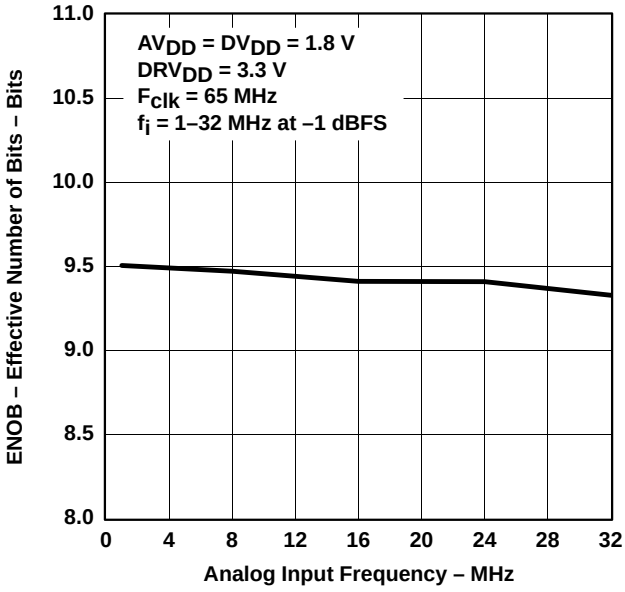


Figure 21

ADS5103
EFFECTIVE NUMBER OF BITS
vs
ANALOG INPUT FREQUENCY

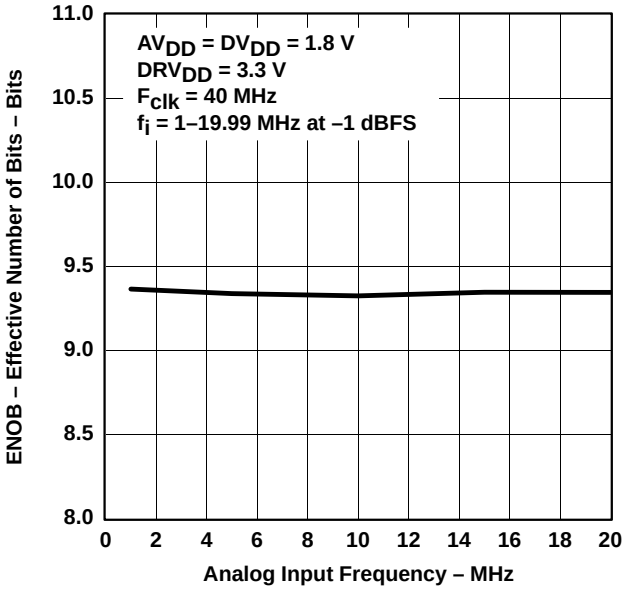


Figure 22

TYPICAL CHARACTERISTICS

ADS5102
SPURIOUS FREE DYNAMIC RANGE
vs
ANALOG INPUT FREQUENCY

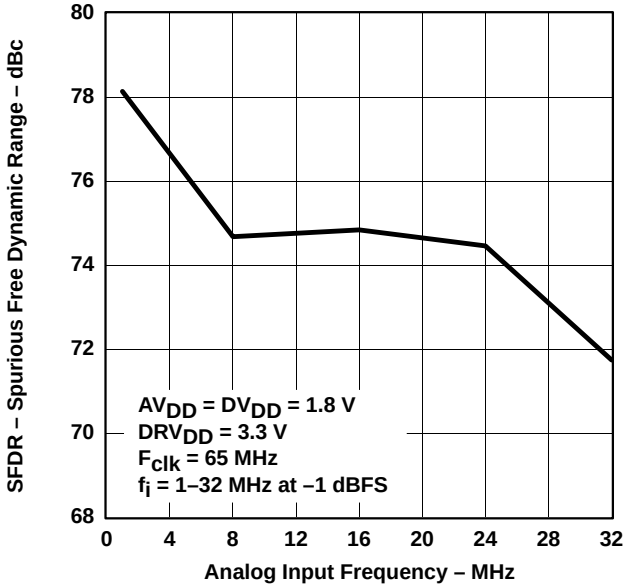


Figure 23

ADS5103
SPURIOUS FREE DYNAMIC RANGE
vs
ANALOG INPUT FREQUENCY

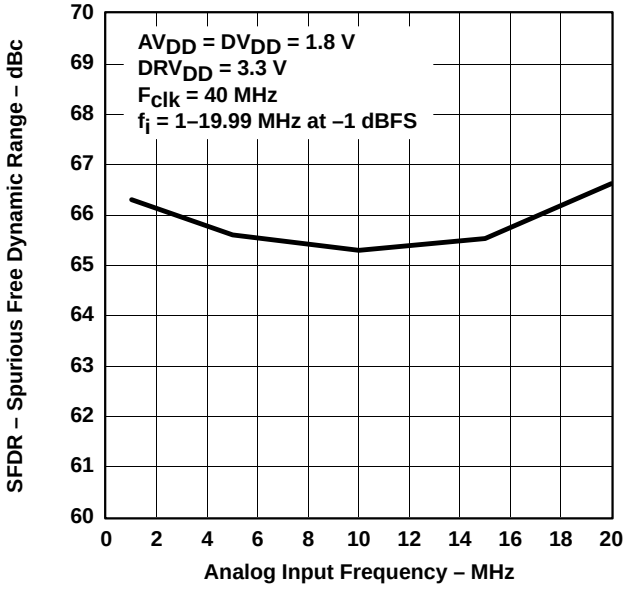


Figure 24

ADS5102
SFDR, SINAD
vs
CLOCK DUTY CYCLE

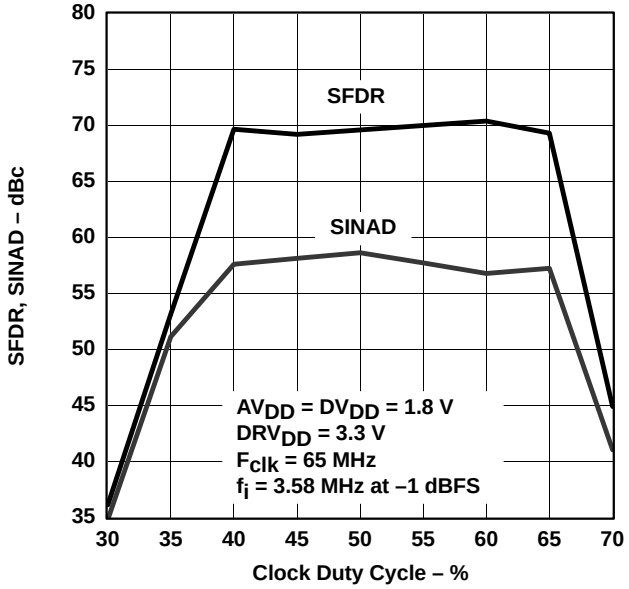


Figure 25

ADS5103
SFDR, SINAD
vs
CLOCK DUTY CYCLE

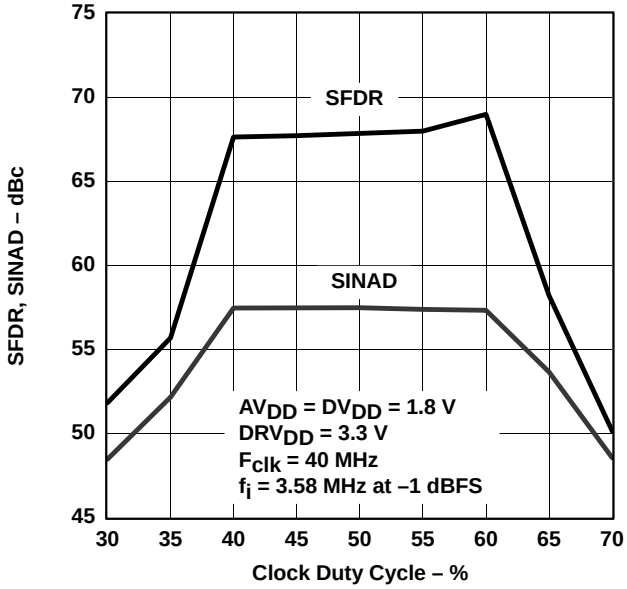


Figure 26

TYPICAL CHARACTERISTICS

ADS5102
SFDR, SINAD
vs
CLOCK DUTY CYCLE

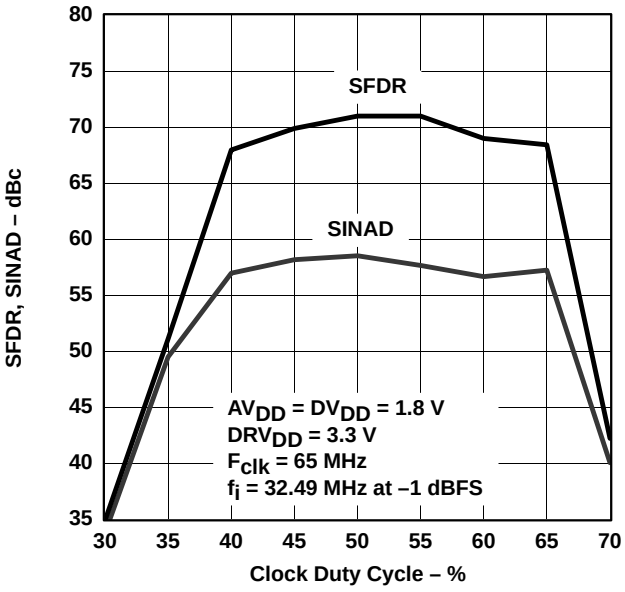


Figure 27

ADS5103
SFDR, SINAD
vs
CLOCK DUTY CYCLE

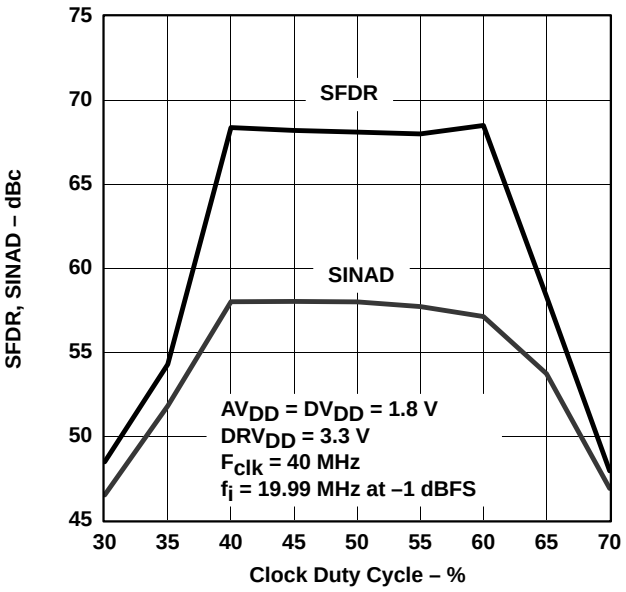


Figure 28

PRINCIPLES OF OPERATION

analog-to-digital converter

The ADS5102/3 is designed using a switched capacitor pipeline architecture fabricated in CMOS process. The pipeline architecture is implemented with 10 stages, thus allowing for high conversion speed and exceptionally low power. Each of these 10 stages produces one digital bit per stage. Both rising and falling edges of the clock are used so the signal propagates thru the pipeline every half clock or five total clocks. Digital error correction uses another 1/2 clock cycle at the end; thus the total pipeline latency is 5.5 clocks. (Refer to timing diagram on page 7)

10-stage operation

The signal is sampled by the SHA. The first stage is digitized by 1.5 bits and sent to the digital error correction block. This digitized value is then applied to a DAC, which recreates the analog value that has been digitized. This value is then fed into a summing junction with the original input signal. The summing junction subtracts the converted value from the original signal. This is known as the residue voltage. This residue voltage is then amplified by a factor of 2x and transferred to the next stage. This is repeated for each of the 10 stages.

Each of the 10 pipeline stages, as well as the sample and hold amplifier, is differential in nature. This allows rejection of any common mode signal. Thus a signal seen on Ain+ and Ain– is differentially seen as 0 V on the output. This fully differential architecture allows higher ac performance of the ADC by reducing noise susceptibility.

PRINCIPLES OF OPERATION

analog input sample and hold amplifier circuit

The sample and hold amplifier is implemented using switch capacitor techniques. A simplified functional block diagram is shown in Figure 29. The SHA is in sample mode when CLK is high and in hold mode when CLK is low. In sample mode, the input switches, P1, are closed and the differential input signal is sampled onto caps Cs. An internal common-mode voltage is applied to the sampling caps (C_S) when the two P1P switches are closed. As the CLK falling edge occurs, the SHA is now placed into hold or amplification mode. In this mode, P1 switches are now opened and switches P2 are closed. This is the amplification state and the signal is transferred to the output of the amplifier with a nominal gain of 1. C_L of Figure 29 represents the load capacitance of the following stage. R-C values of the input determine the analog input bandwidth of the SHA (and therefore the whole ADC) which is 950 MHz for the ADS5102/3. This wide bandwidth assures no distortion to the Nyquist frequency of 32.5 MHz. In under sampling applications, it is common to require the analog input bandwidth to be 5 times greater than the IF Nyquist frequency. As such, the ADS5102/3 supports IF frequencies approaching 200 MHz in under sampling applications.

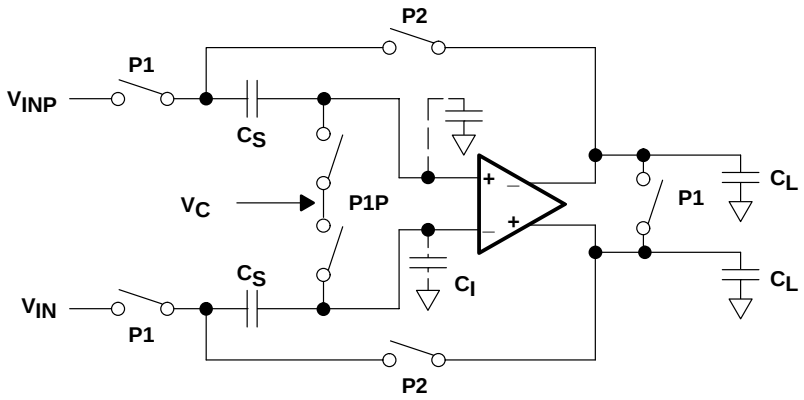


Figure 29. Simplified Functional Block Diagram

Because the input to the sample and hold amplifier is a switched capacitor circuit, the input resistance is dynamic and based on the sampling rate of the converter. The impedance of each input is defined by the equation:

$$Z_I = \frac{1}{F \times C_S}$$

Where:

C_S = Sampling capacitor = 0.4 pF typical
F = CLK frequency in Hz

The key for selecting an amplifier to correctly drive the ADS5102/3 is to ensure that the output frequency of the amplifier is much lower than the input impedance of the ADS5102/3, which at 65 MSPS is 38.46 kΩ . For system accuracy comparable to 1 LSB, this means selecting an amplifier with output impedance of ~ 31 Ω for sampling rates of 65 MSPS.

reference configurations

The ADS5102/3 provides an internal voltage reference which should be suitable for most 10 bit systems. The typical full scale voltage for the device is determined by VFS = VREFT – VREFB. Since the input is fully differential, the full scale input is twice the single ended value or 1 V differential. It is recommended to externally de-couple both VREFT and VREFB with a 0.1 µF capacitor to bypass all high frequency noise to ground. It is necessary to connect BG and AV_{DD} with a 100 kΩ resistor and decouple with a 1 µF capacitor to AGND (refer to Figure 30 for correct configuration).

PRINCIPLES OF OPERATION

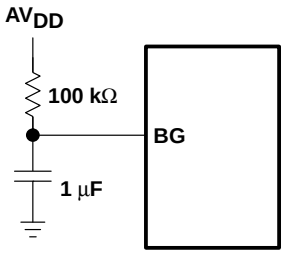


Figure 30. BG Reference Configuration

For systems that require more absolute accuracy or lower temperature coefficient drift than provided by the internal VREF, an external voltage reference can be applied to the VREFB and VREFT inputs. To use external reference, connect the PDREF pin to a logic high and this internally disconnects the VREF from the ADC. In this mode it is also necessary to connect the BG and REFT pins together on the PWB. It is recommended to use the input levels of VREFB = 0.75 V and VREFB = 1.25 V to achieve optimum ADC performance. It is also recommended to apply a common-mode voltage to the input of 1 V.

clock input

The clock input is designed for 1.8 V or 3.3 V CMOS logic levels (depends on DR_{VDD}) and it is recommended to use standard CMOS logic levels as inputs. The logic threshold internally is set to $DRV_{DD}/2$ or nominally 1.65 V. Since both edges of the clock are used in the switch capacitor architecture, it is important to provide a clock with (ideally) a 50% duty cycle. The performance variation with clock duty cycle can be examined from Figures 25, 26, 27 and 28.

Clock jitter is also important for performance of the ADC to be maintained. Any clock jitter appears as noise when sampling input frequencies. Clock Jitter reduces the signal to noise ratio (SNR) and is more severe as the input frequency increases. The theoretical SNR limits based on clock jitter can be calculated as follows:

$$\text{Theoretical SNR}_{(\text{clock jitter})}\ (\text{dB}) = 20 \log \left(\frac{1}{2 \times \pi \times F_I \times \text{CLK}_{(\text{jitter})}} \right)$$

Where:

F_I = Highest input frequency to the ADC in Hz
$\text{CLK}_{(\text{jitter})}$ = the amount of jitter on the clock in sec

Therefore for a Nyquist frequency input of 32.5 MHz and a design trying to achieve the most available performance from the ADS5102/3, the clock jitter must be less than 3.98 ps rms. In under sampling applications, the same equations apply and clock jitter becomes more critical and may be the limiting factor in system performance. The aperture jitter of the SHA also contributes to overall jitter. For worst case designs, the jitter of clock and aperture can be considered to add in quadrature, i.e.

Total Jitter = Square root of ($\text{CLK}_{\text{jitter}}^2$ + $\text{Aperture}_{\text{jitter}}^2$)

The aperture jitter of the ADS5103 is 2 ps rms and at frequencies approaching Nyquist, the total jitter should be accounted for.

PRINCIPLES OF OPERATION

digital outputs

The outputs of the ADS5102/3 are also CMOS and are programmable for either 3.3 V or 1.8 V CMOS logic levels. This is controlled by the DRV_{DD} supply. Either 3.3 V or 1.8 V can be applied to DRV_{DD} with excellent results. The output format is offset binary with D0 (LSB) and D9 (MSB). See Table 1 for output coding with a differential input signal applied. There is a 5.5 clock latency from the sampling to valid data output on D0–D9.

The outputs can be placed into active mode by taking $\overline{OE}$ low or 3-state by taking $\overline{OE}$ high. The timing relations between $\overline{OE}$ and output bus enable/disable times are shown in the timing diagram (refer to page 7). The capacitive loading on the digital outputs is very important to achieve best performance. The total load capacitance is typically made up of two sources, next stage input capacitance and PWB etch run capacitance. The total capacitance of these two loads should be held to less than 15 pF. If for some reason, this cannot be met, it is recommended to use logic buffers such as ‘244 placed physically very close to the ADC output. This isolates the ADC output from the load capacitance and performance specs are achieved. Another technique is to place a small resistor in series with the outputs. This resistance dampens the current spikes into the capacitive loads and thus improve ADC performance. The value of this resistor varies with sampling rate but generally 22 Ω is a good value. Again this depends on the load capacitance.

The digital output of these devices is offset binary and follows the following format.

Table 1. Output Coding

ANALOG INPUT IN +	SIGNAL VOLTAGE IN –	STEP	DIGITAL OUTPUT CODE MSB									LSB
REFT†	REFB†	1023	1	1	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•
(REFT – REFB) / 2	(REFT – REFB) / 2	512	1	0	0	0	0	0	0	0	0	0
•	•	511	0	1	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•
REFB	REFT	0	0	0	0	0	0	0	0	0	0	0

† Where there is either an internal voltage reference or an external voltage reference applied to the REFT and REFB pins.

driving the analog input

Since many real world signals are single ended and most modern high speed ADC’s employ differential inputs, it is necessary in many cases to perform single ended to differential conversion prior to the ADC. Also, the ADC performs optimally if a differential signal is applied to the inputs. In some cases, signal conditioning is required in the form of the amplification or filtering. The two preferred techniques for driving the ADC input are: 1) With an active amplifier specifically designed to drive ADC’s; 2) With an RF transformer.

driving the analog input with a differential amplifier

Texas Instruments has developed a family of high quality operational amplifiers that have been designed specifically for driving the input stage of modern ADC’s. These devices allow for amplification and filtering prior to the ADC. This stage can be used to set the maximum signal voltage to match the full scale input of the ADC. The best solution for driving the ADS5102/3 ADC’s is the THS4501 amplifier. Figure 31 shows how to use this device with a gain of 2. The ADC common mode output voltage can be directly connected to the op amp to provide the proper levels. The THS4501 provides optimum matching of op amp output to the input of the ADS5102/3. This configuration provides signal amplification, filtering, and single-ended to differential conversion. It is recommended to provide de-coupling capacitors of 0.1 μF and 0.001 μF on the CML output. This filters out any high frequency noise prior the ADC input.

PRINCIPLES OF OPERATION

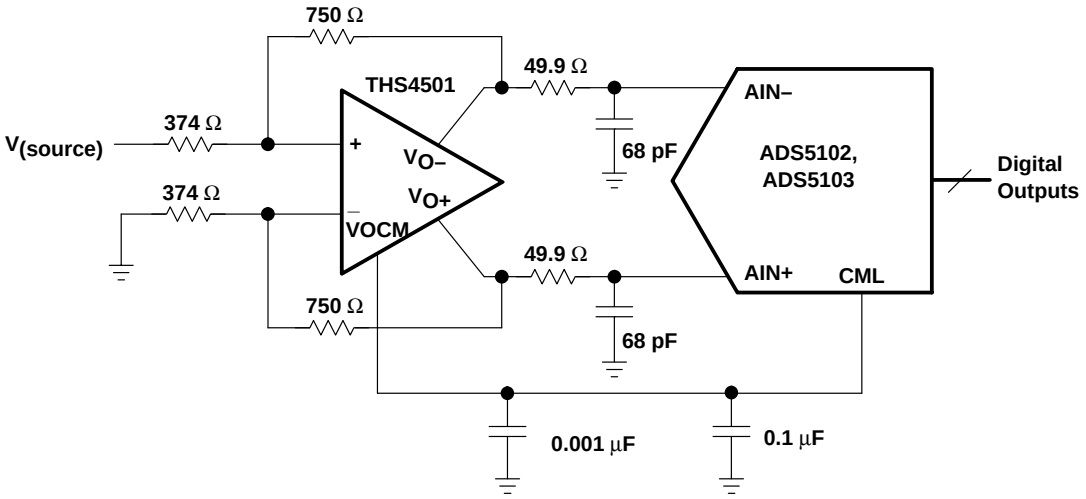


Figure 31. Driving the ADS5102/3 With Differential Amp (Gain = 2)

driving the analog input with a transformer

When little or no signal conditioning is required, a simple transformer is an excellent way to drive the input of the ADS5102/3 family. The transformer provides single-ended to differential conversion and at frequencies under 200 MHz produces very little distortion of the incoming signal. Figure 32 shows the preferred circuit diagram for implementing a transformer-coupled input. The signal source is ac-coupled and fed to the primary side of the RF transformer. Since the ADC input must be biased to the correct common mode voltage, the CML output of the ADC is connected to the secondary center tap. It is recommended to provide decoupling capacitors of 0.1 μF and 0.001 μF on the CML output. This filters out any high frequency noise prior the ADC input.

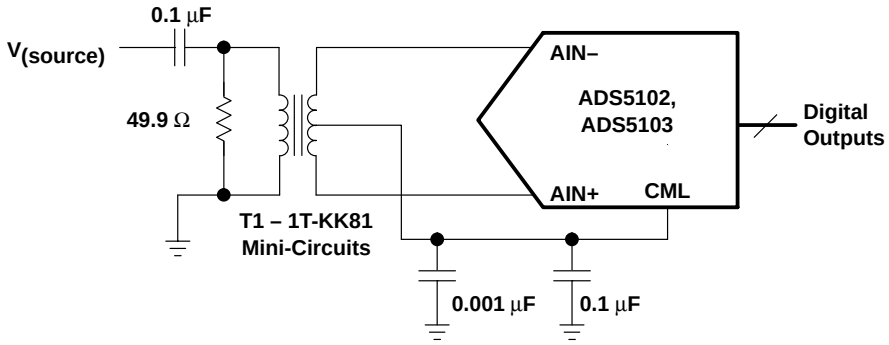


Figure 32. Driving the ADS5102/3 With a Transformer

PRINCIPLES OF OPERATION

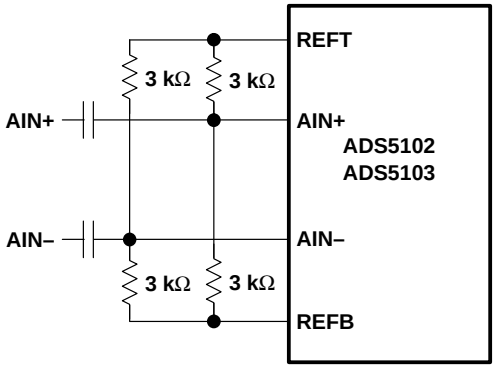


Figure 33. Driving the Analog Inputs

setting the bias resistor—RBIAS

Each device in this family requires an external resistor be connected from pin 14 to ground. The value of this resistor is determined by which device is being used. Refer to Table 2 for the correct resistor value. This resistor only dissipates less than 1 mW of power. The resistor accuracy of 1% is adequate.

Table 2. Resistor Value

DEVICE	RBIAS VALUE	CONNECT FROM
ADS5103	8.25 kΩ	Pin 14 to AGND
ADS5102	4.42 kΩ	

DEFINITION OF SPECIFICATIONS

Analog Input Bandwidth—The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay—The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.

Aperture Uncertainity (Jitter)—The sample-to-sample variation in aperture delay**.**

Differential Nonlinearity (DNL)—The maximum deviation of any single LSB transition at the digital output from an ideal 1 LSB step at the analog input. Ideally, each transition step is 1 LSB wide. DNL is the measured error from theoretical in step size. A DNL of less than –1 LSB implies no missing codes.

Integral Nonlinearity (INL)—is the summation of the differential nonlinearity errors and indicates the worst case deviation from an *best fit straight line* that is drawn from 1/2 LSB of the first transition to 1/2 LSB above the last transition. The best fit is determined using the least squares curve fitting method.

Duty Cycle—is the ratio of the clock time high over the full clock period (time high plus time low) and then also the time low over the total clock period. At a given clock rate, these specs define the acceptable duty cycle allowed on the clock.

Sampling Rate (Fs)—The rate at which the converter tested to ensure conversion of analog signals to digital. The maximum rate specified is the rate and which the device is production tested to ensure performance specs are met. Expressed in mega samples per second (MSPS).

Output Propagation Delay—The delay between the 50% point of the falling edge of clock signal and the time when all output data bits are within valid logic levels.

Offset Error—In an ideal ADC the first transition from 0000000000 should occur at 1/2 LSB above REFB. Offset Error is defined as the difference between this ideal first transition and the voltage level where the first transition actually occurs. Expressed in % full scale range (%FSR) but may also be expressed in volts. This can be thought of as shifting the transfer function either left or right along the X-axis.

Overvoltage Recovery Time—The amount of time required for the converter to recover to 0.2% accuracy after an analog input signal 150% of full scale is reduced to midscale.

Power Supply Rejection Ratio—The ratio of a change in input offset voltage to a change in power supply voltage.

Total Harmonic Distortion (THD)—The ratio of the peak signal amplitude to the summation of the harmonic components. This is expressed in – dB. THD = 20 Log [input amplitude/(summation of harmonic bins)]. For calculation purposes, the first 7 harmonics are included in the calculations.

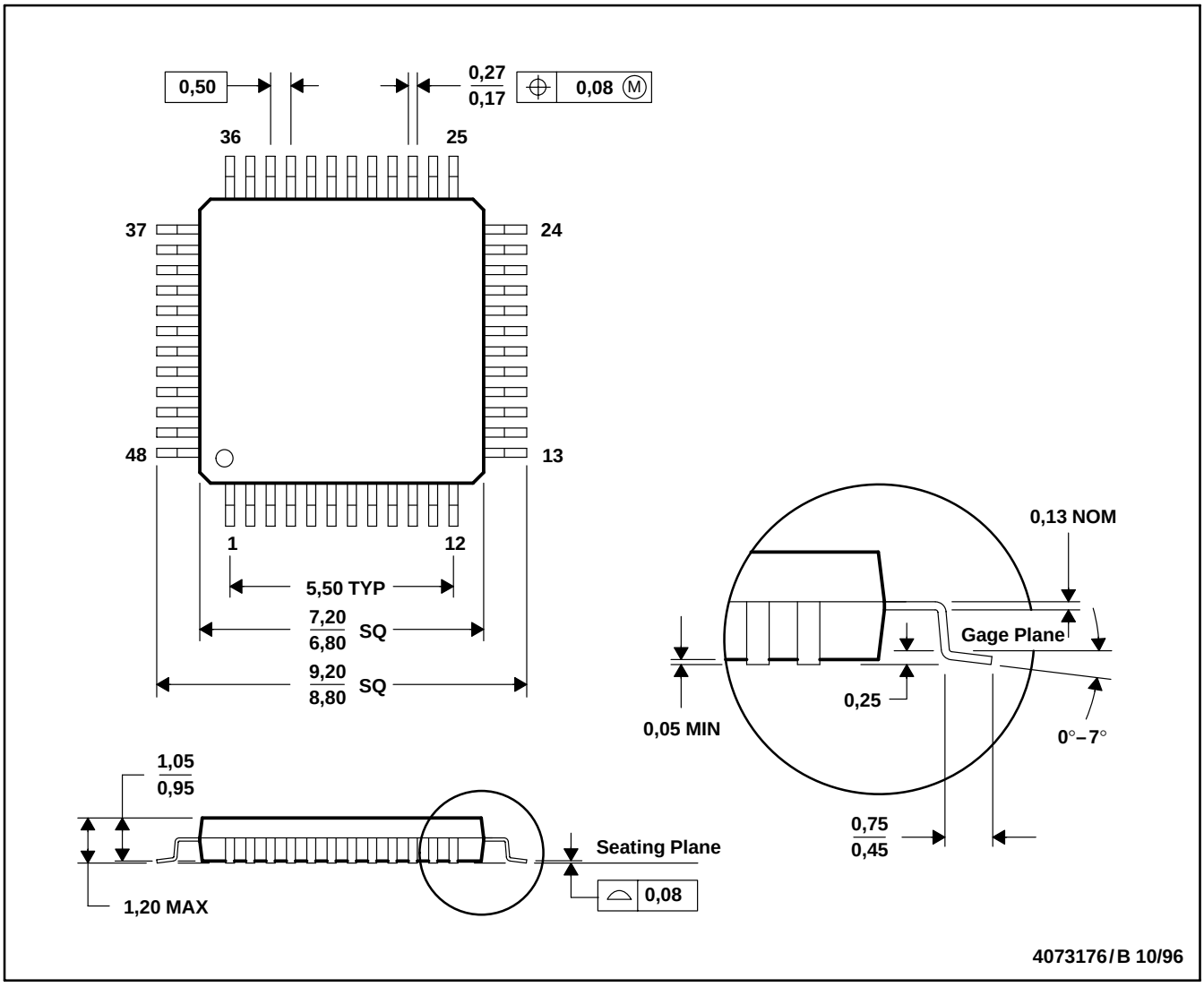
Signal To Noise Distortion (SINAD)—The ratio of the rms signal amplitude (set 1 dB below full scale) to rms value of the sum of all other spectral noise and harmonic components, but excluding dc**.**

Signal to Noise Ratio (SNR)—The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the the sum of all other spectral components, excluding the first five harmonics and dc. Reported in dB**.**

Spurious Free Dynamic Range (SFDR)—The difference between the peak amplitude of a fundamental input sine wave and the largest peak spurious component that appears, excluding dc and the input. The peak spurious component may or may not be a harmonic frequency. May be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (always related back to converter full scale).

MECHANICAL DATA

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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