78Q2120C
10/100BASE-TX Transceiver

DATA SHEET

January 2009

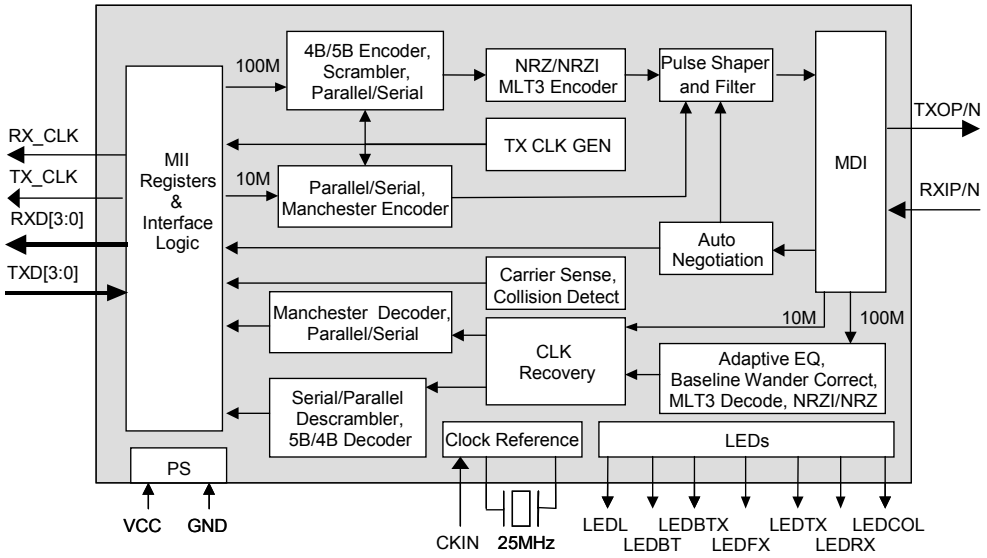
DESCRIPTION

The 78Q2120C is a 10BASE-T/100BASE-TX Fast Ethernet transceiver. It includes integrated MII, ENDECs, scrambler/descrambler, dual-speed clock recovery, and full-featured auto-negotiation function. The transmitter includes an on-chip pulse-shaper and a low-power line driver. The receiver has an adaptive equalizer and a baseline restoration circuit required for accurate clock and data recovery. The transceiver interfaces to Category-5 unshielded twisted pair (Cat-5 UTP) cabling for 100BASE-TX/10BASE-T and Category-3 unshielded twisted pair for 10BASE-T. Connection to the line media is via 1:1 isolation transformers. No external filter is required. Interface to the MAC is accomplished through an IEEE-802.3 compliant Media Independent Interface (MII). The product is fabricated in an advanced CMOS process for high performance and low power operation.

FEATURES

- **10BASE-T/100BASE-TX IEEE-802.3 compliant TX and RX functions requiring a dual 1:1 isolation transformer interface to the line**
- **Integrated MII, 10BASE-T/100BASE-TX ENDEC, 100BASE-TX scrambler/descrambler, and full-featured auto-negotiation function**
- **Full duplex operation capable**
- **PCS Bypass supports 5-bit symbol interface**
- **Register-programmable transmit amplitude**
- **Dual speed digital clock recovery**
- **Automatic polarity correction during auto-negotiation and 10BASE-T signal reception**
- **Power-saving and power-down modes including transmitter disable**
- **LED indicators: LINK, TX, RX, COL, 100, 10, FDX**
- **User programmable Interrupt pin**
- **64-Pin TQFP (JEDEC LQFP) package**
- **Single 3.3 V ± 0.3V Supply**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

GENERAL

Power Management

The 78Q2120C has three power saving modes:

- Chip Power-Down
- Receive Power Management
- Transmit High Impedance Mode

Chip power-down is activated by setting the PWRDN bit in MII register MR0.11 or pulling high the PWRDN pin. When the chip is in the power-down mode, all on-chip circuitry is shut off, and the device consumes minimum power. While in the power-down state, the 78Q2120C still responds to management transactions.

Receive power management (RXCC mode) is activated by setting the RXCC bit in MII register MR16.0. In this mode of operation, the adaptive equalizer, the clock recovery phase lock loop (PLL), and all other receive circuitry will be powered down when no valid MLT-3 signal is present at the UTP receive line interface. As soon as a valid signal is detected, all circuits will automatically be powered up to resume normal operation. During this mode of operation, RX_CLK will be inactive when there is no data being received. Note that the RXCC mode is not supported during 10BASE-T operation.

Transmit high impedance mode is activated by setting the TXHIM bit in MII register MR16.12. In this mode of operation, the transmit UTP drivers are in a high impedance state and TX_CLK is tri-stated. A weak internal pull-up is enabled on TX_CLK. The receive circuitry remains fully operational. The default state of MR16.12 is a logic low for disabling the transmit high impedance mode. The transmitter is fully functional when MR16.12 is cleared.

Analog Biasing and Supply Regulation

The 78Q2120C requires no external component to generate on-chip bias voltages and currents. High accuracy is maintained through a closed-loop trimmed biasing network.

On-chip digital logic runs off an internal voltage regulator. Hence only a single Vcc supply is required to power-up the device. The on-chip regulator is not affected by the power-down mode.

Clock Selection

The 78Q2120C will use the on-chip crystal oscillator as the clock source if the CKIN pin is tied low. In this mode of operation, a 25MHz crystal should be connected between the XTLP and XTLN pins. Alternatively, an external 25MHz clock signal can be connected to the CKIN pin. The chip senses activity on the CKIN pin, and will automatically configure itself to use the external clock. In this mode of operation, a crystal is not required and the XTLP and XTLN pins should be left floating or connected together.

Transmit Clock Generation

The transmitter uses an on-chip frequency synthesizer to generate the transmit clock. In 100BASE-TX operation, the synthesizer multiplies the reference clock by 5 to obtain the internal 125MHz serial transmit clock. In 10BASE-T mode, it generates an internal 20MHz transmit clock by multiplying the 25MHz reference clock by 4/5. The synthesizer references either the local 25 MHz crystal oscillator, or the externally applied clock, depending on the selected mode of operation.

Receive Signal Qualification

The integrated signal qualifier has separate squelch and unsquelch thresholds. It also includes a built-in timer to ensure fast and accurate signal detection and line noise rejection. Upon detection of two or more valid 10BASE-T or 100BASE-TX pulses on the line receive port, signal detect is indicated. The signal detect threshold is then lowered by about 40%. All adaptive circuits are released from their initial states and allowed to lock onto the incoming data. In 100BASE-TX operation, signal detect is de-asserted when no signal is presented for a period of about 1.2us. In 10BASE-T operation, signal detect is de-asserted whenever no Manchester data is received. In either case, the signal detect threshold will return to the squelched level whenever the signal detect indication is de-asserted. Signal detect is also used to control the operation of the clock/data recovery circuit to assure fast acquisition.

Receive Clock Recovery

In 100BASE-TX mode, the 125MHz receive clock is extracted using a digital DLL-based loop. When no receive signal is present, the CDR is directed to lock onto the 125MHz transmit serial clock. When signal detect is asserted, the CDR will use the received MLT-3 signal as the clock reference. The recovered clock is used to re-time the data signal and for conversion of the data to NRZ format.

In 10BASE-T mode, the 10MHz receive clock is recovered digitally from the Manchester data using a DLL locked to the reference clock. When Manchester-coded preambles are detected, the

CDR immediately re-aligns the phase of the clock to synchronize with the incoming data. Hence clock acquisition is fast and immediate.

100BASE-TX OPERATION

100BASE-TX Transmit

The 78Q2120C contains all of the necessary circuitry to convert the transmit MII signaling from a MAC to an IEEE-802.3 compliant data-stream driving Cat-5 UTP cabling. The internal PCS interface maps 4 bit nibbles from the MII to 5 bit code groups as defined in Table 24-1 of IEEE-802.3. These 5 bit code groups are then scrambled and converted to a serial stream before being sent to the MLT-3 pulse shaping circuitry and line driver. The pulse-shaper uses current modulation to produce the desired output waveform. Controlled rise/fall time in the MLT-3 signal is achieved using an accurately controlled voltage ramp generator. The line driver requires an external 1:1 isolation transformer to interface with the line media. The center-tap of the primary side of the transformer must be connected to the Vcc supply.

100BASE-TX Receive

The 78Q2120C receives a 125MBaud MLT-3 signal through a 1:1 transformer. The signal then goes through a combination of adaptive offset adjustment (baseline wander correction) and adaptive equalization. The effect of these circuits is to sense the amount of dispersion and attenuation caused by the cable and transformer, and restore the received pulses to logic levels. The amount of gain and equalization applied to the pulses varies with the detected attenuation and dispersion and, therefore, with the length of the cable. The 78Q2120C can compensate for cable loss of up to 10dB at 16 MHz. This loss is represented as test-chan 5 in Annex A of the ANSI X3.263:199X specification. The equalized MLT-3 data signal is bi-directionally sliced and the resulting NRZI bit-stream is presented to the CDR where it is re-timed and decoded to NRZ format. The re-timed serial data passes through a serial to parallel converter, then is descrambled and aligned into 5 bit code groups. The receive PCS interface maps these code groups to 4 bit data for the MII as outlined in Table 24-1 in Clause 24 of IEEE-802.3.

PCS Bypass Mode (Auto-negotiate must be off)

The PCS Bypass mode is entered by pulling PCSBP high or by setting register bit MR 16.1. In this mode the 78Q2120C accepts scrambled 5 bit code words at the TX_ER and TXD[3:0] pins, TX_ER being the MSB of the data input. The 5 bit code groups are converted to MLT-3 signal for transmission.

The received MLT-3 signal is converted to 5 bit NRZ code groups and output from the RX_ER and RXD[3:0] pins, RX_ER being the MSB of the data output. The RX_DV and TX_EN pins are unused in PCS Bypass mode.

10BASE-T OPERATION

10BASE-T Transmit

The 78Q2120C takes 4-bit parallel NRZ data via the MII interface and passes it through a parallel to serial converter. The data is then passed through a Manchester encoder, pre-emphasis pulse-shaper, media filter, and finally to the twisted-pair line driver. The pulse-shaper and filter ensure the output waveforms meet the voltage template and spectral content requirements detailed in Clause 14 of IEEE-802.3. Interface to the twisted-pair media is through a center-tapped 1:1 transformer. No external filtering is required. During auto-negotiation and 10BASE-T idle periods, link pulses are transmitted.

The 78Q2120C employs an onboard timer to prevent the MAC from capturing a network through excessively long transmissions. When this timer expires, the chip enters the jabber state and transmission is halted. The jabber state is exited after the MII goes idle for 500±250ms.

10BASE-T Receive

The 78Q2120C receives Manchester-encoded 10BASE-T data through the twisted pair inputs and re-establishes logic levels through a slicer with a smart squelch function. The slicer automatically adjusts its level after detection of valid data with the appropriate levels. Data is passed on to the CDR where the clock is recovered, and the data is re-timed and decoded. From there, data enters the serial-to-parallel converter for transmission to the MAC via the Media Independent Interface. Interface to the twisted-pair media is through an external 1:1 transformer. Polarity information is detected and corrected within internal circuitry.

Polarity Correction

The 78Q2120C is capable of either automatic or manual polarity reversal for 10BASE-T and auto-negotiation functions. Register bits MR16.5 and MR16.4 control this feature. The default is automatic mode where MR16.5 is low and MR16.4 indicates if the detection circuitry has inverted the input signal. To enter manual mode, MR16.5 should be set high and MR16.4 will then control the signal polarity.

SQE TEST

The 78Q2120C supports the Signal Quality Error (SQE) function detailed in IEEE-802.3. At an interval of 1μs after each negative transition of the TXEN pin in 10BASE-T mode, the COL pin will go high for a period of 1μs. SQE is not signaled during transmission after collision is detected. SQE is automatically disabled when repeater mode is enabled. This function can be disabled through register bit MR16.11.

Natural Loopback

When enabled, whenever the 78Q2120C is transmitting and not receiving on the twisted pair media (10BASE-T Half Duplex mode), data on the TXD[3:0] pins is looped back onto the RXD[3:0] pins. During a collision, data from the RXI pins is routed to the RXD[3:0] pins. The natural loopback function is enabled through register bit MR16.10.

Repeater Mode

When the RPTR pin is high or register bit MR16.15 is set, the 78Q2120C is placed in repeater mode. In this mode, full duplex operation is prohibited, CRS responds only to receive activity and, in 10BASE-T mode, the SQE test function is disabled.

AUTO-NEGOTIATION

The 78Q2120C supports the auto-negotiation functions of Clause 28 of IEEE-802.3 for 10/100 Mbps operation over copper wiring. This function can be enabled via a pin selection or register settings. If the ANEGA pin is tied high, the auto-negotiation function defaults to ON and bit MR0.12 (ANEGEN) is high after reset. Software can disable the auto-negotiation function by writing to bit MR0.12. If the ANEGA pin is tied low, the function defaults to OFF and bit MR0.12 is set low after reset and cannot be written to.

The contents of register MR4 are sent to the 78Q2120C's link partner during auto-negotiation using fast link pulse coding. Bits MR4.8:5 reflect the state of the TECH[2:0] pins after reset. If TECH[2:0] = '111', then all 4 bits are high. If TECH[2:0] = '001', then only bit 5 is high. After reset, software can change any of these bits from a '1' to a '0'; but not from a '0' to a '1'. Therefore, a technology permitted by the setting of the TECH pins can be disabled, but cannot be enabled through register selection.

With auto-negotiation enabled, the 78Q2120C will start sending fast link pulses at power on, loss of link or upon a command to restart. At the same time, it will look for either 10BASE-T idle, 100BASE-TX idle, or fast link pulses from its link partner. If either idle pattern is detected, the 78Q2120C configures itself in half-duplex mode at the appropriate speed. If it detects fast link pulses, it decodes and analyzes the link code transmitted by the link partner. When three identical link code words are received (ignoring the acknowledge bit) the link code word is stored in register MR5. Upon receiving three more identical link code words, with the acknowledge bit set, the 78Q2120C configures itself to the highest priority technology common to the two link partners. The technology priorities are, in descending order:

100BASE-TX, Full Duplex
100BASE-TX, Half Duplex
10BASE-T, Full Duplex
10BASE-T, Half Duplex

Once auto-negotiation is complete, register bits MR18.11:10 will reflect the actual speed and duplex that was chosen.

If auto-negotiation fails to establish a link for any reason, register bit MR18.12 will reflect this and auto negotiation will restart from the beginning. Writing a '1' to bit MR0.9(RANEG) will also cause auto-negotiation to restart.

MEDIA INDEPENDENT INTERFACE

MII Transmit and Receive Operation

The MII interface on the 78Q2120C provides independent transmit and receive paths for both 10Mb/s and 100Mb/s data rates as described in Clause 22 of the IEEE-802.3 standard.

The transmit clock, TX_CLK, provides the timing reference for the transfer of TX_EN, TXD[3:0], and TX_ER signals from the MAC to the 78Q2120C. TXD[3:0] is captured on the rising edge of TX_CLK when TX_EN is asserted. TX_ER is also captured on the rising edge of TX_CLK and is asserted by the MAC to request that an error code group is to be transmitted. The assertion of TX_ER is ignored when the 78Q2120C is operating in 10BASE-T mode.

The receive clock, RX_CLK, provides the timing reference to transfer RX_DV, RXD[3:0], and RX_ER signals from the 78Q2120C to the MAC. RX_DV transitions synchronously with respect to RX_CLK and is asserted when the 78Q2120C is presenting valid data on RXD[3:0]. RX_ER is asserted and is synchronous to RX_CLK when a code group violation has been detected in the current receive packet.

Station Management Interface

The station management interface consists of circuitry which implements the serial protocol as described in Clause 22.2.4.5 of IEEE-802.3. A 16-bit shift register receives serial data applied to the MDIO pin at the rising-edge of the MDC clock signal. Once the preamble is received, the station management control logic looks for the start-of-frame sequence and a read or write op-code, followed by the PHYAD and REGAD fields. For a read operation, the MDIO port becomes enabled as an output and the register data is loaded into a shift register for transmission. The 78Q2120C can work with a one bit preamble rather than the 32 bits prescribed by IEEE-802.3. This allows for faster programming of the registers. If a register does not exist at an address indicated by the REGAD field or if the PHYAD field does not match the 78Q2120C PHYAD indicated by the PHYAD pins, a read of the MDIO port will return all ones. For a write operation, the data is shifted in and loaded into the appropriate register after the sixteenth data bit has been received.

When the PHYAD field is all zeros, the Station Management Entity (STA) is requesting a broadcast data transaction. All PHYs sharing the same Management Interface must respond to this broadcast request. The 78Q2120C will respond to the broadcast data transaction.

ADDITIONAL FEATURES

LED Indicators

There are seven LED pins that can be used to indicate various states of operation of the 78Q2120C. There is an LED pin that indicates the link is up (LEDL), others that indicate the 78Q2120C is either transmitting (LEDTX) or receiving (LEDRX), one that signals a collision event (LEDCOL), two more that reflect the data rate (LEDBTX and LEDBT), and one that reflects full duplex mode of operation (LEDFDX).

Interrupt Pin

The 78Q2120C has an Interrupt pin (INTR) that is asserted whenever any of the eight interrupt bits of MR17.7:0 are set. These interrupt bits can be disabled via the MR17.15:8 Interrupt Enable bits. The Interrupt Polarity bit, MR16.14, controls the active level of the INTR pin. When the INTR pin is not asserted, this pin is held in a high impedance state. An external pull-up or pull-down resistor may be required for use with the INTR pin.

APPLICATIONS REQUIREMENTS

RXIP/N Termination Connection

The input circuitry of the TERIDIAN 78Q2120C has changed for continuing performance improvements. Device revision C09 requires that the RXIP/N termination resistors and transformer center tap connections be directly connected to VCC for proper receiver operation. Refer to Figure 1: Typical Applications Circuit for the schematic showing the required RXIP/N termination resistors and transformer center tap connections to VCC for revision 78Q2120C.

PIN DESCRIPTION

LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
A	Analog Pin	CI	TTL-level Input (5V compatible)
CIU	TTL-level Input w/ Pull-up (5V compatible)	CIO	TTL-compatible Bi-directional Pin (5V compatible)
CID	TTL-level Input w/ Pull-down (5V compatible)	COZ	Tristate-able CMOS output
CIS	TTL-level Input w/ Schmitt Trigger (5V compatible)	G	Ground
CO	CMOS Output	S	Supply

MII (MEDIA INDEPENDENT INTERFACE)

NAME	PIN	TYPE	DESCRIPTION
TX_CLK	27	COZ	TRANSMIT CLOCK: TX_CLK is a continuous clock, which provides a timing reference for the TX_EN, TX_ER and TXD[3:0] signals from the MAC. The clock frequency is 25MHz in 100BASE-TX mode and 2.5MHz in 10BASE-T mode. This pin is tristated in the isolate mode and the TXHIM mode.
TX_EN	28	CI	TRANSMIT ENABLE: TX_EN is asserted by the MAC to indicate that valid data for transmission is present on the TXD[3:0] pins.
TXD[3:0]	32-29	CI	TRANSMIT DATA: TXD[3:0] receives data from the MAC for transmission on a nibble basis. This data is captured on the rising edge of TX_CLK when TX_EN is high.
TX_ER	26	CI	TRANSMIT ERROR: TX_ER is asserted high by the MAC to request that an error code-group be transmitted when TX_EN is high. In PCS bypass mode this pin becomes the MSB of the transmit 5-bit code group.
CRS	34	COZ	CARRIER SENSE: When the 78Q2120C is not in repeater mode, CRS is high whenever a non-idle condition exists on either the transmitter or the receiver. In repeater mode, CRS is only active when a non-idle condition exists on the receiver. This pin is tristated in the isolate mode.
COL	33	COZ	COLLISION: COL is asserted high when a collision has been detected on the media. In 10BASE-T mode, COL is also used for the SQE test function. This pin is tristated in the isolate mode. During half duplex operation, the rising edge of COL will occasionally occur upon the rising edge of TX_CLK.
RX_CLK	24	COZ	RECEIVE CLOCK: RX_CLK is a continuous clock, which provides a timing reference to the MAC for the RX_DV, RX_ER and RXD[3:0] signals. The clock frequency is 25MHz in 100BASE-TX mode, and 2.5MHz in 10BASE-T mode. To reduce power consumption in 100BASE-TX mode, the 78Q2120C provides an optional mode, enabled through MR16.0, in which RX_CLK is held inactive (low) when no receive data is detected. This pin is tristated in the isolate mode.
RX_DV	23	COZ	RECEIVE DATA VALID: RX_DV is asserted high to indicate that valid data is present on the RXD[3:0] pins. In 100BASE-TX mode, it transitions high with the first nibble of the preamble and is pulled low when the last data nibble has been received. In 10BASE-T mode, it transitions high when the start-of-frame delimiter (SFD) is detected. This pin is tristated in the isolate mode.
RXD[3:0]	19-22	COZ	RECEIVE DATA: Received data is provided to the MAC via RXD[3:0]. These pins are tristated in the isolate mode.

MII (continued)

NAME	PIN	TYPE	DESCRIPTION
RX_ER	25	COZ	RECEIVE ERROR: RX_ER is asserted high when an error is detected during a frame reception. In PCS bypass mode, this pin becomes the MSB of the receive 5-bit code group. This pin is tristated in the isolate mode.
MDC	18	CIS	MANAGEMENT DATA CLOCK: MDC is the clock used for transferring data via the MDIO pin.
MDIO	17	CIO	MANAGEMENT DATA INPUT/OUTPUT: MDIO is a bi-directional port used to access management registers within the 78Q2120C. This pin requires an external pull-up resistor as specified in IEEE-802.3.

PHY ADDRESS

NAME	PIN	TYPE	DESCRIPTION
PHYAD[4:0]	12-16	CI	PHY ADDRESS: Allows 31 configurable PHY addresses. The 78Q2120C always responds to broadcast data transactions via the MII interface when the PHYAD bits are all zero, independent of the logic levels of the PHYAD pins.

PMA (PHYSICAL MEDIA ATTACHMENT) INTERFACE

NAME	PIN	TYPE	DESCRIPTION
PCSBP	64	CID	PCS BYPASS: When high, the 100BASE-TX PCS is bypassed, as well as the scrambler and descrambler functions. Scrambled 5-bit code groups for transmission are applied to the TX_ER, TXD[3:0] pins and received on the RX_ER, RXD[3:0] pins. The RX_DV and TX_EN signals are not valid in this mode. PCS bypass mode is only valid when 100BASE-TX is enabled and auto-negotiation is disabled. This mode can also be entered by setting MR16.1.

CONTROL AND STATUS

NAME	PIN	TYPE	DESCRIPTION
RST	6	CIU	ACTIVE-LOW RESET: When pulled low, the pin resets the chip. The reset pulse must be long enough to guarantee stabilization of the supply voltage and startup of the oscillator. Refer to the Electrical Specifications for the reset pulse requirements. There are 2 other ways to reset the chip: i) through the internal power-on-reset (activated when the chip is being powered up) ii) through the MII register bit (MR0.15)
PWRDN	7	CID	POWER-DOWN: The 78Q2120C may be placed in a low power consumption state by setting this signal to logic high. While in the power-down state, the 78Q2120C still responds to management transactions. This power-down state can also be activated using the PWRDN bit in the MII register (MR0.11).

CONTROL AND STATUS (CONTINUED)

NAME	PIN	TYPE	DESCRIPTION
ISO	2	CI	ISOLATE: When set to logic one, the 78Q2120C will present a high impedance on its MII output pins. This allows for multiple chips to be attached to the same MII interface. When the 78Q2120C is isolated, it still responds to management transactions. This high impedance state can also be achieved using the ISO bit in the MII register (MR0.10).
ISODEF	1	CI	ISOLATE DEFAULT: This pin determines the power-up/reset default of the ISO bit (MR0.10). If it is connected to VCC, the ISO bit will have a default value of '1'. Otherwise, the bit defaults to '0'. When this signal is tied to VCC, it allows multiple chips to be connected to the same MII interface.
ANEGA	47	CI	AUTO-NEGOTIATION ABILITY: Connect to logic high to enable the auto-negotiation function. When connected to logic low, the auto-negotiation logic is disabled and manual technology selection is done through TECH[2:0] pins. This pin is reflected as the ANEGA bit in MR1.3.
TECH[2:0]	44-46	CI	TECHNOLOGY ABILITY/SELECT: TECH[2:0] sets the technology ability of the chip which is reflected in MR0.13,8, MR1.14:11 and MR4.12:5.

TECH[2:0]	Technology Ability
111	Both 10BASE-T and 100BASE-TX, and Both half and full duplex
000	None
001	10BASE-T, half duplex
010	100BASE-TX, half duplex
011	Both 10BASE-T and 100BASE-TX, half duplex only
100	None
101	10BASE-T Both half and full duplex
110	100BASE-TX Both half and full duplex

RPTR	50	CID	REPEATER MODE: When pulled high, this pin puts the chip into repeater mode. In this mode, full duplex is prohibited, CRS responds to receive activity only. In 10BASE-T mode, the SQE test function is disabled. This mode can also be enabled by setting bit MR16.15

MDI (MEDIA DEPENDENT INTERFACE)

NAME	PIN	TYPE	DESCRIPTION
TXOP/N	61,62	A	TRANSMIT OUTPUT POSITIVE/NEGATIVE: Transmitter differential outputs for both 10BASE-T and 100BASE-TX operation.
RXIP/N	52,51	A	RECEIVE INPUT POSITIVE/NEGATIVE: Receiver differential inputs for both 10BASE-T and 100BASE-TX operation.

LED INDICATORS

The LED pins use standard logic drivers. They output a logic low when the LED is meant to be on and a logic high when it is meant to be off. The LED should be connected in series with a resistor between the output pin and the power supply.

NAME	PIN	TYPE	DESCRIPTION
LEDL	40	CO	LED LINK: ON for link up.
LEDTX	39	CO	LED TRANSMIT: ON when there is a transmission (normally OFF).
LEDRX	38	CO	LED RECEIVE: ON when there is a reception (normally OFF).
LEDCOL	37	CO	LED COLLISION: In half duplex mode, this is a collision indicator and turns ON when a collision occurs. In full duplex mode, this LED is held OFF.
LEDBTX	36	CO	LED 100BASE-TX: ON for 100BASE-TX connection and OFF for other connections. LEDBTX is OFF during auto-negotiation.
LEDBT	48	CO	LED 10BASE-T: ON for 10BASE-T connection and OFF for other connections. LEDBT is OFF during auto-negotiation.
LEDFDX	49	CO	LED FULL DUPLEX: ON when in full duplex mode and OFF when in half duplex mode.

OSCILLATOR/CLOCK

NAME	PIN	TYPE	DESCRIPTION
CKIN	4	CIS	CLOCK INPUT: Connects to a 25 MHz TTL compatible clock source. This pin should be held low when XTLP and XTLN are being used as the 25 MHz clock source.
XTLP/N	59,58	A	CRYSTAL PINS: Should be connected to a 25 MHz crystal. When CKIN is being used as the 25 MHz clock source, these pins should be left floating or connected together.

MISCELLANEOUS PIN

NAME	PIN	TYPE	DESCRIPTION
INTR	35	COZ	INTERRUPT PIN: This pin is used to signal an interrupt to the media access controller. The pin is held in the high impedance state when an interrupt is not indicated. The pin will be forced high or low to signal an interrupt depending upon the value of the INPOL bit (MR16.14). The events which trigger an interrupt can be programmed via the Interrupt Control Register located at address MR17.
NC	54,56	--	No Connect. Do not connect to ground or supply.

POWER SUPPLY AND GROUND

NAME	PIN	TYPE	DESCRIPTION
VCC	8,11,41, 43,57,63	S	3.3V SUPPLY
GND	3,5,9,10, 42,53,55,60	G	GROUND

REGISTER DESCRIPTION

The 78Q2120C implements 11 16-bit registers, which are accessible via the MDIO and MDC pins. The supported registers are shown below in the following table. Attempts to read unsupported registers will be ignored and the MDIO pin will not be enabled as an output, as per the IEEE 802.3 specification. All of the registers except those which are unique to the 78Q2120C, will respond to the broadcast PHYAD value of '00000'. The registers specific to the 78Q2120C occupy address space MR16-22.

ADDRESS	SYMBOL	NAME	DEFAULT (HEX)
0	MR0	Control	(3100)
1	MR1	Status	(7809)
2	MR2	PHY Identifier 1	000E
3	MR3	PHY Identifier 2	70C9
4	MR4	Auto-Negotiation Advertisement	(01E1)
5	MR5	Auto-Negotiation Link Partner Ability	0000
6	MR6	Auto-Negotiation Expansion	0000
7	MR7	Not Implemented	0000
8-14	MR8-14	Reserved	0000
15	MR15	Not Implemented	0000
16	MR16	Vendor Specific	(0140)
17	MR17	Interrupt Control/Status Register	0000
18	MR18	Diagnostic Register	0000
19	MR19	Transceiver Control	4XXX
20-22	MR20-MR22	Reserved	0000

Legend:

TYPE	DESCRIPTION	TYPE	DESCRIPTION
R	Readable by management.	W	Writeable by management.
SC	Writeable by management. Self Clearing.	RC	Readable by management. Cleared upon a read operation.
0/1	Default value upon power up or reset.	(0/1)	Default value dependent on pin settings. The value in bracket indicates typical case.

MR0: Control Register

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
0.15	RESET	R/SC	0	Reset: Setting this bit to '1' resets the device and sets all registers to their default states. This bit is self-clearing.
0.14	LOOPBK	R/W	0	Loopback: When this bit is set to '1', no transmission of data on the network medium occurs and any receive data on the network medium is ignored. The loopback signal path will encompass most of the digital circuitry.
0.13	SPEEDSL	R/W	(1)	Speed Selection: This bit determines the speed of operation of the 78Q2120C. Setting this bit to '1' indicates 100Base-TX operation and a '0' indicates 10Base-T mode. This bit will default to a '1' upon reset. If the TECH[2:0] pins are all logic zero and auto-negotiation is not enabled, this bit will be writeable. If auto-negotiation is not enabled and the TECH[2:0] pins are set to indicate that only 10Base-T is supported, this bit will be forced to logic zero and will not be writeable. If auto-negotiation is not enabled and the TECH[2:0] pins are set to indicate that only 100Base-TX is supported, this bit will be forced to logic one and will not be writeable. When auto-negotiation is enabled, this bit will not be writeable and will have no effect on the 78Q2120C. If the TECH[2:0] pins are brought to zero from another value, this bit will retain its original value until it is overwritten.
0.12	ANEGEN	R/W	(1)	Auto-Negotiation Enable: Setting this bit to '1' enables the auto-negotiation process. This bit can only be set if the ANEGA pin is a logic one and will default to '1' upon reset. If this bit is cleared to '0', manual speed and duplex mode selection is accomplished through bits 0.13 (*SPEEDSL*) and 0.8 (*DUPLEX*) of the Control Register or the TECH[2:0] pins according to the table shown in the section describing the TECH[2:0] pins. If the ANEGA pin is brought from '0' to '1' and reset is not asserted, this bit will remain at '0' until a '1' is written.
0.11	PWRDN	R/W	0	Power-Down: The device may be placed in a low power consumption state by setting this bit to '1'. While in the power-down state, the device will still respond to management transactions. Setting the PWRDN pin high also activates the power-down state.
0.10	ISO	R/W	(0)	Isolate: When set to '1', the device presents a high-impedance on its MII output pins. This allows for multiple PHY's to be attached to the same MII interface. When the device is isolated, it still responds to management transactions. The default value of this bit depends on the ISODEF pin. When ISODEF pin is tied high, the *ISO* bit defaults to high. Otherwise, it defaults to low. The Isolate mode can also be activated using the ISO pin.
0.9	RANEG	R/SC	0	Restart Auto-Negotiation: Normally, the Auto-Negotiation process is started at power up. The process can be restarted by setting this bit to '1'. This bit is self-clearing.

MR0: Control Register (continued)

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
0.8	DUPLEX	R/W	(1)	Duplex Mode: This bit determines whether the device supports full-duplex or half-duplex. A '1' indicates full-duplex operation and a '0' indicates half-duplex. This bit will default to '0' upon reset and will be writeable if the TECH[2:0] pins are all logic zero and auto-negotiation is not enabled. If auto-negotiation is not enabled and the TECH[2:0] pins are set to indicate that only full-duplex is supported, this bit will be forced to '1' and will not be writeable. If auto-negotiation is not enabled and the TECH[2:0] pins are set to indicate that only half-duplex is supported, this bit will be forced to '0' and will not be writeable. When auto-negotiation is enabled, this bit will not be writeable and will have no effect on the device. If the TECH[2:0] pins are brought to zero from another value, this bit will retain its original value until it is overwritten.
0.7	COLT	R/W	0	Collision Test: When this bit is set to '1', the device will assert the COL signal in response to the assertion of the TX_EN signal. Collision test is disabled if the PCSBP pin is high. Collision test can be activated regardless of the duplex mode of operation.
0.6:0	RSVD	R	0	Reserved

MR1: Status Register

Bits 1.15 through 1.11 reflect the ability of the 78Q2120C as configured by the TECH[2:0] pins. They do not reflect any ability changes made via the MII Management interface to bits 0.13 (*SPEEDSL*) , 0.12 (*ANEGEN*) and 0.8 (*DUPLEX*).

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
1.15	100T4	R	0	100BASE-T4 Ability: Reads '0' to indicate the 78Q2120C does not support 100Base-T4 mode.
1.14	100X_F	R	(1)	100BASE-TX Full Duplex Ability: 0 : Not able 1 : Able
1.13	100X_H	R	(1)	100BASE-TX Half Duplex Ability: 0 : Not able 1 : Able
1.12	10T_F	R	(1)	10BASE-T Full Duplex Ability: 0 : Not able 1 : Able
1.11	10T_H	R	(1)	10BASE-T Half Duplex Ability: 0 : Not able 1 : Able
1.10	100T2_F	R	0	100BASE-T2 Full Duplex Ability: Reads '0' to indicate the 78Q2120C does not support 100Base-T2 full duplex mode.

MR1: Status Register

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
1.9	100T2_H	R	0	100BASE-T2 Half Duplex Ability: Reads '0' to indicate the 78Q2120C does not support 100Base-T2 full duplex mode.
1.8	EXTS	R	0	Extended Status Information Availability: Reads '0' to indicate the 78Q2120C does not support Extended Status information on MR15.
1.7	RSVD	R	0	Reserved
1.6	MFPS	R	0	Management Frame Preamble Suppression Support: A "0" indicates that the 78Q2120C can read management frames with a preamble.
1.5	ANEGC	R	0	Auto-Negotiation Complete: A logic one indicates that the Auto-Negotiation process has been completed, and that the contents of registers MR4,5,6 are valid.
1.4	RFAULT	RC	0	Remote Fault: A logic one indicates that a remote fault condition has been detected and remains set until it is cleared. This bit can only be cleared by reading this register (MR1) via the management interface.
1.3	ANEGA	R	(1)	Auto-Negotiation Ability: When set, this bit indicates the device's ability to perform Auto-Negotiation. The value of this bit is determined by the *ANEGEN* bit (MR0.12).
1.2	LINK	R	0	Link Status: A logic one indicates that a valid link has been established. If the link status should transition from an OK status to a NOT-OK status, this bit will become cleared and remains cleared until it is read.
1.1	JAB	RC	0	Jabber Detect: In 10Base-T mode, this bit is set during a jabber event. After a jabber event, the bit remains set until cleared by a read operation.
1.0	EXTD	R	1	Extended Capability: Reads '1' to indicate the 78Q2120C provides an extended register set (MR2 and beyond).

MR2: PHY Identifier Register 1

BIT	SYMBOL	TYPE	VALUE	DESCRIPTION
2.15:0	OUI [23:6]	R	000Eh	Organizationally Unique Identifier: This value is 00-C0-39 for TERIDIAN Semiconductor Corporation. This register contains the first 16-bits of the identifier.

MR3: PHY Identifier Register 2

BIT	SYMBOL	TYPE	VALUE	DESCRIPTION
3.15:10	OUI [5:0]	R	1Ch	Organizationally Unique Identifier: Remaining 6 bits of the OUI.
3.9:4	MN	R	0Ch	Model Number: The last 2 digits of the model number 78Q2120C are encoded into the 6 bits.
3.3:0	RN	R	9h	Revision Number: The value '1001' corresponds to the ninth revision of the silicon.

MR4: Auto-Negotiation Advertisement Register

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
4.15	NP	R	0	Next Page: Not supported. Reads logic zero.
4.14	RSVD	R	0	Reserved
4.13	RF	R/W	0	Remote Fault: Setting this bit to '1' allows the device to indicate to the link partner a Remote Fault Condition.
4.12:5	TAF	R/W	(0Fh)	Technology Ability Field: The default value of this field is dependent upon the MR1.15:11 register bits. This field can be overwritten by management to auto-negotiate to an alternate common technology. Writing to this register has no effect until auto-negotiation is re-initiated.
4.12	A7	R	0	Reserved for future technology.
4.11	A6	R/W	0	Reserved
4.10	A5	R/W	0	Reserved.
4.9	A4	R	0	100BASE-T4: The 78Q2120C does not support 100BASE-T4 operation.
4.8	A3	R/W	(1)	100BASE-TX Full Duplex: If the MR1.14 bit is '1', this bit will be set to '1' upon reset and will be writeable. Otherwise, this bit cannot be set to '1' by the management.
4.7	A2	R/W	(1)	100BASE-TX: If the MR1.13 bit is '1', this bit will be set to '1' upon reset and will be writeable. Otherwise, this bit cannot be set to '1' by the management.
4.6	A1	R/W	(1)	10BASE-T Full Duplex: If the MR1.12 bit is '1', this bit will be set to '1' upon reset and will be writeable. Otherwise, this bit cannot be set to '1' by the management.
4.5	A0	R/W	(1)	10BASE-T: If the MR1.11 bit is '1', this bit will be set to '1' upon reset and will be writeable. Otherwise, this bit cannot be set to '1' by the management.
4.4:0	S4:0	R	01h	Selector Field: Hard coded with the value of '00001' for IEEE 802.3.

MR5: Auto-Negotiation Link Partner Ability Register

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
5.15	NP	R	0	Next Page: When '1' is read, it indicates the link partner wishes to engage in Next Page exchange.
5.14	ACK	R	0	Acknowledge: When '1' is read, it indicates the link partner has successfully received at least 3 consecutive and consistent FLP bursts.
5.13	RF	R	0	Remote Fault: When '1' is read, it indicates the link partner has a fault.
5.12:5	A7:0	R	0	Technology Ability Field: This field contains the technology ability of the link partner. The bit definition is the same as MR4.12:5.
5.4:0	S4:0	R	00h	Selector Field: This field contains the type of message sent by the link partner. For IEEE 802.3 compliant link partner, this field should be '00001'.

MR6: Auto-Negotiation Expansion Register

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
6.15:5	RSVD	R	0	Reserved
6.4	PDF	RC	0	Parallel Detection Fault: When '1' is read, it indicates that more than one technology has been detected during link up. This bit is cleared when read.
6.3	LPNPA	R	0	Link Partner Next Page Able: When '1' is read, it indicates the link partner supports the Next Page function.
6.2	NPA	R	0	Next Page Able: Reads '0' since the 78Q2120C does not support Next Page function.
6.1	PRX	RC	0	Page Received: Reads '1' when a new link code word has been received into the Auto-Negotiation Link Partner Ability Register. This bit is cleared upon read.
6.0	LPANEGA	R	0	Link Partner Auto-Negotiation Able: When '1' is read, it indicates the link partner is able to participate in the Auto-Negotiation function.

MR16: Vendor Specific Register

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
16.15	RPTR	R/W	(0)	Repeater Mode: When set, the 78Q2120C is put into Repeater mode of operation. In this mode, full duplex is prohibited, CRS responds to receive activity only and, in 10Base-T mode, the SQE test function is disabled.
16.14	INPOL	R/W	0	When this bit is '0', the INTR pin is forced low to signal an interrupt. Setting this bit to '1' causes the INTR pin to be forced high to signal an interrupt.
16.13	RSVD	R	0	Reserved
16.12	TXHIM	R/W	0	Transmitter High-Impedance Mode: When set, the TXOP/TXON transmit pins and the TX_CLK pin are put into a high-impedance state. The receive circuitry remains fully functional.
16.11	SQEI	R/W	0	SQE Test Inhibit: Setting this bit to '1' disables 10Base-T SQE testing. By default, this bit is '0' and the SQE test is performed by generating a COL pulse following the completion of a packet transmission.
16.10	NL10	R/W	0	10Base-T Natural Loopback: Setting this bit to '1' causes transmit data received on the TXD0-3 pins to be automatically looped back to the RXD[0:3] pins when 10Base-T mode is enabled.
16.9	RSVD	R/W	0	Reserved
16.8	RSVD	R/W	1	Reserved
16.7	RSVD	R/W	0	Reserved
16.6	RSVD	R/W	1	Reserved
16.5	APOL	R/W	0	Auto Polarity: During auto-negotiation and 10BASE-T mode, the 78Q2120C is able to automatically invert the received signal due to a wrong polarity connection. It does so by detecting the polarity of the link pulses. Setting this bit to '1' disables this feature.
16.4	RVSPOL	R/W	0	Reverse Polarity: The reverse polarity is detected either through 8 inverted 10Base-T link pulses (NLP) or through one burst of inverted clock pulses in the auto-negotiation link pulses (FLP). When the reverse polarity is detected and if the Auto Polarity feature is enabled, the 78Q2120C will invert the receive data input and set this bit to '1'. If Auto Polarity is disabled, then this bit is writeable. Writing a '1' to this bit forces the polarity of the receive signal to be reversed.
16.3:2	RSVD	R/W	0h	Reserved: Must set to '00'.

MR16: Vendor Specific Register (continued)

Bit	Symbol	Type	Default	Description
16.1	PCSBP	R/W	(0)	PCS Bypass Mode: When set, the 100Base-TX PCS and scrambling/ descrambling functions are bypassed. Scrambled 5-bit code groups for transmission are applied to the TX_ER, TXD[3:0] pins and received on the RX_ER, RXD[3:0] pins. The RX_DV and TX_EN signals are not valid in this mode. PCSBP mode is valid only when 100Base-TX mode is enabled and auto-negotiation is disabled.
16.0	RXCC	R/W	0	Receive Clock Control: This function is valid only in 100Base-TX mode. When set to '1', the RX_CLK signal will be held low when there is no data being received (to save power). The RX_CLK signal will restart 1 clock cycle before the assertion of RX_DV and be shut off 64 clock cycles after RX_DV goes low. RXCC is disabled when the loopback mode is enabled (MR0.14 is high). This bit should be kept at logic zero when PCS Bypass mode is used.

MR17: Interrupt Control/Status Register

The Interrupt Control/Status Register provides the means for controlling and observing events which trigger an interrupt on the INTR pin. This register can also be used in a polling mode via the MII Serial Interface as a means to observe key events within the PHY via one register address. Bits 0 through 7 are status bits, which are each set to logic one based upon an event. These bits are cleared after the register is read. Bits 8 through 15 of this register, when set to logic one, enable their corresponding bit in the lower byte to signal an interrupt on the INTR pin. The level of this interrupt can be set via the MR16.14 (*INPOL*) bit.

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
17.15	JABBER_IE	R/W	0	Jabber Interrupt Enable
17.14	RXER_IE	R/W	0	Receive Error Interrupt Enable
17.13	PRX_IE	R/W	0	Page Received Interrupt Enable
17.12	PDF_IE	R/W	0	Parallel Detect Fault Interrupt Enable
17.11	LP-ACK_IE	R/W	0	Link Partner Acknowledge Interrupt Enable
17.10	LS_CHG_IE	R/W	0	Link Status Change Interrupt Enable
17.9	RFAULT_IE	R/W	0	Remote Fault Interrupt Enable
17.8	ANEG-COMP_IE	R/W	0	Auto-Negotiation Complete Interrupt Enable
17.7	JAB_INT	RC	0	Jabber Interrupt: This bit is set high when a Jabber event is detected by the 10Base-T circuitry.
17.6	RXER_INT	RC	0	Receive Error Interrupt: This bit is set high when the RX_ER signal transitions high.
17.5	PRX_INT	RC	0	Page Received Interrupt: This bit is set high when a new page has been received from the link partner during auto-negotiation.
17.4	PDF_INT	RC	0	Parallel Detect Fault Interrupt: This bit is set high by the auto-negotiation logic when a parallel detect fault condition is indicated.

MR17: Interrupt Control/Status Register (continued)

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
17.3	LP-ACK_INT	RC	0	Link Partner Acknowledge Interrupt: This bit is set high by the auto-negotiation logic when FLP bursts are received with the acknowledge bit set.
17.2	LS_CHG_INT	RC	0	Link Status Change Interrupt: This bit is set when the link transitions from an OK status to a FAIL status.
17.1	RFAULT_INT	RC	0	Remote Fault Interrupt: This bit is set when a remote fault condition has been indicated by the link partner.
17.0	ANEG-COMP_INT	RC	0	Auto-Negotiation Complete Interrupt: This bit is set by the auto-negotiation logic upon successful completion of auto-negotiation.

MR18: Diagnostic Register

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
18.15:13	RSVD	R	00h	Reserved: Must set to '00h'.
18.12	ANEGF	RC	0	Auto-Negotiation Fail Indication: This bit is set when auto-negotiation completes and no common technology was found. It remains set until read.
18.11	DPLX	R	0	Duplex Indication: This bit indicates the result of the auto-negotiation for duplex arbitration as follows: 0 : Half-duplex was the highest common denominator 1 : Full-duplex was the highest common denominator
18.10	RATE	R	0	Rate Indication: This bit indicates the result of the auto-negotiation for data rate arbitration as follows: 0 : 10Base-T was the highest common denominator 1 : 100Base-TX was the highest common denominator
18.9	RXSD	R	0	Receiver Signal Detect Indication: In 10Base-T mode, this bit indicates that Manchester data has been detected. In 100Base-TX mode, it indicates that the receive signal activity has been detected (but not necessarily locked on to).
18.8	RX_LOCK	R	0	Receive PLL Lock Indication: Indicates that the Receive PLL has locked onto the receive signal for the selected speed of operation (10Base-T or 100Base-TX).
18.7:0	RSVD	R	00h	Reserved: Must set to '00h'.

MR19: Transceiver Control

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
19.15:12	RSVD	R	0100	Reserved
19.11:10	TXO[1:0]	R/W	01	Transmit Amplitude Selection: Sets the transmit output amplitude to account for transmit transformer insertion loss. 00 : Gain set for 0.0dB of insertion loss 01 : Gain set for 0.4dB of insertion loss 10 : Gain set for 0.8dB of insertion loss 11 : Gain set for 1.2dB of insertion loss
19.9:0	RSVD	R	XXXh	Reserved

MR20: Reserved

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
20.15:0	Reserved	na	XXXXh	Reserved

MR21: Reserved

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
21.15:0	Reserved	na	XXXXh	Reserved

MR22: Reserved

BIT	SYMBOL	TYPE	DEFAULT	DESCRIPTION
22.15:0	Reserved	na	XXXXh	Reserved

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum rating may permanently damage the device.

PARAMETER	RATING
DC Supply Voltage (Vcc)	-0.5 to 4.0 VDC
Storage Temperature	-65 to 150°C
Pin Voltage (CMOS inputs)	-0.3 to 5.5 VDC
Pin Voltage (CMOS outputs except TXOP/N)	-0.3 to (Vcc+0.6) VDC
Pin Voltage (TXOP/N only)	-0.3 to (Vcc+1.4) VDC
Pin Current	± 120 mA

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted, all specifications are valid over these temperatures and supply voltage ranges:

PARAMETER	RATING
DC Voltage Supply (Vcc)	3.3 ± 0.3 VDC
Ambient Operating Temperature (Ta)	0 to +70°C
Maximum Junction Temperature	125°C
Package Thermal Conductivity (θja)	45°C/W

DC CHARATERISTICS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current	I_{CC}	Vcc = 3.3V;				
		Auto-Negotiation		48	56	mA
		10BT (Idle)		26	32	
		10BT (Normal Activity)		88	110	
		100BTX		88	110	
Supply Current	I_{CC}	Power-down mode			5	mA

DIGITAL I/O CHARACTERISTICS:

Pins of type CI, CIU, CID, CIO:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input Voltage Low	Vil				0.8	V
Input Voltage High	Vih		2.0		5.5	V
Input Current	Iil, Iih		-1		1	µA
Pull-up Resistance	Rpu	Type CIU only	38	56	78	kΩ
Pull-down Resistance	Rpd	Type CID only	38	56	78	kΩ
Input Capacitance	Cin			8		pF

Pins of type CIS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Low-to-High Threshold	Vt+		1.3		1.7	V
High-to-Low Threshold	Vt-		0.80		1.20	V
Input Current	Iil, Iih		-1		1	µA
Input Capacitance	Cin			8		pF

Pins of type COZ:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage Low	Vol	Iol = 4mA			0.4	V
Output Voltage High	Voh	Ioh = -4mA	2.4			V
Output Transition Time	Tt	C_L = 20pF			6	ns
Tristate Output Leakage Current	Iz		-1		1	µA

Pins of type CO:

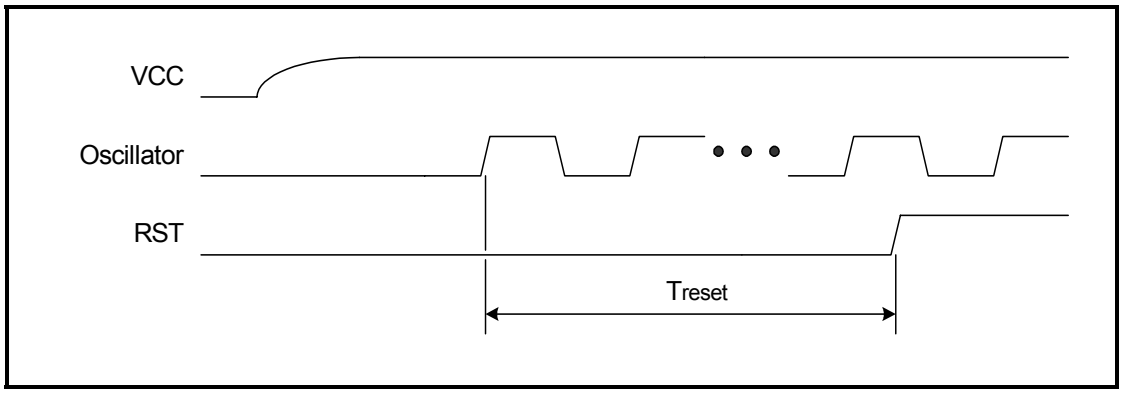
PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage Low	Vol	Iol = 8mA			0.4	V
Output Voltage High	Voh	Ioh = -8mA	2.4			V
Output Transition Time	Tt	C_L = 20pF			6	ns

Pins of type CIO:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage Low	Vol	Iol = 4mA			0.4	V
Output Voltage High	Voh	Ioh = -4mA	2.4			V
Output Transition Time	Tt	C_L = 20pF			6	ns

DIGITAL TIMING CHARACTERISTICS

RST Characteristics

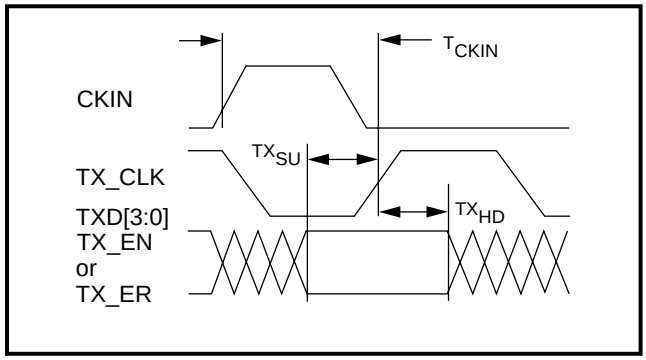


RST Pulse Duration

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
RST Pulse Assertion	Treset	VCC = 3.3V and oscillator stabilized	30			Oscillator Clock Cycles

MII Transmit Interface

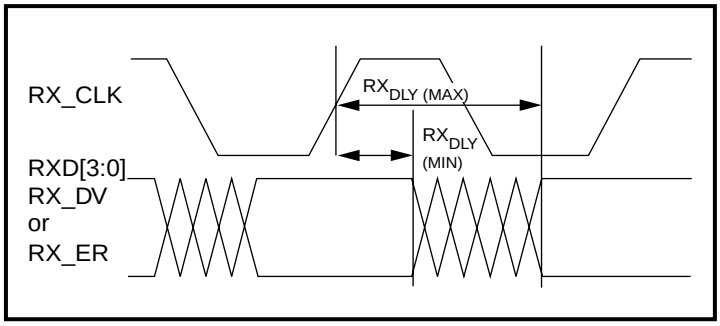
CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Setup Time: TX_CLK to TXD[3:0], TX_EN, TX_ER	TX_{SU}		15			ns
Hold Time: TX_CLK to TXD[3:0], TX_EN, TX_ER	TX_{HD}		0			ns
CKIN-to-TX_CLK Delay	T_{CKIN}		0		40	ns
TX_CLK Duty-Cycle			40		60	%



Transmit Inputs to the 78Q2120C

MII Receive Interface

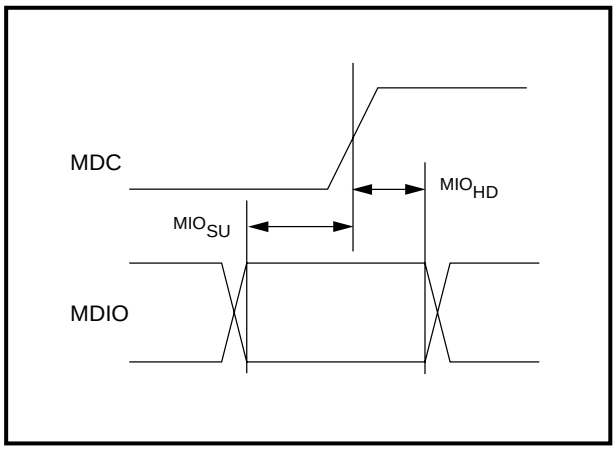
CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Receive Output Delay: RX_CLK to RXD[3:0], RX_DV, RX_ER	RX_{DLY}		10		30	ns
RX_CLK Duty-Cycle			40		60	%



Receive Outputs from the 78Q2120C

MDIO Interface Input Timing

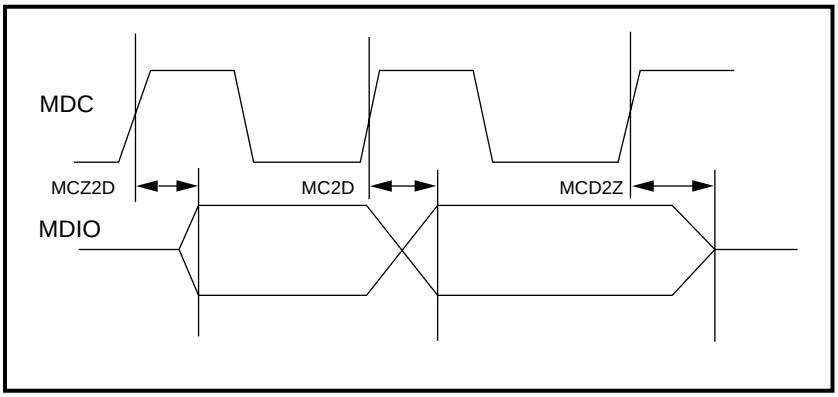
CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Setup Time: MDC to MDIO	MIO_{SU}		10			ns
Hold Time: MDC to MDIO	MIO_{HD}		10			ns
Max Frequency: MDC	F_{max}				25	MHz



MDIO as an Input to the 78Q2120C

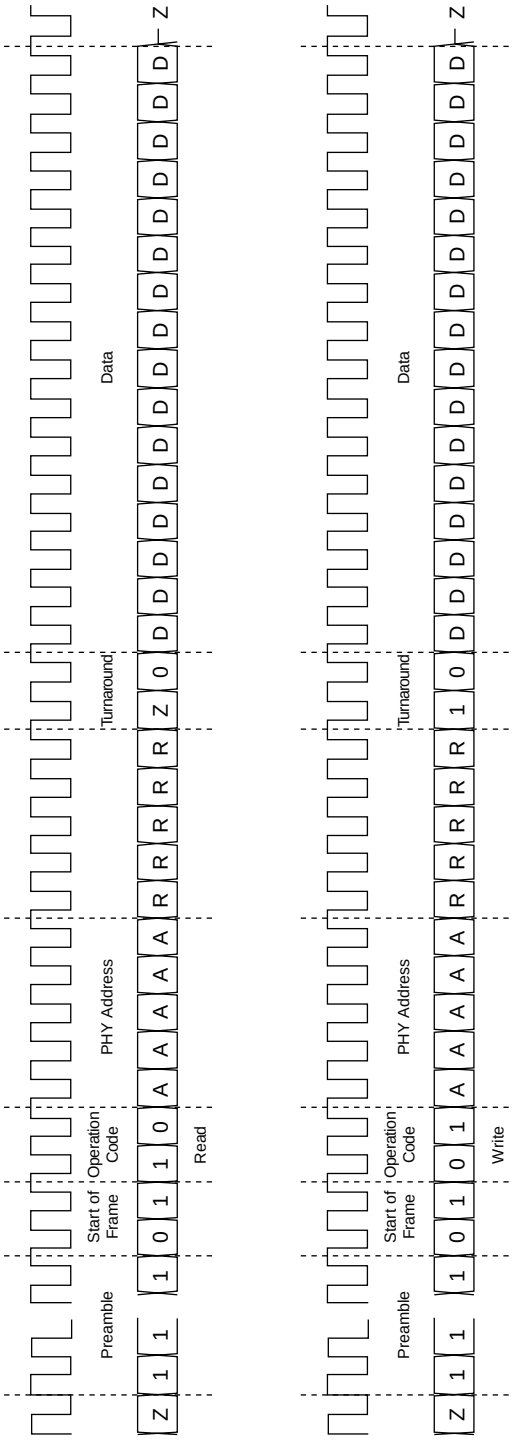
MDIO Interface Output Timing

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
MDC to MDIO data delay	MC2D				30	ns
MDIO output from high Z to driven after MDC	MCZ2D				30	ns
MDIO output from driven to high Z after MDC	MCD2Z				30	ns



MDIO as an Output from the 78Q2120C

MDIO Interface Output Timing



100BASE-TX System Timing

System timing requirements for 100BASE-TX operation are listed in Table 24-2 of Clause 24 of IEEE 802.3.

PARAMETER	CONDITION	NOM	UNIT
TX_EN Sampled to first bit of "J" on MDI output		12	BT
First bit of "J" on MDI input to CRS assert		16	BT
First bit of "T" on MDI input to CRS de-assert		23	BT
First bit of "J" on MDI input to COL assert		20	BT
First bit of "T" on MDI input to COL de-assert		24	BT
TX_EN Sampled to CRS assert	RPTR = low	6	BT
TX_EN sampled to CRS de-assert	RPTR = low	6	BT

10BASE-T System Timing

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TX_EN (MII) to TD Delay				6	BT
RD to RXD at (MII) Delay				6	BT
Collision delay				9	BT
SQE test wait			1		μs
SQE test duration			1		μs
Jabber on-time*		20		150	ms
Jabber off-time*		250		750	ms

***** Guarantee by design. The specifications in the following table are included for information only.

ANALOG ELECTRICAL CHARACTERISTICS

100BASE-TX Transmitter

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Peak Output Amplitude (|Vp+|, |Vp-|) (see note below)	Best-fit over 14 bit times; 0.5 dB Transformer loss	950		1050	mVpk
Output Amplitude Symmetry	$\frac{\lvert Vp+\rvert}{\lvert Vp-\rvert}$	0.98		1.02	
Output Overshoot	Percent of Vp+, Vp-			5	%
Rise/Fall time (tr, tf)	10-90% of Vp+, Vp-	3		5	ns
Rise/Fall time Imbalance	$\lvert tr - tf \rvert$			500	ps
Duty Cycle Distortion	Deviation from best-fit time-grid; 010101... Sequence			±250	ps
Jitter	Scrambled Idle			1.4	ns

Note: Measured at the line side of the transformer.

Test Condition: Transformer P/N: TLA-6T103

Line Termination: 100Ω ±1%

100BASE-TX Transmitter (Informative)

The specifications in the following table are included for information only. They are mainly a function of the external transformer and termination resistors used for measurements.

PARAMETER	CONDITION	MIN	MAX	UNIT
Return Loss	2 < f < 30 MHz 30 < f < 60 MHz 60 < f < 80 MHz	16 $16 - 20\log\left(\frac{f}{30\,MHz}\right)$ 10		dB
Open-Circuit Inductance	-8 < Iin < 8 mA	350		µH

100BASE-TX Receiver

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Signal Detect Assertion Threshold		500	600	700	mVppd
Signal Detect De-assertion Threshold		275	350	425	mVppd
Differential Input Resistance			20		kΩ
Jitter Tolerance (pk-pk)	Not tested in production	4			ns
Baseline Wander Tracking		-75		+75	%
Signal Detect Assertion Time	Not tested			1000	μs
Signal Detect De-assertion Time	Not tested			4	μs

10BASE-T Transmitter

The Manchester-encoded data pulses, the link pulse and the start-of-idle pulse are tested against the templates and using the procedures found in Clause 14 of IEEE 802.3.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Peak Differential Output Signal (see note below)	All data patterns	2.2		2.8	V
Harmonic Content (dB below fundamental)	All ones data Not tested	27			dB
Link Pulse Width			100		ns
Start-of-Idle Pulse Width	Last bit 0 Last bit 1		300 350		ns ns

Note: Measured at the line side of the transformer.

Test Condition: Transformer P/N: TLA-6T103

Line Termination: 100Ω ±1%

10BASE-T Transmitter (Informative)

The specifications in the following table are included for information only. They are mainly a function of the external transformer and termination resistors used for measurements.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Output return loss		15			dB
Output Impedance Balance	1 MHz < freq < 20 MHz	$29 - 17\log\left(\frac{f}{10}\right)$			dB
Peak Common-mode Output Voltage				50	mV
Common-mode rejection	15 V_{pk}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.			100	mV
Common-mode rejection jitter	15 V_{pk}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.			1	ns

10BASE-T Receiver

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DLL Phase Acquisition Time			10		BT
Jitter Tolerance (pk-pk)		30			ns
Input Squelched Threshold		500	600	700	mVppd
Input Unsquelched Threshold		275	350	425	mVppd
Differential Input Resistance			20		kΩ
Bit Error Ratio			10^{-10}		
Common-mode rejection	Square wave 0 < f < 500 kHz Not tested	25			V

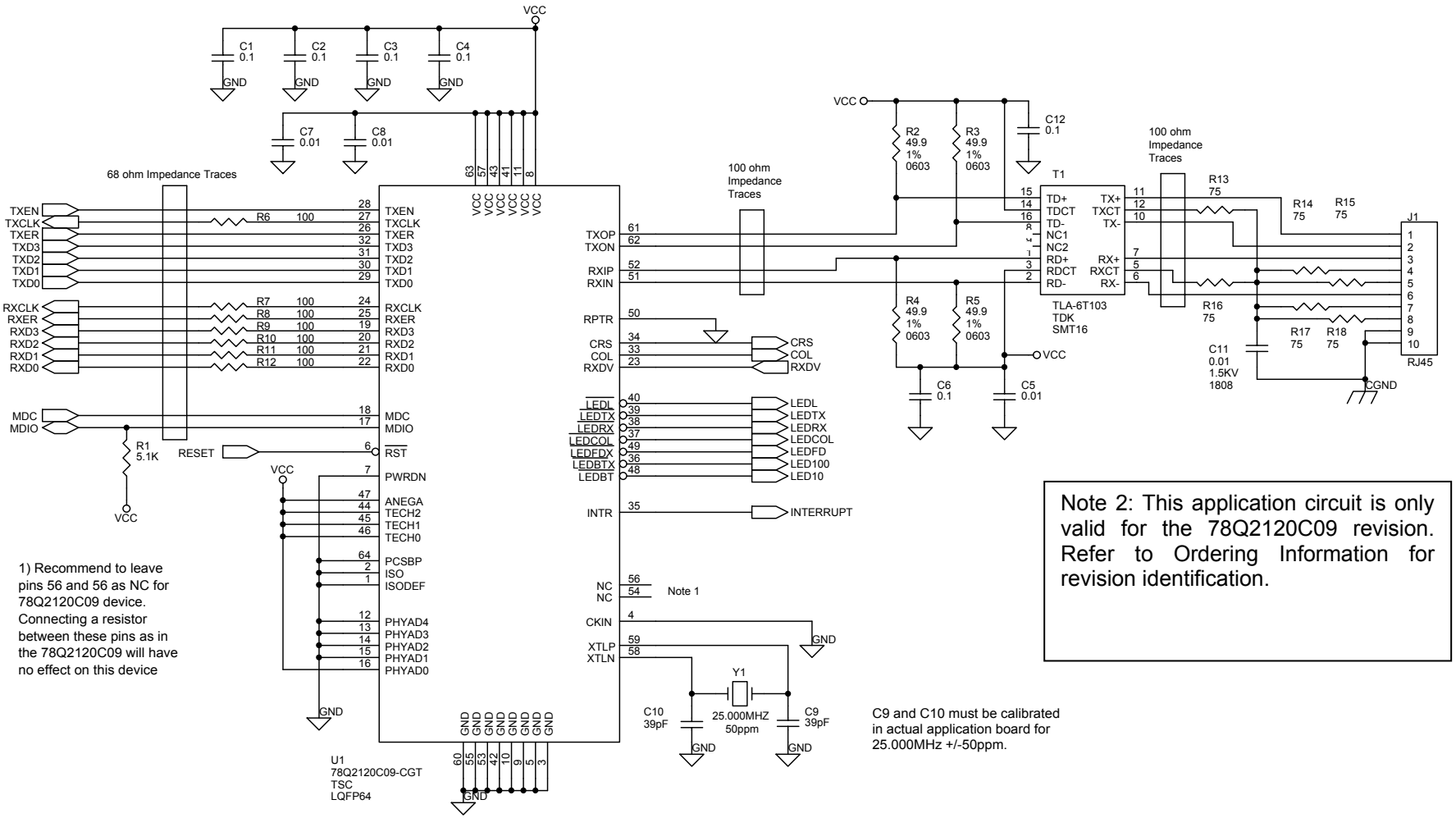


FIGURE 1: TYPICAL APPLICATIONS CIRCUIT

ISOLATION TRANSFORMERS

Two simple 1:1 isolation transformers are required at the line interface. Transformers with integrated common-mode choke are recommended for exceeding FCC requirements. This table gives the recommended line transformer characteristics:

NAME	VALUE	CONDITION
Turns Ratio	1 CT : 1 CT ± 5%	
Open-Circuit Inductance	350 μH (min)	@ 10 mV, 10 kHz
Leakage Inductance	0.40 μH (max)	@ 1 MHz (min)
Inter-Winding Capacitance	25 pF (max)	
D.C. Resistance	0.9 Ω (max)	
Insertion Loss	0.4 dB (typ)	0 - 65 MHz
HIPOT	1500 Vrms	

Note: The 100Base-TX amplitude specifications assume a transformer loss of 0.4 dB. For the transmit line transformer with higher insertion losses, up to 1.2 dB of insertion loss can be compensated by selecting the appropriate setting in the Transmit Amplitude Selection bits in register MR19.11:10.

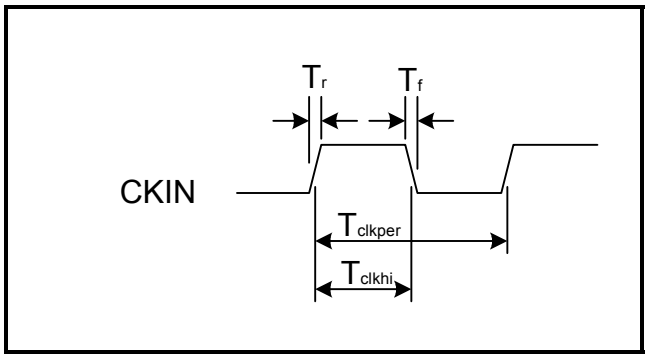
REFERENCE CRYSTAL

If the internal crystal oscillator is to be used, a crystal with the following characteristics should be chosen:

NAME	VALUE	UNITS
Frequency	25.00000	MHz
Load Capacitance*	4**	pF
Frequency Tolerance	±50	PPM
Aging	±2	PPM/yr
Temperature Stability (0 - 70°C)	±5	PPM
Oscillation Mode	Parallel Resonance, Fundamental Mode	
Parameters at 25°C ± 2°C ; Drive Level = 0.5 mW		
Drive Level	50 - 100	μW
Shunt Capacitance (max)	8	pF
Motional Capacitance (min)	10	f F
Series Resistance (max)	60	Ω
Spurious Response (max)	> 5 dB below main within 500 kHz	

***** Equivalent differential capacitance across the XTLP/XTLN pins.

** If crystal with a larger load is used, external shunt capacitors to ground should be added to make up the equivalent capacitance difference.



External CKIN Oscillator Characteristics

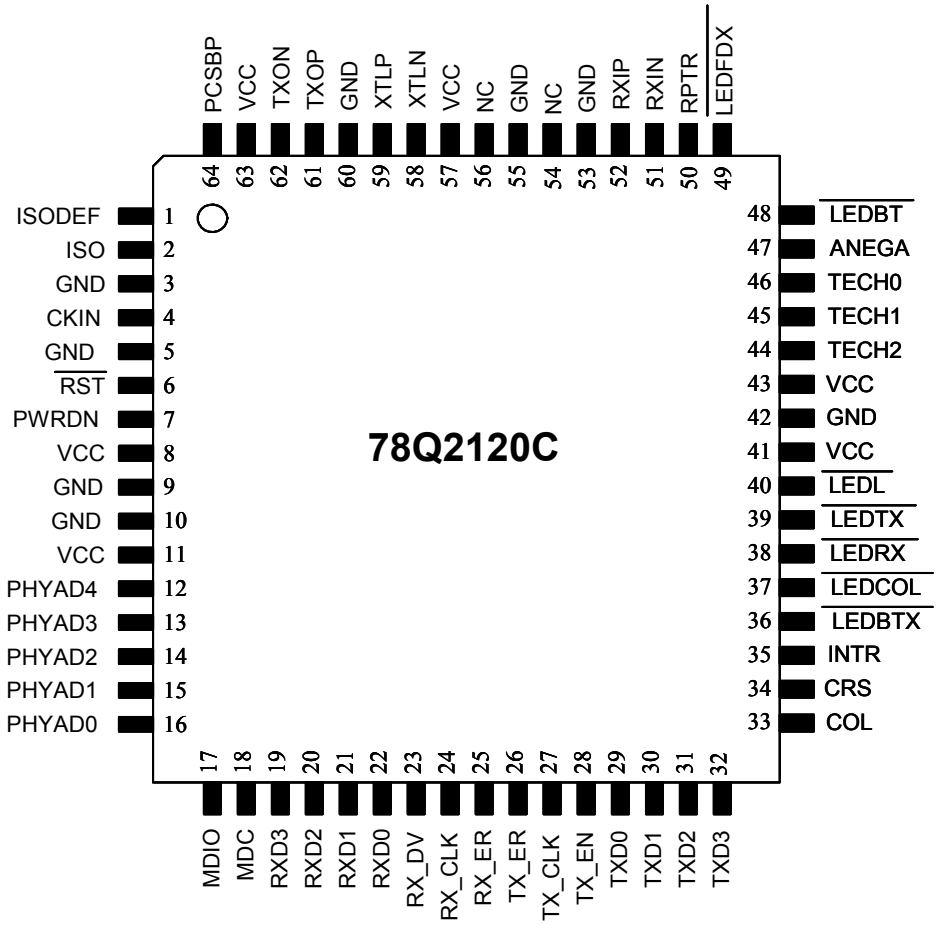
EXTERNAL CKIN OSCILLATOR CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN	NOM	MAX	UNIT
CKIN Frequency	f	See Note 1		25.000		MHz
CKIN Period	Tclkper	See Note 1		40		ns
CKIN Duty Cycle		Tclkhi / Tclkper	45		55	%
Rise / Fall Time	Tr, Tf				4.0	ns
Absolute Jitter		Input signaling requirements = CI			0.1	ns

Note 1: IEEE 802.3 frequency tolerance ±50 ppm

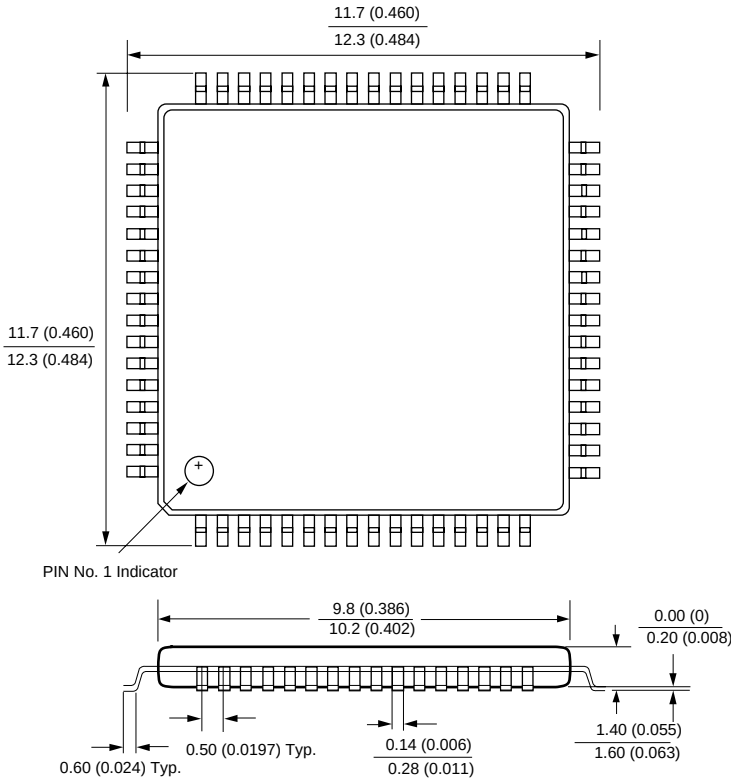
PACKAGE PIN DESIGNATIONS

(Top View)



MECHANICAL SPECIFICATIONS

64-LQFP (Top View)



ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
78Q2120C (Revision 9) 64-pin LQFP	78Q2120C09-64CGT	78Q2120C-CGT xxxxxxxxxx9
78Q2120C (Revision 9) 64-pin LQFP - Lead Free	78Q2120C09-64CGT/F	78Q2120C-CGT xxxxxxxxxx9F

REVISION HISTORY

Rev. #	Date	Comments
1.0	September 2004	Final Data Sheet release
1.1	January 2005	1. Revised ordering number (added 64) 2. Changed CKIN table title
1.2	August 2005	Company name and logo change
1.3	January 2009	Revised ordering number (deleted A)

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