



RF Power Field Effect Transistors

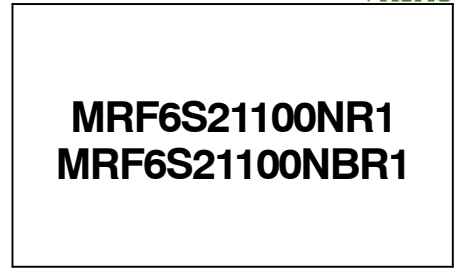
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio, WLL and TD-SCDMA applications.

- Typical 2-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 1050$ mA, $P_{out} = 23$ Watts Avg., $f = 2157.5$ MHz, Channel Bandwidth = 3.84 MHz, PAR = 8.5 dB @ 0.01% Probability on CCDF.
 Power Gain — 14.5 dB
 Drain Efficiency — 25.5%
 IM3 @ 10 MHz Offset — -37 dBc in 3.84 MHz Bandwidth
 ACPR @ 5 MHz Offset — -40 dBc in 3.84 MHz Bandwidth
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2140 MHz, 100 Watts CW Output Power

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Integrated ESD Protection
- Designed for Lower Memory Effects and Wide Instantaneous Bandwidth Applications
- 225°C Capable Plastic Package
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.



2110-2170 MHz, 23 W AVG., 28 V
 2 x W-CDMA
 LATERAL N-CHANNEL
 RF POWER MOSFETs

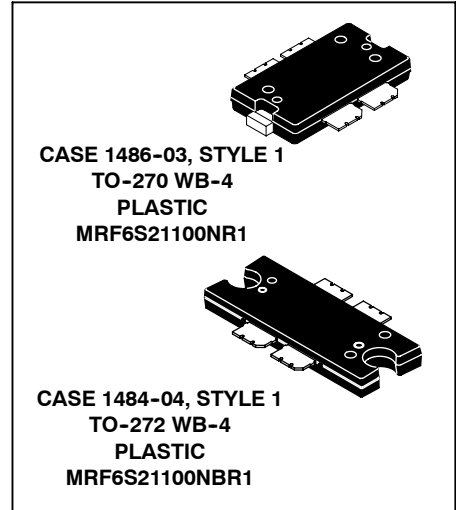


Table 1. Maximum Ratings

| Rating | Symbol | Value | Unit |
|--------------------------------------|-----------|--------------|------|
| Drain-Source Voltage | V_{DSS} | -0.5, +68 | Vdc |
| Gate-Source Voltage | V_{GS} | -0.5, +12 | Vdc |
| Storage Temperature Range | T_{stg} | - 65 to +150 | °C |
| Case Operating Temperature | T_C | 150 | °C |
| Operating Junction Temperature (1,2) | T_J | 225 | °C |

Table 2. Thermal Characteristics

| Characteristic | Symbol | Value (2,3) | Unit |
|---|-----------------|--------------|------|
| Thermal Resistance, Junction to Case Case Temperature 80°C, 100 W CW Case Temperature 73°C, 23 W CW | $R_{\theta JC}$ | 0.57 0.66 | °C/W |

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

LIFETIME BUY

LAST ORDER 1 JUL 11 LAST SHIP 30 JUN 12

Table 3. ESD Protection Characteristics

| Test Methodology | Class |
|---------------------------------------|--------------|
| Human Body Model (per JESD22-A114) | 1B (Minimum) |
| Machine Model (per EIA/JESD22-A115) | A (Minimum) |
| Charge Device Model (per JESD22-C101) | IV (Minimum) |

Table 4. Moisture Sensitivity Level

| Test Methodology | Rating | Package Peak Temperature | Unit |
|--------------------------------------|--------|--------------------------|------|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3 | 260 | °C |

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

Off Characteristics

| | | | | | |
|---|-----------|---|---|----|-----------------|
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 68\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) | I_{DSS} | — | — | 10 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) | I_{DSS} | — | — | 1 | μAdc |
| Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$) | I_{GSS} | — | — | 1 | μAdc |

On Characteristics

| | | | | | |
|---|--------------|-----|------|-----|-----|
| Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 330\ \mu\text{Adc}$) | $V_{GS(th)}$ | 1 | 2 | 3 | Vdc |
| Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_D = 1050\text{ mAdc}$) | $V_{GS(Q)}$ | — | 2.8 | — | Vdc |
| Fixture Gate Quiescent Voltage ⁽¹⁾ ($V_{DD} = 28\text{ Vdc}$, $I_D = 1050\text{ mAdc}$, Measured in Functional Test) | $V_{GG(Q)}$ | 2.2 | 3.1 | 4.4 | Vdc |
| Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 3.3\text{ Adc}$) | $V_{DS(on)}$ | — | 0.24 | — | Vdc |

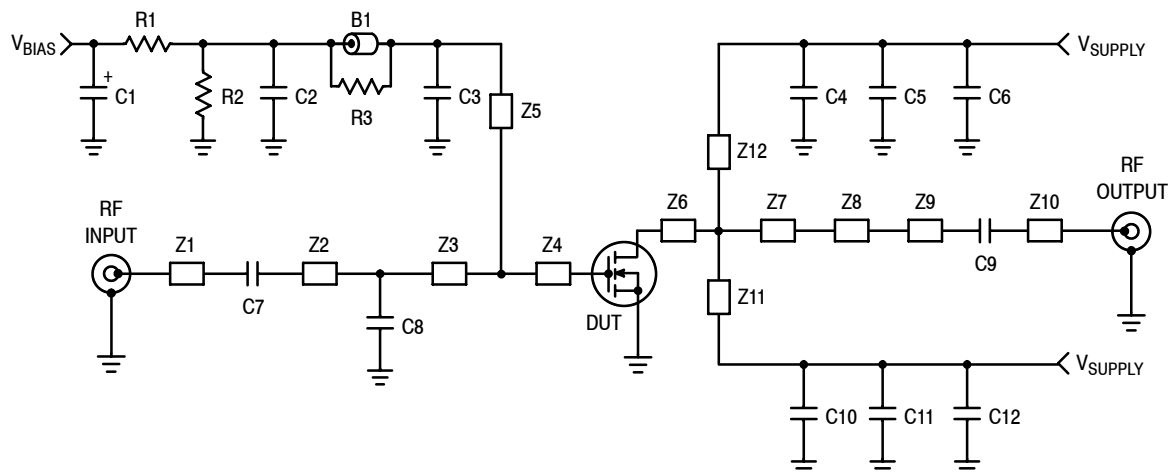
Dynamic Characteristics ⁽²⁾

| | | | | | |
|---|-----------|---|-----|---|----|
| Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$) | C_{rss} | — | 1.5 | — | pF |
|---|-----------|---|-----|---|----|

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1050\text{ mA}$, $P_{out} = 23\text{ W Avg.}$, $f_1 = 2112.5\text{ MHz}$, $f_2 = 2157.5\text{ MHz}$, 2-carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset. IM3 measured in 3.84 MHz Bandwidth @ $\pm 10\text{ MHz}$ Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.

| | | | | | |
|------------------------------|----------|-----|------|-----|-----|
| Power Gain | G_{ps} | 13 | 14.5 | 16 | dB |
| Drain Efficiency | η_D | 24 | 25.5 | 36 | % |
| Intermodulation Distortion | IM3 | -47 | -37 | -35 | dBc |
| Adjacent Channel Power Ratio | ACPR | -50 | -40 | -38 | dBc |
| Input Return Loss | IRL | — | -12 | -10 | dB |

- $V_{GG} = 11/10 \times V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
- Part is internally matched both on input and output.



| | | | |
|---------|----------------------------|----------|---|
| Z1, Z10 | 0.743" x 0.084" Microstrip | Z7 | 0.259" x 0.880" Microstrip |
| Z2 | 0.893" x 0.084" Microstrip | Z8 | 0.215" x 0.230" Microstrip |
| Z3 | 0.175" x 0.084" Microstrip | Z9 | 0.787" x 0.084" Microstrip |
| Z4 | 0.420" x 0.800" Microstrip | Z11, Z12 | 1.171" x 0.120" Microstrip |
| Z5 | 1.231" x 0.040" Microstrip | PCB | Arlon CuClad 250GX-0300-55-22, 0.030", $\epsilon_r = 2.5$ |
| Z6 | 0.100" x 0.880" Microstrip | | |

Figure 1. MRF6S21100NR1(NBR1) Test Circuit Schematic

Table 6. MRF6S21100NR1(NBR1) Test Circuit Component Designations and Values

| Part | Description | Part Number | Manufacturer |
|------------------|---|--|--------------|
| B1 | Ferrite Bead | 25008051107Y0 | Fair-Rite |
| C1 | 10 μ F, 35 V Tantalum Capacitor | T491D106K035AT | Kemet |
| C2 | 0.01 μ F Chip Capacitor | C1825C103J1GAC | Kemet |
| C3, C4, C10 | 5.1 pF Chip Capacitors | ATC100B5R1BT500XT | ATC |
| C5, C6, C11, C12 | 10 μ F, 50 V Chip Capacitors | GRM55DR61H106KA88L | Murata |
| C7 | 10 pF Chip Capacitor | ATC100B100BT500XT | ATC |
| C8 | 1.1 pF Chip Capacitor | ATC100B1R1BT500XT | ATC |
| C9 | 5.1 pF Chip Capacitor (MRF6S21100NR1) 8.2 pF Chip Capacitor (MRF6S21100NBR1) | ATC100B5R1BT500XT ATC100B8R2BT500XT | ATC ATC |
| R1 | 1 k Ω , 1/4 W Chip Resistor | CRCW12061001FKEA | Vishay |
| R2 | 10 k Ω , 1/4 W Chip Resistor | CRCW12061002FKEA | Vishay |
| R3 | 10 Ω , 1/4 W Chip Resistor | CRCW120610R0FKEA | Vishay |

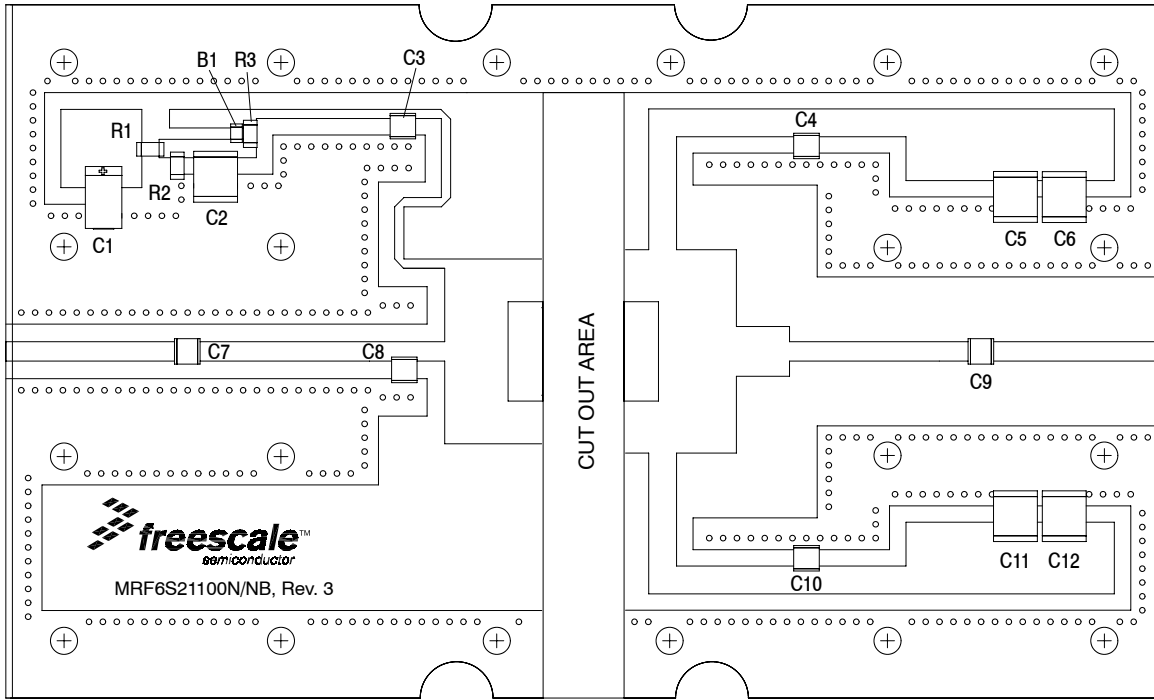


Figure 2. MRF6S21100NR1(NBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

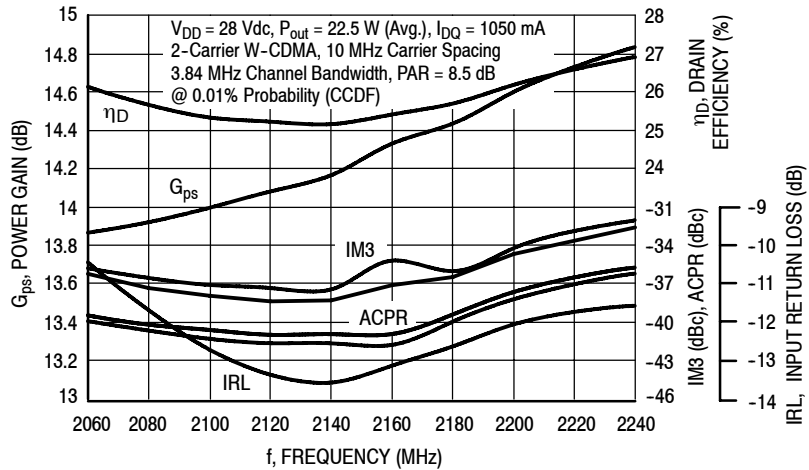


Figure 3. 2-Carrier W-CDMA Broadband Performance @ $P_{out} = 22.5$ Watts Avg.

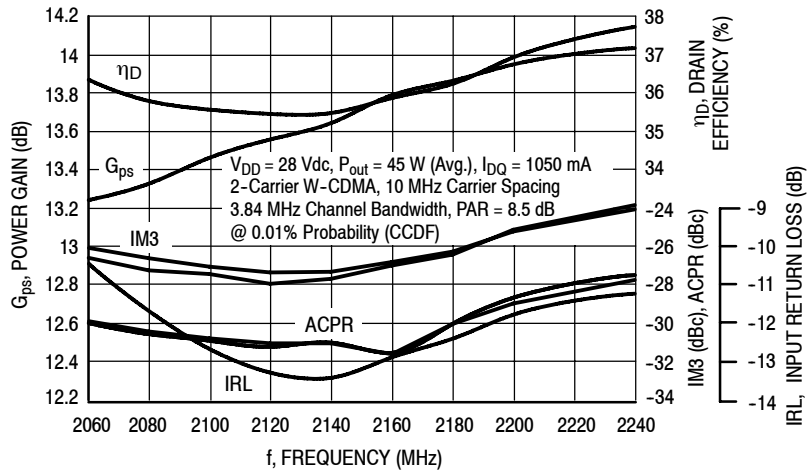


Figure 4. 2-Carrier W-CDMA Broadband Performance @ $P_{out} = 45$ Watts Avg.

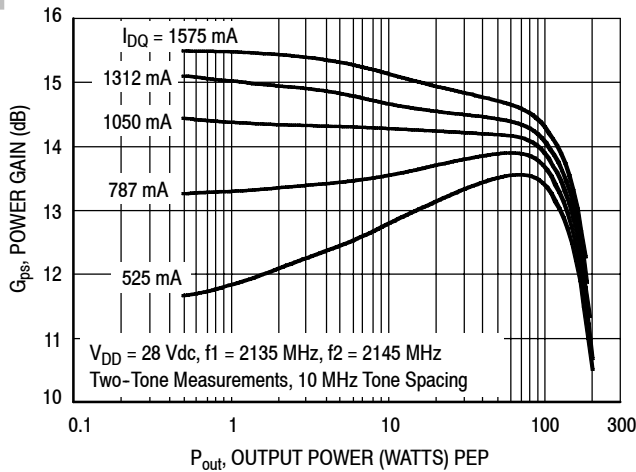


Figure 5. Two-Tone Power Gain versus Output Power

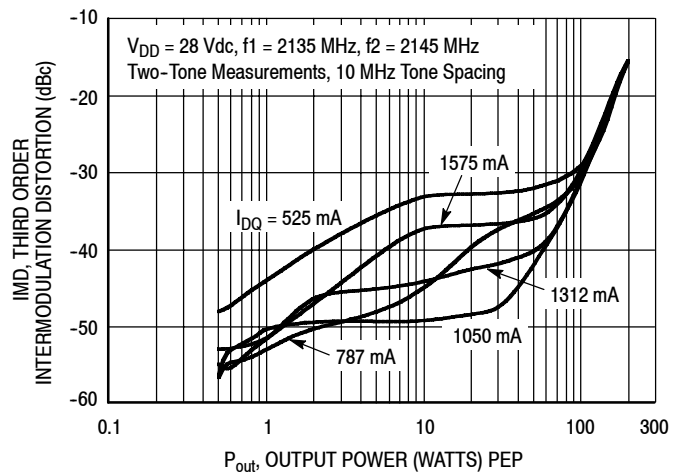


Figure 6. Third Order Intermodulation Distortion versus Output Power

MRF6S21100NR1 MRF6S21100NBR1

TYPICAL CHARACTERISTICS

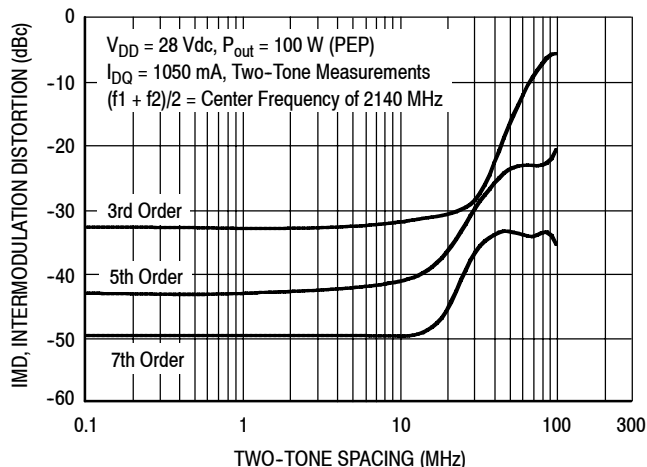


Figure 7. Intermodulation Distortion Products versus Tone Spacing

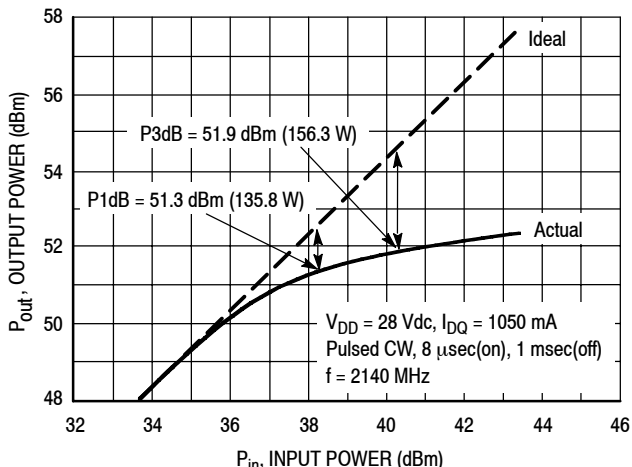


Figure 8. Pulsed CW Output Power versus Input Power

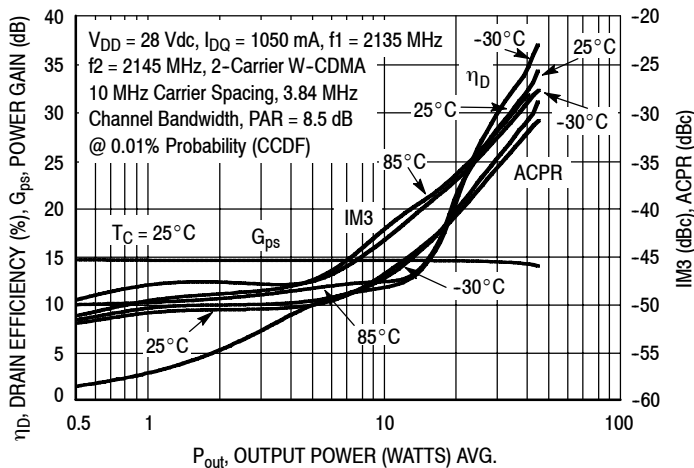


Figure 9. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

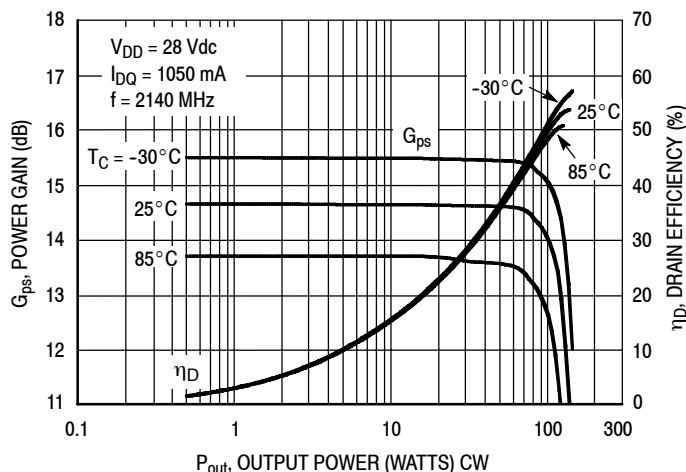


Figure 10. Power Gain and Drain Efficiency versus CW Output Power

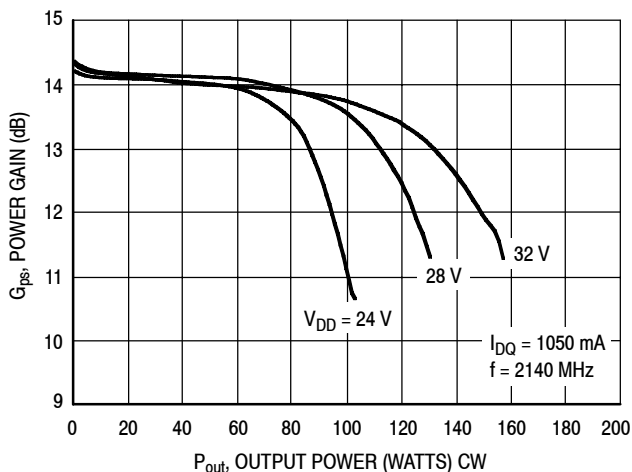
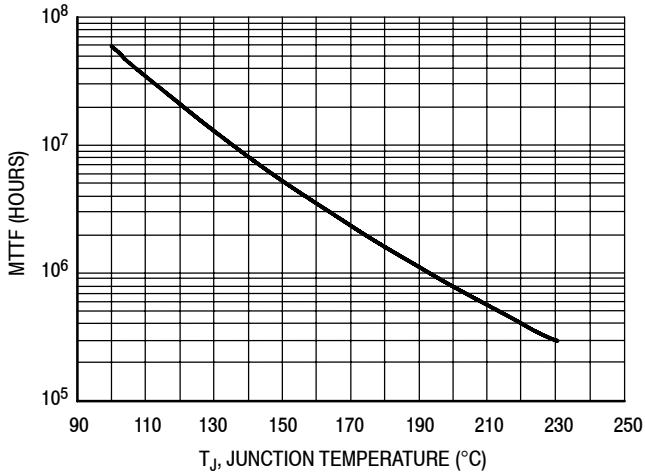


Figure 11. Power Gain versus Output Power

LIFETIME BUY

LAST ORDER 1 JUL 11 LAST SHIP 30 JUN 12

TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 28$ Vdc, $P_{out} = 23$ W Avg., and $\eta_D = 25.5\%$.

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 12. MTTF versus Junction Temperature

W-CDMA TEST SIGNAL

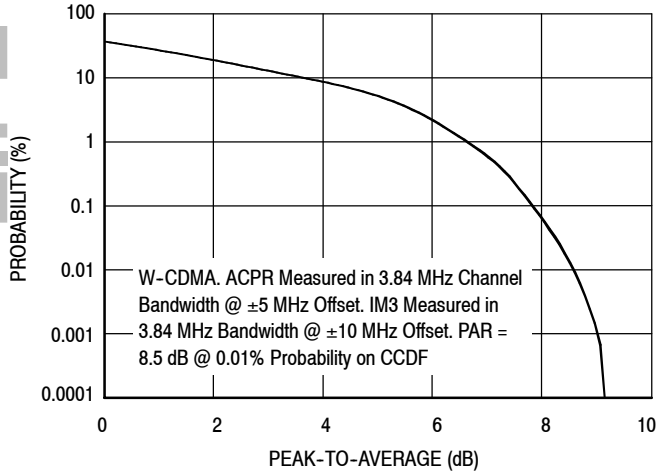


Figure 13. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single-Carrier Test Signal

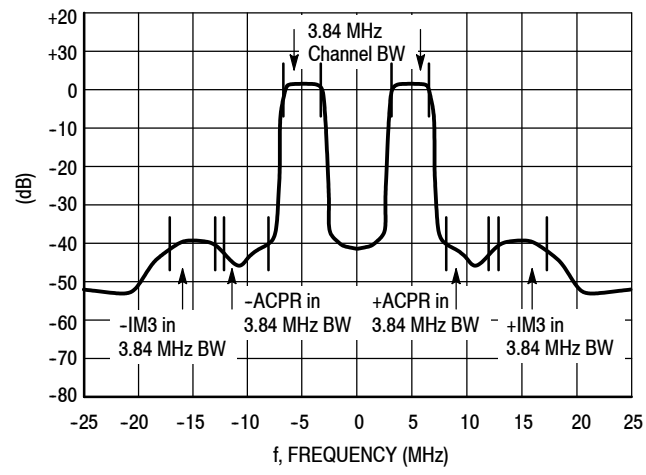
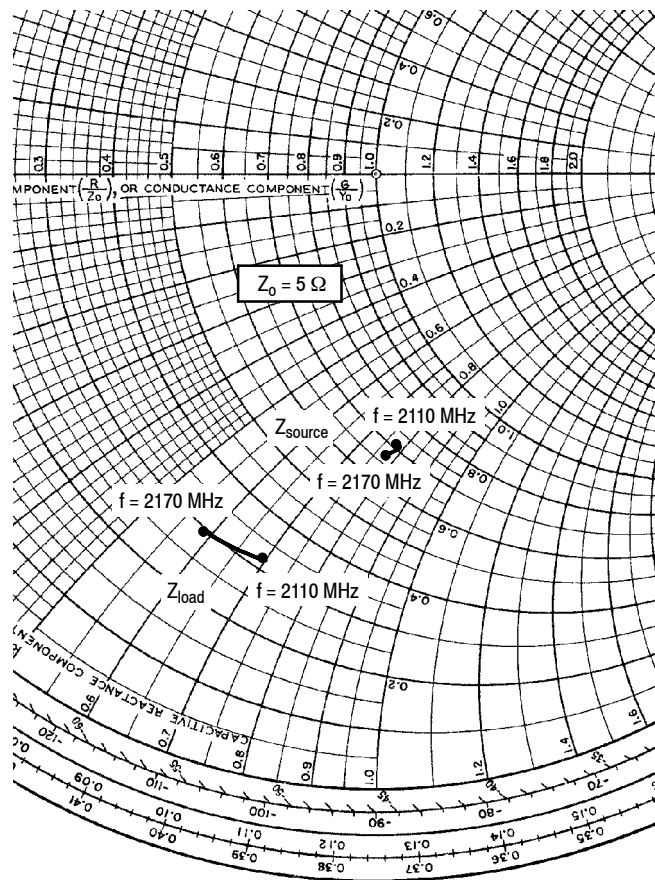
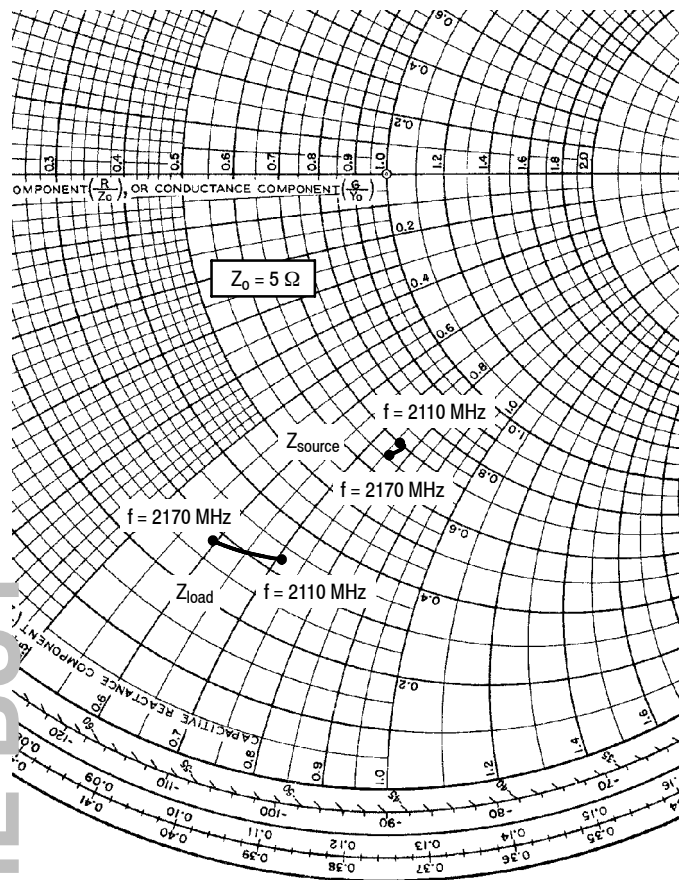


Figure 14. 2-Carrier W-CDMA Spectrum



MRF6S21100NR1

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1050 \text{ mA}$, $P_{out} = 23 \text{ W Avg.}$

| f MHz | Z_{source} Ω | Z_{load} Ω |
|----------|--------------------------|------------------------|
| 2110 | $3.51 - j3.78$ | $1.62 - j3.54$ |
| 2140 | $3.50 - j3.83$ | $1.51 - j3.26$ |
| 2170 | $3.29 - j3.78$ | $1.41 - j2.95$ |

MRF6S21100NBR1

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1050 \text{ mA}$, $P_{out} = 23 \text{ W Avg.}$

| f MHz | Z_{source} Ω | Z_{load} Ω |
|----------|--------------------------|------------------------|
| 2110 | $3.56 - j3.92$ | $1.62 - j3.47$ |
| 2140 | $3.55 - j3.97$ | $1.53 - j3.19$ |
| 2170 | $3.34 - j3.90$ | $1.44 - j2.89$ |

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

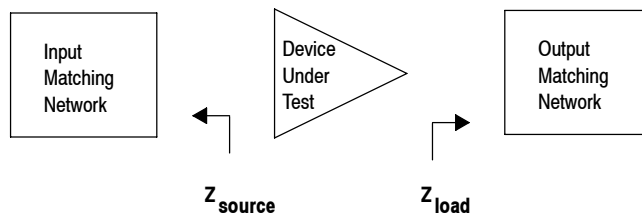
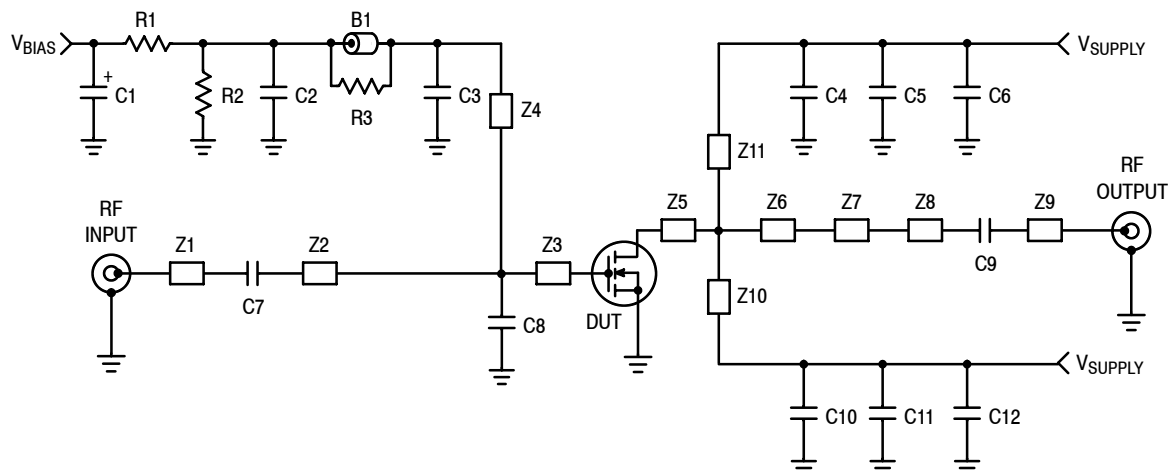


Figure 15. Series Equivalent Source and Load Impedance

TD-SCDMA CHARACTERIZATION



| | | | |
|----|----------------------------|-----|--|
| Z1 | 1.250" x 0.084" Microstrip | Z7 | 0.320" x 0.880" Microstrip |
| Z2 | 0.930" x 0.084" Microstrip | Z8 | 0.370" x 0.200" Microstrip |
| Z3 | 0.470" x 0.800" Microstrip | Z9 | 0.650" x 0.084" Microstrip |
| Z4 | 0.090" x 0.800" Microstrip | Z10 | 1.230" x 0.084" Microstrip |
| Z5 | 1.500" x 0.040" Microstrip | Z11 | 0.870" x 0.120" Microstrip |
| Z6 | 0.160" x 0.880" Microstrip | PCB | Arlon CuClad 250GX-0300-55-22, 0.030", $\epsilon_r = 2.55$ |

Figure 16. MRF6S21100NR1(NBR1) Test Circuit Schematic

Table 7. MRF6S21100NR1(NBR1) Test Circuit Component Designations and Values

| Part | Description | Part Number | Manufacturer |
|------------------|-------------------------------------|--------------------|--------------|
| B1 | Ferrite Bead | 25008051107Y0 | Fair-Rite |
| C1 | 10 μ F, 35 V Tantalum Capacitor | T491D106K035AT | Kemet |
| C2 | 0.01 μ F Chip Capacitor | C1825C103J1GAC | Kemet |
| C3, C4, C10 | 5.1 pF Chip Capacitors | ATC100B5R1BT500XT | ATC |
| C5, C6, C11, C12 | 10 μ F, 50 V Chip Capacitors | GRM55DR61H106KA88L | Murata |
| C7 | 10 pF Chip Capacitor | ATC100B100BT500XT | ATC |
| C8 | 1.1 pF Chip Capacitor | ATC100B1R1BT500XT | ATC |
| C9 | 8.2 pF Chip Capacitor | ATC100B8R2BT500XT | ATC |
| R1 | 1 k Ω , 1/4 W Chip Resistor | CRCW12061001FKEA | Vishay |
| R2 | 10 k Ω , 1/4 W Chip Resistor | CRCW12061002FKEA | Vishay |
| R3 | 10 Ω , 1/4 W Chip Resistor | CRCW120610R0FKEA | Vishay |

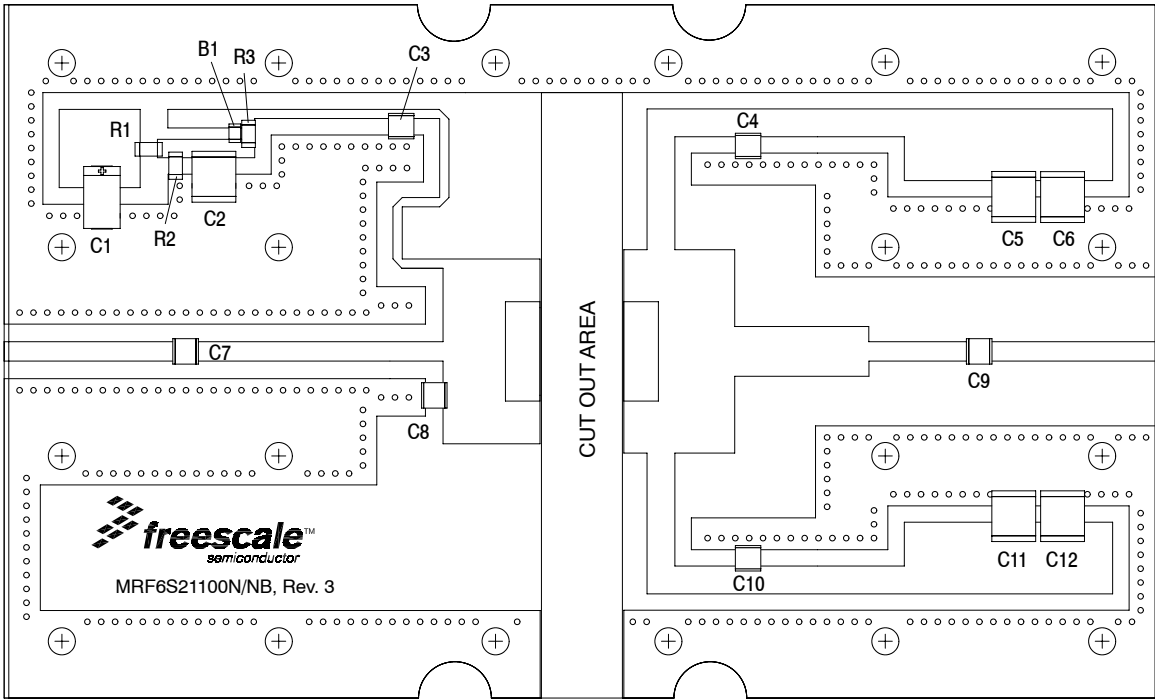


Figure 17. MRF6S21100NR1(NBR1) Test Circuit Component Layout — TD-SCDMA

TYPICAL CHARACTERISTICS

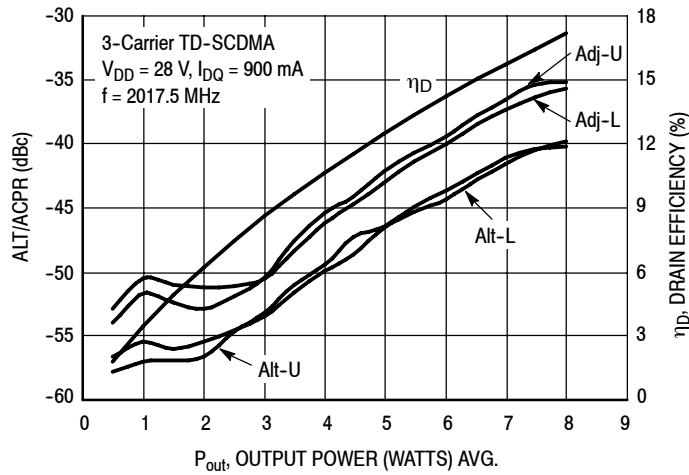


Figure 18. 3-Carrier TD-SCDMA ACPR, ALT and Drain Efficiency versus Output Power

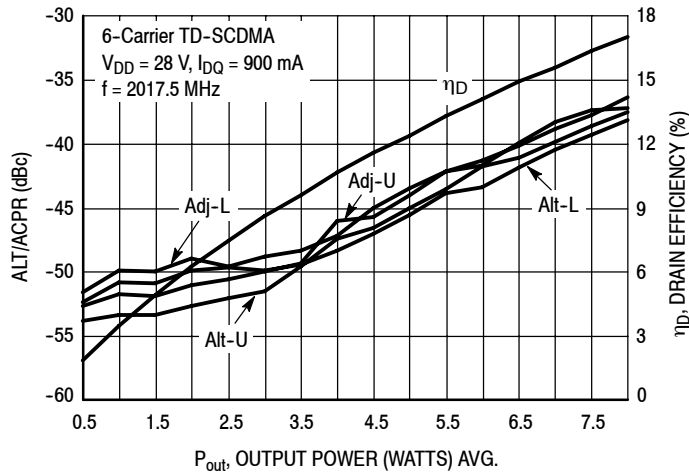


Figure 19. 6-Carrier TD-SCDMA ACPR, ALT and Drain Efficiency versus Output Power

TD-SCDMA TEST SIGNAL

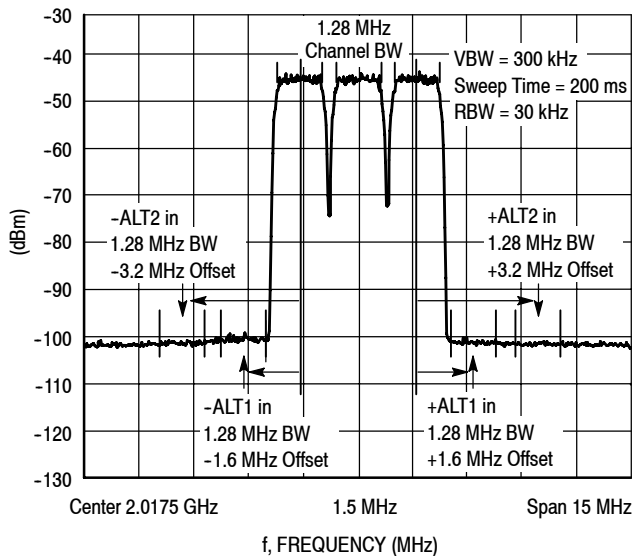


Figure 20. 3-Carrier TD-SCDMA Spectrum

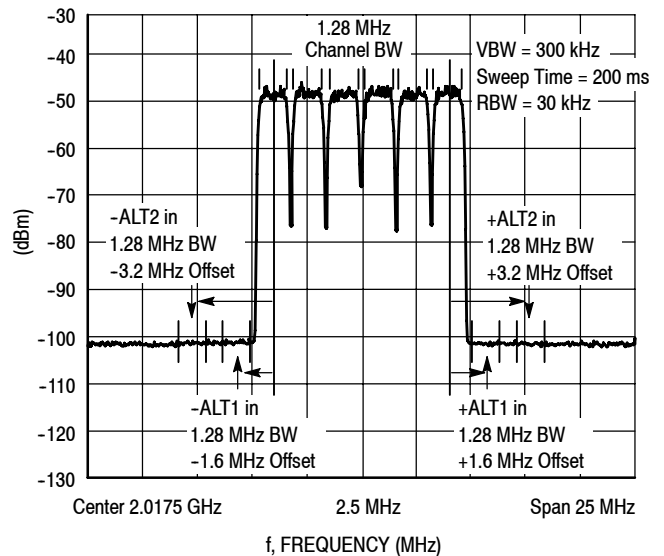
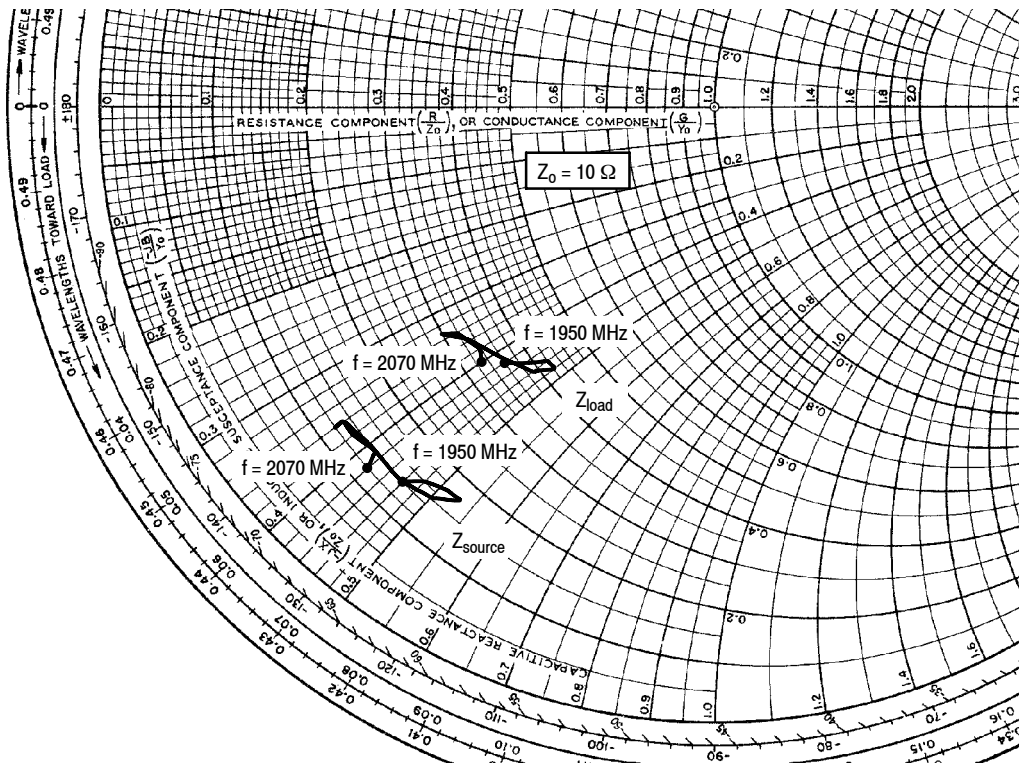


Figure 21. 6-Carrier TD-SCDMA Spectrum



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 900 \text{ mA}$

| f MHz | Z_{source} Ω | Z_{load} Ω |
|-------|-----------------------|---------------------|
| 1950 | 1.43 - j4.56 | 3.61 - j4.19 |
| 1960 | 1.57 - j4.80 | 3.86 - j4.40 |
| 1970 | 1.72 - j5.12 | 4.18 - j4.62 |
| 1980 | 1.65 - j5.27 | 4.21 - j4.81 |
| 1990 | 1.48 - j4.98 | 3.91 - j4.59 |
| 2000 | 1.38 - j4.45 | 3.56 - j4.07 |
| 2010 | 1.35 - j4.01 | 3.31 - j3.62 |
| 2020 | 1.30 - j3.57 | 3.14 - j3.40 |
| 2030 | 1.21 - j3.62 | 2.99 - j3.31 |
| 2040 | 1.25 - j3.61 | 3.02 - j3.31 |
| 2050 | 1.34 - j3.76 | 3.19 - j3.44 |
| 2060 | 1.37 - j4.08 | 3.38 - j3.75 |
| 2070 | 1.24 - j4.24 | 3.33 - j3.99 |

Z_{source} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

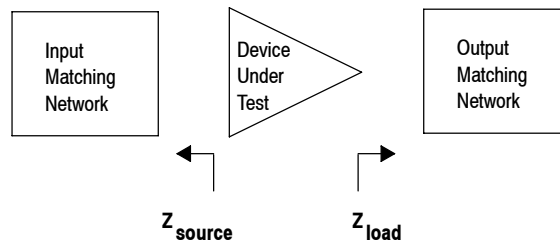
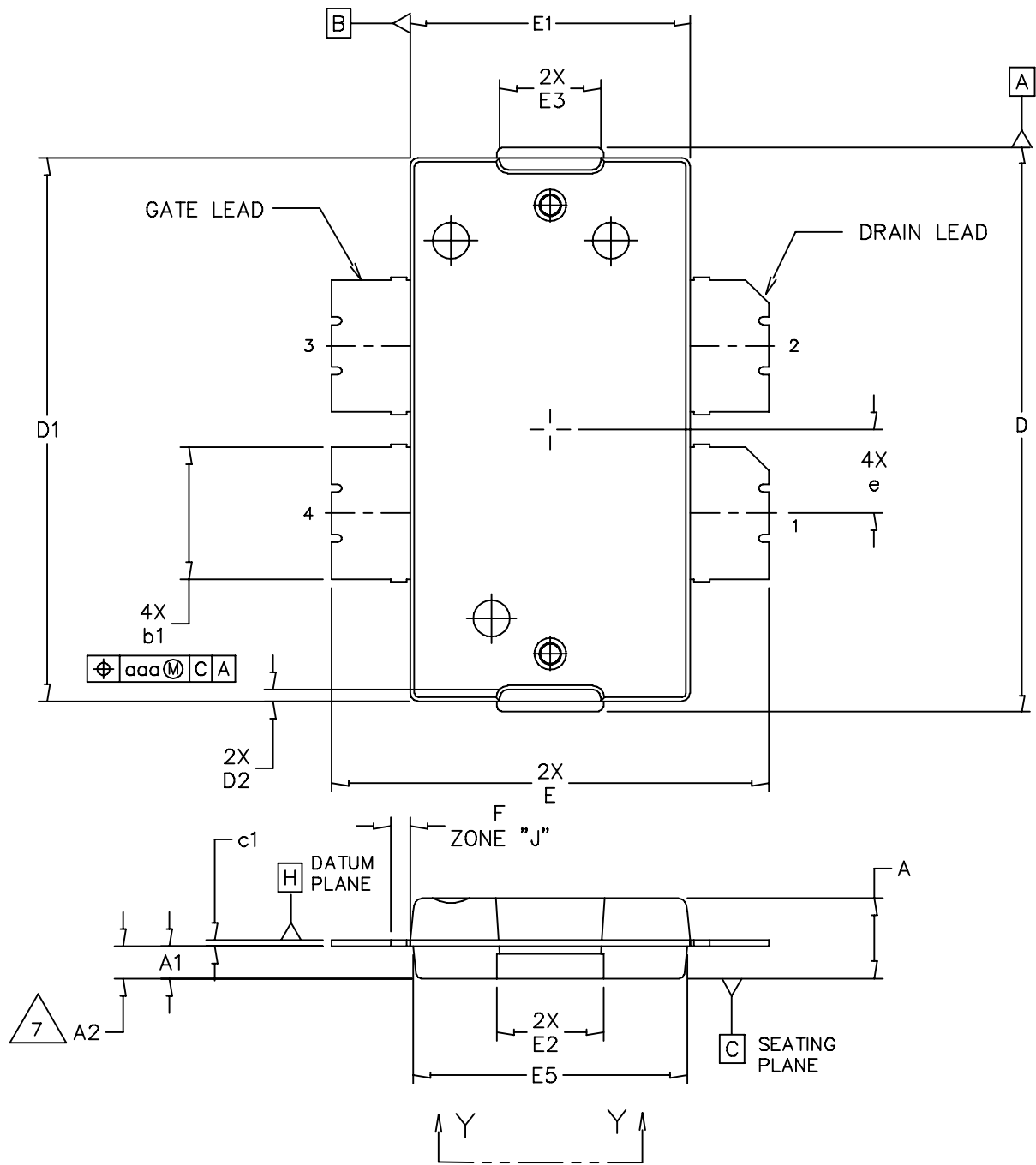


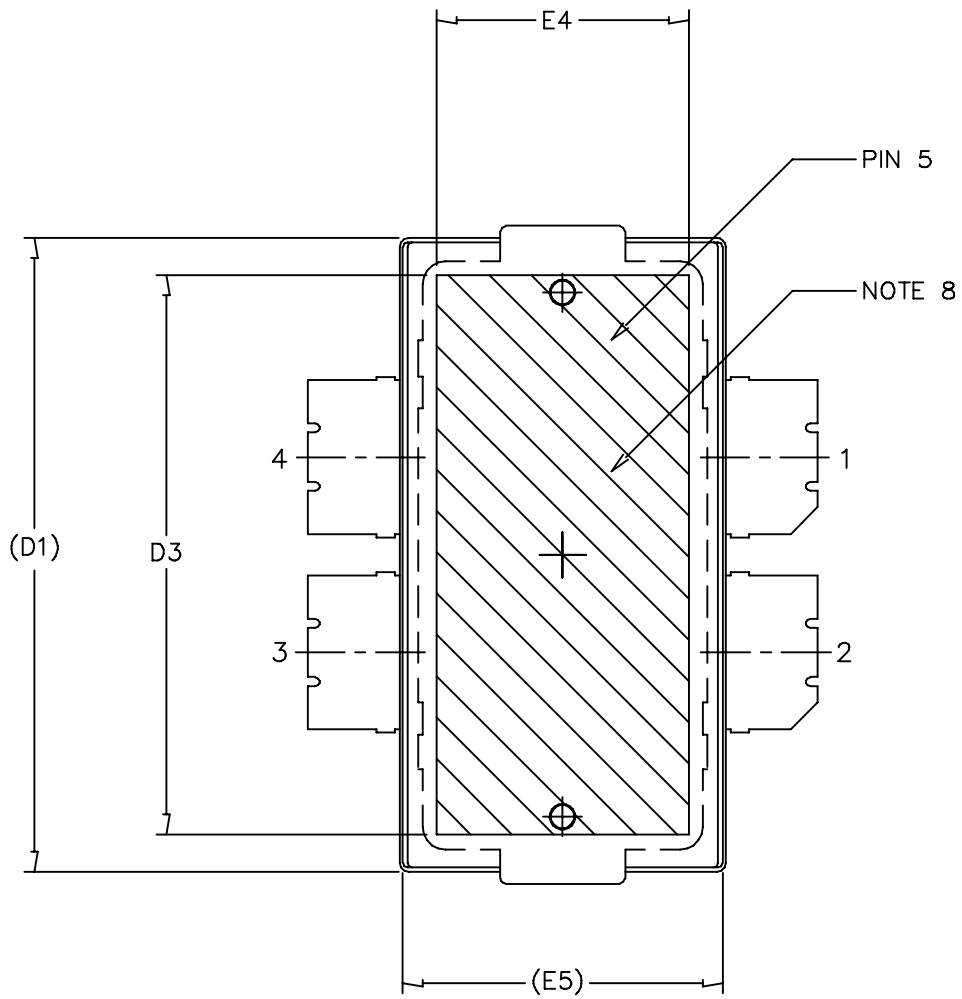
Figure 22. Series Equivalent Source and Load Impedance — TD-SCDMA

PACKAGE DIMENSIONS



| | | | | | |
|---|--|--------------------------|--|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | | MECHANICAL OUTLINE | | PRINT VERSION NOT TO SCALE | |
| TITLE: TO-270 4 LEAD, WIDE BODY | | DOCUMENT NO: 98ASA10577D | | REV: D | |
| | | CASE NUMBER: 1486-03 | | 13 AUG 2007 | |
| | | STANDARD: NON-JEDEC | | | |

MRF6S21100NR1 MRF6S21100NBR1



| | | | |
|---|--------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: TO-270 4 LEAD, WIDE BODY | | DOCUMENT NO: 98ASA10577D | REV: D |
| | | CASE NUMBER: 1486-03 | 13 AUG 2007 |
| | | STANDARD: NON-JEDEC | |

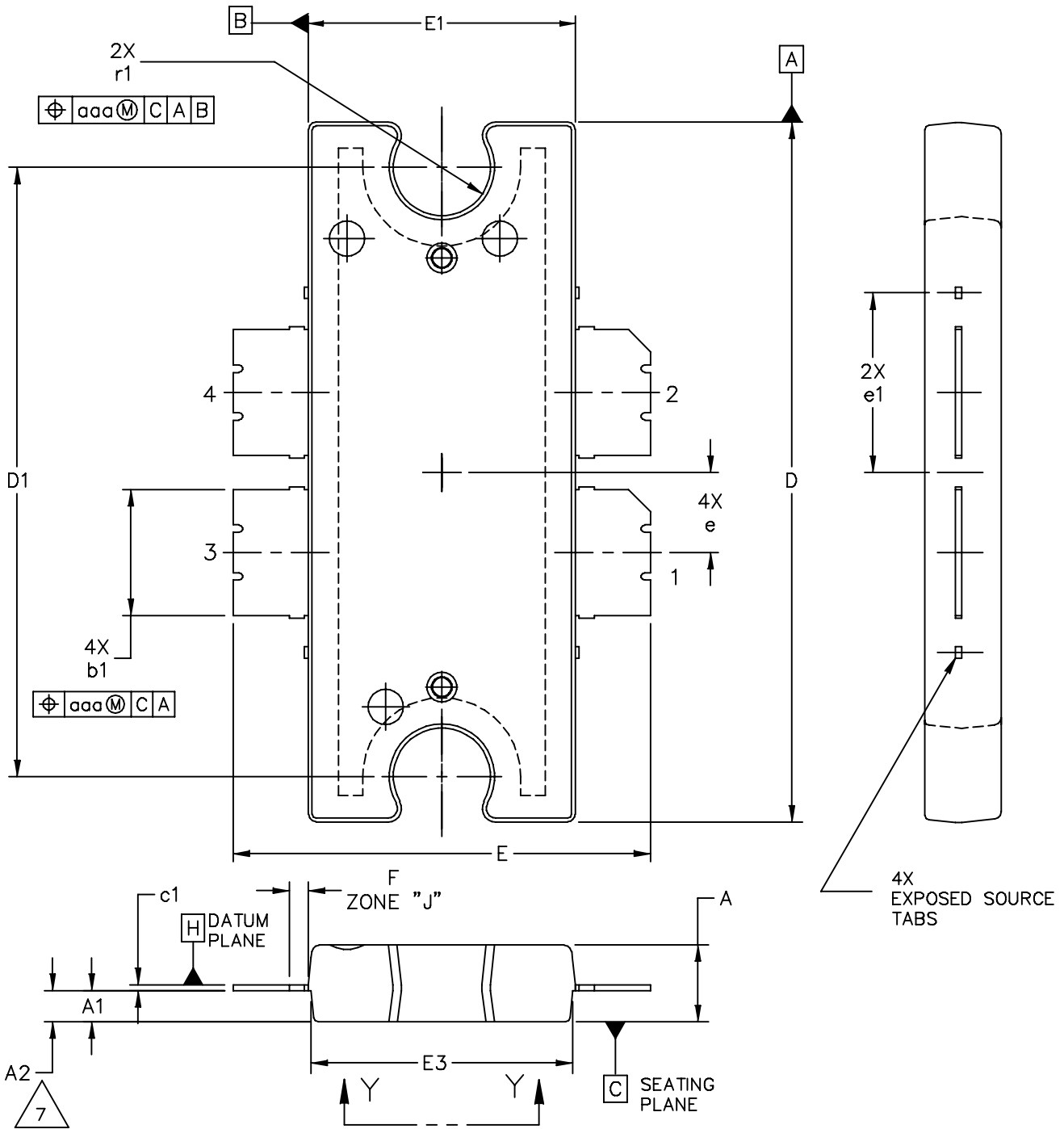
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

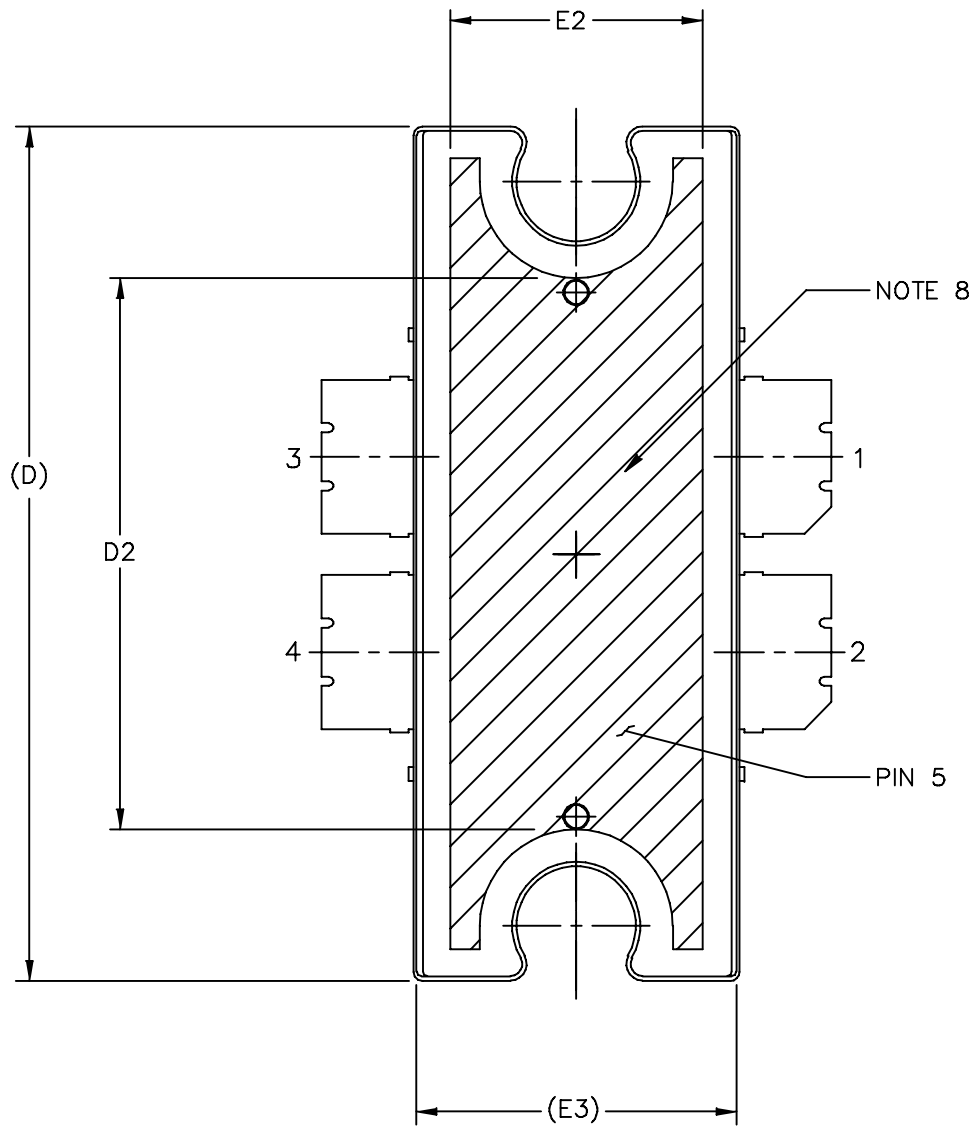
STYLE 1:

PIN 1 - DRAIN PIN 2 - DRAIN
 PIN 3 - GATE PIN 4 - GATE
 PIN 5 - SOURCE

| DIM | INCH | | MILLIMETER | | DIM | INCH | | MILLIMETER | |
|---|------|------|--------------------|-------|--------------------------|----------------------------|------|-------------|------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| A | .100 | .104 | 2.54 | 2.64 | F | .025 BSC | | 0.64 BSC | |
| A1 | .039 | .043 | 0.99 | 1.09 | b1 | .164 | .170 | 4.17 | 4.32 |
| A2 | .040 | .042 | 1.02 | 1.07 | c1 | .007 | .011 | .18 | .28 |
| D | .712 | .720 | 18.08 | 18.29 | e | .106 BSC | | 2.69 BSC | |
| D1 | .688 | .692 | 17.48 | 17.58 | aaa | .004 | | .10 | |
| D2 | .011 | .019 | 0.28 | 0.48 | | | | | |
| D3 | .600 | --- | 15.24 | --- | | | | | |
| E | .551 | .559 | 14 | 14.2 | | | | | |
| E1 | .353 | .357 | 8.97 | 9.07 | | | | | |
| E2 | .132 | .140 | 3.35 | 3.56 | | | | | |
| E3 | .124 | .132 | 3.15 | 3.35 | | | | | |
| E4 | .270 | --- | 6.86 | --- | | | | | |
| E5 | .346 | .350 | 8.79 | 8.89 | | | | | |
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | | | MECHANICAL OUTLINE | | | PRINT VERSION NOT TO SCALE | | | |
| TITLE: TO-270 4 LEAD WIDE BODY | | | | | DOCUMENT NO: 98ASA10577D | | | REV: D | |
| | | | | | CASE NUMBER: 1486-03 | | | 13 AUG 2007 | |
| | | | | | STANDARD: NON-JEDEC | | | | |



| | | | |
|---|--|--------------------------|----------------------------|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE: TO-272 4 LEAD, WIDE BODY | | DOCUMENT NO: 98ASA10575D | REV: E |
| | | CASE NUMBER: 1484-04 | 31 AUG 2007 |
| | | STANDARD: NON-JEDEC | |



| | | | |
|---|--------------------------|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: TO-272 4 LEAD, WIDE BODY | DOCUMENT NO: 98ASA10575D | REV: E | |
| | CASE NUMBER: 1484-04 | 31 AUG 2007 | |
| | STANDARD: NON-JEDEC | | |

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:
 PIN 1 - DRAIN PIN 2 - DRAIN
 PIN 3 - GATE PIN 4 - GATE
 PIN 5 - SOURCE

| DIM | INCH | | MILLIMETER | | DIM | INCH | | MILLIMETER | |
|-----|----------|------|------------|-------|-----|----------------|------|----------------|------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| A | .100 | .104 | 2.54 | 2.64 | b1 | .164 | .170 | 4.17 | 4.32 |
| A1 | .039 | .043 | 0.99 | 1.09 | c1 | .007 | .011 | .18 | .28 |
| A2 | .040 | .042 | 1.02 | 1.07 | r1 | .063 | .068 | 1.60 | 1.73 |
| D | .928 | .932 | 23.57 | 23.67 | e | .106 BSC | | 2.69 BSC | |
| D1 | .810 BSC | | 20.57 BSC | | e1 | .239 INFO ONLY | | 6.07 INFO ONLY | |
| D2 | .600 | --- | 15.24 | --- | aaa | .004 | | .10 | |
| E | .551 | .559 | 14 | 14.2 | | | | | |
| E1 | .353 | .357 | 8.97 | 9.07 | | | | | |
| E2 | .270 | --- | 6.86 | --- | | | | | |
| E3 | .346 | .350 | 8.79 | 8.89 | | | | | |
| F | .025 BSC | | 0.64 BSC | | | | | | |

| | | | |
|---|--------------------------|--------------------|----------------------------|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE: TO-272 4 LEAD WIDE BODY | DOCUMENT NO: 98ASA10575D | | REV: E |
| | CASE NUMBER: 1484-04 | | 31 AUG 2007 |
| | STANDARD: NON-JEDEC | | |

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|----------|-----------|---|
| 2 | Jan. 2007 | <ul style="list-style-type: none"> • Added "TD-SCDMA" to data sheet description paragraph, p. 1 • Removed Total Device Dissipation from Max Ratings table as data was redundant (information already provided in Thermal Characteristics table), p. 1 • Added $V_{GG(Q)}$ and removed Min and Max value for $V_{GS(Q)}$ in On Characteristics table to account for the test fixture's resistor divider network, p. 2 • Removed Forward Transconductance from On Characteristics table as it no longer provided usable information, p. 2 • Updated Part Numbers in Table 6, Component Designations and Values, to RoHS compliant part numbers, p. 3 • Adjusted scale for Fig. 5, Two-Tone Power Gain versus Output Power, to better match the device's capabilities, p. 5 • Removed lower voltage tests from Fig. 11, Power Gain versus Output Power, due to fixed tuned fixture limitations, p. 6 • Replaced Fig. 12, MTTF versus Junction Temperature with updated graph. Removed Amps² and listed operating characteristics and location of MTTF calculator for device, p. 7 • Added TD-SCDMA test circuit schematic, component designations and values, component layout, typical characteristic curves, test signal and series impedance, p. 9-12 • Added Product Documentation and Revision History, p. 17 |
| 3 | Dec. 2008 | <ul style="list-style-type: none"> • Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13232, p. 1, 2 • Changed Storage Temperature Range in Max Ratings table from -65 to +175 to -65 to +150 for standardization across products, p. 1 • Added Case Operating Temperature limit to the Maximum Ratings table and set limit to 150°C, p. 1 • Operating Junction Temperature increased from 200°C to 225°C in Maximum Ratings table, related "Continuous use at maximum temperature will affect MTTF" footnote added and changed 200°C to 225°C in Capable Plastic Package bullet, p. 1 • Corrected V_{DS} to V_{DD} in the RF test condition voltage callout for $V_{GS(Q)}$, On Characteristics table, p. 2 • Updated PCB information to show more specific material details, Figs. 1, 16, Test Circuit Schematic, p. 3, 9 • Updated Part Numbers in Tables 6, 7, Component Designations and Values, to latest RoHS compliant part numbers, p. 3, 9 • Corrected Fig. 15, Series Equivalent Source and Load Impedance's Z_{source} and Z_{load} copy to single-ended, p. 8 • Replaced Case Outline 1486-03, Issue C, with 1486-03, Issue D, p. 13-15. Added pin numbers 1 through 4 on Sheet 1. • Replaced Case Outline 1484-04, Issue D, with 1484-04, Issue E, p. 16-18. Added pin numbers 1 through 4 on Sheet 1, replacing Gate and Drain notations with Pin 1 and Pin 2 designations. |

LIFETIME BUY

LAST ORDER 1 JUL 11 LAST SHIP 30 JUN 12

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2005-2008. All rights reserved.

