

MOSFETs Silicon N-Channel MOS (U-MOSIII)

# SSM3K15ACTC

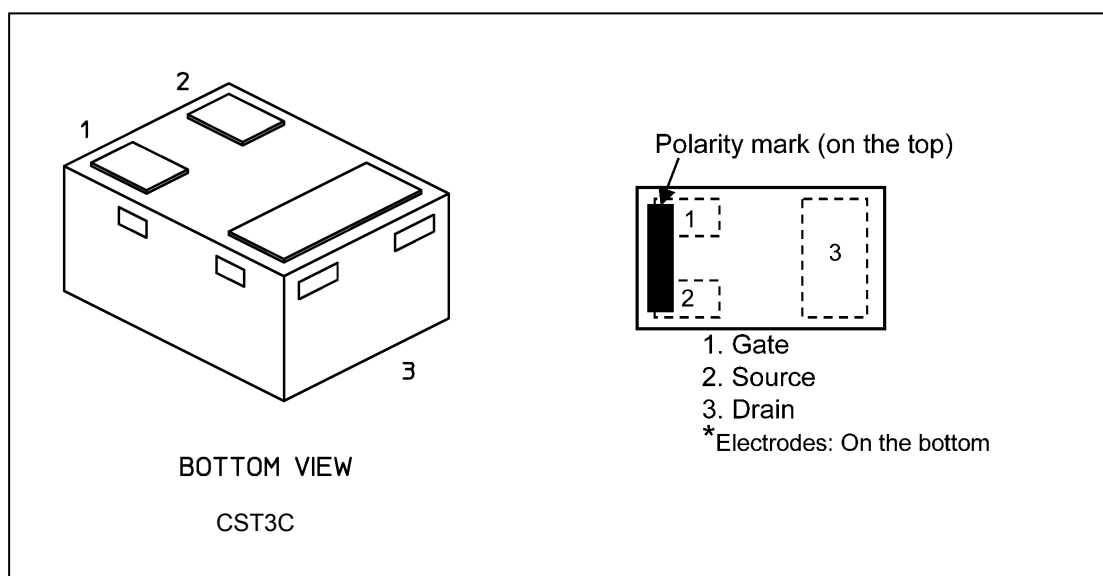
## 1. Applications

- Load Switches

## 2. Features

- (1) 2.5 V drive
- (2) Low drain-source on-resistance
  - :  $R_{DS(ON)} = 3.6 \Omega$  (max) (@ $V_{GS} = 4 V$ )
  - $R_{DS(ON)} = 6.0 \Omega$  (max) (@ $V_{GS} = 2.5 V$ )

## 3. Packaging and Pin Assignment



Start of commercial production

2016-05

### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ °C}$ )

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	30	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	V
Drain current (DC) (Note 1)	$I_D$	100	mA
Drain current (pulsed) (Note 1)	$I_{DP}$	400	
Power dissipation (Note 2)	$P_D$	500	mW
Channel temperature	$T_{ch}$	150	$^{\circ}\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	$^{\circ}\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150  $^{\circ}\text{C}$ .

Note 2: Device mounted on a 25.4 mm  $\times$  25.4 mm  $\times$  1.6 mm FR4 glass epoxy board (Cu pad: 645 mm<sup>2</sup>)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

### 5. Electrical Characteristics

#### 5.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	—	—	1	$\mu\text{A}$
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 0.1\text{ mA}, V_{GS} = 0\text{ V}$	30	—	—	V
Drain-source breakdown voltage (Note 1)	$V_{(BR)DSX}$	$I_D = 0.1\text{ mA}, V_{GS} = -10\text{ V}$	16	—	—	V
Gate threshold voltage (Note 2)	$V_{th}$	$V_{DS} = 3\text{ V}, I_D = 0.1\text{ mA}$	0.8	—	1.5	V
Drain-source on-resistance (Note 3)	$R_{DS(ON)}$	$I_D = 10\text{ mA}, V_{GS} = 2.5\text{ V}$	—	3.5	6.0	$\Omega$
		$I_D = 10\text{ mA}, V_{GS} = 4\text{ V}$	—	2.3	3.6	
Forward transfer admittance (Note 3)	$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 10\text{ mA}$	35	—	—	mS

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to below (1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .

Take this into consideration when using the device.

Note 3: Pulse measurement.

#### 5.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 3\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	13.5	—	pF
Reverse transfer capacitance	$C_{rss}$		—	6.5	—	
Output capacitance	$C_{oss}$		—	8.0	—	
Switching time (turn-on time)	$t_{on}$	$V_{DD} = 5\text{ V}, I_D = 10\text{ mA},$ $V_{GS} = 0\text{ to }5\text{ V}, R_G = 50\text{ }\Omega$ Duty $\leq 1\%$ , $V_{IN}$ : $t_r, t_f < 5\text{ ns}$ , Common source, See Chapter 5.3.	—	5.5	—	ns
Switching time (turn-off time)	$t_{off}$		—	35	—	

#### 5.3. Switching Time Test Circuit

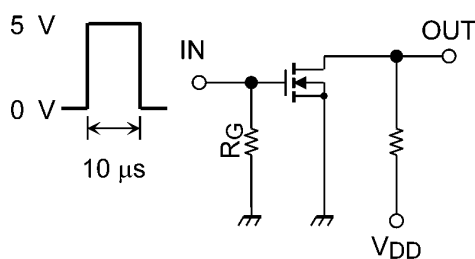


Fig. 5.3.1 Switching Time Test Circuit

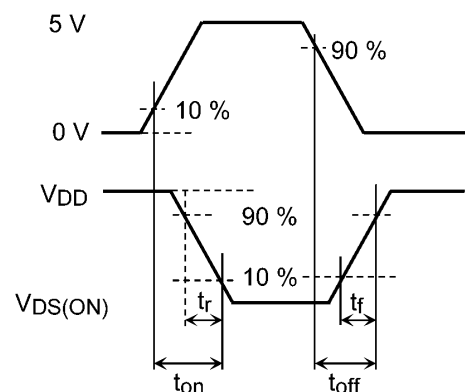


Fig. 5.3.2 Input Waveform/Output Waveform

#### 5.4. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	$V_{DSF}$	$I_D = -100\text{ mA}, V_{GS} = 0\text{ V}$	—	-0.85	-1.2	V

Note 1: Pulse measurement.

## 6. Marking

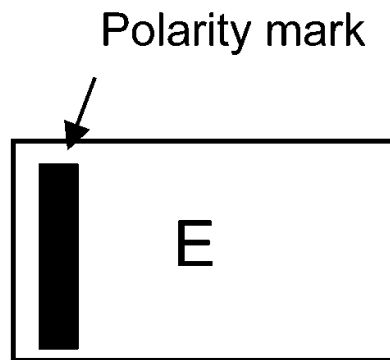
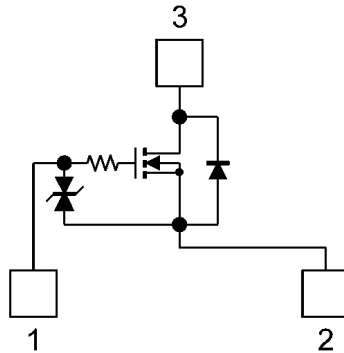
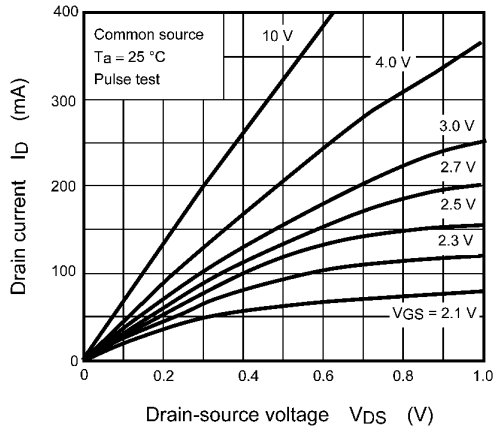


Fig. 6.1 Marking

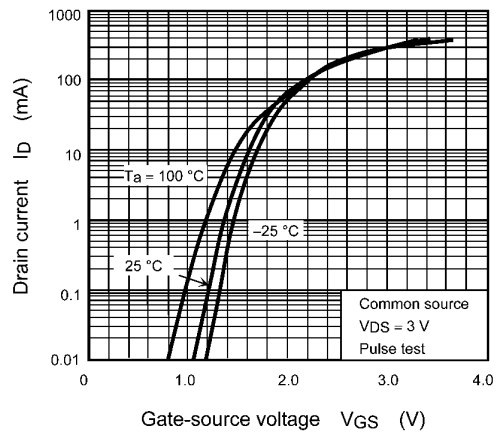
## 7. Equivalent Circuit



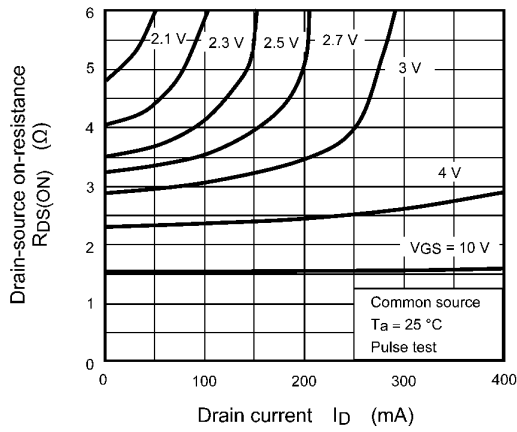
### 8. Characteristics Curves (Note)



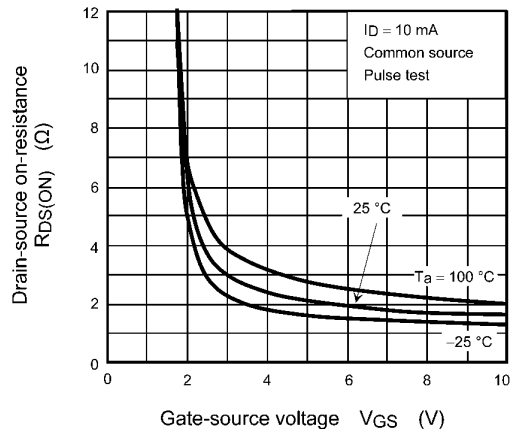
**Fig. 8.1**  $I_D - V_{DS}$



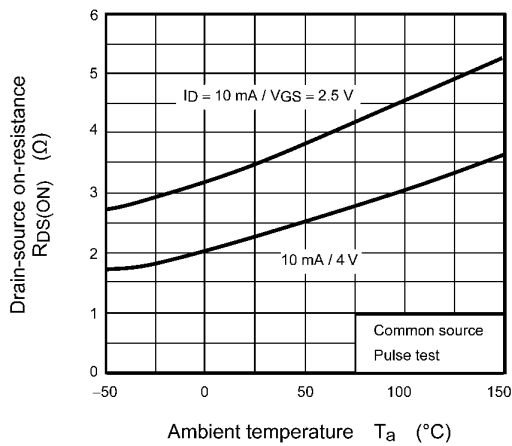
**Fig. 8.2**  $I_D - V_{GS}$



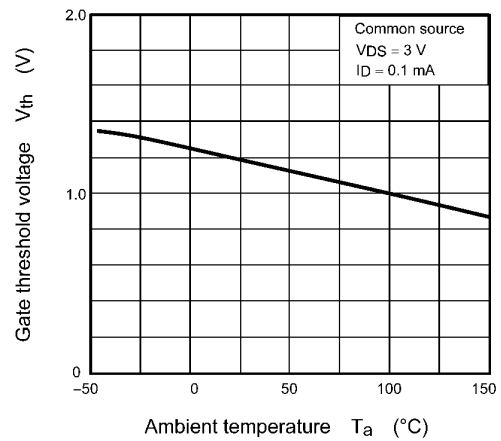
**Fig. 8.3**  $R_{DS(ON)} - V_{GS}$



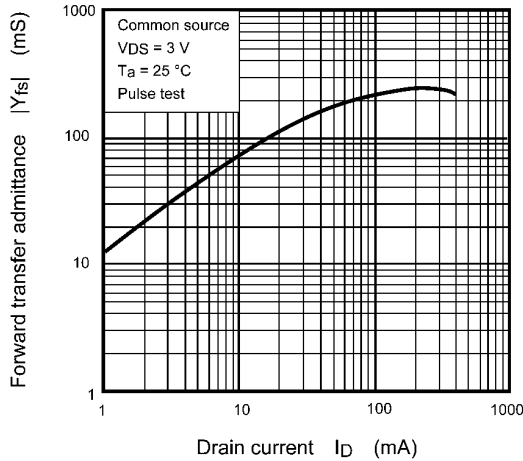
**Fig. 8.4**  $R_{DS(ON)} - I_D$



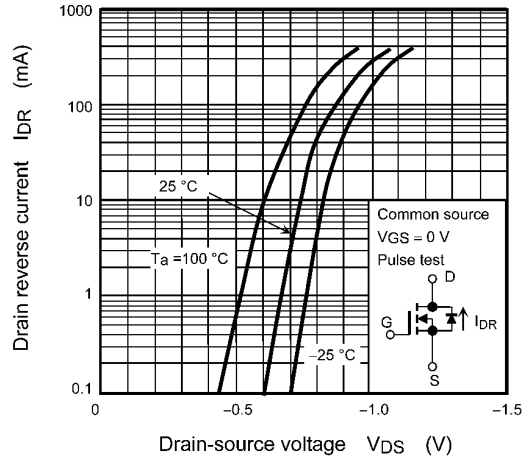
**Fig. 8.5**  $R_{DS(ON)} - T_a$



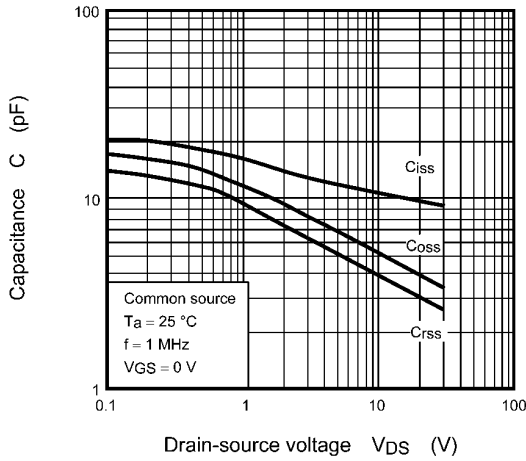
**Fig. 8.6**  $V_{th} - T_a$



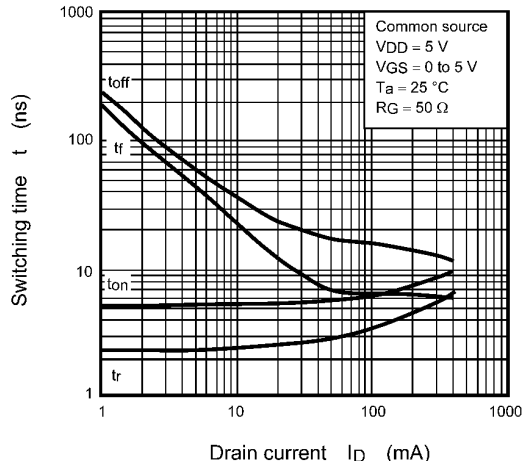
**Fig. 8.7**  $|Y_{fs}| - I_D$



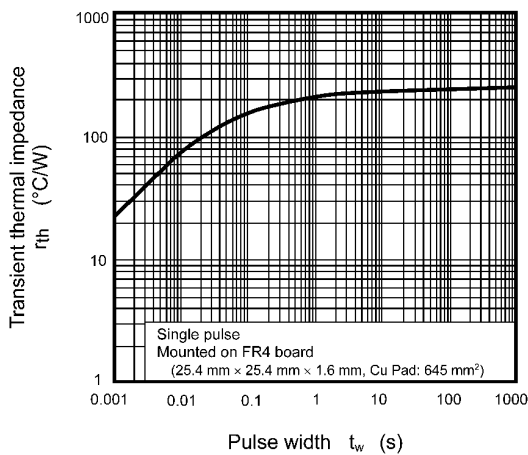
**Fig. 8.8**  $I_{DR} - V_{DS}$



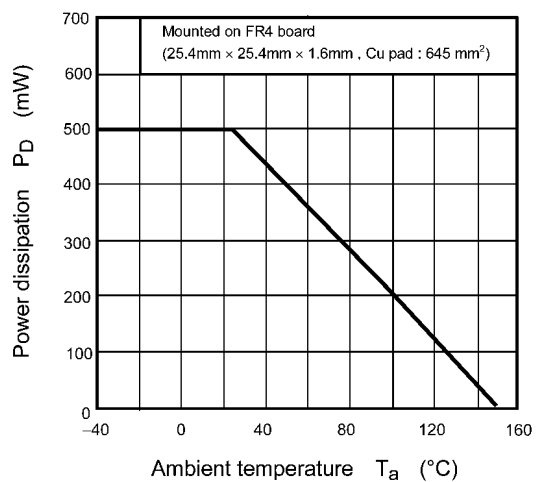
**Fig. 8.9**  $C - V_{DS}$



**Fig. 8.10**  $t - I_D$



**Fig. 8.11**  $r_{th} - t_w$

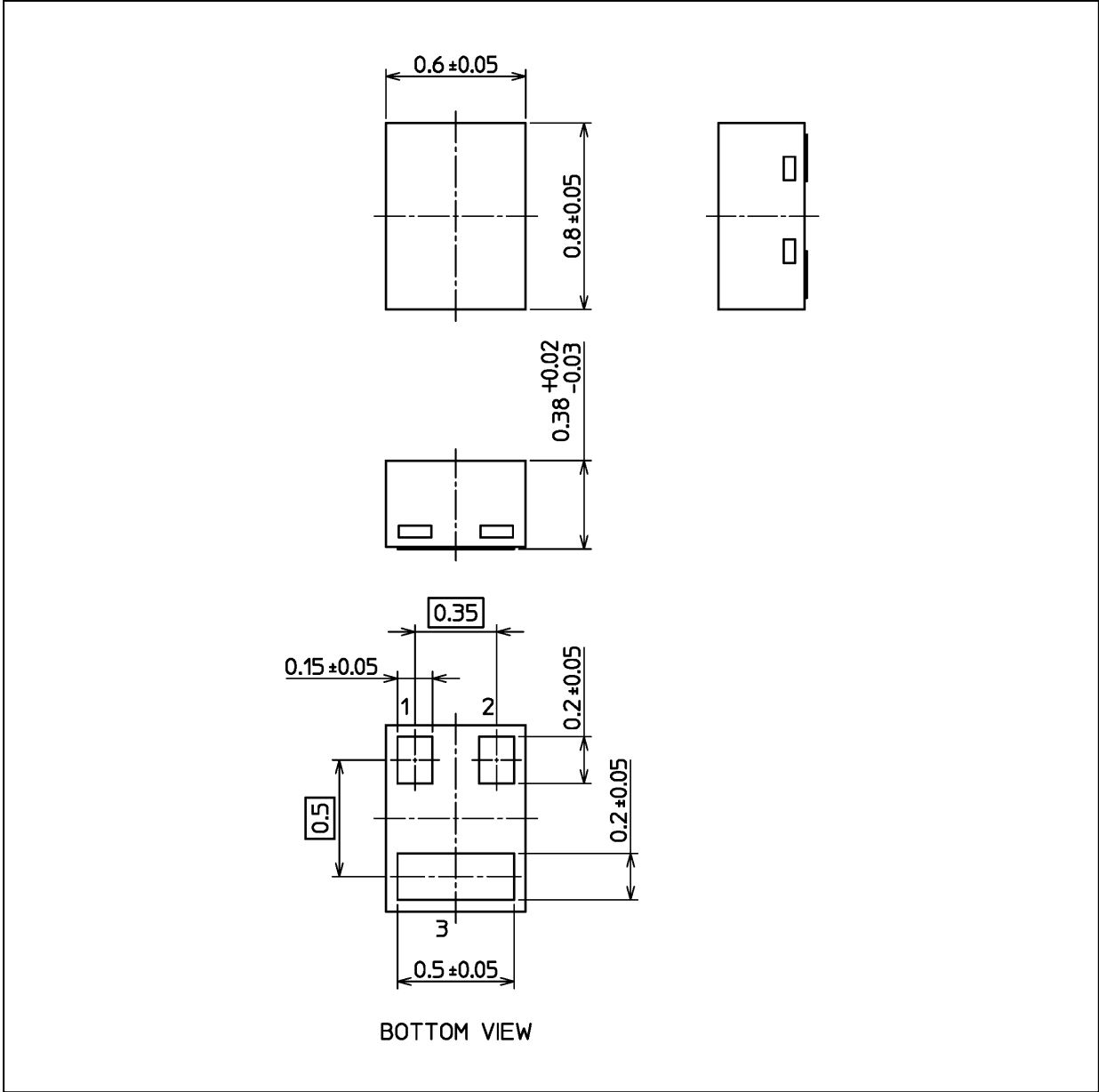


**Fig. 8.12**  $P_D - T_a$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.55 mg (typ.)

Package Name(s)
Nickname: CST3C

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