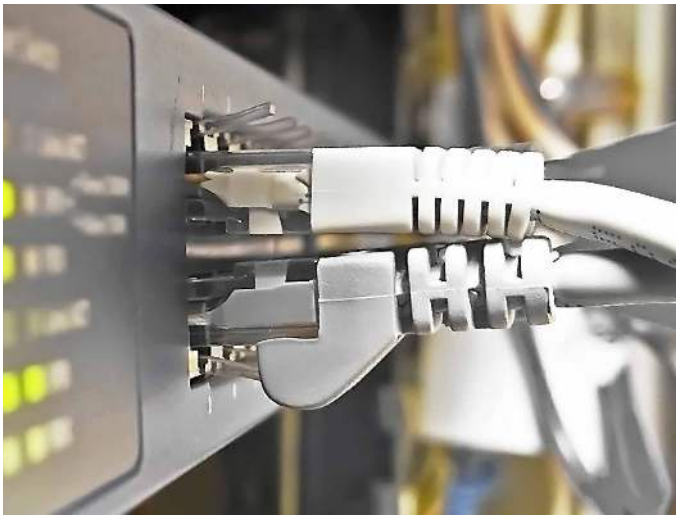
LAYERSCAPE® LX2160A COMMUNICATIONS PROCESSOR

The Layerscape LX2160A SoC delivers the high performance needed for compute-intensive networking applications. Equipped with sixteen Arm®v8 Cortex®-A72 CPU cores, 25 GHz SerDes technology and low FinFET power, this processor supports up to 100 Gbit/s Ethernet and 50 Gbit/s security offload.



OVERVIEW

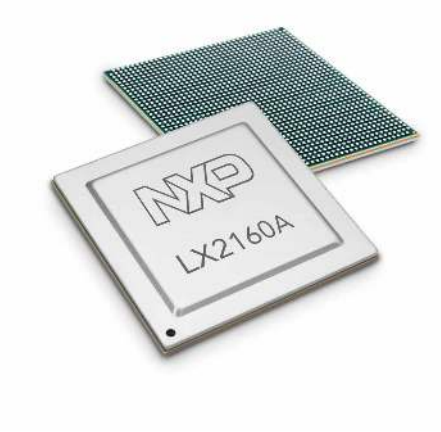
The LX2160A has everything needed for compute-intensive networking applications in a single chip. Sixteen 64-bit Armv8 A72 cores, high integration, and low power make it well-suited for applications that install datacenter-like processing into the highly-constrained power and board space budgets of networking equipment. An innovative caching structure stores packets on-chip until software is ready, minimizing external memory usage for lower latency, lower power, smaller footprint, and lower cost solutions. General-purpose processing capability is complemented with a 50 Gbit/s security engine and a 100 Gbit/s compression/compression engine. The wire rate I/O processor has 18 integrated MACs including dual 100 Gbit Ethernet ports and a 122 Gbit/s L2 switch. The LX2120A and LX2080A are pin-compatible family members that support 12 and 8 cores, respectively.

FEATURES

- 16 64-bit Armv8 Cortex-A72 CPU cores, running up to 2.2 GHz
- 16 MB cache
- 2 x DDR4 72b including ECC, to 3200 MT/s, maximum capacity of 256 GB
- 2 MB packet caching buffer
- 24 SerDes lanes, operating up to 25 GHz
- Up to 16 Ethernet ports
- Supported Ethernet speeds include 1, 2.5, 10, 25, 40, 50, and 100 Gbit/s
- 122 Gbit/s Layer 2 Ethernet switch
- Up to 24 PCIe Gen3 lanes, supporting six ports, as wide as x8
- 50 Gbit/s security accelerator
- 100 Gbit/s data compression/decompression engine
- 4 x SATA3.0
- Secure boot and Arm TrustZone technology
- SD, eMMC, 2 x DUART, 8 x I2C, 2 x USB3.0, 2 x CAN (FD optional)

TARGET APPLICATIONS

The LX2160A addresses traditional networking control and data plane, data center offload, 5G, industrial, and autonomous driving applications.

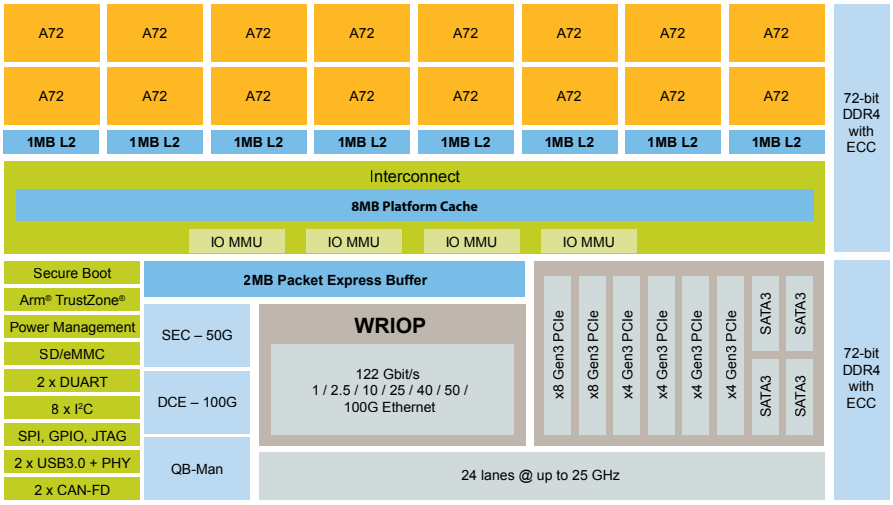


Application	Examples	Relevant Features
Autonomous driving	• L2 - L4 compute engine • Sensor data management • Central connectivity hub	• AEC Q100 Grade 3 to 105 °C • Product longevity to 2035 • < 10 FIT reliability • CAN Flexible Datarate
White box switching	• Control plane for L2 switches in TOR and EOR applications • Host VMs on the switch	• 50 Gbit/s IPsec offload • Datacenter-friendly 25 GE ports
Data center offload	• 2x 25 Gbps Network Interface Card • Control plane on FPGA-based NIC	• PCIe x8 Gen3 with SR-IOV • Low power due to FinFET process technology • Data-center friendly 25 Gbit Ethernet ports
5G packet processing	• C-RAN • Macro base station • O-RAN Central Unit • O-RAN Distributed Unit and Radio Units in conjunction with NXP LA1200 baseband processor.	• PDCP, transport, MAC/RLC software • 30 Gbit/s IPsec elephant flow • 50 Gbit/s LTE Air crypto • Hardware QoS • Reference design with LA1200 baseband processor

RELATED SOFTWARE

- **Linux® SDK for Layerscape Processors**
- **CodeWarrior® Embedded Software Development Tools for Armv8 64-bit based Layerscape Series Processors**

LAYERSCAPE LX2160A BLOCK DIAGRAM



LAYERSCAPE LX2 FAMILY MEMBERS

	LX2160A	LX2120A	LX2080A
Cores	16	12	8
L2 cache	8 MB	6 MB	8 MB
SerDes	24 at up to 25 GHz		
PCIe	6 x Gen3		
DDR	2 x DDR4, 3200 MT/s, 256 GB capacity		
Plat cache + PEB	10 MB		
WRIOP	122 Gbit/s L2 switch, supporting combinations of 16 ports of 1, 2.5, 10, 25, 40, 50 and 100 Gbit Ethernet		
SEC	50 Gbit/s		
DCE	100 Gbit/s		
Package	40 x 40 mm, 1517 pins		

www.nxp.com/LX2160A

Document Number: LX2160AFS REV 2
Date of Release: January 2022