ADS816x 8-Channel, 16-Bit, 1-MSPS, SAR ADC With Direct Sensor Interface

1 Features

- Compact low-power data acquisition system:
  - MUX breakout enables single external driver amplifier
  - 16-bit SAR ADC
  - Low-drift integrated reference and buffer
  - 0.5 × V_{REF} output for analog input DC biasing
- Excellent AC and DC performance:
  - SNR: 92 dB, THD: –110 dB
  - INL: ±0.3 LSB, 16-bit no missing codes
- Multiplexer with channel sequencer:
  - Multiple channel-sequencing options:
    - Manual mode, on-the-fly mode, auto sequence mode, custom channel sequencing
  - Early switching enables direct sensor interface
  - Fast response time with on-the-fly mode
- System monitoring features:
  - Per channel programmable window comparator
  - False trigger avoidance with programmable hysteresis
- Enhanced-SPI digital interface:
  - 1-MSPS throughput with 16-MHz SCLK
  - High-speed, 70-MHz digital interface
- Wide operating range:
  - External V_{REF} input range: 2.5 V to 5 V
  - AVDD from 3 V to 5.5 V
  - DVDD from 1.65 V to 5.5 V
  - –40°C to +125°C temperature range

2 Applications

- Analog input modules
- Multiparameter patient monitors
- Anesthesia delivery systems
- LCD tests
- Intra-DC interconnect (metro)
- Optical modules

3 Description

The ADS816x is a family of 16-bit, 8-channel, high-precision successive approximation register (SAR) analog-to-digital converters (ADCs) operating from a single 5-V supply with a 1-MSPS (ADS8168), 500-kSPS (ADS8167), and 250-kSPS (ADS8166) total throughput.

The input multiplexer supports extended settling time, which makes driving the analog inputs easier. The output of the multiplexer and ADC analog inputs are available as device pins. This configuration allows one ADC driver op amp to be used for all eight analog inputs of the multiplexer.

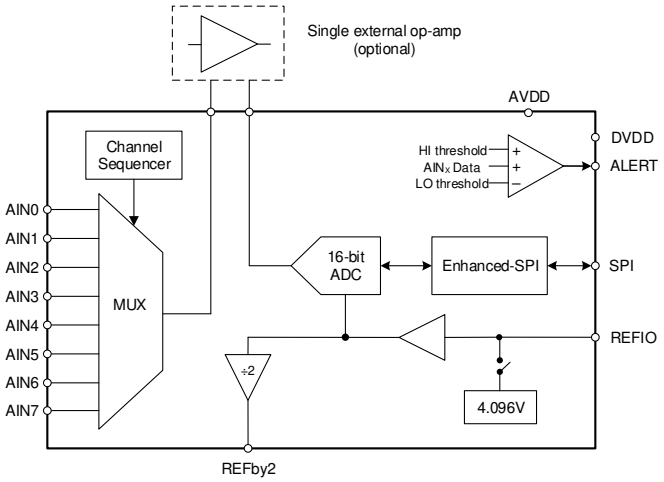
The ADS816x features a digital window comparator with programmable high and low alarm thresholds per analog input channel. The single op-amp solution with programmable alarm thresholds enables low power, low cost, and smallest form-factor applications.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS816x	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

ADS816x Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2018) to Revision C **Page**

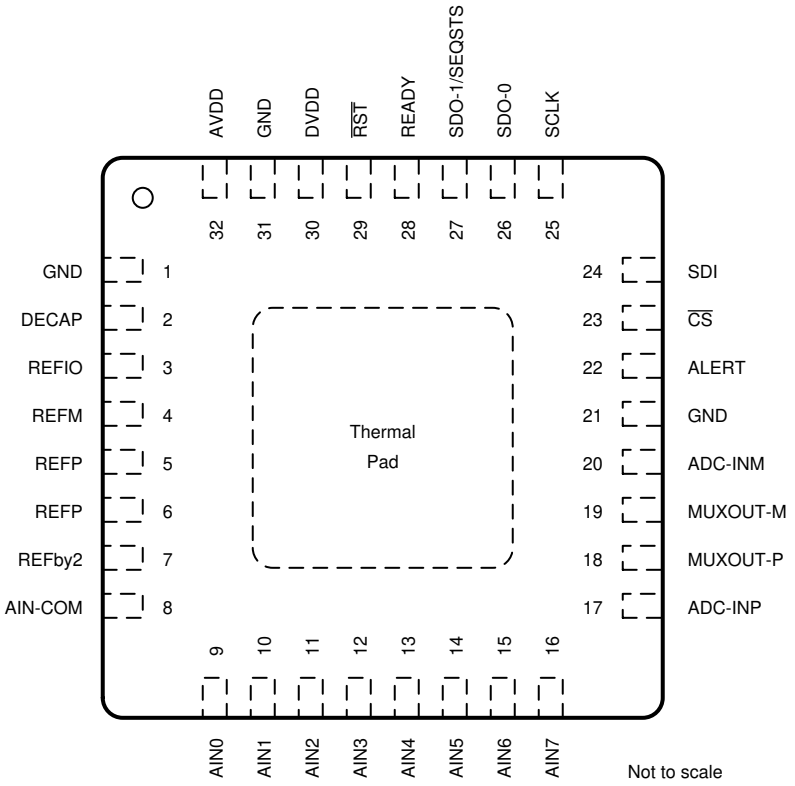
- Changed document title from *ADS816x 8-Channel, 16-Bit, 1-MSPS, SAR ADC With Easy-to-Drive Analog Inputs* to *ADS816x 8-Channel, 16-Bit, 1-MSPS, SAR ADC With Direct Sensor Interface* ... 1
- Changed *Low-leakage multiplexer with sequencer* to *Multiplexer with channel sequencer* in *Features* section ... 1
- Changed *Wide input range* to *Wide operating range* in *Features* section, changed and added sub-bullets to this Features bullet ... 1
- Deleted hysteresis from alarm threshold discussion in *Description* section ... 1
- Changed title of *ADS816x Block Diagram* figure ... 1
- Changed *AUTO_SEQ_CFG1 = 0x84* to *AUTO_SEQ_CFG1 = 0x44* in *Auto Sequence Mode* section ... 34
- Changed default settings from 1 to 0xFF in *Channel Sample Count* column of *Custom Channel Sequencing Configuration Space* table ... 36
- Changed reset value from *R/W-0000 0001b* to *R/W-1111 1111b* in *REPEAT_INDEX_m Registers* section ... 60
- Changed description of registers 78h, 7Ah, 7Ch, and 7Eh in *Digital Window Comparator Configuration Registers Mapping* table ... 61
- Changed *ALERT_LO_STATUS Register* section and name ... 66
- Changed *ALERT_STATUS Register* section and name ... 68
- Changed *CURR_ALERT_LO_STATUS Register* section and name ... 69
- Changed *CURR_ALERT_STATUS Register* section and name ... 71

Changes from Revision A (July 2018) to Revision B **Page**

- Changed document status from Advanced Information to Production Data ... 1

5 Pin Configuration and Functions

RHB Package
32-Pin VQFN
Top View



Pin Functions

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
ADC-INM	20	Analog input	Negative ADC analog input
ADC-INP	17	Analog input	Positive ADC analog input
AIN0	9	Analog input	Analog input channel 0
AIN1	10	Analog input	Analog input channel 1
AIN2	11	Analog input	Analog input channel 2
AIN3	12	Analog input	Analog input channel 3
AIN4	13	Analog input	Analog input channel 4
AIN5	14	Analog input	Analog input channel 5
AIN6	15	Analog input	Analog input channel 6
AIN7	16	Analog input	Analog input channel 7
AIN-COM	8	Analog input	Common analog input
ALERT	22	Digital output	Digital ALERT output; active high. This pin is the output of the logical OR of the enabled channel ALERTs.
AVDD	32	Power supply	Analog power-supply pin. Connect a 1-µF capacitor from this pin to GND.
$\overline{CS}$	23	Digital input	Chip-select input pin; active low. The device starts converting the active input channel on the rising edge of $\overline{CS}$. The device takes control of the data bus when $\overline{CS}$ is low. The SDO-x pins go Hi-Z when $\overline{CS}$ is high.
DECAP	2	Power supply	Connect a 1-µF capacitor to GND for the internal power supply.
DVDD	30	Power supply	Interface power-supply pin. Connect a 1-µF capacitor from this pin to GND.

Pin Functions (continued)

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
GND	1, 21, 31	Power supply	Ground
MUXOUT-M	19	Analog output	MUX negative analog output
MUXOUT-P	18	Analog output	MUX positive analog output
READY	28	Digital output	Multifunction output pin. When $\overline{CS}$ is held high, READY reflects the device conversion status. READY is low when a conversion is in process. When $\overline{CS}$ is low, the status of READY depends on the output protocol selection.
REFby2	7	Analog output	The output voltage on this pin is equal to half the voltage on the REFP pin. Connect a 1-µF capacitor from this pin to GND.
REFIO	3	Analog input/output	Reference voltage input; internal reference is a 4.096-V output. Connect a 1-µF capacitor from this pin to GND.
REFM	4	Analog input	Reference ground potential; short this pin to GND externally.
REFP	5, 6	Analog input/output	Reference buffer output, ADC reference input. Short pins 5 and 6 together.
$\overline{RST}$	29	Digital input	Asynchronous reset input pin. A low pulse on the $\overline{RST}$ pin resets the device. All register bits return to their default states.
SCLK	25	Digital input	Clock input pin for the serial interface. All system-synchronous data transfer protocols are timed with respect to the SCLK signal.
SDI	24	Digital input	Serial data input pin. This pin is used to transfer data or commands into the device.
SDO-0	26	Digital output	Serial communication pin: data output 0.
SDO-1/ SEQSTS	27	Digital output	Multifunction output pin. By default, this pin indicates the channel scanning status in the auto and custom channel sequence modes. In dual SDO data transfer mode this pin functions as a serial communication pin: data output 1.
Thermal pad		Supply	Exposed thermal pad; connect to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD to GND	–0.3	7	V
DVDD to GND	–0.3	7	V
AINx(2), AIN-COM, MUXOUT-P, MUXOUT-M, ADC-INP, ADC-INM	GND – 0.3	AVDD + 0.3	V
REFP	REFM – 0.3	AVDD + 0.3	V
REFIO	REFM – 0.3	AVDD + 0.3	V
REFM	GND – 0.1	GND + 0.1	V
Digital input pins	GND – 0.3	DVDD + 0.3	V
Digital output pins	GND – 0.3	DVDD + 0.3	V
Input current to any pin except supply pins	–10	10	mA
Junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) AINx refers to AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7 pins.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Internal reference		4.5	5	5.5	V
	External reference		3	5	5.5	
DVDD	Operating		1.65	3	5.5	V
	Specified throughput		2.35	3	5.5	
ANALOG INPUTS - SINGLE ENDED CONFIGURATION						
FSR	Full-scale input range		0		V_{REF}	V
V_{IN}	Absolute input voltage	AINx(1) to REFM and CHx_CHy_CFG(2) = 00b	–0.1		V_{REF} + 0.1	V
		AINy(3) to REFM and CHx_CHy_CFG = 01b	–0.1		0.1	
V_{IN}	Absolute input voltage	AIN-COM	–0.1		0.1	V
ANALOG INPUTS - PSEUDO-DIFFERENTIAL CONFIGURATION						
FSR	Full-scale input range		$–V_{REF}/2$		$V_{REF}/2$	V
V_{IN}	Absolute input voltage	AINx to REFM and CHx_CHy_CFG = 00b	–0.1		V_{REF} + 0.1	V
		AINy to REFM and CHx_CHy_CFG = 10b	$V_{REF}/2$ – 0.1		$V_{REF}/2$ + 0.1	
V_{IN}	Absolute input voltage	AIN-COM	$V_{REF}/2$ – 0.1		$V_{REF}/2$ + 0.1	V
EXTERNAL REFERENCE INPUT						
V_{REFIO}	REFIO input voltage	REFIO configured as input pin	2.5		AVDD – 0.3	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

(1) AINx refers to analog inputs AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.
(2) CHx_CHy_CFG bits set the analog input configuration as single-ended or pseudo-differential pair. See the AIN_CFG register for more details.
(3) AINy refers to analog inputs AIN1, AIN3, AIN5, and AIN7 when CHx_CHy_CFG = 01b or 10b. See the Multiplexer Configurations section for more details.

6.4 Thermal Information

THERMAL METRIC(1)		ADS816x RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, REFIO configured as output pin, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C_{SH}	ADC Input capacitance			60		pF
C_{INMUX}	MUX Input capacitance			13		pF
I_{LMUX_ON}	MUX input on-channel leakage current	REFM < V_{IN} < REFP	–750	±10	750	nA
DC PERFORMANCE						
	Resolution			16		Bits
NMC	No missing codes		16			
INL	Integral nonlinearity		–0.8	±0.35	0.8	LSB
DNL	Differential nonlinearity		–0.5	±0.2	0.5	LSB
V_{OS}	Input offset error		–10	±0.5	10	LSB
	Input offset error match		–1	±0.5	1	LSB
dV_{OS}/dT	Input offset thermal drift			0.25		µV/°C
G_E	Gain error	Referred to REFIO	–0.06	±0.002	0.06	%FSR
	Gain error match	Referred to REFIO	–0.005	±0.0025	0.005	%FSR
dG_E/dT	Gain error thermal drift	Referred to REFIO		±1		ppm/°C
TNS	Transition noise	V_{IN} = V_{REF}/2		0.6		LSB
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion	f_{IN} = 2 kHz	91.6	93.5		dB
SNR	Signal-to-noise-ratio	f_{IN} = 2 kHz	91.8	93.6		dB
THD	Total harmonic distortion	f_{IN} = 2 kHz		-110		dB
SFDR	Spurious-free dynamic range	f_{IN} = 2 kHz		112		dB
	Isolation crosstalk	f_{IN} = 100 kHz		-115		dB
REFERENCE BUFFER						
V_{RO}	Reference buffer offset voltage	V_{RO} = V_{REFP} - V_{REFIO}, T_A = 25°C	–250		250	µV
C_{REFP}	Decoupling capacitor on REFP			22		µF
R_{ESR}	External series resistance		0		1.3	Ω
REFby2 BUFFER						
V_{REFby2}	REFby2 output voltage			V_{REFP}/2		V
I_{REFby2}	DC Sourcing current from REFby2				2	mA
C_{REFby2}	Decoupling capacitor on REFby2		1			µF
INTERNAL REFERENCE OUTPUT						
V_{REFIO}	REFIO output voltage(1)	T_A = 25°C, REFIO configured as output pin	4.091	4.096	4.101	V
dV_{REFIO}/dT	Internal reference temperature drift			4	18	ppm/°C
C_{REFIO}	Decoupling capacitor on REFIO	REFIO configured as output	1			µF
EXTERNAL REFERENCE INPUT						
I_{REFIO}	REFIO input current	REFIO configured as input pin		0.1	1	µA
C_{REF}	Internal capacitance on REFIO pin	REFIO configured as input pin		10		pF
SAMPLING DYNAMICS						
	Aperture delay			4		ns
$t_{j\text{-}RMS}$	Aperture jitter			2		ps RMS

(1) Does not include the variation in voltage resulting from solder effects.

Electrical Characteristics (continued)

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, REFIO configured as output pin, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{-3\text{-dB(small)}}$	Small-signal bandwidth	Measured at ADC inputs		23		MHz
POWER SUPPLY CURRENTS						
I_{AVDD}	Analog supply current	ADS8168, AVDD = 5 V		5.3	6.4	mA
		ADS8167, AVDD = 5 V		3.9	5	
		ADS8166, AVDD = 5 V		3	4.1	
		Static, no conversion		2.3		
		Static, PD_REFBUF = 1		1.6		
		Static, PD_REF = 1		800		µA
		Static, PD_REFBUF, PD_REF and PD_REFby2 = 1		180		µA
I_{DVDD}	Digital supply current	DVDD = 3 V, C_{LOAD} = 10 pF, no conversion		0.45		µA

6.6 Timing Requirements

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

			MIN	NOM	MAX	UNIT
CONVERSION CYCLE						
f_{CYCLE}	Sampling frequency	ADS8168			1000	kHz
		ADS8167			500	
		ADS8166			250	
t_{CYCLE}	ADC cycle-time period	ADS8168	1			µs
		ADS8167	2			
		ADS8166	4			
t_{wh_CSZ}	Pulse duration: $\overline{CS}$ high		30			ns
t_{wl_CSZ}	Pulse duration: $\overline{CS}$ low		30			ns
t_{ACQ}	Acquisition time		300			ns
t_{qt_ACQ}	Quite acquisition time		30			ns
t_{d_CNVCAP}	Quiet aperture time		20			ns
ASYNCHRONOUS RESET AND LOW POWER MODES						
t_{wl_RST}	Pulse duration: $\overline{RST}$ low		100			ns
SPI-COMPATIBLE SERIAL INTERFACE						
f_{CLK}	Serial clock frequency	2.35 V ≤ DVDD ≤ 5.5 V, V_{IH} > 0.7 DVDD, V_{IL} < 0.3 DVDD			70	MHz
		1.65 V ≤ DVDD < 2.35 V, V_{IH} ≥ 0.8 DVDD, V_{IL} ≤ 0.2 DVDD			20	
		1.65 V ≤ DVDD < 2.35 V, V_{IH} ≥ 0.9 DVDD, V_{IL} ≤ 0.1 DVDD			68	
t_{CLK}	Serial clock time period		$1/f_{CLK}$			ns
t_{ph_CK}	SCLK high time		0.45		0.55	t_{CLK}
t_{pl_CK}	SCLK low time		0.45		0.55	t_{CLK}
t_{ph_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK capture edge		15			ns
t_{su_CKDI}	Setup time: SDI data valid to the SCLK capture edge		3			ns
t_{ht_CKDI}	Hold time: SCLK capture edge to (previous) data valid on SDI		4			ns
t_{ht_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising		7.5			ns
SOURCE-SYNCHRONOUS SERIAL INTERFACE						
f_{CLK}	Serial clock frequency	2.35 V ≤ DVDD ≤ 5.5 V, SDR (DATA_RATE = 0b)			70	MHz
		2.35 V ≤ DVDD ≤ 5.5 V, DDR (DATA_RATE = 1b)			35	
t_{CLK}	Serial clock time period		$1/f_{CLK}$			ns

6.7 Switching Characteristics

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A= 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONVERSION CYCLE						
t_{CONV}	Conversion time	ADS8168			660	ns
		ADS8167			1200	
		ADS8166			2500	
ASYNCHRONOUS RESET, AND LOW POWER MODES						
t_{d_RST}	Delay time: $\overline{RST}$ rising to READY rising				4	ms
t_{PU_ADC}	Power-up time for converter module	Change PD_ADC = 1b to 0b	1			ms
t_{PU_REFIO}	Power-up time for internal reference	Change PD_REF = 1b to 0b	5			ms
t_{PU_REFBUF}	Power-up time for internal reference buffer	Change PD_REFBUF = 1b to 0b	10			ms
t_{PU_Device}	Power-up time for device		10			ms
SPI-COMPATIBLE SERIAL INTERFACE						
t_{den_CSDO}	Delay time: $\overline{CS}$ falling to data enable				15	ns
t_{dz_CSDO}	Delay time: $\overline{CS}$ rising to SDO going to Hi-Z				15	ns
t_{d_CKDO}	Delay time: SCLK launch edge to (next) data valid on SDO				19	ns
$t_{d\_CSRDY\_t}$	Delay time: $\overline{CS}$ falling to READY falling				15	ns
SOURCE-SYNCHRONOUS SERIAL INTERFACE (External Clock)						
$t_{d\_CKSTR\_r}$	Delay time: SCLK launch edge to READY rising				23	ns
$t_{d\_CKSTR\_f}$	Delay time: SCLK launch edge to READY falling				23	ns
$t_{off\_STRDO\_f}$	Time offset: READY falling to (next) data valid on SDO		–2		2	ns
$t_{off\_STRDO\_r}$	Time offset: READY rising to (next) data valid on SDO		–2		2	ns
t_{ph_STR}	Strobe output high time	2.35 V ≤ DVDD ≤ 5.5 V	0.45		0.55	t_{STR}
t_{pl_STR}	Strobe output low time	2.35 V ≤ DVDD ≤ 5.5 V	0.45		0.55	t_{STR}

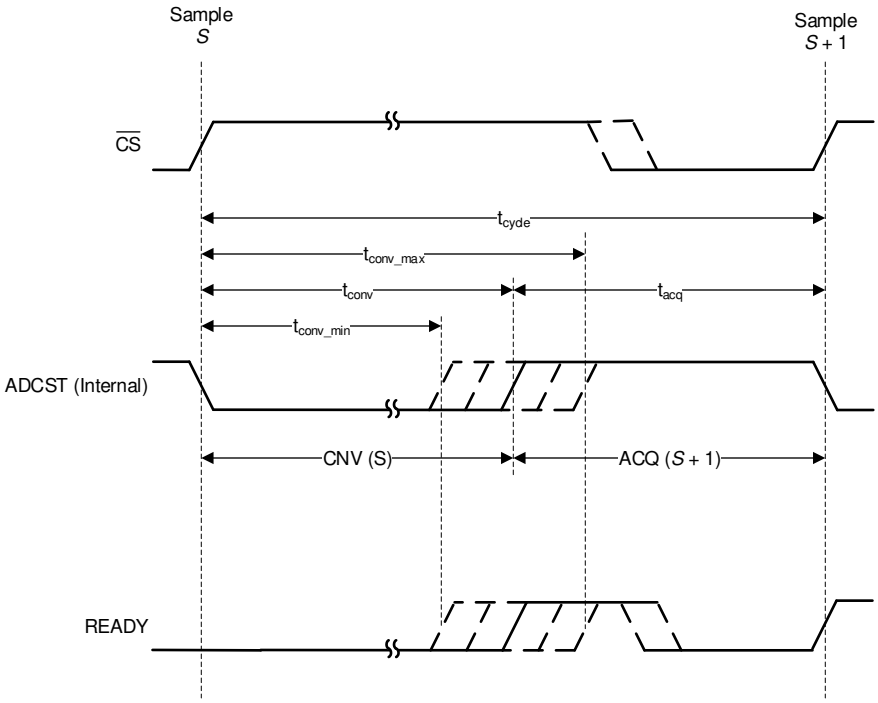


Figure 1. Conversion Cycle Timing

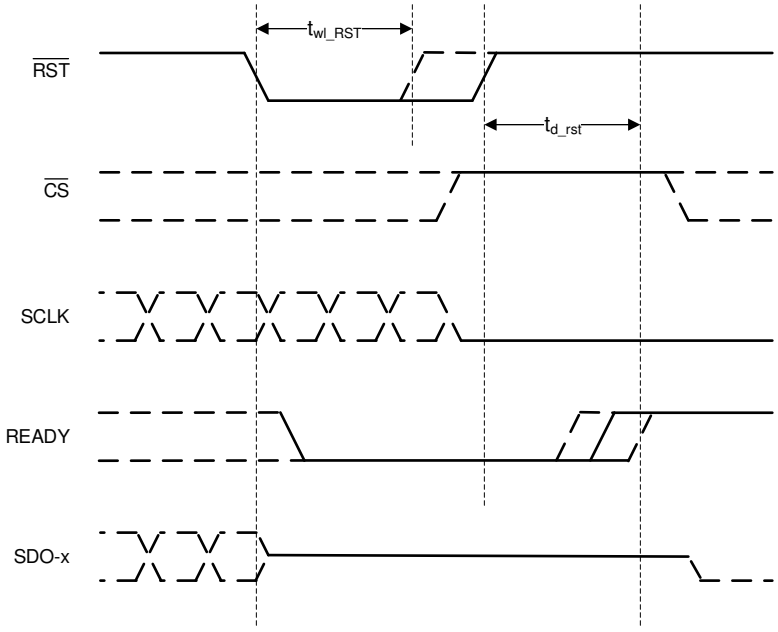
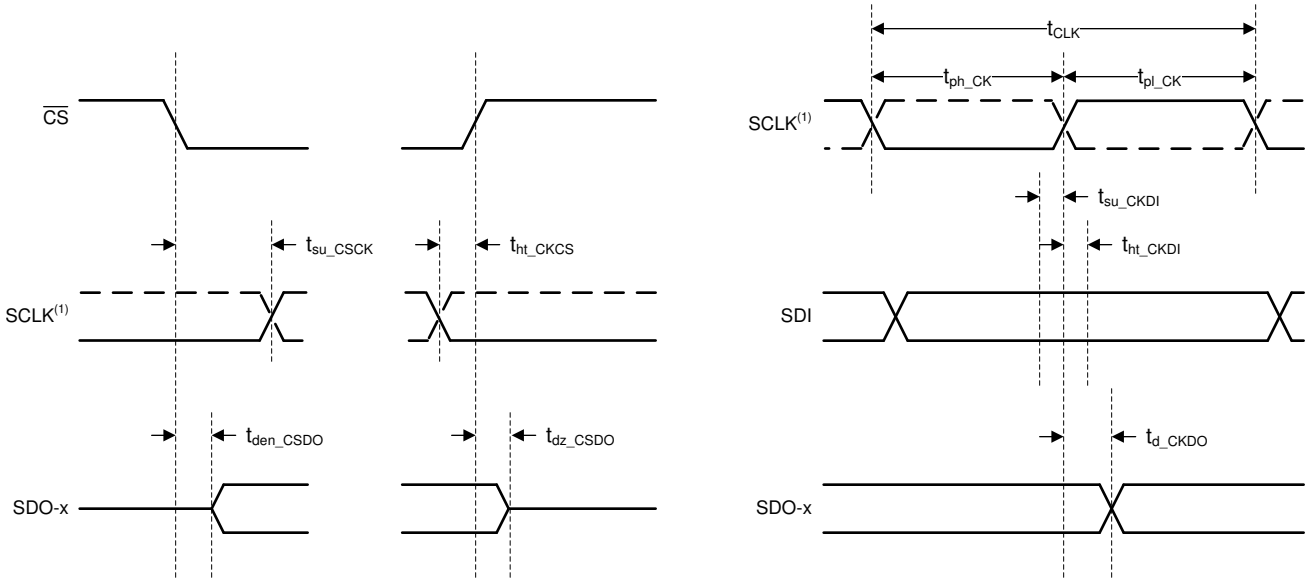


Figure 2. Asynchronous Reset Timing



(1) The SCLK polarity, launch edge, and capture edge depend on the SPI protocol selected.

Figure 3. SPI-Compatible Serial Interface Timing

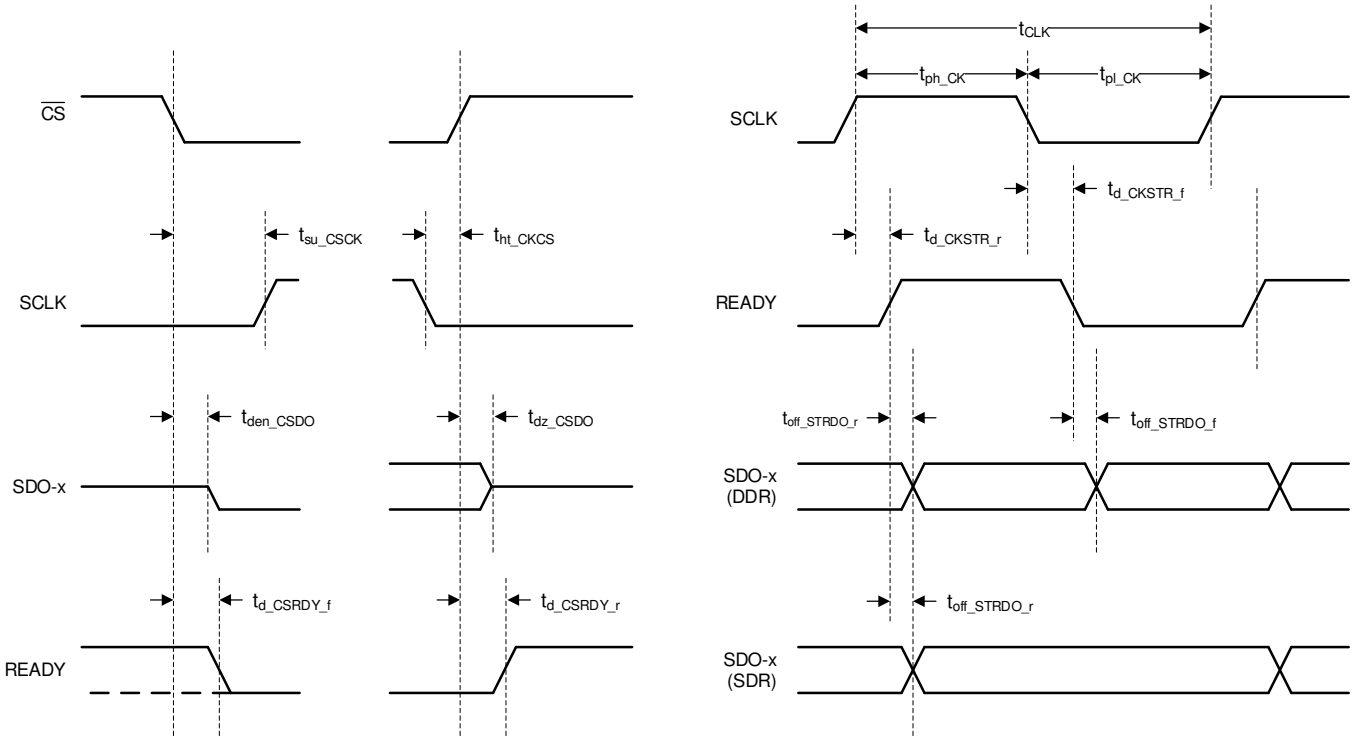


Figure 4. Source-Synchronous Serial Interface Timing

6.8 Typical Characteristics

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, REFIO configured as output pin, and maximum throughput (unless otherwise noted)

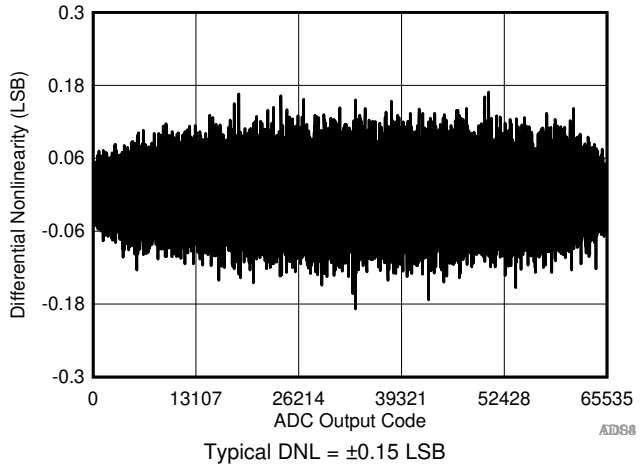


Figure 5. Typical DNL

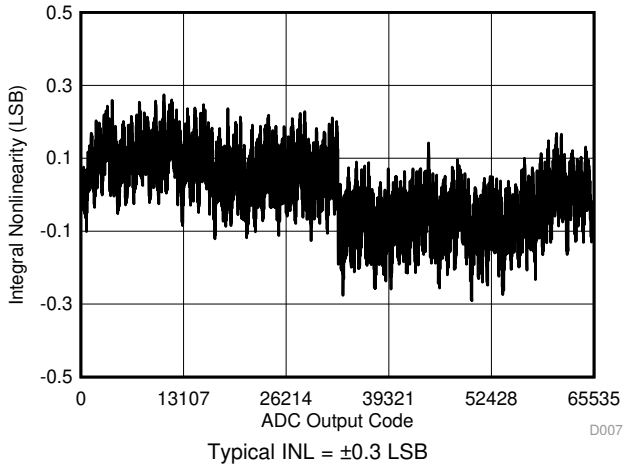


Figure 6. Typical INL

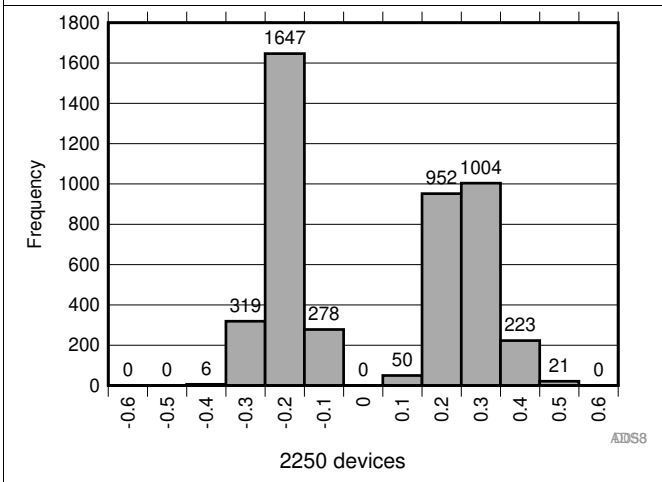


Figure 7. Typical INL Distribution (LSB)

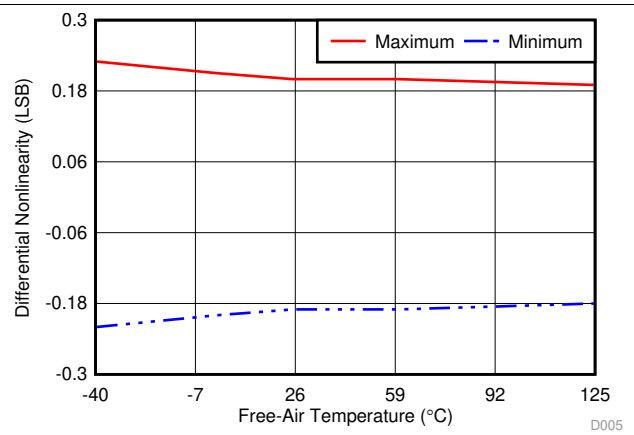


Figure 8. DNL vs Temperature

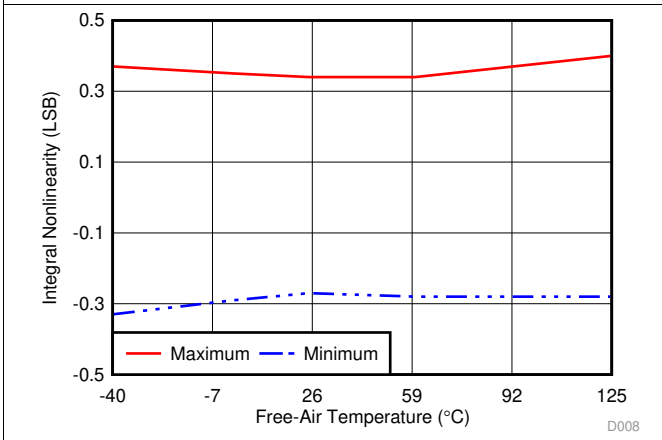


Figure 9. INL vs Temperature

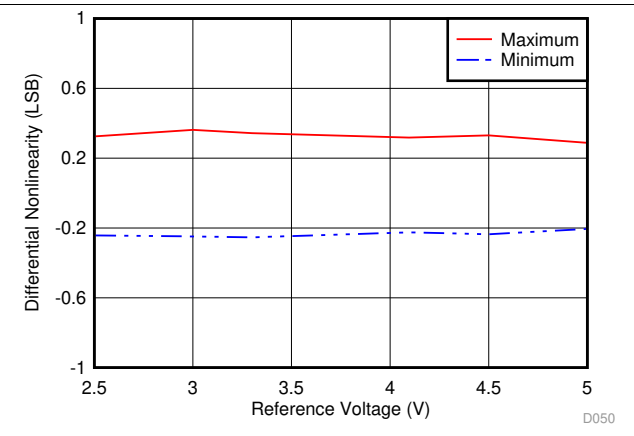


Figure 10. DNL vs Reference Voltage

Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, REFIO configured as output pin, and maximum throughput (unless otherwise noted)

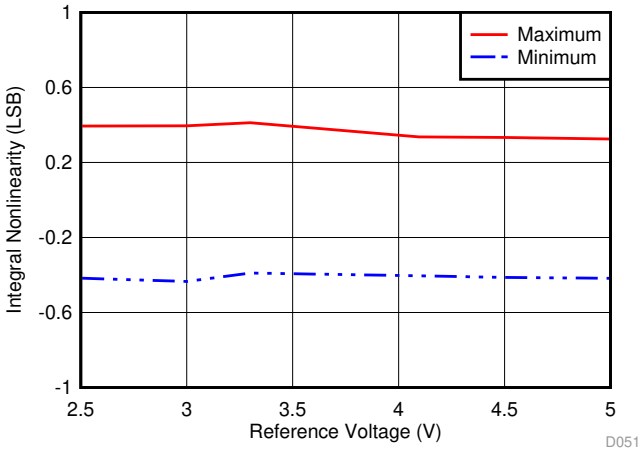


Figure 11. INL vs Reference Voltage

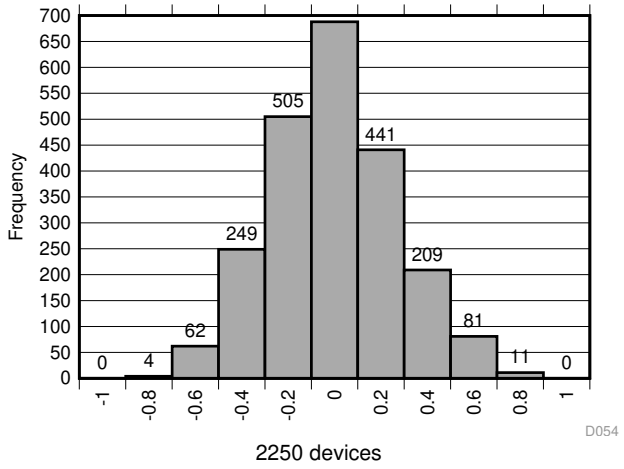


Figure 12. Typical Offset Distribution (LSB)

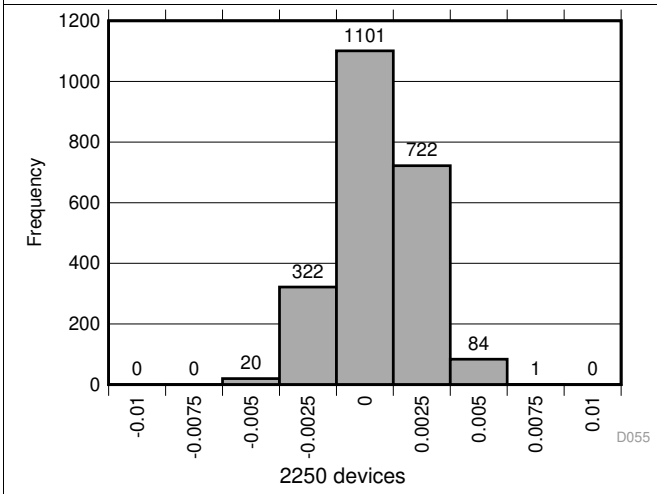


Figure 13. Typical Gain Error Distribution (%FSR)

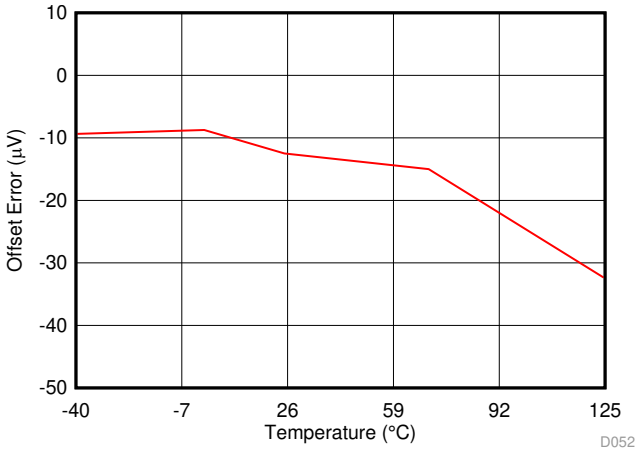


Figure 14. Offset Error vs Temperature

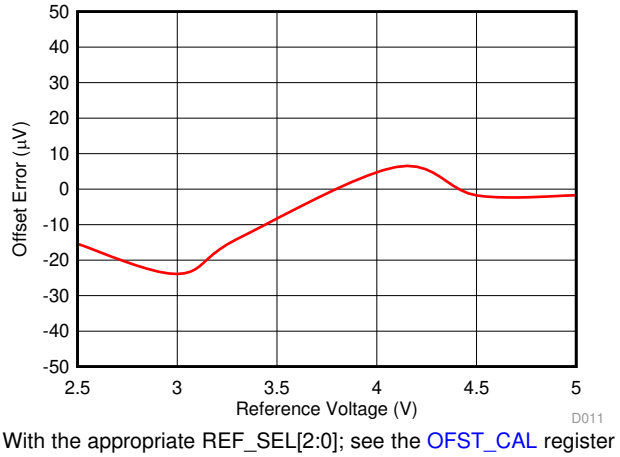


Figure 15. Offset Error vs Reference Voltage

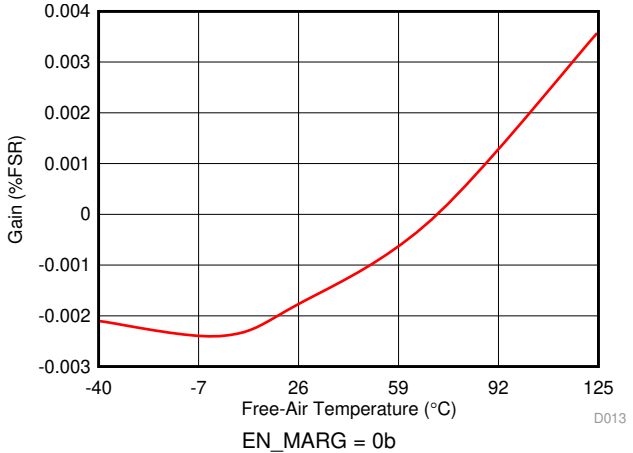


Figure 16. Gain Error (ADC + REFBUF) vs Temperature

Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, REFIO configured as output pin, and maximum throughput (unless otherwise noted)

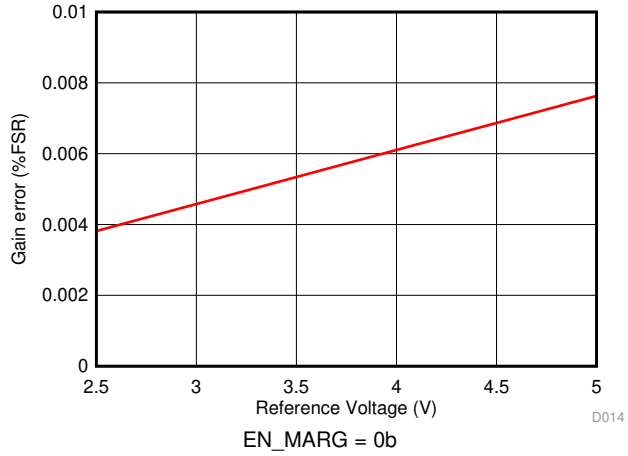


Figure 17. Gain Error (ADC + REFBUF) vs Reference Voltage

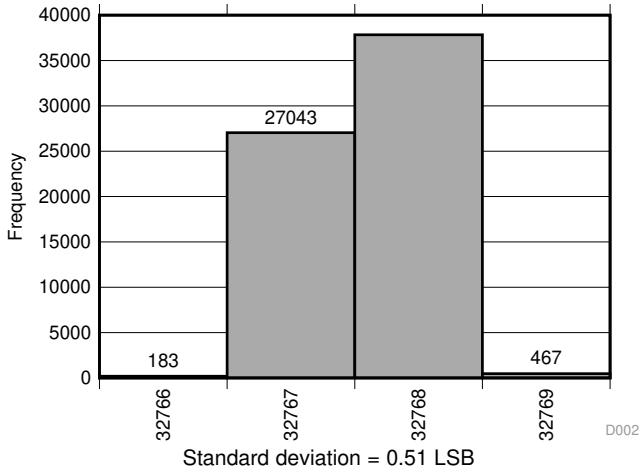


Figure 18. DC Input Histogram

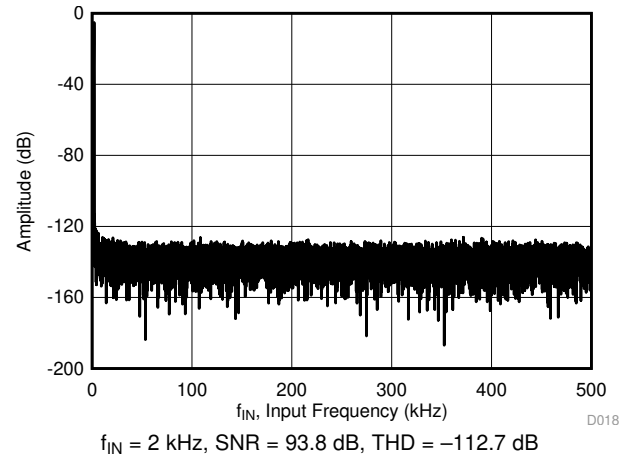


Figure 19. Typical FFT, ADS8168

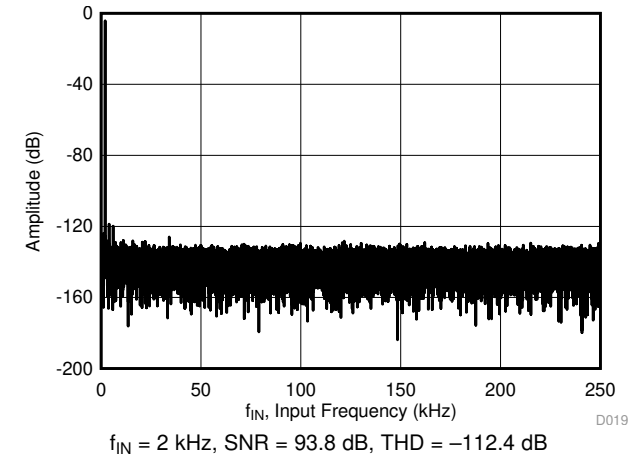


Figure 20. Typical FFT, ADS8167

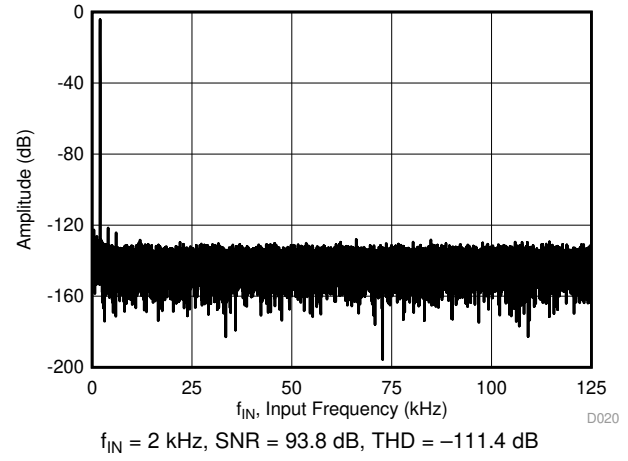


Figure 21. Typical FFT, ADS8166

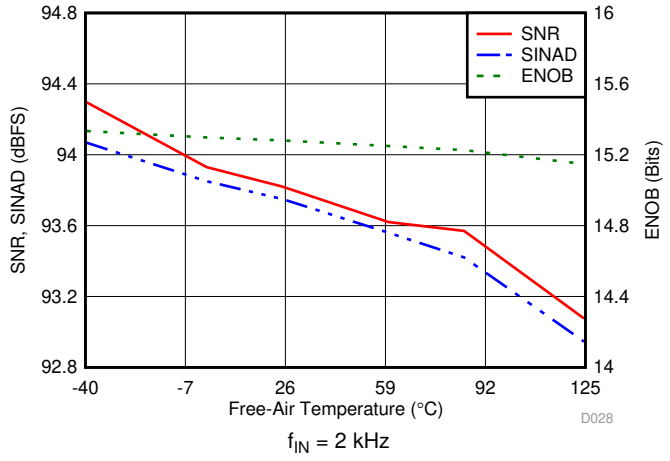


Figure 22. Noise Performance vs Temperature

Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, REFIO configured as output pin, and maximum throughput (unless otherwise noted)

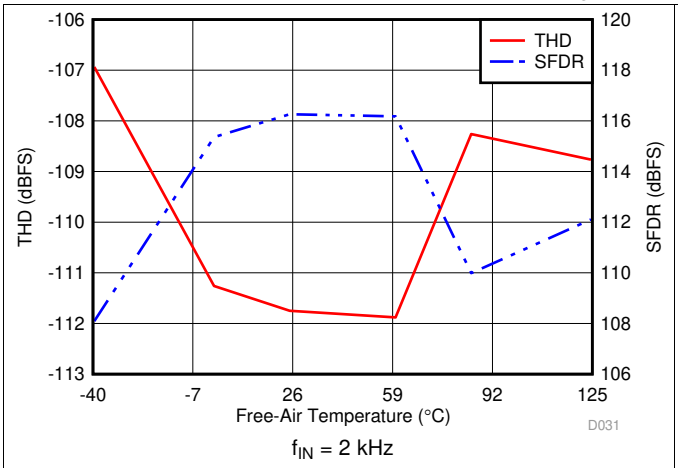


Figure 23. Distortion Performance vs Temperature

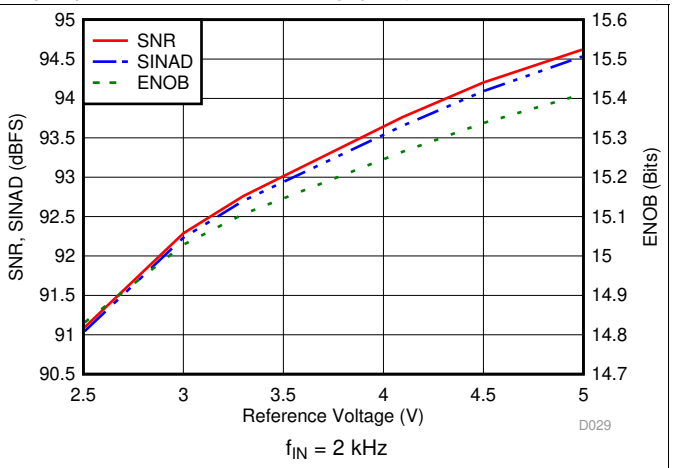


Figure 24. Noise Performance vs Reference Voltage

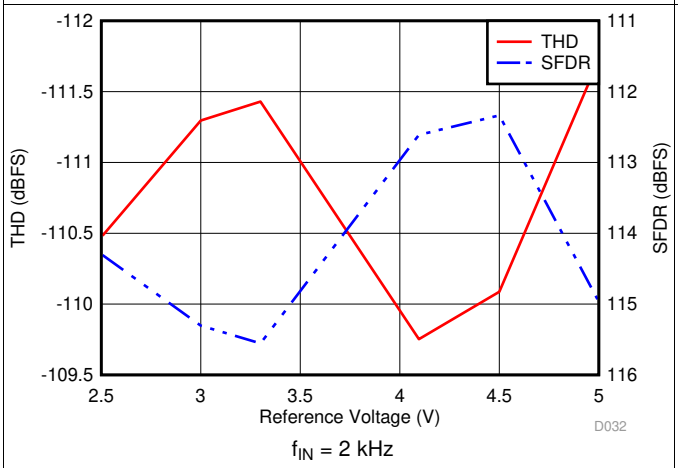


Figure 25. Distortion Performance vs Reference Voltage

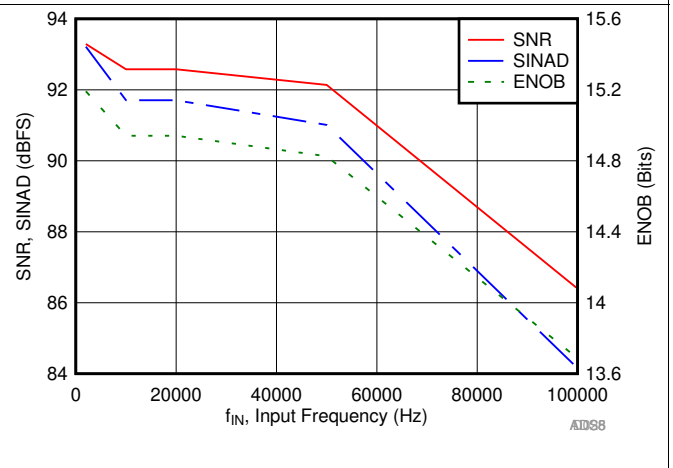


Figure 26. Noise Performance vs Input Frequency

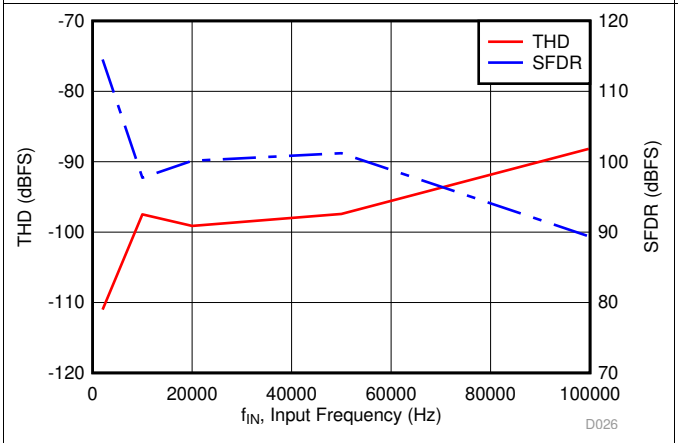


Figure 27. Distortion Performance vs Input Frequency

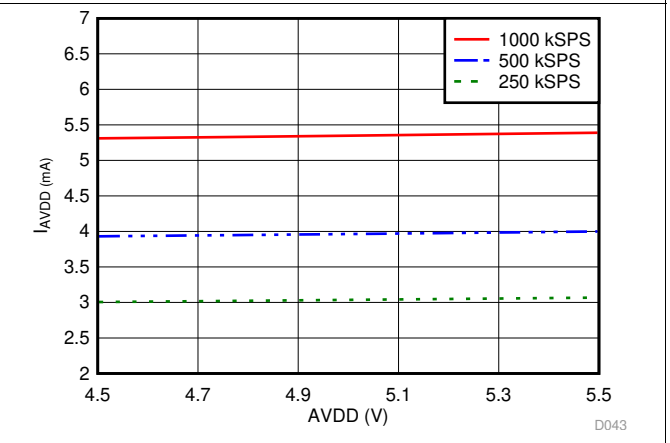


Figure 28. Analog Supply Current vs Supply Voltage

Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, REFIO configured as output pin, and maximum throughput (unless otherwise noted)

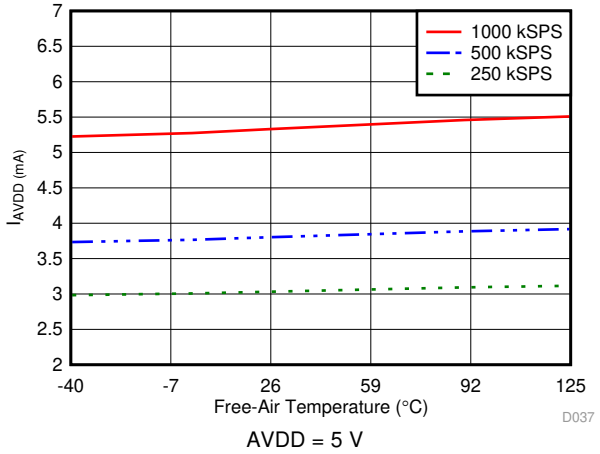


Figure 29. Analog Supply Current vs Temperature

7 Detailed Description

7.1 Overview

The ADS816x is a 16-bit, successive approximation register (SAR) analog-to-digital converter (ADC) with an analog multiplexer. This device integrates a reference, reference buffer, REFby2 buffer, low-dropout regulator (LDO), and features high performance at full throughput and low power consumption.

The ADS816x supports unipolar, single-ended and pseudo-differential analog input signals. The analog multiplexer is optimized for low distortion and extended settling time. The internal reference generates a low-drift, 4.096-V reference output. The integrated reference buffer supports burst mode for data acquisition of external reference voltages in the range 2.5 V to 5 V. For DC level shifting of the analog input signals, the device has a REFby2 output. The REFby2 output is derived from the output of the integrated reference buffer (the REFP pin).

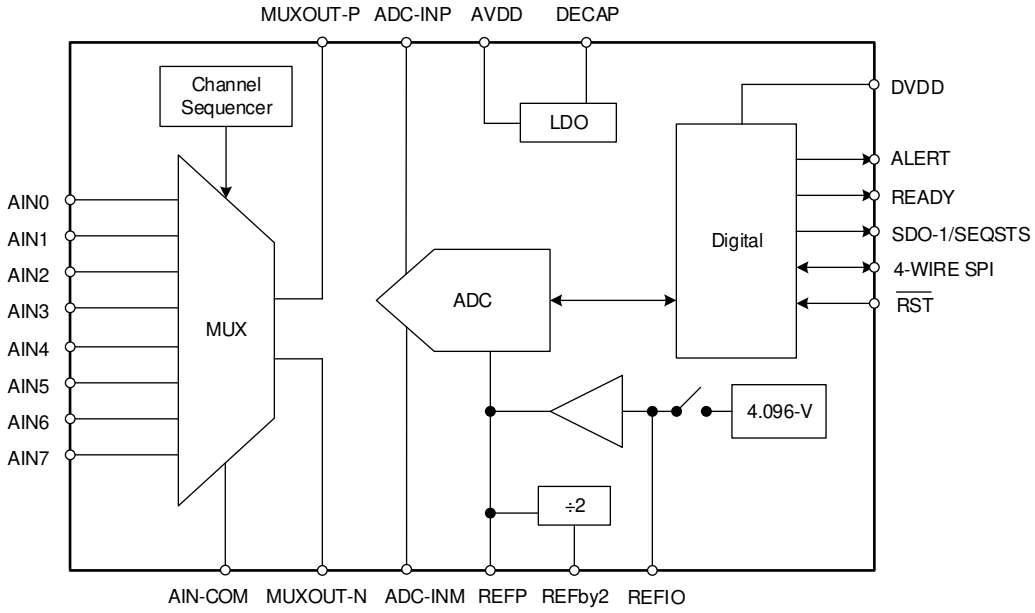
When a conversion is initiated, the differential input between the ADC-INP and ADC-INM pins is sampled on the internal capacitor array. The device uses an internal clock to perform conversions. During the conversion process, both analog inputs of the ADC are disconnected from the internal circuit. At the end of conversion process, the device reconnects the sampling capacitors to the ADC-INP and ADC-INM pins and enters an acquisition phase.

The integrated LDO allows the device to operate on a single supply, AVDD. The device consumes only 26.5 mW, 19.5 mW, and 15 mW of power when operating at 1 MSPS (ADS8168), 500 kSPS (ADS8167), and 250 kSPS (ADS8166), respectively, with the internal reference, reference buffer, REFby2 buffer, and LDO enabled.

The enhanced-SPI digital interface is backward-compatible with traditional SPI protocols. Configurable features boost analog performance and simplify board layout, timing, firmware, and support full throughput at lower clock speeds. These features enable a variety of microcontrollers, digital signal processors (DSPs), and field-programmable gate arrays (FPGAs) to be used.

The ADS816x enables optical line cards, test and measurement, medical, and industrial applications to achieve fast, low-noise, low-distortion, and low-power data acquisition in a small form-factor.

7.2 Functional Block Diagram



7.3 Feature Description

The ADS816x is comprised of five modules: the converter (SAR ADC), multiplexer (MUX), the reference module, the enhanced-SPI interface, and the low-dropout regulator (LDO); see the *Functional Block Diagram* section.

The LDO module is powered by the AVDD supply, and generates the bias voltage for the internal circuit blocks of the device. The reference buffer drives the capacitive switching load present at the reference pins during the conversion process. The multiplexer selects among eight analog input channels as the input for the converter module. The converter module samples and converts the analog input into an equivalent digital output code. The enhanced-SPI interface module facilitates communication and data transfer between the device and the host controller.

7.3.1 Analog Multiplexer

Figure 30 shows the small-signal equivalent circuit of the sample-and-hold circuit. Each sampling switch is represented by resistance (R_{S1} and R_{S2}, typically 50 Ω) in series with an ideal switch (SW). The sampling capacitors, C_{S1} and C_{S2}, are typically 60 pF.

The multiplexer on-resistance (R_{MUX}), is typically a 40-Ω resistor in series between the ON channel and the MUXOUT-P or MUXOUT-M pins. The multiplexer analog input typically has a 13-pF on-channel capacitance (C_{MUX}).

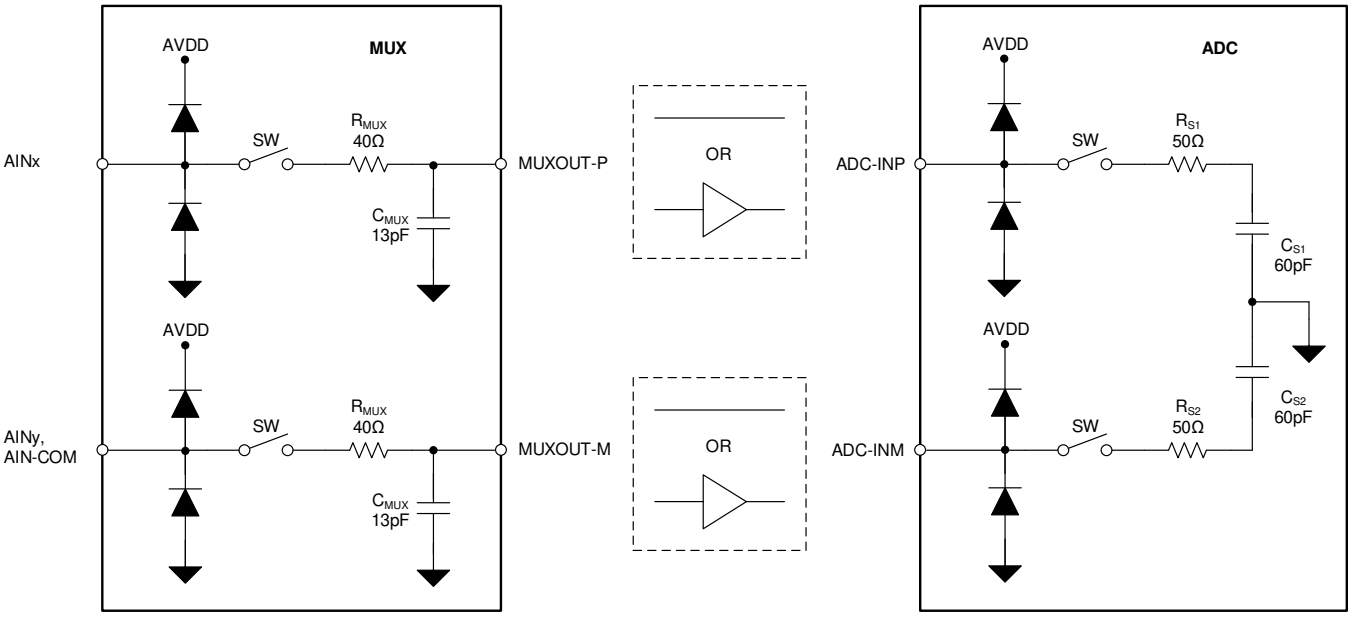


Figure 30. Input Sampling Stage Equivalent Circuit

During the input signal acquisition phase, the ADC-INP and ADC-INM inputs are individually sampled on C_{S1} and C_{S2}, respectively. During the conversion process, the device converts for the voltage difference between the two sampled values: $V_{ADC-INP} - V_{ADC-INM}$.

Each analog input pin has electrostatic discharge (ESD) protection diodes to AVDD and GND. Keep the analog inputs within the specified range to avoid turning the diodes on.

Feature Description (continued)

7.3.1.1 Multiplexer Configurations

The ADS816x supports single-ended and pseudo-differential analog input signals. The flexible analog input channel configuration supports interfacing various types of sensors. Figure 31 shows how the analog inputs can be configured.

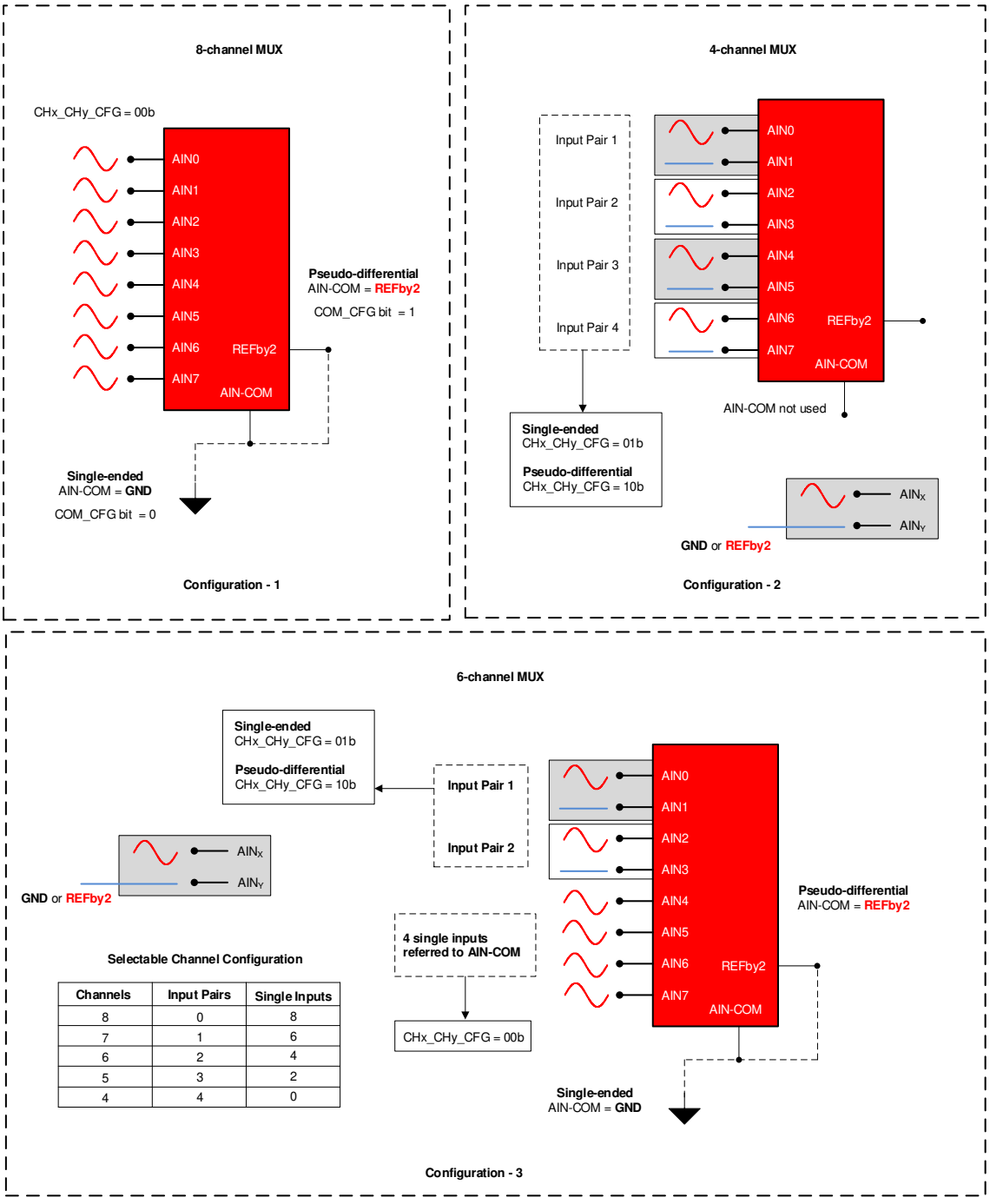


Figure 31. Analog Input Configurations

Feature Description (continued)

The analog inputs can be configured as:

- **Configuration 1**: Eight-channel MUX with the AIN_CFG register set to 00h. The AIN-COM input range is decided by the COM_CFG register.
  - Single-ended inputs with the AIN-COM input set to GND (set the COM_CFG register to 00h).
  - Pseudo-differential inputs with the AIN-COM input set to V_{REF} / 2 (set the COM_CFG register to 01h).
- **Configuration 2**: Four-channel MUX.
  - As shown in Table 1, the AIN_CFG register selects the analog input range of individual pairs.
- **Configuration 3**: Single-ended and pseudo-differential inputs.
  - Among the eight analog inputs of the MUX, some inputs can be configured as pairs and some inputs are configured as individual channels. Table 1 lists options for channel configuration.
  - For channels configured as pairs, the AIN_CFG register selects the single-ended or pseudo-differential configuration for individual pairs.
  - For individual channels, the COM_CFG register decides the single-ended or pseudo-differential configuration.

Table 1. Channel Configuration Options(1)(2)

SERIAL NUMBER	TOTAL CHANNELS	INPUT PAIRS	INDIVIDUAL CHANNELS
1	8	0	8
2	7	1	6
3	6	2	4
4	5	3	2
5	4	4	0

(1) Channel pairs can be formed as [AIN0 - AIN1], [AIN2 - AIN3], [AIN4 - AIN5], and [AIN6 - AIN7].
(2) When channels are configured as pairs, AIN0, AIN2, AIN4, and AIN6 are positive inputs.

NOTE

The COM_CFG register sets the input voltage range of the AIN-COM pin. AIN-COM pin must be connected to GND (set the COM_CFG register to 0b) or REFby2 (set the COM_CFG register to 1b) externally. When using the MUX in a four-channel configuration, the COM_CFG register has no effect; connect the AIN-COM pin to GND to avoid noise coupling.

7.3.1.2 Multiplexer With Minimum Crosstalk

For precision measurement in a multichannel system, coupling (such as crosstalk) from one channel to another can distort the measurement. In conventional multiplexers, as shown in Figure 32, the off channel parasitic capacitance between the drain and the source of the switch (C_{DSY}) couples the off channel signal to the on channel.

Figure 32 shows that the ADS816x uses a T-switch structure. In this switch architecture, the off channel parasitic capacitance is connected to ground, which significantly reduces coupling. Care must be taken to avoid signal coupling on the printed circuit board (PCB), as described in the *Layout* section.

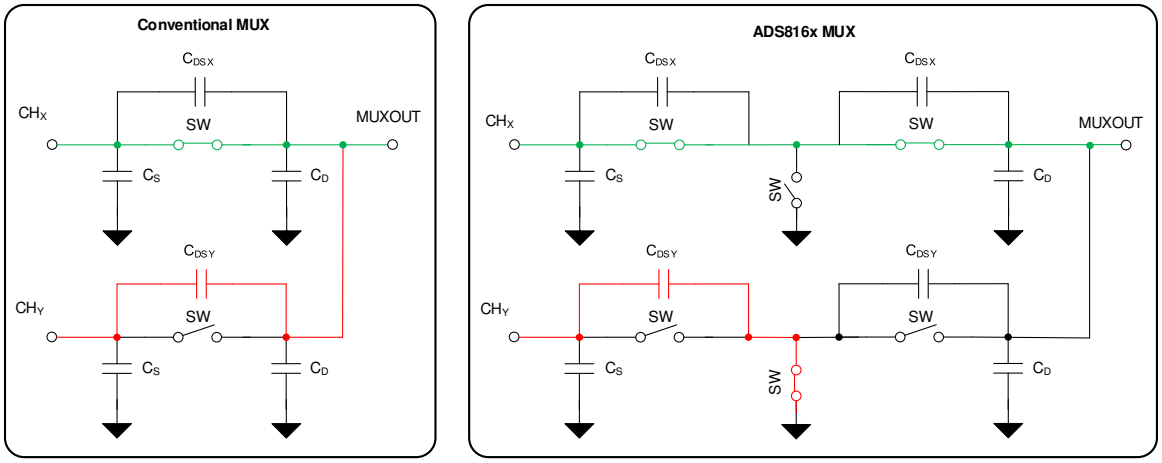


Figure 32. Isolation Crosstalk in a Conventional MUX versus the ADS816x

7.3.1.3 Early Switching for Direct Sensor Interface

Figure 33 shows the small-signal equivalent model of the ADS816x analog inputs. The multiplexer input has a switch resistance (R_{MUX}) and parasitic capacitance (C_{MUX}). The parasitic capacitance causes a charge kickback on the MUX analog input at the same time as the ADC sampling capacitor causes a charge kickback on ADC inputs.

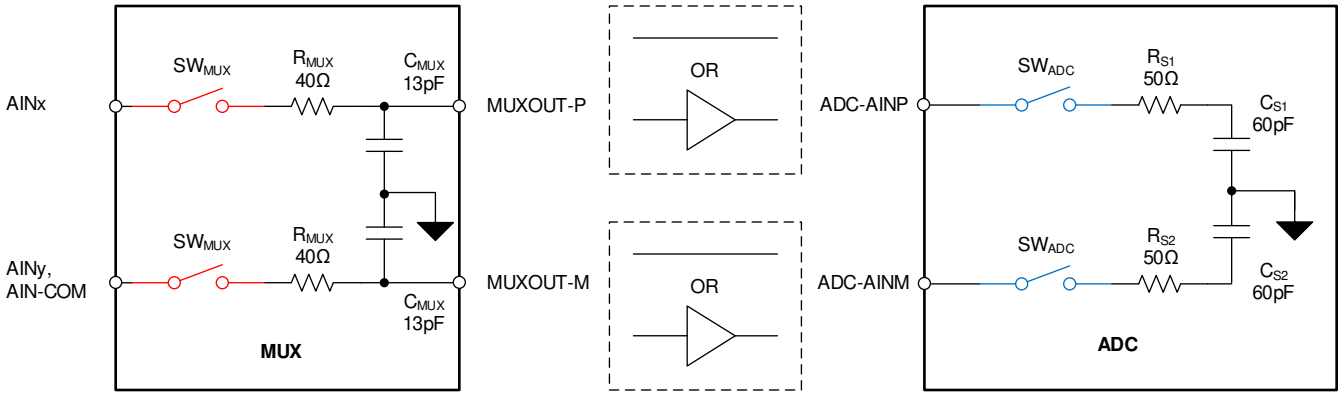


Figure 33. Synchronous and Timed Switching of the MUX and ADC Input Switches

In conventional multichannel SAR ADCs, the acquisition time of the ADC is also the settling time available at the analog inputs of the multiplexer because these times are internally connected. Thus, high-bandwidth op amps are required at the analog inputs of the multiplexer to settle the charge kickback. However, multiple high-bandwidth op amps significantly increase power dissipation, cost, and size of the solution.

The analog inputs of the ADS816x provide a long settling time (t_{CYCLE} – 100 ns), resulting in long acquisition time at the MUX inputs when using a driver amplifier between the MUX outputs and the ADC inputs. Figure 34 shows a timing diagram of this long acquisition phase. The low parasitic capacitance together with the enhanced settling time eliminate the need to use an op amp at the multiplexer input in most applications.

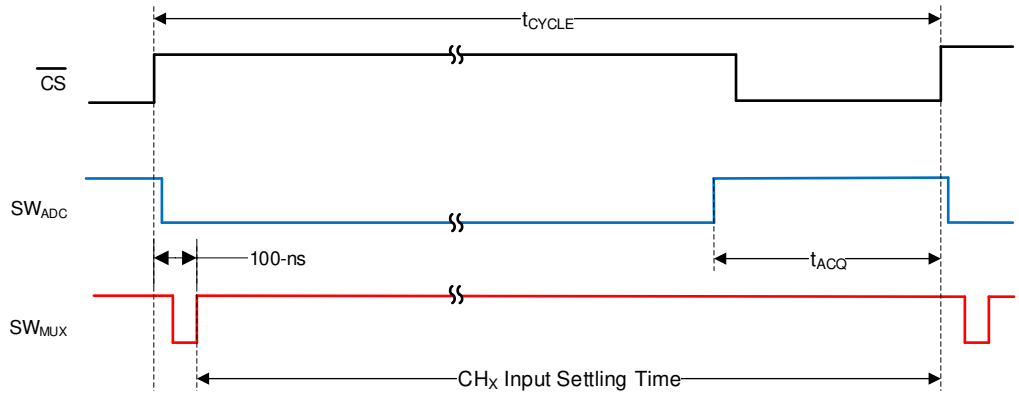


Figure 34. Early Switching of the MUX Enables a Long Acquisition Phase

Averaging several output codes of a particular MUX input channel without switching the MUX achieves better accuracy and noise performance. The output of the multiplexer does not create a charge kickback as long as SDI is set to 0 (that is, as long as SDI returns the NOP command); see Figure 43 and Figure 45. The multiplexer does not switch during subsequent conversions except for the first time when a channel is selected. Thus high-impedance sources (such as the voltage from the resistor dividers) can be connected to the analog inputs of the multiplexer without an op amp.

7.3.2 Reference

The ADS816x has a precision, low-drift reference internal to the device. See the *Internal Reference* section for details about using the internal reference.

For best SNR performance, the input signal range must be equal to the full-scale input range of the ADC. To maximize ENOB, an external reference voltage source can be used as described in the *External Reference* section.

7.3.2.1 Internal Reference

The device features an internal reference source with a nominal output value of 4.096 V. On power-up, the internal reference is enabled by default. A minimum 1-µF decoupling capacitor, as illustrated in Figure 35, is recommended to be placed between the REFIO and REFM pins. The capacitor must be placed as close to the REFIO pin as possible. The output impedance of the internal band-gap circuit creates a low-pass filter with this capacitor to band-limit the noise of the reference. The internal reference is also temperature compensated to provide excellent temperature drift over an extended industrial temperature range of –40°C to +125°C. By default the internal reference is on and the voltage at REFIO is 4.096 V. The REFIO pin has ESD protection diodes to the AVDD and GND pins.

The initial accuracy specification for the internal reference can be degraded if the die is exposed to any mechanical or thermal stress. Heating the device when being soldered to a PCB and any subsequent solder reflow is a primary cause for shifts in the internal reference voltage output. The main cause of thermal hysteresis is a change in die stress and is therefore a function of the package, die-attach material, and molding compound, as well as the layout of the device itself.

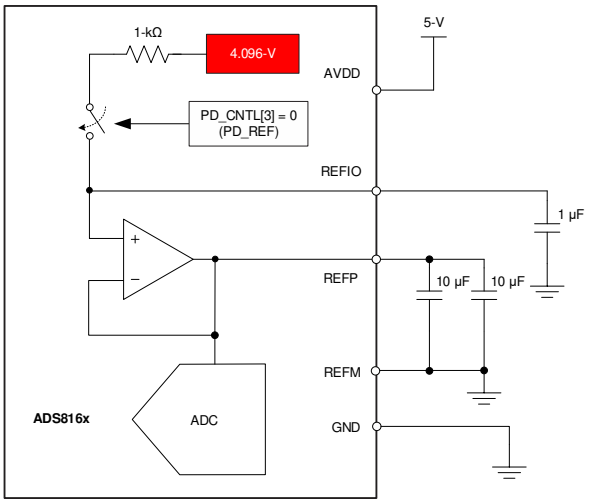


Figure 35. Device Connections for Using an Internal 4.096-V Reference

7.3.2.2 External Reference

Figure 36 shows the connections for using the device with an external reference. A reference without a low-impedance output buffer can be used because the input leakage current of the internal reference buffer is less than 1 µA.

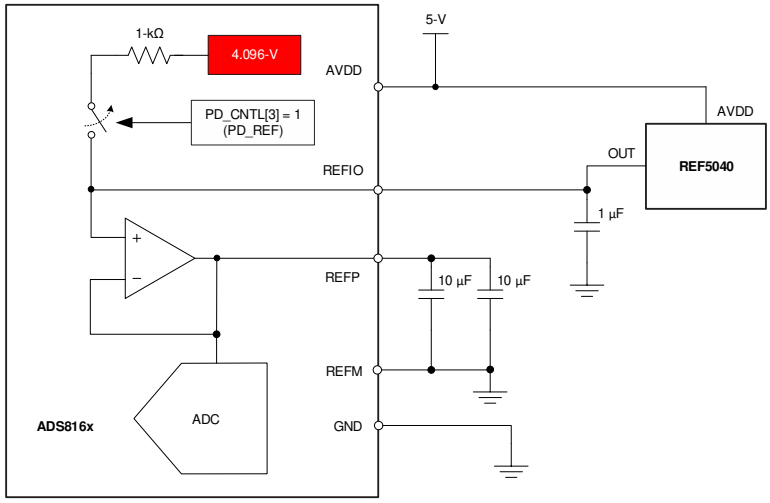


Figure 36. Device Connections for Using an External Reference

7.3.3 Reference Buffer

The ADC starts converting the sampled analog input channel on the $\overline{CS}$ rising edge and the internal capacitors are switched to the REFP pins as per the successive approximation algorithm. Most of the switching charge required during the conversion process is provided by an external decoupling capacitor C_{REFP}. If the charge lost from C_{REFP} is not replenished before the next $\overline{CS}$ rising edge, the voltage on the REFP pins is less than V_{REFP}. The subsequent conversion occurs with this different reference voltage, and causes a proportional error in the output code. The internal reference buffer of the device maintains the voltage on the REFP pins within 0.5 LSB of V_{REFP}. All typical characteristics of the device are specified with the internal reference buffer and the specified value of C_{REFP}.

In burst-mode operation, the ADC samples the selected analog input channel for a long duration of time and then performs a burst of conversions. During the sampling time, the sampling capacitor (C_S) is connected to the differential input pins and no charge is drawn from the REFP pins. However, during the very first conversion cycle, there is a step change in the current drawn from the REFP pins. This sudden change in load triggers a transient settling response in the reference buffer. For a fixed input voltage, any transient settling error at the end of the conversion cycle results in a change in output codes over the subsequent conversions. The internal reference buffer of the ADS816x, when used with the recommended value of C_{REFP}, keeps the transient settling error at the end of each conversion cycle within 0.5 LSB. Therefore, the device supports burst-mode operation with every conversion result as per the data sheet specifications.

Figure 37 shows the block diagram of the internal reference and reference buffer.

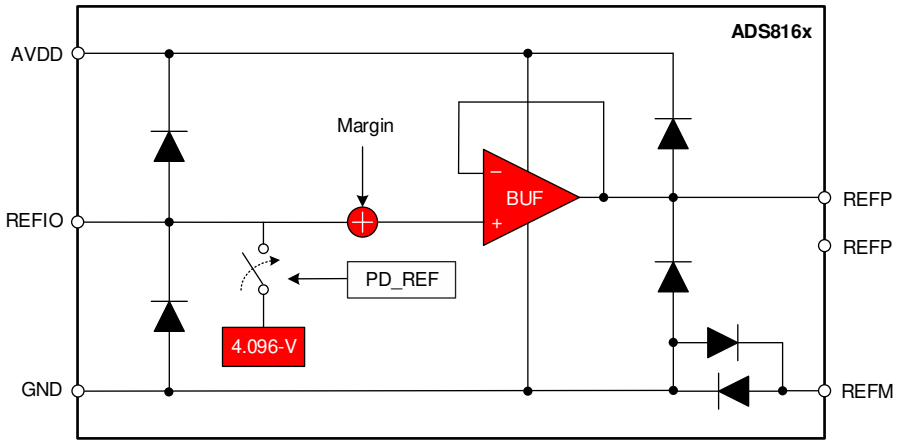


Figure 37. Internal Reference and Reference Buffer Block Diagram

For the minimum ADC input offset error (V_{OS}), set the REF_SEL[2:0] bits to the value closest to V_{REF} (see the OFST_CAL register). The internal reference buffer has a typical gain of 1 V/V with a minimal offset error ($V_{(RO)}$), and the output of the buffer is available between the REFP and the REFM pins. Set the REF_OFST[4:0] (see the REF_MRG1 register) bits to add or subtract an intentional offset voltage as described in Table 22.

Short the two REFP pins externally. Short the REFM pin to GND externally. Place a decoupling capacitor C_{REFP} between the REFP and the REFM pins as close to the device as possible; see Figure 36. See the *Layout* section for layout recommendations.

7.3.4 REFby2 Buffer

To use the maximum dynamic range of the ADC, the input signal must be biased around the mid-scale of the ADC input range. In the ADS816x, where the absolute input range is 0 V to the reference voltage (V_{REF}), mid-scale is V_{REF} / 2. The REFby2 buffer generates the V_{REF} / 2 signal for mid-scale shifting of the input signal. Figure 38 shows that REFBy2 can be used in various types of sensor signal conditioning circuits.

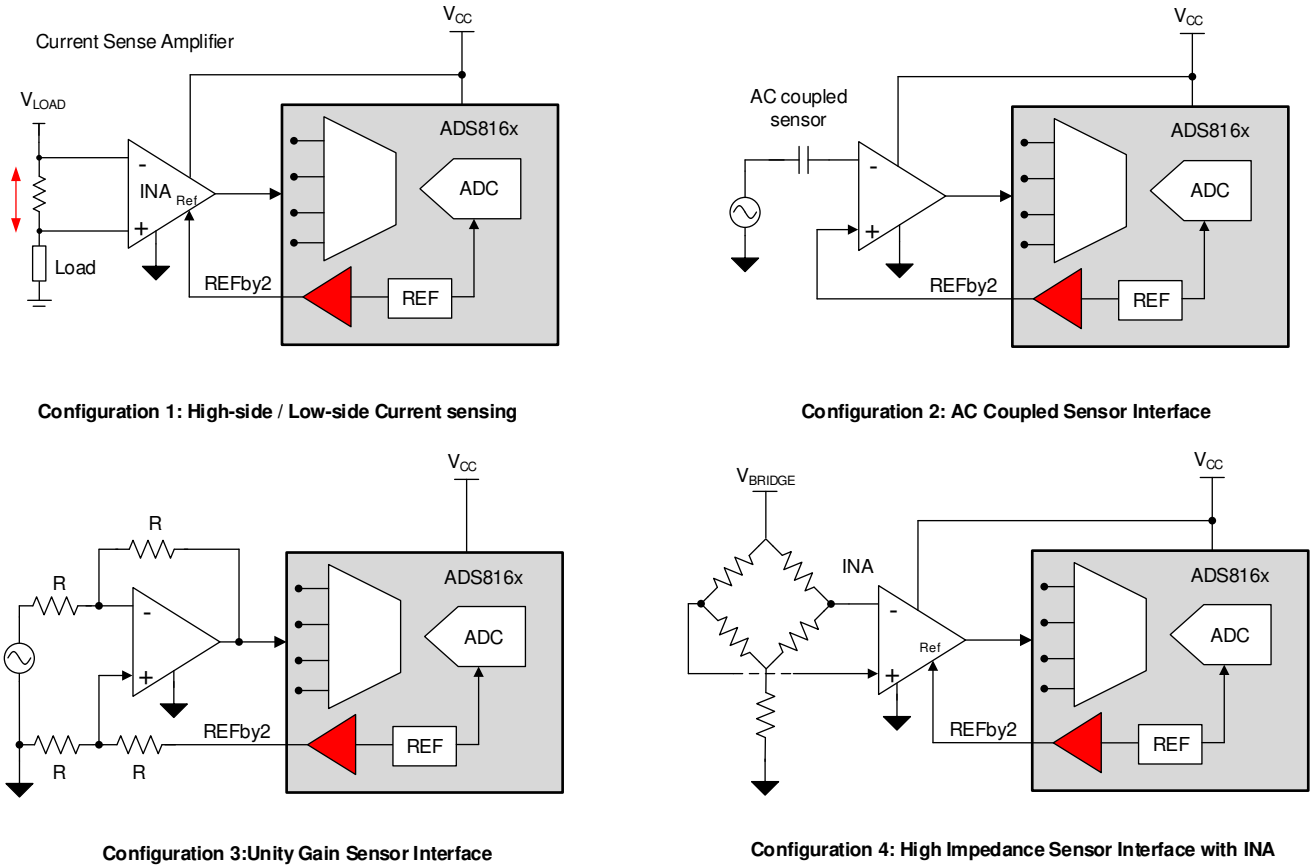


Figure 38. Signal Conditioning With the REFby2 Buffer

A resistor divider at the output of the reference buffer, as shown in Figure 39, generates the V_{REF} / 2 signal. When not using the internal reference buffer (see the PD_CNTL register), any voltage applied at the REFP pin is applied to the resistor divider. The output of the resistor divider is buffered and available at the REFby2 pin.

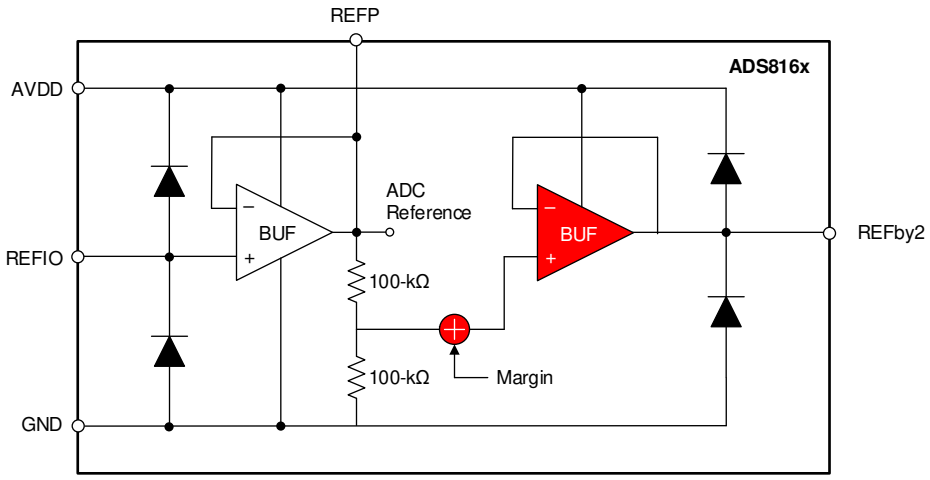


Figure 39. REFby2 Buffer Model

The REFby2 buffer is capable of sourcing up to 2 mA of DC current. The REFby2 pin has ESD diode connections to AVDD and GND.

7.3.5 Converter Module

The converter module samples the analog input signal (provided between the ADC-INP and ADC-INM pins), compares this signal with the reference voltage (between the REFP pins and REFM pin), and generates an equivalent digital output code.

The converter module receives the $\overline{RST}$ and $\overline{CS}$ inputs from the interface module, and outputs the conversion result back to the interface module.

7.3.5.1 Internal Oscillator

The device features an internal oscillator (OSC) that provides the conversion clock. Conversion duration varies, but is bounded by the minimum and maximum value of t_{conv}.

7.3.5.2 ADC Transfer Function

The device supports single-ended and pseudo-differential analog inputs. The device output is in straight binary format. Figure 40 and Table 2 show the ideal transfer characteristics for a 16-bit ADC with unipolar inputs.

Equation 1 gives the least significant bit (LSB) for the ADC:

$$1\ LSB = V_{REF} / 2^{16} \quad (1)$$

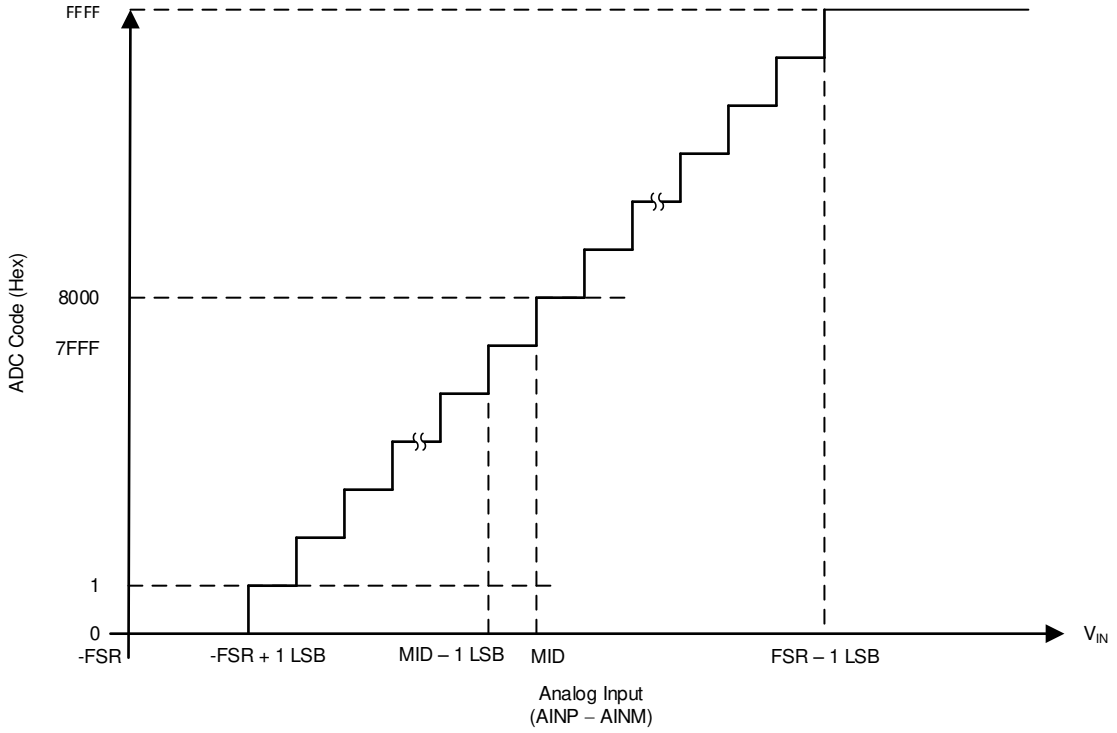


Figure 40. Converter Transfer Characteristics

Table 2. Transfer Characteristics

DESCRIPTION	SINGLE-ENDED INPUT VOLTAGE (V_{REF} = 4.096 V)	PSEUDO-DIFFERENTIAL INPUT VOLTAGE (V_{REF} = 4.096 V)	OUTPUT CODE (HEX)
FSR – 1 LSB	4.0959375 V	2.0479375 V	FFFF
MID + 1 LSB	2.0480625 V	0.0000625 V	8001
MID	2.048 V	0 V	8000
MID – 1 LSB	2.0479375 V	–0.0000625 V	7FFF
–FSR + 1 LSB	0.0000625 V	–2.0479375 V	0001
–FSR	0 V	–2.048 V	0000

7.3.6 Low-Dropout Regulator (LDO)

To enable single-supply operation, the device features an internal low-dropout regulator (LDO). The LDO is powered by the AVDD supply, and the 2.85-V (nominal) output is available on the DECAP pin. This LDO output powers the critical analog blocks within the device, and must not be used for any other external purposes.

Decouple the DECAP pin with the GND pin, as shown in Figure 41, by placing a 1-µF, X7R-grade, ceramic capacitor with a 6.3-V rating from DECAP to GND. There is no upper limit on the value of the decoupling capacitor; however, a larger decoupling capacitor results in higher power-up time for the device. See the *Layout* section for layout recommendations.

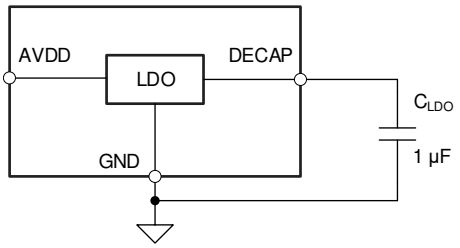


Figure 41. Internal LDO Connections

7.4 Device Functional Modes

The multiplexer includes a sequence control logic that supports various features as described in the *Channel Selection Using Internal Multiplexer* section.

7.4.1 Channel Selection Using Internal Multiplexer

The ADS816x includes an 8-channel, linear, and low-leakage current analog multiplexer. The multiplexer performs a break-before-make operation when switching channels. There are four modes of switching the multiplexer input channels: manual mode, on-the-fly mode, auto sequence mode, and custom channel sequencing mode.

These modes can be selected by configuring the SEQ_MODE[1:0] bits in the DEVICE_CFG register. On power-up the default mode is manual mode, SEQ_MODE[1:0] = 00b, and the default input channel is AIN0. The multiplexer configuration registers can be accessed over the SPI; see Figure 50. The SPI interface eliminates the need for separate MUX control lines.

Device Functional Modes (continued)

7.4.1.1 Manual Mode

In manual mode, the channel ID of the desired analog input is configured in the CHANNEL_ID register. On power-up or after device reset, AIN0 is selected and CHANNEL_ID[2:0] = 000b. Manual mode can be enabled from any other sequencing mode by programming the SEQ_MODE[1:0] bits to 00b in the DEVICE_CFG register. Figure 42 shows the timing information for changing channels in manual mode.

The channel information can be updated in a microcontroller (MCU)-friendly 3-byte access. As the 24-bits of channel configuration are sent over SDI, conversion data are clocked out over SDO. The data on SDO are MSB aligned and the first 16 clocks correspond to 16 bits of conversion data. The last eight bits of the SDO can be ignored by the MCU.

As shown in Figure 42, the command to switch to AINy is sent in the Nth cycle and the data corresponding to channel AINy is available in the (N + 2)th cycle. This switch occurs because the SDI commands are processed and the ADC starts conversions on the rising edge of $\overline{CS}$. Thus, the conversion is processed on the previous channel (AINx) and not on the updated channel ID (AINy).

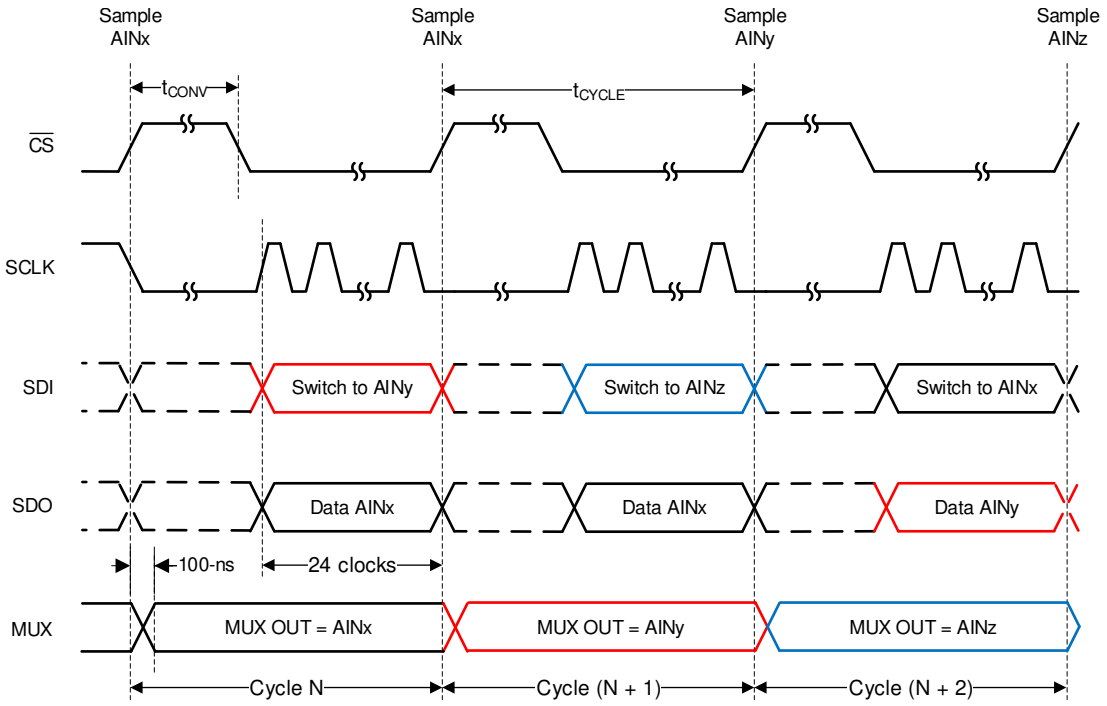


Figure 42. Manual Mode Timing Diagram

Device Functional Modes (continued)

As shown in Figure 43, after selecting AINy the output of the multiplexer does not create a charge kickback as long as SDI is set to 0 (that is, as long as SDI returns the NOP command). Therefore, high-impedance sources such as the voltage from resistor dividers can be connected to the analog inputs of the multiplexer without an op amp.

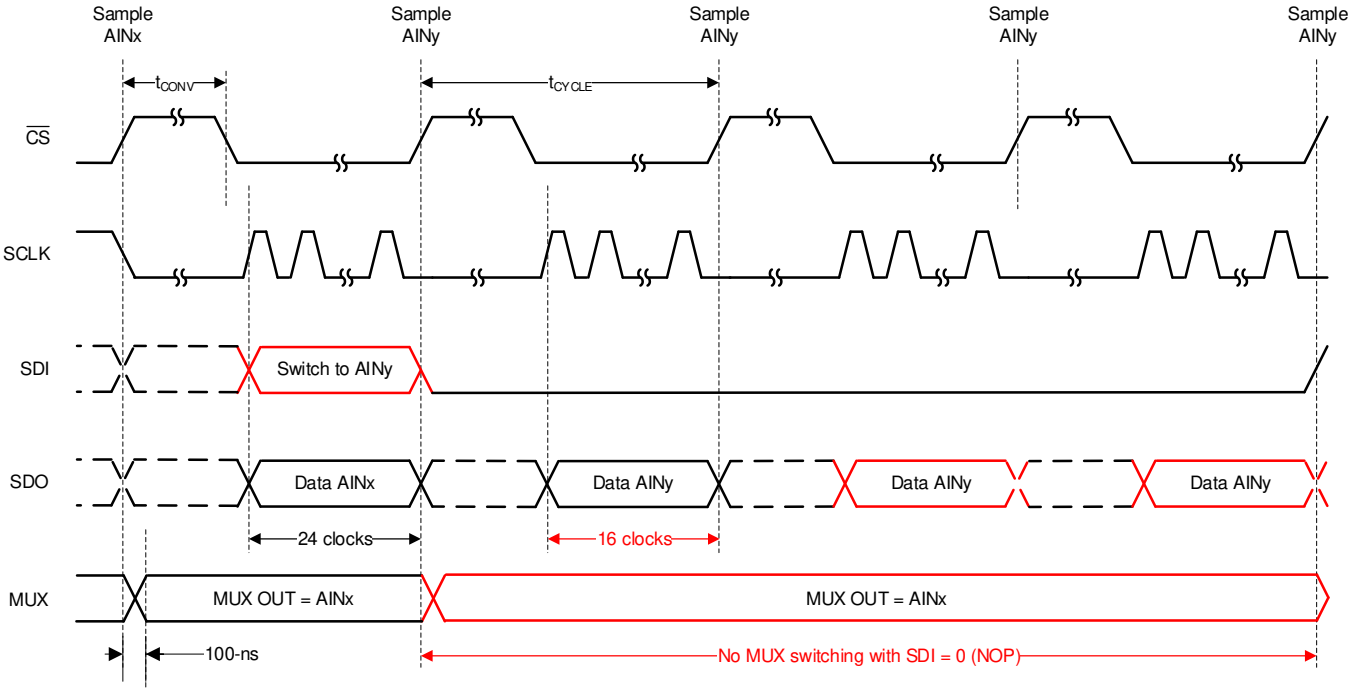


Figure 43. Manual Mode With No Channel Switching Timing Diagram

7.4.1.2 On-The-Fly Mode

There is a latency of one cycle when switching channels using the register access, just as in manual mode. The newly selected channel data are available two cycles after selecting the desired channel. The ADS816x supports on-the-fly switching of the analog input channels of the multiplexer. This mode can be enabled by programming the SEQ_MODE[1:0] bits to 01b in the DEVICE_CFG register. When enabled, the analog input channel for the next conversion is determined by the first five bits sent over SDI. The desired analog input channel can be selected by setting the MSB to 1 and the following four bits as the channel ID. If the MSB is 0 then the SDI bitstream is decoded as a normal frame on the rising edge of CS. Table 3 lists the channel selection commands for this mode.

Table 3. On-the-Fly Mode Channel Selection Commands

SDI BITS [15:11]	SDI BITS [10:0]	DESCRIPTION
1 0000	Don't care	Select analog input 0
1 0001	Don't care	Select analog input 1
1 0010	Don't care	Select analog input 2
1 0011	Don't care	Select analog input 3
1 0100	Don't care	Select analog input 4
1 0101	Don't care	Select analog input 5
1 0110	Don't care	Select analog input 6
1 0111	Don't care	Select analog input 7
1 1000 to 1 1111	Don't care	Error bit is set; select analog input 0

To set the device in on-the-fly mode, configure EN_ON_THE_FLY to 1b in the ON_THE_FLY_CFG register as shown in Figure 44 using a 3-byte register access. When in this mode, the 16-bit data transfer can be used to reduce the required clock speed for operating at full throughput.

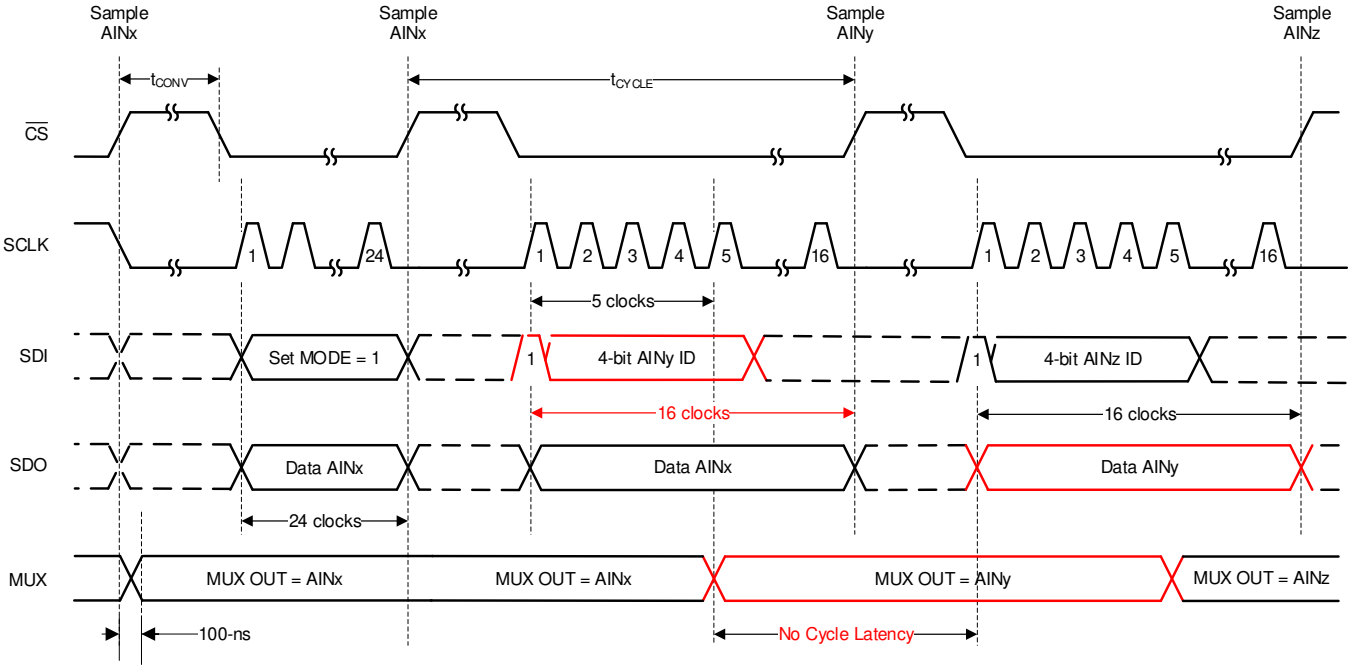


Figure 44. On-the-Fly Mode With No MUX Channel Selection Latency

After selecting AINy, as shown in Figure 45, the output of the multiplexer does not create a charge kickback as long as SDI is set to 0 (that is, as long as SDI returns the NOP command). Thus, high-impedance sources such as the voltage from resistor dividers can be connected to the analog inputs of the multiplexer without an op amp.

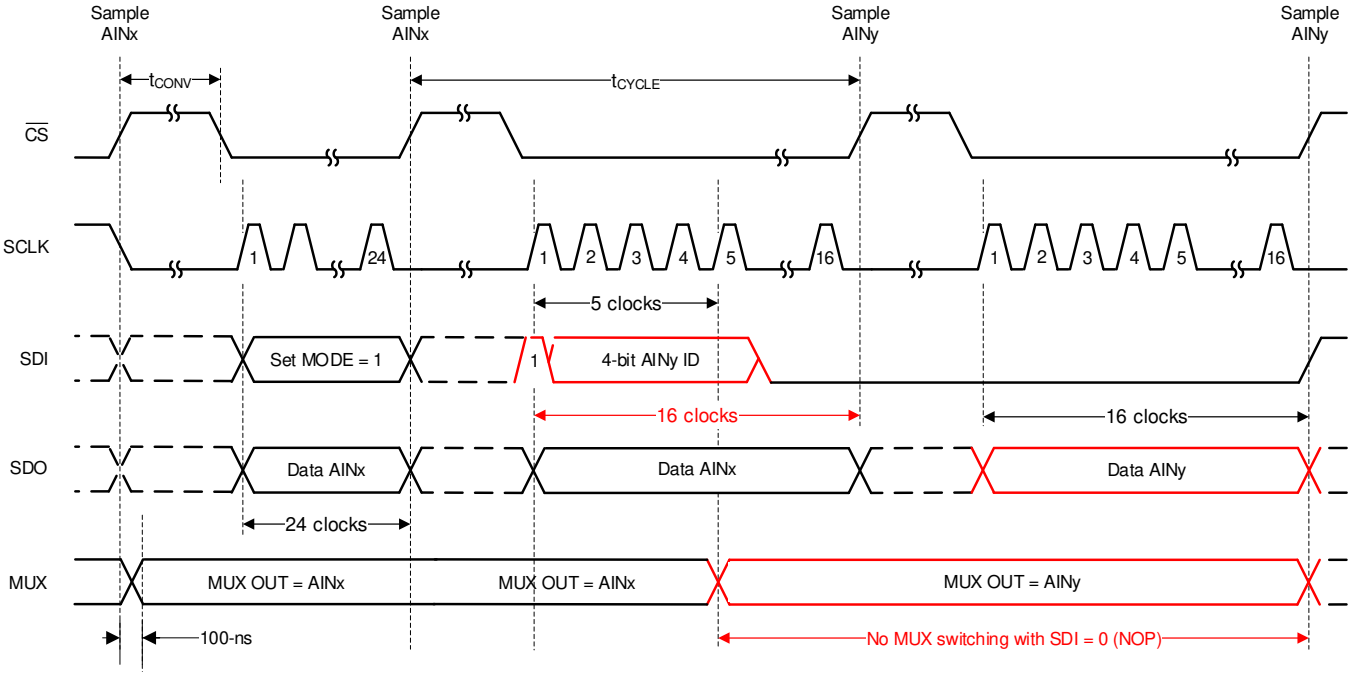


Figure 45. On-the-Fly Mode With No Channel Switching Timing Diagram

7.4.1.3 Auto Sequence Mode

In auto sequence mode, the internal channel sequencer can selectively scan channels from AIN0 through AIN7 in ascending order. To select auto sequence mode, configure SEQ_MODE to 10b in the DEVICE_CFG register using a 3-byte register access. One or more channels among AIN[7:0] can be enabled by configuring the AUTO_SEQ_CFG1 register. By default all analog input channels are enabled. After enabling the desired channels, the sequence can be started by setting SEQ_START to 1b. The ADC auto-increments through the enabled channels after every $\overline{CS}$ rising edge. When SEQ_START is set to 1b, the SDO-1/SEQSTS pin is at logic 1 as shown in Figure 46 until the last channel conversion frame is complete. After the last enabled channel conversion is complete, channel AIN0 is selected and SDO-1/SEQSTS is in a high-impedance state.

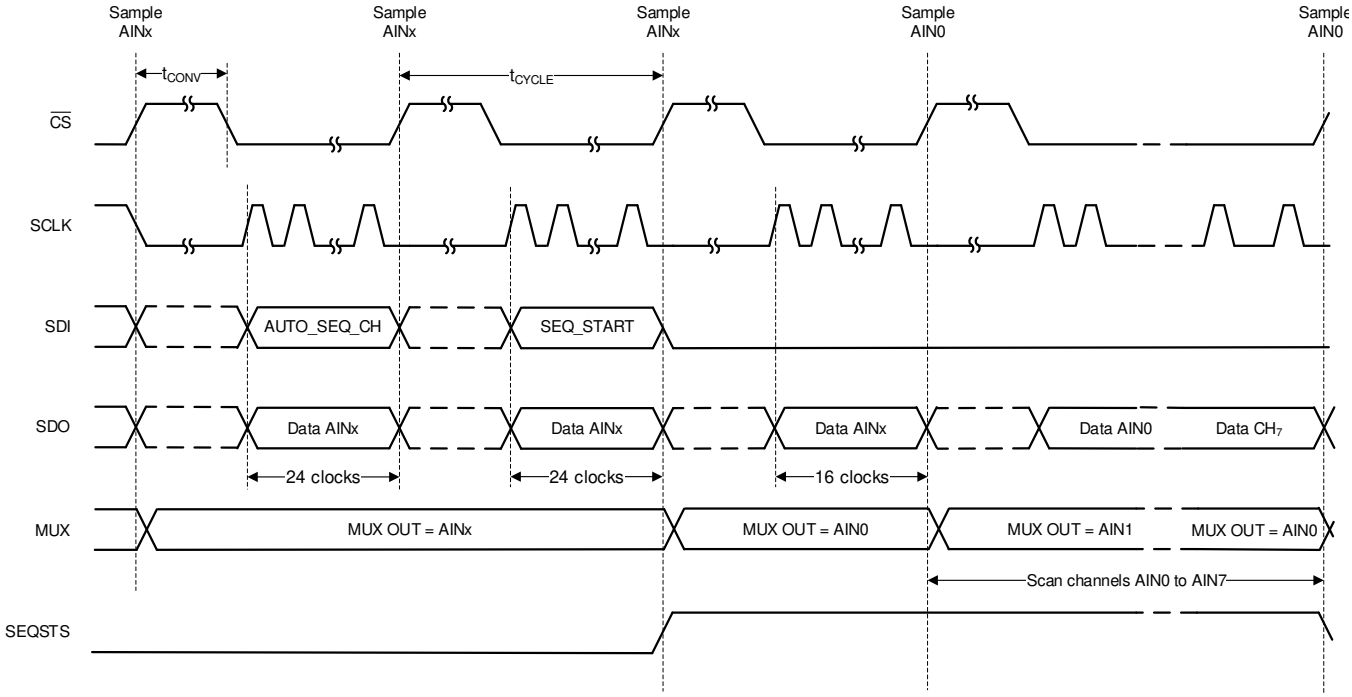


Figure 46. Starting a Sequence in Auto Sequence Mode

As an example, Figure 47 depicts a timing diagram for when the device is scanning AIN2 and AIN6 in auto sequence mode. When AIN6 is converted, SDO-1/SEQSTS is Hi-Z and AIN0 is selected as the active channel. At the end of sequence, if more conversion frames are launched the device returns valid data corresponding to AIN0.

To use the device in auto sequence mode follow these steps:

- Set the SEQ_MODE[1:0] bits in the DEVICE_CFG register to 10b.
- Configure the AUTO_SEQ_CFG1 register. In Figure 47, AUTO_SEQ_CFG1 = 0x44.
- Set the SEQ_START bits in the SEQ_START register to 1b to start executing the sequence.

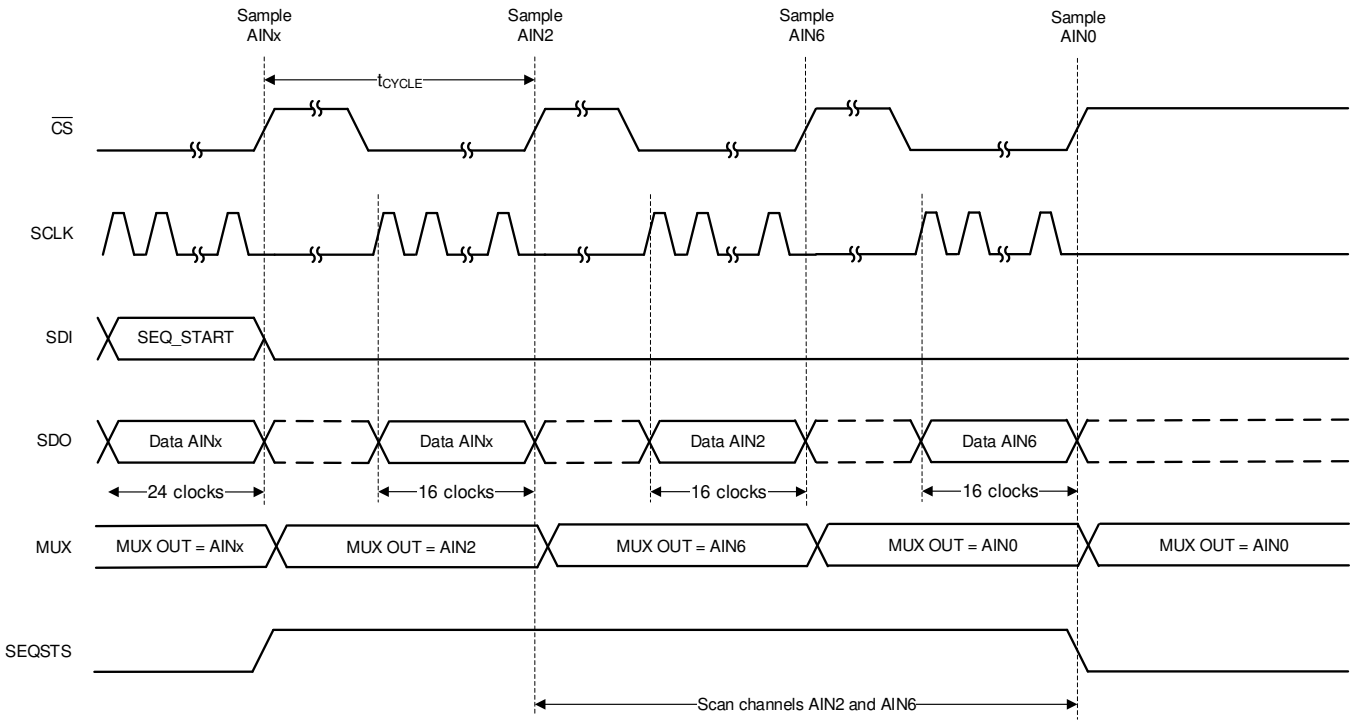


Figure 47. Example: Scanning Channels 2 and 6 in Auto Sequence Mode

To repeat a channel sequence indefinitely, set the AUTO_REPEAT bit in the AUTO_SEQ_CFG2 register to 1b. Figure 48 shows that when the AUTO_REPEAT bit is enabled, the MUX scans through the channels enabled in the AUTO_SEQ_CFG1 register and repeats the sequence after the last channel data are converted.

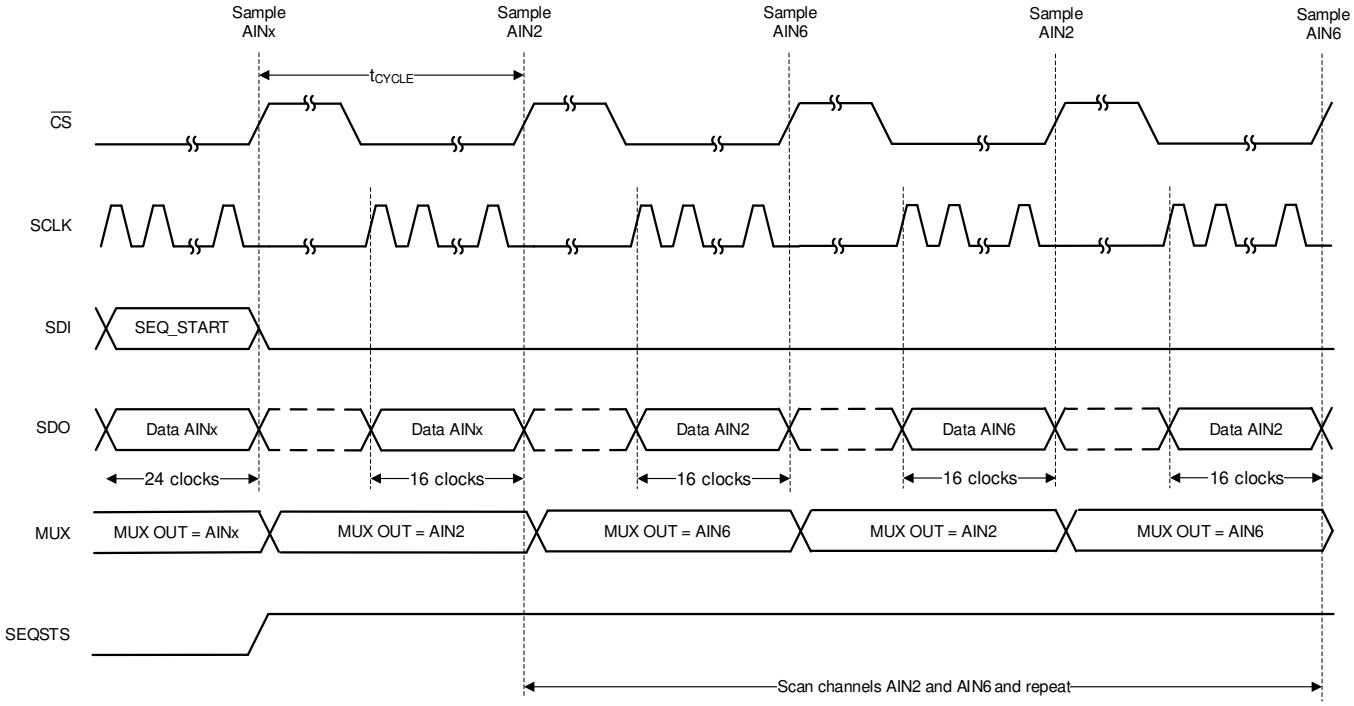


Figure 48. Example: Scanning Channels 2 and 6 in Auto Sequence Mode With AUTO_REPEAT = 1

Figure 48 provides a timing diagram for when the device is scanning AIN2 and AIN6 in auto sequence mode with AUTO_REPEAT = 1b. When AIN6 is converted, AIN2 is selected as the active channel and the device continues scanning through the enabled channels again.

To use the device in auto sequence with the repeat mode enabled follow these steps:

- Set the SEQ_MODE[1:0] bits in the DEVICE_CFG register to 10b.
- Configure the AUTO_SEQ_CFG1 register. In Figure 47, AUTO_SEQ_CFG1 = 0x44.
- Set AUTO_REPEAT to 1b.
- Set the SEQ_START bit in the SEQ_START register to 1b to start executing the sequence.

To terminate an ongoing channel sequence set the SEQ_ABORT bit in the SEQ_ABORT register 1. When SEQ_ABORT is set, the auto sequence stops and AIN0 is selected as the active input channel.

7.4.1.4 Custom Channel Sequencing Mode

In this mode the internal channel sequencer can selectively scan channels from AIN0 through AIN7 in any order as defined by a user-programmable lookup table. Table 4 describes the configurability of this lookup table. The device can be configured in custom channel sequencing mode by programming the SEQ_MODE[1:0] bits to 11b in the DEVICE_CFG register using a 3-byte register access. Table 4 shows that the channel scanning sequence is programmed by configuring the channel IDs in the register as space. A channel sample count can also be programmed and associated with every channel ID. By default the channel sample count is 1, which means the sequence executes in the order of programmed channel IDs. If the channel sample count is greater than 1 then the corresponding channel is sampled and converted for a programmed number of times before switching to the next channel.

Table 4. Custom Channel Sequencing Configuration Space

REGISTER ADDRESS	CHANNEL ID[2:0]	REGISTER ADDRESS	CHANNEL SAMPLE COUNT[7:0]
0x8C	Index 0 : 3-bit channel ID (default = 0)	0x8D	Index 0 : 8-bit sample count (default = 0xFF)
0x8E	Index 1 : 3-bit channel ID (default = 0)	0x8F	Index 1 : 8-bit sample count (default = 0xFF)
0x90	Index 2 : 3-bit channel ID (default = 0)	0x91	Index 2 : 8-bit sample count (default = 0xFF)
0x92	Index 3 : 3-bit channel ID (default = 0)	0x93	Index 3 : 8-bit sample count (default = 0xFF)
0x94	Index 4 : 3-bit channel ID (default = 0)	0x95	Index 4 : 8-bit sample count (default = 0xFF)
0x96	Index 5 : 3-bit channel ID (default = 0)	0x97	Index 5 : 8-bit sample count (default = 0xFF)
0x98	Index 6 : 3-bit channel ID (default = 0)	0x99	Index 6 : 8-bit sample count (default = 0xFF)
0x9A	Index 7 : 3-bit channel ID (default = 0)	0x9B	Index 7 : 8-bit sample count (default = 0xFF)
0x9C	Index 8 : 3-bit channel ID (default = 0)	0x9D	Index 8 : 8-bit sample count (default = 0xFF)
0x9E	Index 9 : 3-bit channel ID (default = 0)	0x9F	Index 9 : 8-bit sample count (default = 0xFF)
0xA0	Index 10 : 3-bit channel ID (default = 0)	0xA1	Index 10 : 8-bit sample count (default = 0xFF)
0xA2	Index 11 : 3-bit channel ID (default = 0)	0xA3	Index 11 : 8-bit sample count (default = 0xFF)
0xA4	Index 12 : 3-bit channel ID (default = 0)	0xA5	Index 12 : 8-bit sample count (default = 0xFF)
0xA6	Index 13 : 3-bit channel ID (default = 0)	0xA7	Index 13: 8-bit sample count (default = 0xFF)
0xA8	Index 14 : 3-bit channel ID (default = 0)	0xA9	Index 14 : 8-bit sample count (default = 0xFF)
0xAA	Index 15: 3-bit channel ID (default = 0)	0xAB	Index 15 : 8-bit sample count (default = 0xFF)

For application-specific scanning requirements, start and stop pointers can be used to define the channel scanning sequence. The start index can be programmed in the CCS_START_INDEX register and the stop index can be programmed in the CCS_END_INDEX register. Table 4 shows that the 4-bit index corresponds to the configuration index. The sequence starts executing from the index programmed in CCS_START_INDEX (default 0) and stop or loop-back from CCS_STOP_INDEX (default 15). The channel scanning sequence can be looped-back to the start index from the stop index by setting the CCS_SEQ_LOOP register to 1b.

After configuring the channel scanning order, start index, and stop index the scanning can be initiated by setting the SEQ_START bit to 1b. The ADC scans through the enabled channels after every $\overline{CS}$ rising edge as defined by the channel scanning order. When SEQ_START is set to 1b, the SDO-1/SEQSTS pin is pulled high until the last channel conversion frame is complete, as described in Figure 46. As illustrated in Figure 47, channel AIN0 is selected and SEQSTS/SDO-1 goes to Hi-Z after the last enabled channel conversion is complete.

As an example, Figure 47 provides a timing diagram for when the channel configuration is set as in Table 5. When AIN6 is converted, SEQSTS/SDO-1 goes to Hi-Z and AIN0 is selected as the active channel. If more conversion frames are launched at the end of the sequence, the device returns valid data corresponding to AIN0.

To use the device in easy capture mode follow these steps:

- Set the SEQ_MODE[1:0] bits in the DEVICE_CFG register to 3.
- Configure the channel sequence by setting registers 0x000C to 0x002B.
- Configure the CCS_START_INDEX and the CCS_END_INDEX registers. In Figure 47, CCS_START_INDEX = 0 and CCS_STOP_INDEX = 1.
- Configure the CCS_SEQ_LOOP register to 1 to indefinitely loop the sequence. In Figure 47, the CCS_SEQ_LOOP register = 0b.
- Set the SEQ_START register to 1b to start executing the sequence.

Table 5. Custom Channel Sequencing Configuration Example

REGISTER ADDRESS	CHANNEL ID[2:0]	REGISTER ADDRESS	CHANNEL SAMPLE COUNT[7:0]
0x8C	010b (Channel 2)	0x8D	1
0x8E	110b (Channel 6)	0x8F	1

7.4.2 Digital Window Comparator

The ADS816x has a programmable digital window comparator for every analog input channel. The integrated digital window comparator allows the host to not read ADC data over the serial interface for comparison purposes. In monitoring applications, the ADC can compare channel data with the set thresholds and alert the system host using the ALERT pin. Furthermore, the digital window comparator does not require software high and low comparisons and thus saves processing cycles.

Window comparison is achieved by comparing the channel output code with a programmable high and low digital threshold. As shown in Figure 49, each analog input channel has a programable hysteresis that is applicable to both the high and low thresholds of the corresponding channel. Thus, low threshold, high threshold, and hysteresis configurations are available for each analog input channel.

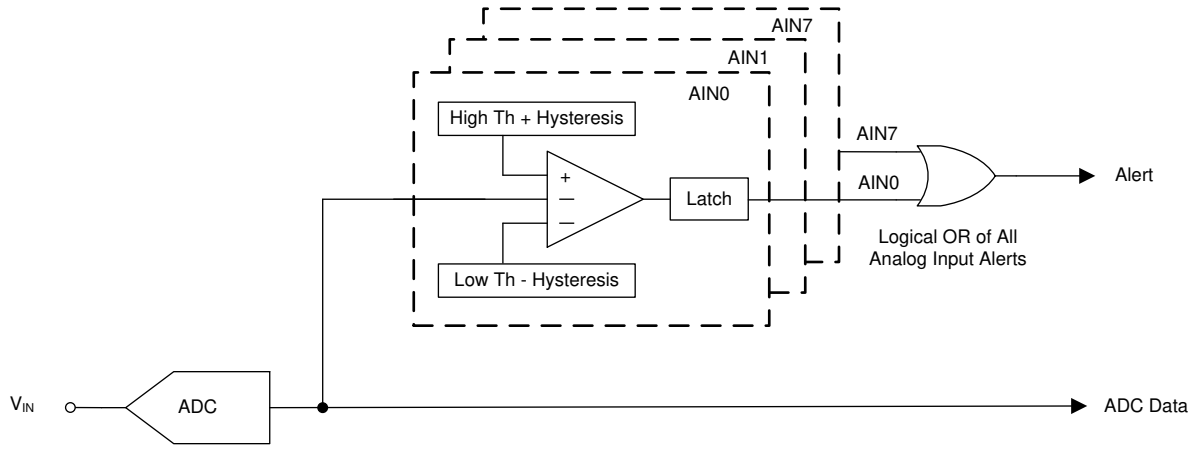


Figure 49. Digital Window Comparator

The thresholds and hysteresis can be configured independently for each analog input channel. The ALERT output of the device is a logical OR of all enabled alert outputs corresponding to the analog inputs. The window comparator can be selectively enabled for the analog inputs by configuring the ALERT_CFG register.

The alert status of an individual analog input channel can be read from the ALERT_STATUS register. See the ALERT_HI_STATUS and ALERT_LO_STATUS registers for further information on the high or low threshold ALERT, respectively. When monitoring only a low threshold, the high threshold can be set to the ADC positive full-scale code. Similarly, when monitoring only a high threshold, the low threshold can be set to the negative full-scale code.

7.5 Programming

7.5.1 Data Transfer Protocols

7.5.1.1 Enhanced-SPI Interface

The device features an enhanced-SPI interface that allows the host controller to operate at slower SCLK speeds and still achieve the required cycle time with a faster response time. Figure 50 shows the ADS816x Interface connections for the minimum number of pins required by the enhanced-SPI interface.

For any data write operation, the host controller can use any of the four legacy, SPI-compatible protocols to configure the device, as described in the *Protocols for Configuring the Device* section. See the *Register Read/Write Operation* section for details about the register read or write operation.

For reading ADC conversion data or register data from the device, the enhanced-SPI interface module offers the following options:

- SPI protocol with a single data output line: SDO-0 (see the *SPI Protocols With a Single SDO* section)
- SPI protocol with dual data output lines: SDO-1 and SDO-0 (see the *SPI Protocols With Dual SDO* section)
- Clock re-timer data transfer (see the *Clock Re-Timer Data Transfer* section)

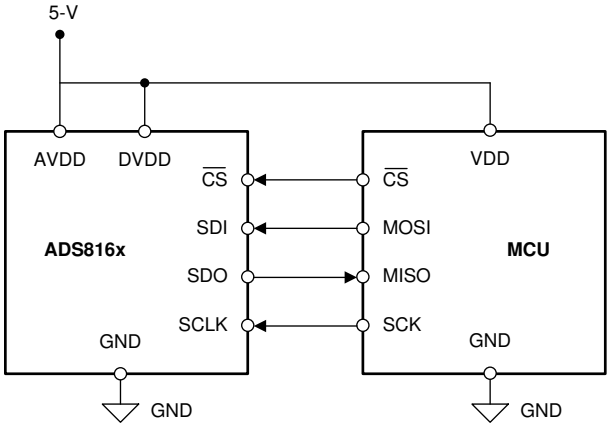


Figure 50. 4-Wire SPI Interface Connection Diagram

7.5.1.1.1 Protocols for Configuring the Device

As described in Table 6, the host controller can use any of the four SPI protocols (SPI-00, SPI-01, SPI-10, or SPI-11) to write data into the device.

Table 6. SPI Protocols for Configuring the Device

PROTOCOL	SCLK POLARITY (At the $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	SDI_MODE[1:0] BITS(1)	SDO_MODE[1:0] BITS(2)	DIAGRAM
SPI-00	Low	Rising	00h	00h	Figure 51
SPI-01	Low	Falling	01h	00h	Figure 51
SPI-10	High	Falling	02h	00h	Figure 52
SPI-11	High	Rising	03h	00h	Figure 52

(1) See the SDI_CNTL register.
(2) See the SDO_CNTL1 register.

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00-S protocol for data read and data write operations. To select a different SPI-compatible protocol, program the SDI_MODE[1:0] bits in the SDI_CNTL register. This first write operation must adhere to the SPI-00-S protocol. Any subsequent data transfer frames must adhere to the newly-selected protocol. The SPI protocol selected by the SDI_MODE[1:0] configuration is applicable to both read and write operations.

Figure 51 and Figure 52 detail the four protocols using an optimal data frame.

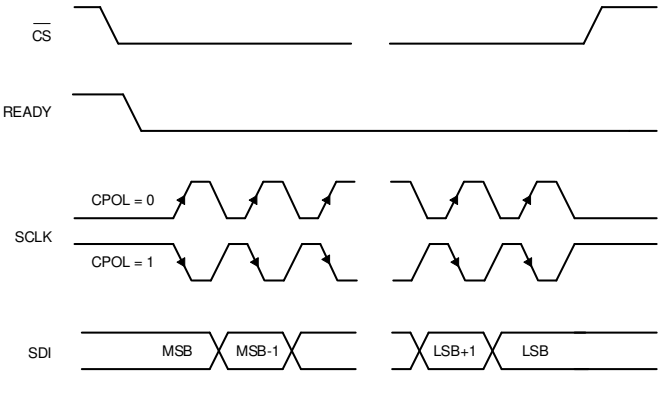


Figure 51. Standard SPI Timing Protocol (CPHA = 0)

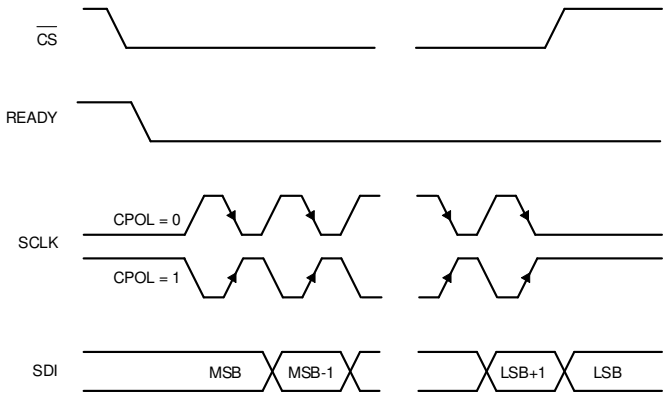


Figure 52. Standard SPI Timing Protocol (CPHA = 1)

NOTE

As explained in the *Register Read/Write Operation* section, a valid register read or write operation to the device requires 24 SCLKs to be provided within a data transfer frame. When reading ADC conversion data, a minimum 16 SCLKs are required within a data transfer frame.

7.5.1.1.2 Protocols for Reading From the Device

The protocols for the data read operation can be broadly classified into three categories:

1. SPI protocols (SPI-00, SPI-01, SPI-10, and SPI-11) with a single SDO (see the *SPI Protocols With a Single SDO* section); for example, SDO-0
2. SPI protocols (SPI-00, SPI-01, SPI-10, and SPI-11) with dual SDOs (see the *SPI Protocols With Dual SDO* section); for example, SDO-1 and SDO-0
3. Source-synchronous protocol for data transfer

7.5.1.1.2.1 SPI Protocols With a Single SDO

As shown in Table 7, Figure 53, and Figure 54, the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00, SPI-01, SPI-10, or SPI-11) to read data from the device.

Table 7. SPI Protocols for Reading From the Device

PROTOCOL	SCLK POLARITY (At the $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_MODE[1:0] BITS	SDO_MODE[1:0] BITS	DIAGRAM
SPI-00	Low	Rising	$\overline{CS}$ falling	00h	00h	Figure 53
SPI-01	Low	Falling	1st SCLK rising	01h	00h	Figure 53
SPI-10	High	Falling	$\overline{CS}$ falling	02h	00h	Figure 54
SPI-11	High	Rising	1st SCLK falling	03h	00h	Figure 54

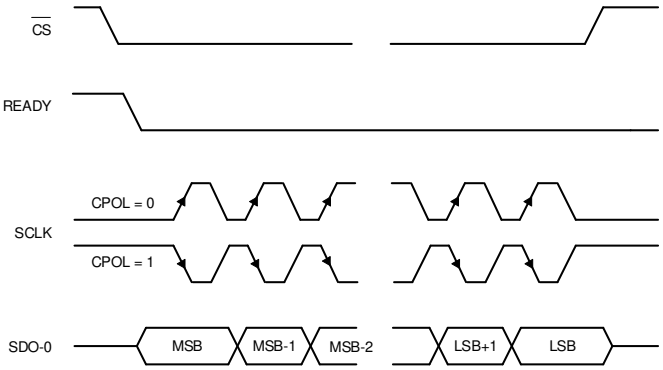


Figure 53. Standard SPI Timing Protocol (CPHA = 0, Single SDO-0)

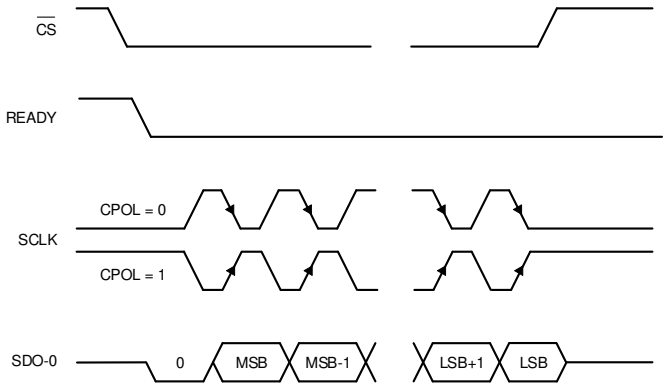


Figure 54. Standard SPI Timing Protocol (CPHA = 1, Single SDO-0)

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00 protocol for data read and data write operations. To select a different SPI-compatible protocol for both of the data transfer operations:

1. Program the SDI_MODE[1:0] bits in the SDI_CNTL register. This first write operation must adhere to the SPI-00 protocol. Any subsequent data transfer frames must adhere to the newly-selected protocol.
2. Set the SDO_MODE[1:0] bits = 00b in the SDO_CNTL1 register.

NOTE

The SPI transfer protocol selected by configuring the SDI_MODE[1:0] bits in the SDI_CNTL register determines the data transfer protocol for both write and read operations.

When using any of the SPI-compatible protocols, the READY output remains low throughout the data transfer frame.

7.5.1.1.2.2 SPI Protocols With Dual SDO

The device provides an option to increase the SDO bus width from one bit (default, single SDO-0) to two bits (dual SDO) when operating with any of the data transfer protocols. In order to operate the device in dual SDO mode, the SDO_WIDTH bit in the SDO_CNTL1 register must be set to 1b. In this mode, the SDO-1/SEQSTS pin functions as SDO-1.

As shown in Figure 55 and Figure 56, two bits of data are launched on the two SDO pins (SDO-0 and SDO-1) on every SCLK launch edge in dual SDO mode.

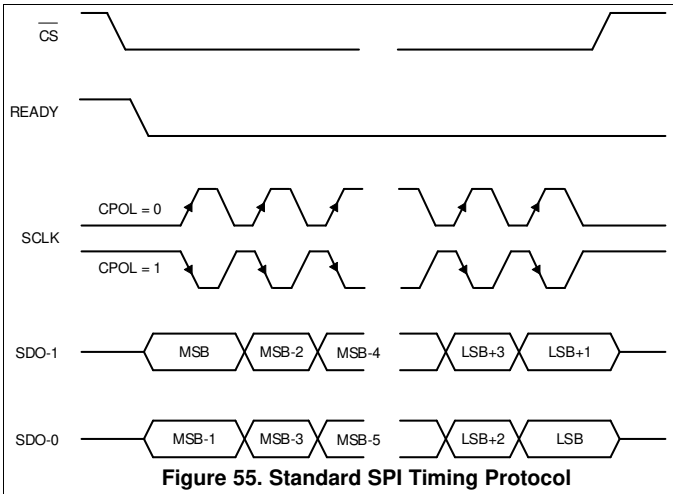


Figure 55. Standard SPI Timing Protocol (CPHA = 0, Dual SDO)

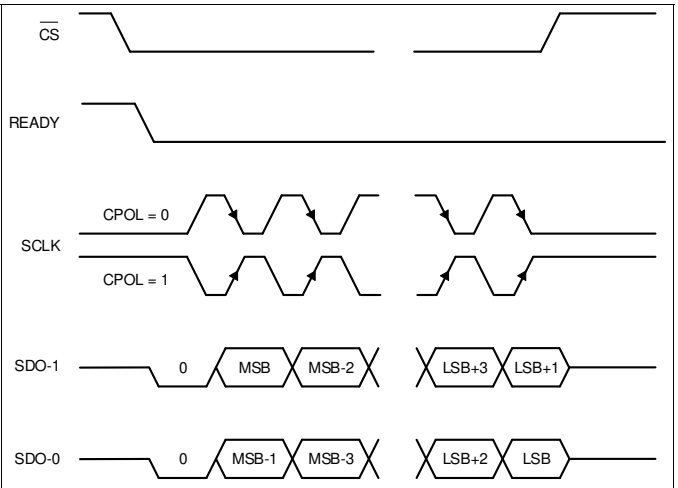


Figure 56. Standard SPI Timing Protocol (CPHA = 1, Dual SDO)

7.5.1.1.2.3 Clock Re-Timer Data Transfer

In clock re-timer data transfer mode, the device provides an output clock that is synchronous with the output data. Furthermore, the host controller can also select the data bus width in this mode of operation. In all modes of operation, the READY pin provides the output clock, synchronous to the device data output.

The clock re-timer data transfer allows the width of the output bus to be configured, similar to the SPI protocols SPI protocols described in Table 6.

7.5.1.1.2.3.1 Output Bus Width Options

The device provides an option to increase the SDO-x bus width from one bit (default, single SDO-x) to two bits (dual SDO-x) when operating with clock re-timer data transfer. In order to operate the device in dual SDO mode, the SDO_WIDTH bit in the SDO_CNTL1 register must be set to 1b. In this mode, the SDO-1/SEQSTS pin functions as SDO-1.

NOTE

For any particular data transfer, SPI or clock re-timer, the device follows the same timing specifications for single and dual SDO modes. The only difference is that in the dual SDO mode the device requires half as many clock cycles to output the same number of bits when in single SDO mode, thus reducing the minimum required clock frequency for a certain sampling rate of the ADC.

7.5.2 Register Read/Write Operation

This device features configuration registers (as described in the *Interface and Hardware Configuration Registers* section). These devices support the commands listed in Table 8 to access the internal configuration registers.

Table 8. Supported Commands

B[23:19]	B[18:8]	B[7:0]	COMMAND ACRONYM	COMMAND DESCRIPTION
00000	00000000000	00000000	NOP	No operation
00001	<11-bit address>	<8-bit data>	WR_REG	Write <8-bit data> to the <11-bit address>
00010	<11-bit address>	00000000	RD_REG	Read contents from the <11-bit address>
00011	<11-bit address>	<8-bit unmasked bits>	SET_BITS	Set <8-bit unmasked bits> from <11-bit address>
00100	<11-bit address>	<8-bit unmasked bits>	CLR_BITS	Clear <8-bit unmasked bits> from <11-bit address>
Remaining combinations	xxxxxxxxx	xxxxxxxx	Reserved	These commands are reserved and treated by the device as no operation

The ADS816x supports two types of data transfer operations: *data write* (the host controller configures the device), and *data read* (the host controller reads data from the device).

Any data write to the device is always synchronous to the external clock provided on the SCLK pin. The WR_REG command writes the 8-bit data into the 11-bit address specified in the command string. The CLR_BITS command clears the specified bits (identified by 1) at the 11-bit address (without affecting the other bits), and the SET_BITS command sets the specified bits (identified by 1) at the 11-bit address (without affecting the other bits).

Figure 57 shows the digital waveform for register read operation. Register read operation consists of two frames: one frame to initiate a register read and a second frame to read data from the register address provided in the first frame. As shown in Figure 57, the 11-bit register address and the 8-bit dummy data are sent over the SDI pin during the first 24-bit frame with the read command (00010b). When $\overline{CS}$ goes from low to high, this read command is decoded and the requested register data are available for reading during the next frame. During the second frame, the first eight bits on SDO correspond to the requested register read. During the second frame SDI can be used to initiate another operation or can be set to 0.

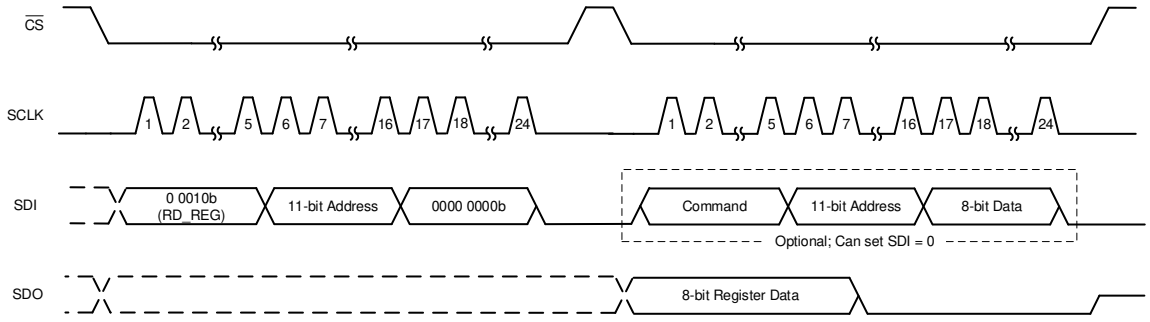


Figure 57. Register Read Operation

Figure 58 shows that for writing data to the register, one 24-bit frame is required. The 24-bit data on SDI consists of a 5-bit write command (00001b), an 11-bit register address, and 8-bit data. The write command is decoded on the $\overline{CS}$ rising edge and the specified register is updated with the 8-bit data specified during register write operation.

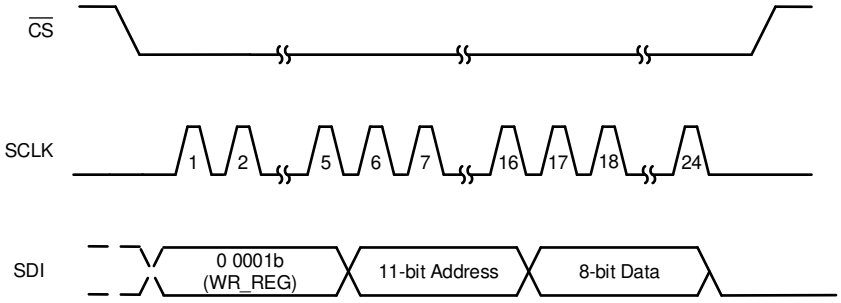


Figure 58. Register Write Operation

7.6 Register Maps

Table 9 lists the access codes for the ADS816x registers.

Table 9. ADS816x Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-W	R/W	Read or write
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1 Interface and Hardware Configuration Registers

Table 10 maps the device features following a hardware configuration of the registers.

Table 10. Configuration Registers Mapping

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION
00h	REG_ACCESS	Enables read/write access to the device configuration registers specified in *Interface and Hardware Configuration Registers*
04h	PD_CNTL	Enable/disable control for reference, reference buffer, REFby2 buffer, and the ADC
08h	SDI_CNTL	SPI-00, SPI-01, SPI-10, or SPI-11 protocol selection.
0Ch	SDO_CNTL1	SDO output protocol selection
0Dh	SDO_CNTL2	Output data rate selection
0Eh	SDO_CNTL3	Reserved
0Fh	SDO_CNTL4	Configuration for the SEQSTS pin when not using SDO-1 for data transfer.
10h	DATA_CNTL	Output data word configuration
11h	PARITY_CNTL	Parity configuration register

7.6.1.1 REG_ACCESS Register (address = 00h) [reset = 00h]

This register enables or disables write access to the device configuration registers specified in Table 10.

Figure 59. REG_ACCESS Register

7	6	5	4	3	2	1	0
REG_ACCESS_BITS							
R/W-0000 0000b							

Table 11. REG_ACCESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REG_ACCESS_BITS	R/W	0000 0000b	Enables or disables write access to the device configuration registers specified in Table 10. Write 1010 1010b to this register to enable write access. Write access is disabled for all values other than REG_ACCESS_BITS = 1010 1010b.

7.6.1.2 PD_CNTL Register (address = 04h) [reset = 00h]

This register controls the low-power modes offered by the device. Write access to this register is disabled on power-up. To enable write access, configure the REG_ACCESS register.

Figure 60. PD_CNTL Register

7	6	5	4	3	2	1	0
0	0	0	PD_REFby2	PD_REF	PD_REFBUF	PD_ADC	0
R-0b	R-0b	R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0b

Table 12. PD_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R	000b	Reserved bits. Reads return 000b.
4	PD_REFby2	R/W	0b	This bit powers down the internal REFby2 buffer. 0b = REFby2 buffer is powered up 1b = REFby2 buffer is powered down
3	PD_REF	R/W	0b	This bit powers down the internal reference. 0b = Internal reference is powered up 1b = Internal reference is powered down
2	PD_REFBUF	R/W	0b	This bit powers down the internal reference buffer. 0b = Internal reference buffer is powered up 1b = Internal reference buffer is powered down
1	PD_ADC	R/W	0b	This bit powers down the converter module. 0b = Converter module is powered up 1b = Converter module is powered down
0	0	R	0b	Reserved bits. Do not write. Reads return 0b.

To power-down the converter module, set the PD_ADC bit in the PD_CNTL register. The converter module powers down on the rising edge of $\overline{CS}$. To power-up the converter module, reset the PD_ADC bit in the PD_CNTL register. The converter module starts to power-up on the rising edge of $\overline{CS}$. Wait for t_{PU_ADC} before initiating any conversion or data transfer operation.

To power-down the internal reference buffer, set the PD_REFBUF bit in the PD_CNTL register. The internal reference buffer powers down on the rising edge of $\overline{CS}$.

To power-down the internal reference, set the PD_REF bit in the PD_CNTL register. The internal reference powers down on the rising edge of $\overline{CS}$.

7.6.1.3 SDI_CNTL Register (address = 008h) [reset = 00h]

This register selects the SPI protocol for writing data to the device. Write access to this register is disabled on power-up. To enable write access, configure the REG_ACCESS register.

Figure 61. SDI_CNTL Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SDI_MODE[1:0]	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-00b	

Table 13. SDI_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R	000000b	Reserved bits. Do not write. Reads return 000000b.
1-0	SDI_MODE[1:0]	R/W	00b	These bits select the protocol for writing data into the device. 00b = Standard SPI with CPOL = 0 and CPHASE = 0 01b = Standard SPI with CPOL = 0 and CPHASE = 1 10b = Standard SPI with CPOL = 1 and CPHASE = 0 11b = Standard SPI with CPOL = 1 and CPHASE = 1

7.6.1.4 SDO_CNTL1 Register (address = 0Ch) [reset = 00h]

This register configures the protocol for reading data from the device. Write access to this register is disabled on power-up. To enable write access, configure the REG_ACCESS register.

Figure 62. SDO_CNTL1 Register

7	6	5	4	3	2	1	0
0	OUTDATA_uC_MODE	DATA_RIGHT_ALIGNED	BYTE_INTERLEAVE	0	SDO_WIDTH	SDO_MODE[1:0]	
R-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-00b	

Table 14. SDO_CNTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R	0b	Reserved bit. Do not write. Read returns 0b.
6	OUTDATA_uC_MODE	R/W	0b	Enables the MCU or processor-friendly data interface. 0b = Length of output data is determined by the DATA_OUT_FORMAT field in the DATA_CNTL register. 1b = Length of output data is fixed to 16-bits when the length based on DATA_OUT_FORMAT is ≤ 16 or 32-bits when the length based on DATA_OUT_FORMAT is > 16.
5	DATA_RIGHT_ALIGNED	R/W	0b	This bit is ignored if OUTDATA_uC_MODE = 0b. When OUTDATA_uC_MODE = 1b: 0b = Data frame is left aligned. The SDOs output the device data bits followed by 0s in a 32-bit output frame. 1b = Data frame is right aligned. The SDOs output 0s followed by device data bits in a 32-bit output frame.
4	BYTE_INTERLEAVE	R/W	0b	This bit is ignored if OUTDATA_uC_MODE = 0b or SDO_WIDTH = 0b. When OUTDATA_uC_MODE = 1b and SDO_WIDTH = 1b: 0b = Bit mode. SDO-1 outputs (MSB, MSB - 2 ..., LSB + 1) and SDO-0 outputs (MSB - 1, MSB - 3, ..., LSB). 1b = Byte mode. If the total number of bits to be read from the device is N (conversion result, parity, channel ID, and so forth) then SDO-1 outputs 8 MSB bits and SDO-0 outputs (N-8) bits when N ≤16 and SDO-1 outputs 16 MSB bits and SDO-0 outputs (N-16) bits when 16 < N ≤ 32.
3	0	R	0b	Reserved bit. Do not write. Read returns 0b.
2	SDO_WIDTH	R/W	0b	This bit sets the width of the output bus. 0b = Data bits are output only on SDO-0 1b = Data bits are output on SDO-0 (MSB - 1, MSB - 3 ..., LSB) and SDO-1 (MSB, MSB - 2 ..., LSB + 1)
1-0	SDO_MODE[1:0]	R/W	00b	These bits select the protocol for reading data from the device. 00b = SDO follows the SPI protocol selected in the SDI_CNTL register 01b = Invalid configuration, not supported by the device 10b = Invalid configuration, not supported by the device 11b = SDO follows the *Clock Re-Timer Data Transfer* section

7.6.1.5 SDO_CNTL2 Register (address = 0Dh) [reset = 00h]

This register configures the output data rates, SDR or DDR, when using the clock re-timer data transfer. Write access to this register is disabled on power-up. To enable write access, configure the REG_ACCESS register.

Figure 63. SDO_CNTL2 Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DATA_RATE
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b

Table 15. SDO_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	000 0000	R	000 0000b	Reserved bit. Do not write. Reads return 000 0000b.
0	DATA_RATE	R/W	0b	This bit is ignored if SDO_MODE[1:0] = 0xb. When SDO_MODE[1:0] = 11b: 0b = SDOs are updated at a single data rate (SDR) with respect to the output clock 1b = SDOs are updated at double data rate (DDR) with respect to the output clock

7.6.1.6 SDO_CNTL3 Register (address = 0Eh) [reset = 00h]

The bits in this register are reserved.

Figure 64. SDO_CNTL3 Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 16. SDO_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	0000 0000	R	0000 0000b	Reserved bits. Do not write. Reads return 0000 0000b.

7.6.1.7 SDO_CNTL4 Register (address = 0Fh) [reset = 00h]

This register configures the behaviour of the SEQ_STS pin when not using dual SDO mode (SDO_WIDTH = 0b). Write access to this register is disabled on power-up. To enable write access, configure the REG_ACCESS register.

Figure 65. SDO_CNTL4 Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SEQSTS_CFG
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b

Table 17. SDO_CNTL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	000 0000	R	000 0000b	Reserved bits. Do not write. Reads return 000 0000b.
0	SEQSTS_CFG	R/W	0b	This pin decides the behaviour of SDO-1 when SDO_WIDTH = 0b. 0b = SDO-1 is Hi-Z 1b = SDO-1 indicates the sequence of the active status

7.6.1.8 DATA_CNTL Register (address = 10h) [reset = 00h]

This register configures the contents of the output data word. Write access to this register is disabled on power-up. To enable write access, configure the REG_ACCESS register.

Figure 66. DATA_CNTL Register

7	6	5	4	3	2	1	0
0	0	DATA_OUT_FORMAT[1:0]		0	0	0	DATA_VAL
R-0b	R-0b	R/W-00b		R-0b	R-0b	R-0b	R/W-0b

Table 18. DATA_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	00	R	000b	Reserved bits. Reads return 00b.
5-4	DATA_OUT_FORMAT[1:0]	R/W	00b	These bits control the composition of the output data frame. 00b = ADC conversion result 01b = ADC conversion result + 4-bit channel ID 10b = ADC conversion result + 4-bit channel ID + 4-bit device status (see Table 32) + 2-bit channel configuration 11b = Reserved Parity bits can be appended to the data output frame. See the PARITY_CNTL register for details.
3-1	000	R	000b	Reserved bits. Reads return 00b.
0	DATA_VAL	R/W	0b	Setting this bit enables debug mode for SDO capture. 0b = Normal operation; device data are output on SDO 1b = The device outputs a fixed 1010 0110 patten that is useful for debugging data capture from the device

7.6.1.9 PARITY_CNTL Register (address = 11h) [reset = 00h]

This register enables or disables the computing parity status for the output from the device. Write access to this register is disabled on power-up. To enable write access, configure the REG_ACCESS register.

Figure 67. PARITY_CNTL Register

7	6	5	4	3	2	1	0
0	0	0	0	0	PARITY_EN	0	0
R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b	R-0b	R-0b

Table 19. PARITY_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0 0000	R	0 0000b	Reserved bits. Do not write. Reads return 0 0000b.
2	PARITY_EN	R/W	0b	Enables the parity computation on the data output bits. 0b = Parity disabled 1b = A 1-bit parity is appended to the data output frame. Data length is 1-bit more than the length specified by DATA_OUT_FORMAT in the DATA_CNTL register.
1-0	00	R	00b	Reserved bits. Do not write. Reads return 00b.

7.6.2 Device Calibration Registers

Table 20 maps the device features following register calibration.

Table 20. Calibration Registers Mapping

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION
18h	OFST_CAL	Setting for optimum ADC offset calibration when using an external reference input
19h	REF_MRG1	Margin setting for the reference buffer to compensate for initial accuracy of the reference voltage
1Ah	REF_MRG2	Enable margin setting of the reference buffer as configured in the REF_MRG1 register
1Bh	REFby2_MRG	REFby2 buffer margin configuration

7.6.2.1 OFST_CAL Register (address = 18h) [reset = 00h]

This register selects the optimal offset calibration when using an external reference input. When using an internal reference, do not write to this register. See the *Reference Buffer* section for more details.

Figure 68. OFST_CAL Register

7	6	5	4	3	2	1	0
0	0	0	0	0	REF_SEL[2:0]		
R-0b	R-0b	R-0b	R-0b	R-0b	R/W-000b		

Table 21. OFST_CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R	0 0000b	Reserved bits. Reads return 0 0000b.
2-0	REF_SEL[2:0]	R/W	000b	These bits select the external reference range for optimal offset. 000b = Optimum offset calibration for V_{REF} = 5.0 V 001b = Optimum offset calibration for V_{REF} = 4.5 V 010b = Optimum offset calibration for V_{REF} = 4.096 V 011b = Optimum offset calibration for V_{REF} = 3.3 V 100b = Optimum offset calibration for V_{REF} = 3.0 V 101b = Optimum offset calibration for V_{REF} = 2.5 V 110b = Optimum offset calibration for V_{REF} = 5.0 V 111b = Optimum offset calibration for V_{REF} = 5.0 V

7.6.2.2 REF_MRG1 Register (address = 19h) [reset = 00h]

This register selects the margining to be added to or subtracted from the reference buffer output; see the *Reference Buffer* section.

Figure 69. REF_MRG1 Register

7	6	5	4	3	2	1	0
0	0	0	REF_OFST[4:0]				
R-0b	R-0b	R-0b	R/W-00000b				

Table 22. REF_MRG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R	000b	Reserved bits. Reads return 000b.
4-0	REF_OFST[4:0]	R/W	00000b	These bits select the reference offset value as per Table 23.

Table 23. REF_OFST[4:0] Settings

REF_OFST[4:0]	$\Delta V_{REFBUFOUT}$ (1)	REF_OFST[4:0]	$\Delta V_{REFBUFOUT}$ (1)
00000b	0 mV	10000b	–4.5 mV
00001b	280 µV	10001b	–4.22 mV
00010b	580 µV	10010b	–3.94 mV
00011b	840 µV	10011b	–3.66 mV
00100b	1.12 mV	10100b	–3.38 mV
00101b	1.4 mV	10101b	–3.1 mV
00110b	1.68 mV	10110b	–2.82 mV
00111b	1.96 mV	10111b	–2.54 mV
01000b	2.24 mV	11000b	–2.26 mV
01001b	2.52 mV	11001b	–1.98 mV
01010b	2.8 mV	11010b	–1.70 mV
01011b	3.08 mV	11011b	–1.42 mV
01100b	3.36 mV	11100b	–1.14 mV
01101b	3.64 mV	11101b	–860 µV
01110b	3.92 mV	11110b	–580 µV
01111b	4.2 mV	11111b	–280 µV

(1) The actual $V_{REFBUFOUT}$ value may vary by ±10% from Table 23.

7.6.2.3 REF_MRG2 Register (address = 1Ah) [reset = 00h]

This register enables or disables the reference buffer margin configuration in the REF_MRG1 register.

Figure 70. REF_MRG2 Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EN_MARG
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b

Table 24. REF_MRG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R	000 0000b	Reserved bits. Reads return 000 0000b.
0	EN_MARG	R/W	0b	This bit enables the reference buffer margining feature. 0b = Margining is disabled 1b = Margining is enabled

7.6.2.4 REFby2_MRG Register (address = 1Bh) [reset = 00h]

This register selects the margining to be added to or subtracted from the REFFby2 buffer output; see the *REFby2 Buffer* section.

Figure 71. REFby2_MRG Register

7	6	5	4	3	2	1	0
0	REFby2_OFST[2:0]			0	0	0	EN_REFby2_MARG
R-0b	R/W-000b			R-0b	R-0b	R-0b	R/W-0b

Table 25. REFby2_MRG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R	0b	Reserved bit. Do not write. Reads return 0b.
6-4	REFBY2_OFST[2:0]	R/W	000b	These bits select the REFby2 offset value as per Table 26.
3-1	0	R	000b	Reserved bits. Do not write. Reads return 000b.
0	EN_REFby2_MARG	R/W	0b	This bit enables the REFby2 buffer margining feature. 0b = Margining is disabled 1b = Margining is enabled

Table 26. REFby2_OFST[2:0] Settings

REFby2_OFST[2:0]	V_{REFby2} (1) (V_{REF} = 4.096 V)	V_{REFby2} (1) (V_{REF} = 5 V)
EN_REFby2_MARG = 0b	2.04800 V	2.50000 V
000b	2.12611 V	2.59155 V
001b	2.13008 V	2.59640 V
010b	2.13406 V	2.60124 V
011b	2.13804 V	2.60610 V
100b	2.14203 V	2.61096 V
101b	2.14602 V	2.61581 V
110b	2.14999 V	2.62065 V
111b	2.15397 V	2.62550 V

(1) The actual V_{REFby2} value may vary by ±10% from Table 26.

7.6.3 Analog Input Configuration Registers

Table 27 maps the device features following channel configuration of the registers.

Table 27. Analog Input Configuration Registers Mapping

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION
24h	AIN_CFG	Analog input signal configuration selection
27h	COM_CFG	AIN-COM pin configuration

7.6.3.1 AIN_CFG Register (address = 24h) [reset = 00h]

This register configures the analog inputs as single-ended or pseudo-differential with or without a common input.

Figure 72. AIN_CFG Register

7	6	5	4	3	2	1	0
CH7_CH6_CFG[1:0]		CH5_CH4_CFG[1:0]		CH3_CH2_CFG[1:0]		CH1_CH0_CFG[1:0]	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 28. AIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH1_CH0_CFG[1:0]	R/W	00b	00b = AIN0 and AIN1 are two separate channels. The MUXOUT-M pin is connected to the AIN-COM pin. See the COM_CFG register for selecting single-ended or pseudo-differential operation. 01b = AIN0 and AIN1 are a single-ended pair. AIN0 connects to MUXOUT-P and AIN1 connects to MUXOUT-M. 10b = AIN0 and AIN1 are a pseudo-differential pair. AIN0 connects to MUXOUT-P and AIN1 connects to MUXOUT-M. 11b = Same as 00b
5-4	CH3_CH2_CFG[1:0]	R/W	00b	00b = AIN2 and AIN3 are two separate channels. The MUXOUT-M pin is connected to the AIN-COM pin. See the COM_CFG register for selecting single-ended or pseudo-differential operation. 01b = AIN2 and AIN3 are a single-ended pair. AIN2 connects to MUXOUT-P and AIN3 connects to MUXOUT-M. 10b = AIN2 and AIN3 are a pseudo-differential pair. AIN2 connects to MUXOUT-P and AIN3 connects to MUXOUT-M. 11b = Same as 00b
3-2	CH5_CH4_CFG[1:0]	R/W	00b	00b = AIN4 and AIN5 are two separate channels. The MUXOUT-M pin is connected to the AIN-COM pin. See the COM_CFG register for selecting single-ended or pseudo-differential operation. 01b = AIN4 and AIN5 are a single-ended pair. AIN4 connects to MUXOUT-P and AIN5 connects to MUXOUT-M. 10b = AIN4 and AIN5 are a pseudo-differential pair. AIN4 connects to MUXOUT-P and AIN5 connects to MUXOUT-M. 11b = Same as 00b
1-0	CH7_CH6_CFG[1:0]	R/W	00b	00b = AIN6 and AIN7 are two separate channels. MUXOUT-M pin connected to AIN-COM pin. See the COM_CFG register for selecting single-ended or pseudo-differential operation. 01b = AIN6 and AIN7 are a single-ended pair. AIN6 connects to MUXOUT-P and AIN7 connects to MUXOUT-M. 10b = AIN6 and AIN7 are a pseudo-differential pair. AIN6 connects to MUXOUT-P and AIN7 connects to MUXOUT-M. 11b = Same as 00b

7.6.3.2 COM_CFG Register (address = 27h) [reset = 00h]

This register selects single-ended or pseudo-differential operation for any analog input channels that are not configured as pairs (see the AIN_CFG register). Depending on the contents of this register, AIN-COM must be connected to either GND or REFby2 on the PCB.

Figure 73. COM_CFG Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	COM_CFG
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b

Table 29. COM_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R	000 0000b	Reserved bits. Reads return 000 0000b.
0	COM_CFG	R/W	0b	This bit selects the analog input channel configuration when = 00b or 11b in the AIN_CFG register: 0b = All individual channels are single-ended inputs; connect the AIN-COM pin to GND 1b = All individual channels are pseudo-differential inputs; connect the AIN-COM pin to REFby2

7.6.4 Channel Sequence Configuration Registers Map

Table 30 maps the device features following channel configuration of the registers.

Table 30. Channel Sequence Configuration Registers Mapping

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION
1Ch	DEVICE_CFG	MUX sequence configuration and device status bits
1Dh	CHANNEL_ID	Analog input channel selection in manual mode (see the *Manual Mode* section)
1Eh	SEQ_START	Control for starting the multiplexer sequence
1Fh	SEQ_STOP	Control for aborting the multiplexer sequence
2Ah	ON_THE_FLY_CFG	Enables or disables on-the-fly mode (see the *On-The-Fly Mode* section)
80h	AUTO_SEQ_CFG1	Channel selection register for auto sequence mode (see the *Auto Sequence Mode* section)
82h	AUTO_SEQ_CFG2	Control for repeating the channels in auto sequence mode

7.6.4.1 DEVICE_CFG Register (address = 1Ch) [reset = 00h]

This register selects the mode of channel sequencing and reading this register returns device status information.

Figure 74. DEVICE_CFG Register

7	6	5	4	3	2	1	0
0	0	0	0	ALERT_STATUS	ERROR_STATUS	SEQ_MODE[1:0]	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-00b	

Table 31. DEVICE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R	0000b	Reserved bits. Do not write. Reads return 0000b.
3	ALERT_STATUS	R	0b	Read only. This bit reflects the ALERT pin logic level.
2	ERROR_STATUS	R	0b	Read only. This bit indicates a device configuration error: 0b = No error 1b = Error in configuration
1-0	SEQ_MODE[1:0]	R/W	00b	Sets the MUX channel selection operation: 00b = Manual mode 01b = On-the-fly mode 10b = Auto sequence mode 11b = Custom channel sequencing mode (see the *Custom Channel Sequencing Mode* section)

Table 32 describes how the ALERT_STATUS, ERROR_STATUS, and SEQ_MODE[1:0] bits can be collectively decoded to indicate events.

Table 32. Decoding the DEVICE_CFG Read Value

ALERT_STATUS	ERROR_STATUS	SEQ_MODE[1:0]	EVENT DESCRIPTION
0	0	00	No ALERT, no error, manual mode
0	0	01	No ALERT, no error, on-the-fly mode
0	0	10	No ALERT, no error, auto sequence mode
0	0	11	No ALERT, no error, custom channel sequencing mode
0	1	00	No ALERT, error, manual mode
0	1	01	No ALERT, error, on-the-fly mode
0	1	10	No ALERT, error, auto sequence mode
0	1	11	No ALERT, error, custom channel sequencing mode
1	0	00	ALERT, no error, manual mode
1	0	01	ALERT, no error, on-the-fly mode
1	0	10	ALERT, no error, auto sequence mode
1	0	11	ALERT, no error, custom channel sequencing mode
1	1	00	ALERT, error, manual mode
1	1	01	ALERT, error, on-the-fly mode
1	1	10	ALERT, error, auto sequence mode
1	1	11	ALERT, error, custom channel sequencing mode

7.6.4.2 CHANNEL_ID Register (address = 1Dh) [reset = 00h]

This register selects the analog input channel; see the *Manual Mode* section.

Figure 75. CHANNEL_ID Register

7	6	5	4	3	2	1	0
0	0	0	0	0	CHANNEL_ID[2:0]		
R-0b	R-0b	R-0b	R-0b	R-0b	R/W-000b		

Table 33. CHANNEL_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R	0 0000b	Reserved bits. Reads return 0 0000b.
2-0	CHANNEL_ID[2:0]	R/W	000b	These bits select the analog input channel as per Table 34.

Table 34. Analog Input Channel Selection Settings

CHANNEL_ID[2:0]	ANALOG INPUT SELECTED
000b	AIN0
001b	AIN1
010b	AIN2
011b	AIN3
100b	AIN4
101b	AIN5
110b	AIN6
111b	AIN7

NOTE

Writing to the CHANNEL_ID register when the device is actively operating in auto sequence mode or custom channel sequencing mode aborts the on-going sequence and the DEVICE_CFG register is set to manual mode.

7.6.4.3 SEQ_START Register (address = 1Eh) [reset = 00h]

This register starts the channel selection sequence when in auto sequence mode or custom channel sequencing mode. Writing to this register has no effect when in manual mode or on-the-fly mode.

Figure 76. SEQ_START Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SEQ_START
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	W-0b

Table 35. SEQ_START Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R	0b	Reserved bits. Do not write.
0	SEQ_START	W	0b	This bit starts the channel scanning sequence when SEQ_MODE[1:0] = auto sequence mode or custom channel sequencing mode. 0b = No effect; any on-going sequence is not stopped 1b = Start channel sequence

7.6.4.4 SEQ_ABORT Register (address = 1Fh) [reset = 00h]

This register stops the channel selection sequence when in auto channel sequence mode or custom channel sequencing mode. Writing to this register has no effect when in manual mode or on-the-fly mode.

Figure 77. SEQ_ABORT Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SEQ_ABORT
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	W-0b

Table 36. SEQ_ABORT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R	0b	Reserved bits. Do not write.
0	SEQ_ABORT	W	0b	This bit stops the channel scanning sequence when SEQ_MODE[1:0] = auto sequence mode or custom channel sequencing mode. 0b = No effect 1b = Stop channel sequence

7.6.4.5 ON_THE_FLY_CFG Register (address = 2Ah) [reset = 00h]

This register enables on-the-fly mode of operation. This mode of operation helps select analog input channels without having to write to device configuration registers.

Figure 78. ON_THE_FLY_CFG Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EN_ON_THE_FLY
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b

Table 37. ON_THE_FLY_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R	000 0000b	Reserved bits. Reads return 000 0000b.
0	EN_ON_THE_FLY	R/W	0b	This bit enables on-the-fly mode. 0b = On-the-fly mode disabled 1b = On-the-fly mode enabled; the first five bits on SDI select the analog input channel for next conversion (see Figure 44)

7.6.4.6 AUTO_SEQ_CFG1 Register (address = 80h) [reset = 00h]

This register selects the channels enabled for auto sequence mode.

Figure 79. AUTO_SEQ_CFG1 Register

7	6	5	4	3	2	1	0
EN_AIN7	EN_AIN6	EN_AIN5	EN_AIN4	EN_AIN3	EN_AIN2	EN_AIN1	EN_AIN0
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 38. AUTO_SEQ_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_AIN7	R/W	0b	This bit enables analog input channel 7 in the auto channel sequence mode; see the *Auto Sequence Mode* section. 0b = AIN7 is not enabled in the scanning sequence 1b = AIN7 is enabled in the scanning sequence
6	EN_AIN6	R/W	0b	This bit enables analog input channel 6 in the auto sequence mode. 0b = AIN6 is not enabled in the scanning sequence 1b = AIN6 is enabled in the scanning sequence
5	EN_AIN5	R/W	0b	This bit enables analog input channel 5 in the auto sequence mode. 0b = AIN5 is not enabled in the scanning sequence 1b = AIN5 is enabled in the scanning sequence
4	EN_AIN4	R/W	0b	This bit enables analog input channel 4 in the auto sequence mode. 0b = AIN4 is not enabled in the scanning sequence 1b = AIN4 is enabled in the scanning sequence
3	EN_AIN3	R/W	0b	This bit enables analog input channel 3 in the auto sequence mode. 0b = AIN3 is not enabled in the scanning sequence 1b = AIN3 is enabled in the scanning sequence
2	EN_AIN2	R/W	0b	This bit enables analog input channel 2 in the auto sequence mode. 0b = AIN2 is not enabled in the scanning sequence 1b = AIN2 is enabled in the scanning sequence
1	EN_AIN1	R/W	0b	This bit enables analog input channel 1 in the auto sequence mode. 0b = AIN1 is not enabled in the scanning sequence 1b = AIN1 is enabled in the scanning sequence
0	EN_AIN0	R/W	0b	This bit enables analog input channel 0 in the auto sequence mode. 0b = AIN0 is not enabled in the scanning sequence 1b = AIN0 is enabled in the scanning sequence

7.6.4.7 AUTO_SEQ_CFG2 Register (address = 82h) [reset = 00h]

This register enables the sequence loop for auto sequence mode.

Figure 80. AUTO_SEQ_CFG2 Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	AUTO_REPEAT
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b

Table 39. AUTO_SEQ_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R	000 0000b	Reserved bits. Reads return 000 0000b.
0	AUTO_REPEAT	R/W	0b	This bit enables looping the sequence indefinitely in auto sequence mode. 0b = Sequence terminates after all enabled channels are scanned 1b = Sequence repeats after scanning all enabled channels

7.6.4.8 Custom Channel Sequencing Mode Registers

Table 20 maps the device features for the custom channel sequencing mode registers; see the *Custom Channel Sequencing Mode* section for mode details.

Table 40. Custom Channel Sequencing Registers

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION
88h	CCS_START_INDEX	Start index for the custom channel sequencing mode sequence
89h	CCS_END_INDEX	End index for the custom channel sequencing mode sequence
8Ah	CCS_SEQ_LOOP	Custom channel sequencing mode loop control
8Ch	CCS_CHID_INDEX_0	Channel ID configuration register index 0
8Dh	REPEAT_INDEX_0	Repeat count register index 0
8Eh	CCS_CHID_INDEX_1	Channel ID configuration register index 1
8Fh	REPEAT_INDEX_1	Repeat count register index 1
90h	CCS_CHID_INDEX_2	Channel ID configuration register index 2
91h	REPEAT_INDEX_2	Repeat count register index 2
92h	CCS_CHID_INDEX_3	Channel ID configuration register index 3
93h	REPEAT_INDEX_3	Repeat count register index 3
94h	CCS_CHID_INDEX_4	Channel ID configuration register index 4
95h	REPEAT_INDEX_4	Repeat count register index 4
96h	CCS_CHID_INDEX_5	Channel ID configuration register index 5
97h	REPEAT_INDEX_5	Repeat count register index 5
98h	CCS_CHID_INDEX_6	Channel ID configuration register index 6
99h	REPEAT_INDEX_6	Repeat count register index 6
9Ah	CCS_CHID_INDEX_7	Channel ID configuration register index 7
9Bh	REPEAT_INDEX_7	Repeat count register index 7
9Ch	CCS_CHID_INDEX_8	Channel ID configuration register index 8
9Dh	REPEAT_INDEX_8	Repeat count register index 8
9Eh	CCS_CHID_INDEX_9	Channel ID configuration register index 9
9Fh	REPEAT_INDEX_9	Repeat count register index 9
A0h	CCS_CHID_INDEX_10	Channel ID configuration register index 10
A1h	REPEAT_INDEX_10	Repeat count register index 10
A2h	CCS_CHID_INDEX_11	Channel ID configuration register index 11
A3h	REPEAT_INDEX_11	Repeat count register index 11
A4h	CCS_CHID_INDEX_12	Channel ID configuration register index 12
A5h	REPEAT_INDEX_12	Repeat count register index 12
A6h	CCS_CHID_INDEX_13	Channel ID configuration register index 13
A7h	REPEAT_INDEX_13	Repeat count register index 13
A8h	CCS_CHID_INDEX_14	Channel ID configuration register index 14
A9h	REPEAT_INDEX_14	Repeat count register index 14
AAh	CCS_CHID_INDEX_15	Channel ID configuration register index 15
ABh	REPEAT_INDEX_15	Repeat count register index 15

7.6.4.8.1 CCS_START_INDEX Register (address = 88h) [reset = 00h]

This register sets the relative sequence index where the custom channel sequencing mode starts execution from.

Figure 81. CCS_START_INDEX Register

7	6	5	4	3	2	1	0
0	0	0	0	SEQ_START_INDEX[3:0]			
R-0b	R-0b	R-0b	R-0b	R/W-0000b			

Table 41. CCS_START_INDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R	0000b	Reserved bits. Reads return 0000b.
3-0	SEQ_START_INDEX[3:0]	R/W	0000b	Relative pointer to the index for the start of the sequence in custom channel sequencing mode.

7.6.4.8.2 CCS_END_INDEX Register (address = 89h) [reset = 00h]

This register sets the relative sequence index where the custom channel sequencing mode stops execution at. The value in the CCS_END_INDEX register must not be less than the value in the CCS_START_INDEX register.

Figure 82. CCS_END_INDEX Register

7	6	5	4	3	2	1	0
0	0	0	0	SEQ_END_INDEX[3:0]			
R-0b	R-0b	R-0b	R-0b	R/W-0000b			

Table 42. CCS_END_INDEX Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R	0000b	Reserved bits. Reads return 0000b.
3-0	SEQ_END_INDEX[3:0]	R/W	0000b	Relative pointer to the index for the end of the sequence in custom channel sequencing mode.

7.6.4.8.3 CCS_SEQ_LOOP Register (address = 8Bh) [reset = 00h]

This register controls the looping of the sequence in custom channel sequencing mode.

Figure 83. CCS_SEQ_LOOP Register

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SEQ_LOOP
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b

Table 43. CCS_SEQ_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R	000 0000b	Reserved bits. Reads return 000 0000b.
0	SEQ_LOOP	R/W	0b	Configures the looping of sequence in custom channel sequencing mode. 0b = Sequence ends at the index location configured in the CCS_END_INDEX[3:0] bits; see the CCS_END_INDEX register 1b = Sequence resumes from the CCS_START_INDEX[3:0] bits (see the CCS_START_INDEX register) after executing the CCS_END_INDEX[3:0] bits.

7.6.4.8.4 CCS_CHID_INDEX_m Registers (address = 8C, 8E, 90, 92, 94, 96, 98, 9A, 9C, 9E, A0, A2, A4, A6, A8, and AAh) [reset = 00h]

In custom channel sequencing mode, the intended sequence of the analog input channels can be programmed in these 16 registers. See the REPEAT_INDEX_m registers for details about repeating a particular channel before switching to the next index.

Figure 84. CCS_CHID_INDEX_m Register

7	6	5	4	3	2	1	0
0	0	0	0	0	CHID[2:0]		
R-0b	R-0b	R-0b	R-0b	R-0b	R/W-000b		

Table 44. CCS_CHID_INDEX_m Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R	0 0000b	Reserved bits. Reads return 0 0000b.
2-0	CHID[2:0]	R/W	000b	These bits configure the analog input channel associated with the index in custom channel sequencing mode. 000b = AIN0 001b = AIN1 010b = AIN2 011b = AIN3 100b = AIN4 101b = AIN5 110b = AIN6 111b = AIN7

7.6.4.8.5 REPEAT_INDEX_m Registers (address = 8D, 8F, 91, 93, 95, 97, 99, 9B, 9D, 9F, A1, A3, A5, A7, A9, and ABh) [reset = 00h]

In custom channel sequencing mode, the analog input selected in the corresponding CCS_CHID_INDEX register can be repeated by configuring the respective register.

Figure 85. REPEAT_INDEX_m Register

7	6	5	4	3	2	1	0
REPEAT[7:0]							
R/W-1111 1111b							

Table 45. REPEAT_INDEX_m Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REPEAT[7:0]	R/W	1111 1111b	These bits configure the number of times the analog input configured in the corresponding CCS_CHID_INDEX register is repeated. Configuring 0000 0000b in this register results in an error.

7.6.5 Digital Window Comparator Configuration Registers Map

Table 46 maps the device features for the digital window comparator; see the *Digital Window Comparator* section.

Table 46. Digital Window Comparator Configuration Registers Mapping

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION
2Eh	ALERT_CFG	ALERT enable control for individual analog input channels
31h and 30h	HI_TRIG_AIN7	High threshold input for the AIN7 digital window comparator
35h and 34h	HI_TRIG_AIN6	High threshold input for the AIN6 digital window comparator
39h and 38h	HI_TRIG_AIN5	High threshold input for AIN5 digital window comparator
3Dh and 3Ch	HI_TRIG_AIN4	High threshold input for the AIN4 digital window comparator
41h and 40h	HI_TRIG_AIN3	High threshold input for the AIN3 digital window comparator
45h and 44h	HI_TRIG_AIN2	High threshold input for the AIN2 digital window comparator
49h and 48h	HI_TRIG_AIN1	High threshold input for the AIN1 digital window comparator
4Dh and 4Ch	HI_TRIG_AIN0	High threshold input for the AIN0 digital window comparator
55h and 54h	LO_TRIG_AIN7	Low threshold input for the AIN7 digital window comparator
59h and 58h	LO_TRIG_AIN6	Low threshold input for the AIN6 digital window comparator
5Dh and 5Ch	LO_TRIG_AIN5	Low threshold input for the AIN5 digital window comparator
61h and 60h	LO_TRIG_AIN4	Low threshold input for the AIN4 digital window comparator
65h and 64h	LO_TRIG_AIN3	Low threshold input for the AIN3 digital window comparator
69h and 68h	LO_TRIG_AIN2	Low threshold input for the AIN2 digital window comparator
6Dh and 6Ch	LO_TRIG_AIN1	Low threshold input for the AIN1 digital window comparator
71h and 70h	LO_TRIG_AIN0	Low threshold input for the AIN0 digital window comparator
33h	HYSTERESIS_AIN7	Threshold hysteresis for the AIN7 digital window comparator
37h	HYSTERESIS_AIN6	Threshold hysteresis for the AIN6 digital window comparator
3Bh	HYSTERESIS_AIN5	Threshold hysteresis for the AIN5 digital window comparator
3Fh	HYSTERESIS_AIN4	Threshold hysteresis for the AIN4 digital window comparator
43h	HYSTERESIS_AIN3	Threshold hysteresis for the AIN3 digital window comparator
47h	HYSTERESIS_AIN2	Threshold hysteresis for the AIN2 digital window comparator
4Bh	HYSTERESIS_AIN1	Threshold hysteresis for the AIN1 digital window comparator
4Fh	HYSTERESIS_AIN0	Threshold hysteresis for the AIN0 digital window comparator
78h	ALERT_LO_STATUS	Indicates the analog input channel-wise ALERT resulting from a low threshold
79h	ALERT_HI_STATUS	Indicates the analog input channel-wise ALERT resulting from a high threshold
7Ah	ALERT_STATUS	Indicates the analog input channel-wise ALERT status
7Ch	CURR_ALERT_LO_STATUS	Indicates the analog input channel-wise ALERT resulting from a low threshold for the last conversion data
7Dh	CURR_ALERT_HI_STATUS	Indicates the analog input channel-wise ALERT resulting from a high threshold for the last conversion data
7Eh	CURR_ALERT_STATUS	Indicates the analog input channel-wise ALERT status for the last conversion data

7.6.5.1 ALERT_CFG Register (address = 2Eh) [reset = 00h]

This register enables or disables the digital window comparator for the individual analog input channels.

Figure 86. ALERT_CFG Register

7	6	5	4	3	2	1	0
ALERT_EN_AIN7	ALERT_EN_AIN6	ALERT_EN_AIN5	ALERT_EN_AIN4	ALERT_EN_AIN3	ALERT_EN_AIN2	ALERT_EN_AIN1	ALERT_EN_AIN0
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 47. ALERT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ALERT_EN_AIN7	R/W	0b	Digital window comparator control for AIN7. 0b = Digital window comparator disabled 1b = Digital window comparator enabled
6	ALERT_EN_AIN6	R/W	0b	Digital window comparator control for AIN6. 0b = Digital window comparator disabled 1b = Digital window comparator enabled
5	ALERT_EN_AIN5	R/W	0b	Digital window comparator control for AIN5. 0b = Digital window comparator disabled 1b = Digital window comparator enabled
4	ALERT_EN_AIN4	R/W	0b	Digital window comparator control for AIN4. 0b = Digital window comparator disabled 1b = Digital window comparator enabled
3	ALERT_EN_AIN3	R/W	0b	Digital window comparator control for AIN3. 0b = Digital window comparator disabled 1b = Digital window comparator enabled
2	ALERT_EN_AIN2	R/W	0b	Digital window comparator control for AIN2. 0b = Digital window comparator disabled 1b = Digital window comparator enabled
1	ALERT_EN_AIN1	R/W	0b	Digital window comparator control for AIN1. 0b = Digital window comparator disabled 1b = Digital window comparator enabled
0	ALERT_EN_AIN0	R/W	0b	Digital window comparator control for AIN0. 0b = Digital window comparator disabled 1b = Digital window comparator enabled

When the digital window comparator is disabled, the bits corresponding to the disabled digital window comparator are not updated in the ALERT_STATUS, ALERT_HI_STATUS, ALERT_LO_STATUS, CURR_ALERT_STATUS, CURR_ALERT_HI_STATUS, or CURR_ALERT_LO_STATUS registers.

7.6.5.2 HI_TRIG_AINx[15:0] Register (address = 4Dh to 30h) [reset = 0000h]

This bank of registers configures the high threshold for the digital window comparator. For 16-bit ADC data output, the comparator thresholds are 16-bits wide and are spread over two 8-bit registers. Use the registers listed in Table 48 to configure the high threshold for the individual analog input channels.

Table 48. HI_TRIG_AINx[15:0] Register Address Map(1)

ANALOG INPUT	REGISTER ADDRESS FOR HI_TRIG_AINx[15:8]	REGISTER ADDRESS FOR HI_TRIG_AINx[7:0]
AIN7	031h	030h
AIN6	035h	034h
AIN5	039h	038h
AIN4	03Dh	03Ch
AIN3	041h	040h
AIN2	045h	044h
AIN1	049h	048h
AIN0	04Dh	04Ch

(1) AINx refers to analog inputs channels AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

Figure 87. MSB Byte Register for HI_TRIG_AINx[15:8]

7	6	5	4	3	2	1	0
HI_TRIG[15:8]							
R/W-0000 0000b							

Figure 88. LSB Byte Register for HI_TRIG_AINx[7:0]

7	6	5	4	3	2	1	0
HI_TRIG[7:0]							
R/W-0000 0000b							

Table 49. HI_TRIG_AINx[15:0] Registers Field Descriptions

Bit	Field	Type	Reset	Description
15:0	HI_TRIG[15:0]	R/W	0000 0000 0000 0000b	High threshold for the digital window comparator

7.6.5.3 LO_TRIG_AINx[15:0] Register (address = 71h to 54h) [reset = 0000h]

This bank of registers configures the low threshold for the digital window comparator. For 16-bit ADC data output, the comparator thresholds are 16-bits wide and are spread over two 8-bit registers. Use the registers listed in Table 50 to configure the low threshold for the individual analog input channels

Table 50. LO_TRIG_AINx[15:0] Register Address Map(1)

ANALOG INPUT	REGISTER ADDRESS FOR LO_TRIG_AINx[15:8]	REGISTER ADDRESS FOR LO_TRIG_AINx[7:0]
AIN7	051h	054h
AIN6	059h	058h
AIN5	05Dh	05Ch
AIN4	061h	060h
AIN3	065h	064h
AIN2	069h	068h
AIN1	06Dh	06Ch
AIN0	071h	070h

(1) AINx refers to analog inputs channels AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

Figure 89. MSB Byte Register for LO_TRIG_AINx[15:8]

7	6	5	4	3	2	1	0
LO_TRIG[15:8]							
R/W-0000 0000b							

Figure 90. LSB Byte Register for LO_TRIG_AINx[7:0]

7	6	5	4	3	2	1	0
LO_TRIG[7:0]							
R/W-0000 0000b							

Table 51. LO_TRIG_AINx[15:0] Registers Field Descriptions

Bit	Field	Type	Reset	Description
15:0	LO_TRIG[15:0]	R/W	0000 0000 0000 0000b	Low threshold for the digital window comparator

7.6.5.4 HYSTERESIS_AINx[7:0] Register (address = 4Fh to 33h) [reset = 00h]

This bank of registers configures the hysteresis around the high and low thresholds for the digital window comparator. For 16-bit ADC data output, the hysteresis is six bits wide.

Figure 91. HYSTERESIS_AINx[7:0] Registers

7	6	5	4	3	2	1	0
HYSTERESIS[5:0]						0	0
R/W-00 0000b						R-0b	R-0b

Table 52. HYSTERESIS_AINx[7:0](1) Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	HYSTERESIS[5:0]	R/W	000 0000b	Low threshold for the digital window comparator

(1) AINx refers to analog inputs channels AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

7.6.5.5 ALERT_LO_STATUS Register (address = 78h) [reset = 00h]

This register reflects the status of the ALERT pin resulting from the low thresholds of the respective analog input channels.

Figure 92. ALERT_LO_STATUS Register

7	6	5	4	3	2	1	0
ALERT_LO_AIN7	ALERT_LO_AIN6	ALERT_LO_AIN5	ALERT_LO_AIN4	ALERT_LO_AIN3	ALERT_LO_AIN2	ALERT_LO_AIN1	ALERT_LO_AIN0
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 53. ALERT_LO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ALERT_LO_AIN7	R/W	0b	This bit indicates that the low threshold for AIN7 has been exceeded. 0b = Low threshold is not exceeded 1b = Low threshold has been exceeded; clear this bit by writing 1b
6	ALERT_LO_AIN6	R/W	0b	This bit indicates that the low threshold for AIN6 has been exceeded. 0b = Low threshold is not exceeded 1b = Low threshold has been exceeded; clear this bit by writing 1b
5	ALERT_LO_AIN5	R/W	0b	This bit indicates that the low threshold for AIN5 has been exceeded. 0b = Low threshold is not exceeded 1b = Low threshold has been exceeded; clear this bit by writing 1b
4	ALERT_LO_AIN4	R/W	0b	This bit indicates that the low threshold for AIN4 has been exceeded. 0b = Low threshold is not exceeded 1b = Low threshold has been exceeded; clear this bit by writing 1b
3	ALERT_LO_AIN3	R/W	0b	This bit indicates that the low threshold for AIN3 has been exceeded. 0b = Low threshold is not exceeded 1b = Low threshold has been exceeded; clear this bit by writing 1b
2	ALERT_LO_AIN2	R/W	0b	This bit indicates that the low threshold for AIN2 has been exceeded. 0b = Low threshold is not exceeded 1b = Low threshold has been exceeded; clear this bit by writing 1b
1	ALERT_LO_AIN1	R/W	0b	This bit indicates that the low threshold for AIN1 has been exceeded. 0b = Low threshold is not exceeded 1b = Low threshold has been exceeded; clear this bit by writing 1b
0	ALERT_LO_AIN0	R/W	0b	This bit indicates that the low threshold for AIN0 has been exceeded. 0b = Low threshold is not exceeded 1b = Low threshold has been exceeded; clear this bit by writing 1b

7.6.5.6 ALERT_HI_STATUS Register (address = 79h) [reset = 00h]

This register reflects the status of the ALERT pin resulting from the high thresholds of the respective analog input channels.

Figure 93. ALERT_HI_STATUS Register

7	6	5	4	3	2	1	0
ALERT_HI_AIN7	ALERT_HI_AIN6	ALERT_HI_AIN5	ALERT_HI_AIN4	ALERT_HI_AIN3	ALERT_HI_AIN2	ALERT_HI_AIN1	ALERT_HI_AIN0
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 54. ALERT_HI_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ALERT_HI_AIN7	R/W	0b	This bit indicates that the high threshold for AIN7 has been exceeded. 0b = High threshold is not exceeded 1b = High threshold has been exceeded; clear this bit by writing 1b
6	ALERT_HI_AIN6	R/W	0b	This bit indicates that the high threshold for AIN6 has been exceeded. 0b = High threshold is not exceeded 1b = High threshold has been exceeded; clear this bit by writing 1b
5	ALERT_HI_AIN5	R/W	0b	This bit indicates that the high threshold for AIN5 has been exceeded. 0b = High threshold is not exceeded 1b = High threshold has been exceeded; clear this bit by writing 1b
4	ALERT_HI_AIN4	R/W	0b	This bit indicates that the high threshold for AIN4 has been exceeded. 0b = High threshold is not exceeded 1b = High threshold has been exceeded; clear this bit by writing 1b
3	ALERT_HI_AIN3	R/W	0b	This bit indicates that the high threshold for AIN3 has been exceeded. 0b = High threshold is not exceeded 1b = High threshold has been exceeded; clear this bit by writing 1b
2	ALERT_HI_AIN2	R/W	0b	This bit indicates that the high threshold for AIN2 has been exceeded. 0b = High threshold is not exceeded 1b = High threshold has been exceeded; clear this bit by writing 1b
1	ALERT_HI_AIN1	R/W	0b	This bit indicates that the high threshold for AIN1 has been exceeded. 0b = High threshold is not exceeded 1b = High threshold has been exceeded; clear this bit by writing 1b
0	ALERT_HI_AIN0	R/W	0b	This bit indicates that the high threshold for AIN0 has been exceeded. 0b = High threshold is not exceeded 1b = High threshold has been exceeded; clear this bit by writing 1b

7.6.5.7 ALERT_STATUS Register (address = 7Ah) [reset = 00h]

This register reflects the ALERT status for the analog input channels.

Figure 94. ALERT_STATUS Register

7	6	5	4	3	2	1	0
ALERT_AIN7	ALERT_AIN6	ALERT_AIN5	ALERT_AIN4	ALERT_AIN3	ALERT_AIN2	ALERT_AIN1	ALERT_AIN0
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 55. ALERT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ALERT_AIN7	R	0b	This bit indicates if either the high or low threshold for AIN7 has been exceeded. 0b = Neither the high are low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
6	ALERT_AIN6	R	0b	This bit indicates if either the high or low threshold for AIN6 has been exceeded. 0b = Neither the high are low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
5	ALERT_AIN5	R	0b	This bit indicates if either the high or low threshold for AIN5 has been exceeded. 0b = Neither the high are low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
4	ALERT_AIN4	R	0b	This bit indicates if either the high or low threshold for AIN4 has been exceeded. 0b = Neither the high are low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
3	ALERT_AIN3	R	0b	This bit indicates if either the high or low threshold for AIN3 has been exceeded. 0b = Neither the high are low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
2	ALERT_AIN2	R	0b	This bit indicates if either the high or low threshold for AIN2 has been exceeded. 0b = Neither the high are low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
1	ALERT_AIN1	R	0b	This bit indicates if either the high or low threshold for AIN1 has been exceeded. 0b = Neither the high are low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
0	ALERT_AIN0	R	0b	This bit indicates if either the high or low threshold for AIN0 has been exceeded. 0b = Neither the high are low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded

If the ALERT bit for a particular channel is set in the ALERT_STATUS register, then the ALERT bit can be cleared by writing 1b to the corresponding bit in the ALERT_HI_STATUS or ALERT_LO_STATUS registers. If both the high and low thresholds have been exceeded for a particular analog input channel, then the corresponding ALERT bit in both the ALERT_HI_STATUS or ALERT_LO_STATUS registers must be set to 1b to clear the ALERT bit.

7.6.5.8 CURR_ALERT_LO_STATUS Register (address = 7Ch) [reset = 00h]

This register reflects the low threshold ALERT status for the analog input channels. The bits in this register are updated after every conversion.

Figure 95. CURR_ALERT_LO_STATUS Register

7	6	5	4	3	2	1	0
ALERT_LO_AIN7	ALERT_LO_AIN6	ALERT_LO_AIN5	ALERT_LO_AIN4	ALERT_LO_AIN3	ALERT_LO_AIN2	ALERT_LO_AIN1	ALERT_LO_AIN0
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 56. CURR_ALERT_LO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ALERT_LO_AIN7	R	0b	This bit indicates if the low threshold for AIN7 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = Low threshold has been exceeded
6	ALERT_LO_AIN6	R	0b	This bit indicates if the low threshold for AIN6 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = Low threshold has been exceeded
5	ALERT_LO_AIN5	R	0b	This bit indicates if the low threshold for AIN5 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = Low threshold has been exceeded
4	ALERT_LO_AIN4	R	0b	This bit indicates if the low threshold for AIN4 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = Low threshold has been exceeded
3	ALERT_LO_AIN3	R	0b	This bit indicates if the low threshold for AIN3 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = Low threshold has been exceeded
2	ALERT_LO_AIN2	R	0b	This bit indicates if the low threshold for AIN2 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = Low threshold has been exceeded
1	ALERT_LO_AIN1	R	0b	This bit indicates if the low threshold for AIN1 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = Low threshold has been exceeded
0	ALERT_LO_AIN0	R	0b	This bit indicates if the low threshold for AIN0 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = Low threshold has been exceeded

The status of the individual bits in this register is evaluated after every conversion. The contents of this register can be used to ascertain if the last output data are within the specified high threshold for the respective analog input channels.

7.6.5.9 CURR_ALERT_HI_STATUS Register (address = 7Dh) [reset = 00h]

This register reflects the high threshold ALERT status for the analog input channels. The bits in this register are updated after every conversion.

Figure 96. CURR_ALERT_HI_STATUS Register

7	6	5	4	3	2	1	0
ALERT_HI_AIN7	ALERT_HI_AIN6	ALERT_HI_AIN5	ALERT_HI_AIN4	ALERT_HI_AIN3	ALERT_HI_AIN2	ALERT_HI_AIN1	ALERT_HI_AIN0
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 57. CURR_ALERT_HI_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ALERT_HI_AIN7	R	0b	This bit indicates if the high threshold for AIN7 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = High threshold has been exceeded
6	ALERT_HI_AIN6	R	0b	This bit indicates if the high threshold for AIN6 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = High threshold has been exceeded
5	ALERT_HI_AIN5	R	0b	This bit indicates if the high threshold for AIN5 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = High threshold has been exceeded
4	ALERT_HI_AIN4	R	0b	This bit indicates if the high threshold for AIN4 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = High threshold has been exceeded
3	ALERT_HI_AIN3	R	0b	This bit indicates if the high threshold for AIN3 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = High threshold has been exceeded
2	ALERT_HI_AIN2	R	0b	This bit indicates if the high threshold for AIN2 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = High threshold has been exceeded
1	ALERT_HI_AIN1	R	0b	This bit indicates if the high threshold for AIN1 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = High threshold has been exceeded
0	ALERT_HI_AIN0	R	0b	This bit indicates if the high threshold for AIN0 has been exceeded by the last converted data from channel AIN7. 0b = High threshold is not exceeded 1b = High threshold has been exceeded

The status of the individual bits in this register is evaluated after every conversion. The contents of this register can be used to ascertain if the last output data are within the specified high threshold for the respective analog input channels.

7.6.5.10 CURR_ALERT_STATUS Register (address = 7Eh) [reset = 00h]

This register reflects the ALERT pin status for the analog input channels. The bits in this register are updated after every conversion.

Figure 97. CURR_ALERT_STATUS Register

7	6	5	4	3	2	1	0
ALERT_AIN7	ALERT_AIN6	ALERT_AIN5	ALERT_AIN4	ALERT_AIN3	ALERT_AIN2	ALERT_AIN1	ALERT_AIN0
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 58. CURR_ALERT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ALERT_AIN7	R	0b	This bit indicates that either the high or low threshold for AIN7 has been exceeded by the last converted data from channel AIN7. 0b = Neither the high or low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
6	ALERT_AIN6	R	0b	This bit indicates that either the high or low threshold for AIN6 has been exceeded by the last converted data from channel AIN7. 0b = Neither the high or low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
5	ALERT_AIN5	R	0b	This bit indicates that either the high or low threshold for AIN5 has been exceeded by the last converted data from channel AIN7. 0b = Neither the high or low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
4	ALERT_AIN4	R	0b	This bit indicates that either the high or low threshold for AIN4 has been exceeded by the last converted data from channel AIN7. 0b = Neither the high or low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
3	ALERT_AIN3	R	0b	This bit indicates that either the high or low threshold for AIN3 has been exceeded by the last converted data from channel AIN7. 0b = Neither the high or low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
2	ALERT_AIN2	R	0b	This bit indicates that either the high or low threshold for AIN2 has been exceeded by the last converted data from channel AIN7. 0b = Neither the high or low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
1	ALERT_AIN1	R	0b	This bit indicates that either the high or low threshold for AIN1 has been exceeded by the last converted data from channel AIN7. 0b = Neither the high or low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded
0	ALERT_AIN0	R	0b	This bit indicates that either the high or low threshold for AIN0 has been exceeded by the last converted data from channel AIN7. 0b = Neither the high or low threshold have been exceeded 1b = Either the high threshold, the low threshold, or both thresholds have been exceeded

Bits in this register reflect the result of the logical OR of the corresponding channel bits in the CURR_ALERT_HI_STATUS and CURR_ALERT_LO_STATUS registers. The status of the individual bits in this register is evaluated after every conversion. The contents of this register can be used to ascertain if the last output data are within the specified high and low thresholds for the respective analog input channels.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Multiplexer Input Connection

Conventional multichannel ADC solutions internally connect the multiplexer output directly to the switched capacitor input of the ADC. Conventionally, a wide bandwidth amplifier is required for each channel. For the ADS816x, only one amplifier is required for many applications. The ADS816x solution shown in Figure 98 has lower power, a smaller PCB area, and lower cost compared to the comparative solution. Furthermore, from a calibration perspective, the offset error in the ADS816x solution is the same in each channel and is set by the multiplexer output amplifier. The offset error in the conventional solution, on the other hand, is different for each channel. Calibrating the offset error for the conventional solution also requires a separate calibration for each channel.

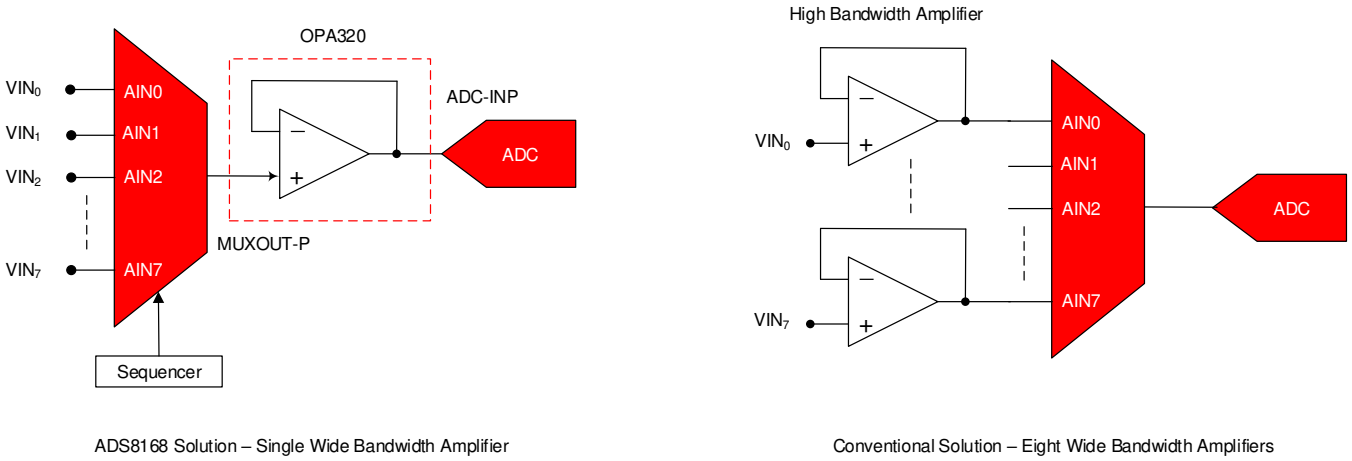


Figure 98. Small-Size and Low-Power 8-Channel DAQ System Using the ADS816x

When connecting the sensor directly to the input of the ADS816x, the maximum switching speed of the multiplexer is limited by multiplexer on-resistance and parasitic capacitance. Figure 99 illustrates the source resistance (R_{S0}, R_{S1}…), multiplexer impedance (R_{MUX}), multiplexer capacitance (C_{MUX}), op amp input capacitance (C_{OPA}), and the stray PCB capacitance at the output of the multiplexer (C_{STRAY}). In this example, the total output capacitance is the combination of the multiplexer output capacitance, the op amp input capacitance, and the stray capacitance ($C_{MUX} + C_{OPA} + C_{STRAY}$) = 15 pF. When switching to a channel, this capacitance must be charged to the sensor output voltage via the source resistance and the multiplexer resistance ($R_{S0} + R_{MUX}$).

Equation 2 can be used to estimate the number of time constants required for N bits of settling. For this example, to achieve 16-bit settling, 11.09 time constants are required. Thus, as computed in Equation 3 and Equation 4, for channel 0 the required settling time is 167 ns.

$$N_{TC} = \ln(2^{16}) = 11.09 \quad (2)$$

$$\text{Settling Time Required} = (R_{S0} + R_{MUX}) \times (C_{MUX} + C_{OPA} + C_{STRAY}) \times N_{TC} \quad (3)$$

$$\text{Settling Time Required} = (1\ \text{k}\Omega) \times (15\ \text{pF}) \times 11.09 = 167\ \text{ns} \quad (4)$$

Application Information (continued)

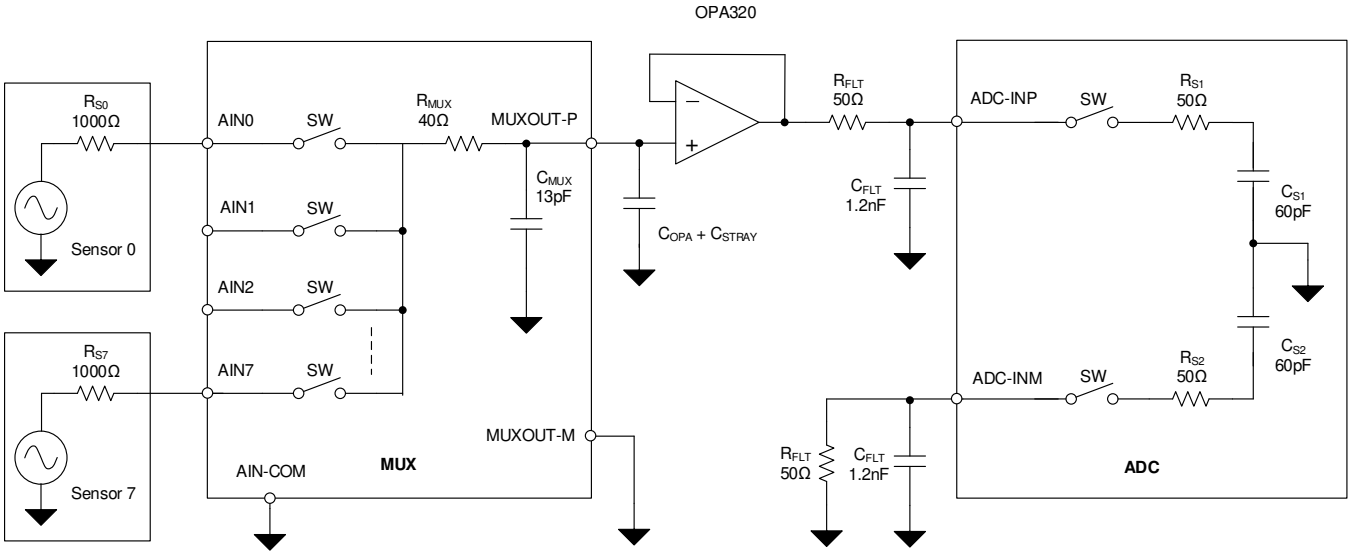


Figure 99. Direct Sensor Interface With the ADS816x in an 8-Channel, Single-Ended Configuration

When operating at 1 MSPS in either manual mode, auto sequence mode, or custom channel sequencing mode, a 900-ns settling time is available at the analog inputs of the multiplexer; see the *Early Switching for Direct Sensor Interface* section. Using Equation 4, the maximum sensor output impedance for a direct connection is 5.4 kΩ.

In some applications, such as temperature sensing, the sensor output impedance can be greater than 10 kΩ. When scanning the multiplexer channels at high throughput, the relatively higher driving impedance results in a settling error. In such cases, Figure 100 shows that the multiplexer inputs can be driven using an amplifier. The multiplexer outputs can be connected to the ADC inputs directly. For best distortion performance, an amplifier can be used between the multiplexer and the ADC as described in the *Selecting an ADC Input Buffer* section.

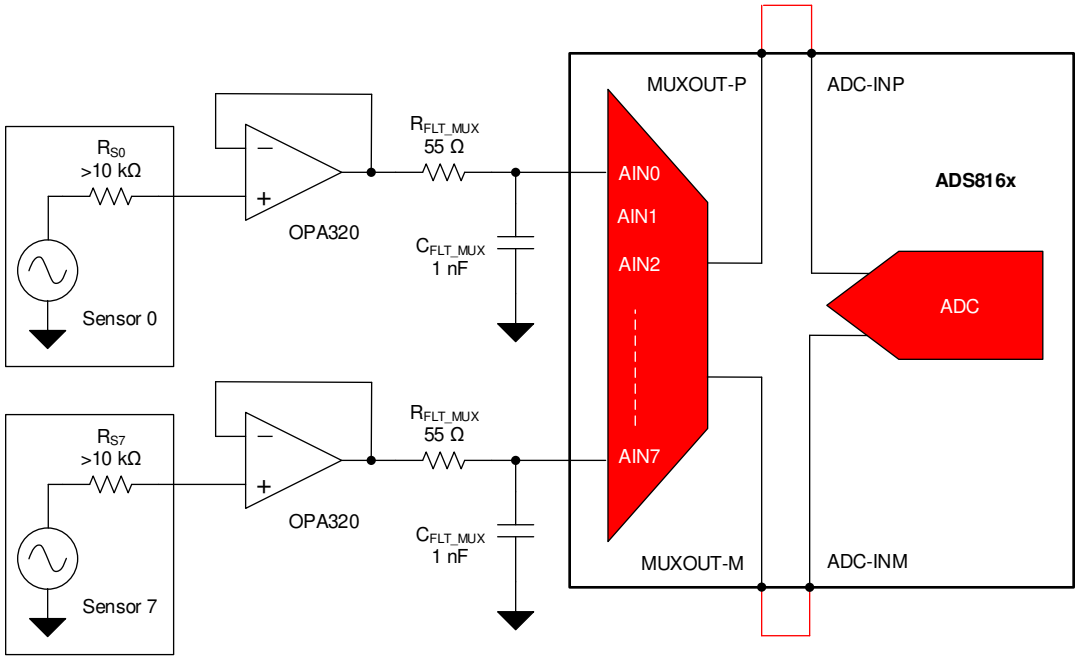


Figure 100. High Output Impedance Sensor Interface

Application Information (continued)

8.1.2 Selecting an ADC Input Buffer

Figure 101 shows the external amplifier, charge bucket filter, and sample-and-hold circuit at the ADC input for the ADS816x. Having a short background on the conversion process helps to understand the design procedure for selecting the amplifier and RC filter. The conversion process is broken up into two phases: the acquisition phase and the conversion phase. During the acquisition phase the SW switches are closed, and the input signal is stored on the sample-and-hold capacitors, C_{S1} and C_{S2}. After the acquisition phase, the switches opens and the voltage stored on the capacitors is converted to a digital code by the SAR algorithm. This conversion process depletes the charge on the sample-and-hold capacitors.

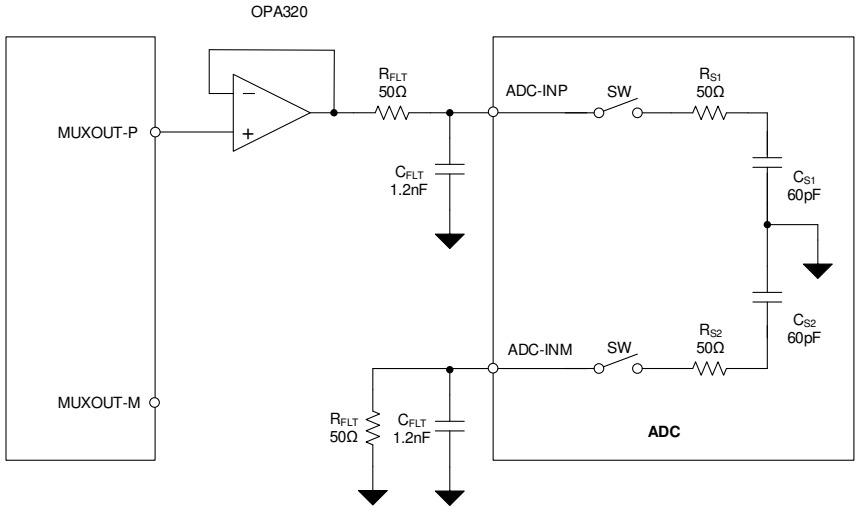


Figure 101. Driving the ADC Inputs (ADC-INP and ADC-INM)

During subsequent acquisition cycles, the sample-and-hold capacitor must be charged to the ADC input voltage that can make step changes in the value because each input may be from a different multiplexer channel. For example, if AIN0 is connected to 4 V and AIN1 is connected to 0.5 V, the sample-and-hold capacitor must charge to 4 V for the first acquisition cycle and then must charge to 0.5 V for the second acquisition cycle. When running at high throughput, the acquisition time is small and a wide bandwidth amplifier is required for proper settling at the ADC inputs (minimum acquisition time for the ADS816x is t_{ACQ} = 330 ns). The RC filter (R_{FLT} and C_{FLT}) is designed to provide a reservoir of charge that helps rapidly charge the internal sample-and-hold capacitor at the start of the acquisition period. For this reason, the RC filter is sometimes called a *charge bucket* or *charge kickback* filter. A method for determining the required amplifier bandwidth and the values of the RC charge bucket filter is provided in this section.

A summary of the equations and an example calculation is provided to determine the amplifier bandwidth and RC charge bucket circuit for the ADS816x assuming a minimum ADC acquisition time is used. Equation 5 finds the amplifier time constant and Equation 6 uses this to computer the amplifiers required unity-gain bandwidth.

$$\tau_{AMP} = \frac{\tau_C}{\sqrt{17}} = \frac{40.9\text{ns}}{\sqrt{17}} = 9.917\text{ns} \tag{5}$$

$$\text{UGBW} = \frac{1}{2\pi \times \tau_{AMP}} = \frac{1}{2\pi \times (9.917\text{ns})} = 16\text{MHz} \tag{6}$$

Equation 7, Equation 8, and Equation 9 calculate C_{SH}, the LSB value, and τ_C, respectively.

$$C_{SH} = 60\text{pF}, t_{ACQ} = 330\text{ns}, N = 16\text{bits}, V_{REF} = 4.096\text{V} \tag{7}$$

$$\text{LSB} = \frac{V_{REF}}{2^N} = \frac{4.096\text{V}}{2^{16}} = 62.5\mu\text{V} \tag{8}$$

$$\tau_C = \frac{-t_{ACQ}}{\ln\left(\frac{0.5 \times \text{LSB}}{100\text{mV}}\right)} = \frac{-330\text{ns}}{\ln\left(\frac{0.5 \times (62.5\mu\text{V})}{100\text{mV}}\right)} = 40.9\text{ns} \tag{9}$$

Application Information (continued)

The value of C_{FLT} is computed in Equation 10 by taking 20 times the internal sample-and-hold capacitance. The factor of 20 is a rule of thumb that is intended to minimize the droop in voltage on the charge bucket capacitor, C_{FLT}, after the start of the acquisition period. The filter resistor, R_{FLT}, is computed in Equation 11 using the op amp time constant and C_{FLT}. These equations model the system as a first-order system, but in reality the system is a higher order. Consequently, the values may need to be adjusted to optimize performance. This optimization and more details on the math behind the component selection are covered in the ADC Precision Labs training videos.

$$C_{FLT} = 20 \times C_{FLT} = 20 \times (60pF) = 1.2nF \tag{10}$$

$$R_{FLT} = \frac{4 \times \tau_{AMP}}{C_{FLT}} = \frac{4 \times (9.917ns)}{1.2nF} = 33.05\Omega \tag{11}$$

8.2 Typical Applications

8.2.1 1-MSPS DAQ Circuit With Lowest Distortion and Noise Performance

Figure 102 shows an 8-channel and 1-MSPS solution with minimum external components. This solution significantly reduces solution size and power by not requiring amplifiers on every analog input.

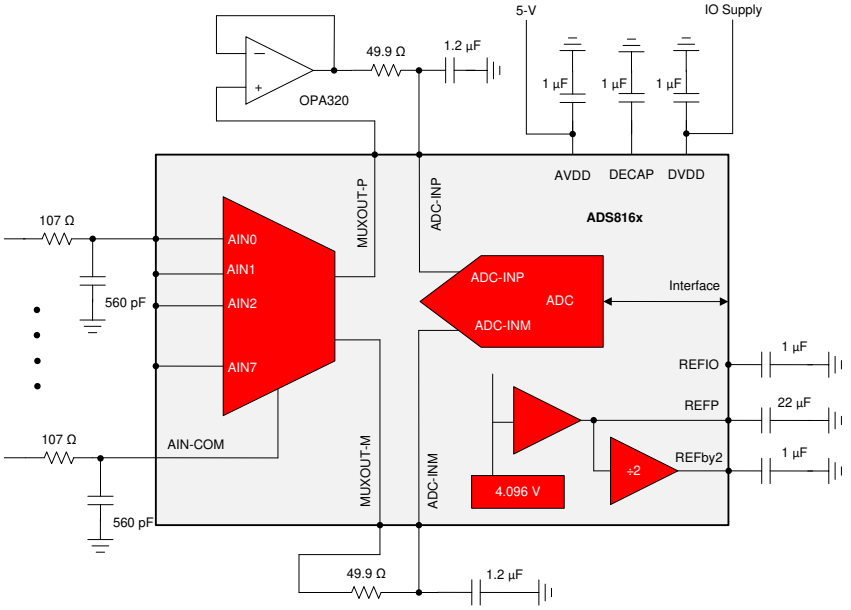


Figure 102. 1-MSPS DAQ Circuit With Lowest Distortion and Noise Performance

8.2.1.1 Design Requirements

Table 59 lists the design parameters for this example.

Table 59. Design Parameters

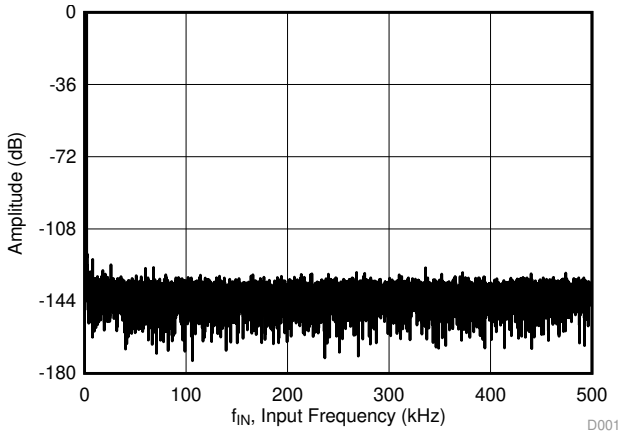
DESIGN PARAMETER	EXAMPLE VALUE
SNR	≥ 92 dB
THD	≤ –108 dB
Throughput	1 MSPS
Input signal frequency	≤100 kSPS

8.2.1.2 Detailed Design Procedure

The procedure discussed in this section can be used for any ADS816x application circuit. See the *Example Schematic* section for the final design for this example.

- All ADS816x applications require the supply and reference decoupling as given in the *Example Schematic* and *Layout* sections.
- Select the buffer amplifier and associated charge bucket filter between the multiplexer output and the ADC input using the method described in the *Selecting an ADC Input Buffer* section. The values given in this section meet the maximum throughput and input signal frequency design requirements given. A lower bandwidth solution can be used in cases where lower power is required.
- Select an input amplifier for rapid settling when the multiplexer switches channels. This selection is covered in the *Multiplexer Input Connection* section. The OPA320 buffer and associated RC filter illustrated in Figure 100 meet these requirements.

8.2.1.3 Application Curve



f_{IN} = 2 kHz, SNR = 92 dB, THD = –109 dB

Figure 103. FFT Plot: ADS8168

8.2.2 8-Channel Photodiode Detector With Smallest Size and Lowest Number of Components

The circuit in Figure 104 shows an 8-channel photodiode detector using the ADS816x. In this example, one common amplifier is used for eight photodiodes. See the *1 MHz, Single-Supply, Photodiode Amplifier Reference Design* reference guide for a detailed description of the transimpedance amplifier.

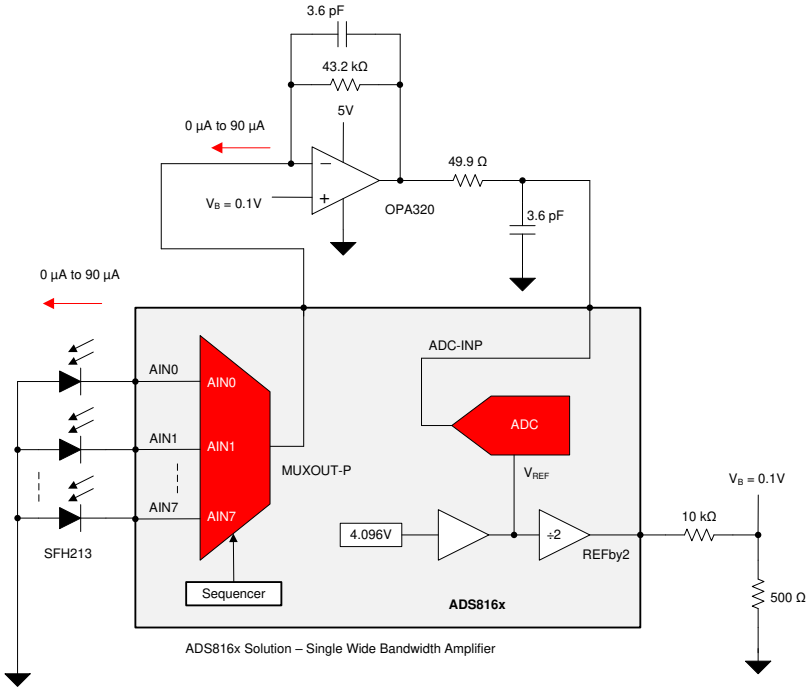


Figure 104. Small Size, 8-Channel Photodetector

8.2.2.1 Design Requirements

The objective of this design is to achieve:

- Smallest solution size
- Transimpedance output of 0.1 V to 4 V for a 0-µA to 90-µA input with a bandwidth of 1 MHz
- The voltage divider is designed to provide a minimum amplifier output of 0.1 V when the photodiode current is zero (dark current) to prevent the amplifier from saturating to the negative rail

8.2.2.2 Detailed Design Procedure

In Figure 104, the photodiodes are connected to the multiplexer input in photovoltaic mode. Depending on the application requirements, either photovoltaic mode or photoconductive mode can be used. The multiplexer in the ADS816x is used as a current multiplexer in this example. One common amplifier for all photodiodes reduces cost, complexity, PCB area, and power consumption. This common amplifier also simplifies system calibration because the gain and offset error are the same for all channels. Finally, the low leakage current of the multiplexer is ideal for photodiode applications.

The OPA320 is used as a transimpedance amplifier that can also drive the ADC inputs. In order to set the output voltage of the OPA320 to 0.1 V in dark conditions, an equivalent bias voltage (V_B) is applied at the noninverting terminal. Equation 12 shows that this bias voltage is derived using a resistive voltage divider on the REFby2 output (2.048V).

$$V_B = (V_{REFby2}V) \times \left(\frac{500\Omega}{10k\Omega + 500\Omega} \right) = 97.5mV \quad (12)$$

Equation 13 shows that the feedback resistor for the transimpedance amplifier can be selected by designing for a 4-V output for a 90-µA input.

$$R_F = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{I_{IN\_MAX}} = \frac{4V - 0.1V}{90\mu A} = 43.3k\Omega \quad (13)$$

Equation 14 computes the value of the feedback capacitance to limit the bandwidth of the transimpedance circuit to 1 MHz.

$$C_F = \frac{1}{2\pi \times f_C \times R_F} = \frac{1}{2\pi \times (1MHz) \times (43.3k\Omega)} = 3.6pF \quad (14)$$

Transimpedance amplifiers can have potential stability concerns. Stability is a function of the feedback capacitance, the capacitance on the inverting input of the amplifier, and the amplifier gain bandwidth. In this case the capacitance on the inverting amplifier input (C_{IN}, as calculated by Equation 15 and Equation 16) includes the photodiode junction capacitance (C_J), the multiplexer capacitance (C_{MUX}), the trace capacitance, and the op amp input differential (C_D) and common-mode (C_{CM2}) capacitances. Equation 17 and Equation 18 compute the minimum gain bandwidth of the amplifier for stability for a given C_{IN}. The minimum required gain bandwidth is 10.9 MHz and the gain bandwidth for the OPA320 is 20 MHz, so the stability test passes.

$$C_{IN} = C_J + C_D + C_{CM2} + C_{MUX} \quad (15)$$

$$C_{IN} = 11pF + 5pF + 4pF + 15pF = 35pF \quad (16)$$

$$F_{GBW} > \frac{C_{IN} + C_F}{2\pi \times R_F \times (C_F)^2} \quad (17)$$

$$F_{GBW} > \frac{35pF + 3.6pF}{2\pi \times 43.3k\Omega \times (3.6pF)^2} = 10.9MHz \quad (18)$$

8.2.3 1-MSPS DAQ Circuit for Factory Automation

The circuit in Figure 105 shows an example of how the ADS816x can be used for a factory automation application.

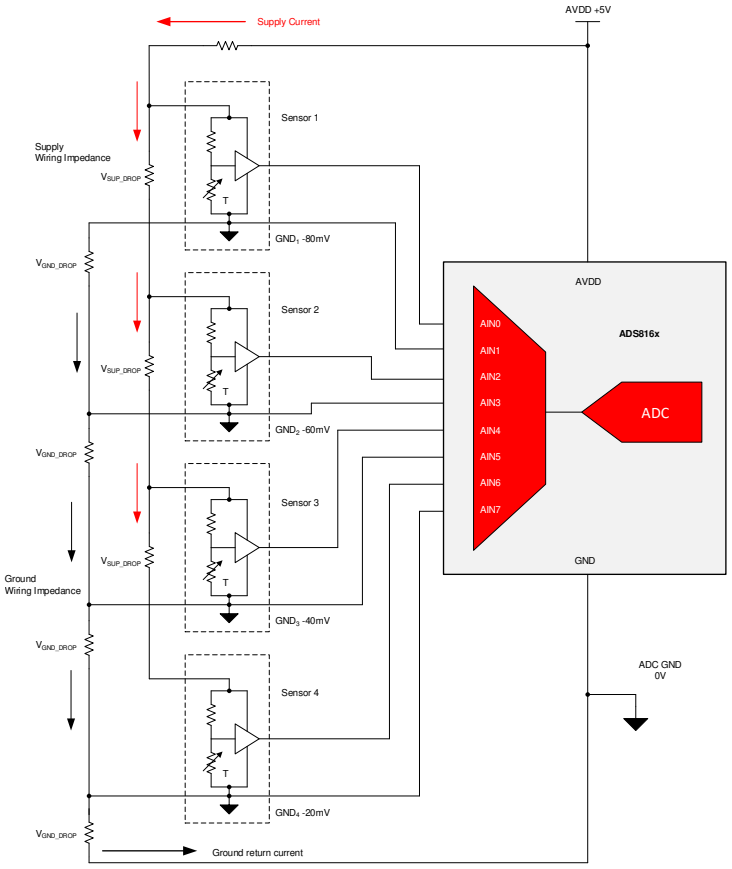


Figure 105. Remote Ground Sense With the ADS816x in Factory Automation

8.2.3.1 Design Requirements

The goal of this design to sense outputs from four sensors, with each sensor being at a different ground potential.

8.2.3.2 Detailed Design Procedure

In Figure 105, the sensors are connected over long leads to the supply, ground, and ADC inputs. Voltage drop resulting from ground wiring impedance causes the ground connections to be at different potentials for each sensor. The ADS816x can be configured into four single-ended pairs with a remote ground sense; see the *Multiplexer Configurations* section. In this input configuration, the error in ground potential is sensed and accounted for in the measurement.

The ADC negative input can sense ground voltages of ±100 mV. The ADC has digital window comparators that can be programed to set an alarm if the sensor output is out of range. Many industrial applications require isolation. When scanning all the channels at 1 MSPS, the serial clock rate can be as low as 16 MHz. This clock rate is suitable for most isolators. Using a common amplifier to drive the ADC input simplifies calibration because all channels have a common error.

9 Power Supply Recommendations

The ADS816x has two separate power supplies: AVDD and DVDD. The internal reference, reference buffer, multiplexer, and the internal LDO operate on AVDD. The ADC core operates on the LDO output (available on the DECAP pin). DVDD is used for setting the logic levels on the digital interface. AVDD and DVDD can be independently set to any value within their permissible ranges. During normal operation, if any voltage on the AVDD supply drops below the AVDD minimum specification, then the AVDD supply is recommended to be ramped down to ≤ 0.7 V before power-up. Also during power-up, AVDD must monotonously rise to the desired operating voltage above the minimum AVDD specification.

When using an internal reference, set AVDD so that 4.5 V ≤ AVDD ≤ 5.5 V.

The AVDD supply voltage value defines the permissible range for the external reference voltage, V_{REF}, on the REFIO pin. To use the external reference voltage (V_{REF}), set AVDD such that 3 V ≤ AVDD ≤ (AVDD + 0.3) V.

As shown in Figure 106, place a minimum 1-µF decoupling capacitor between the AVDD and GND pins and between the DVDD and GND pins. Use a minimum 1-µF decoupling capacitor between the DECAP and GND pins.

There are no specific requirements with regard to the power-supply sequencing of the device. However, issue a reset after the supplies are powered and stable to ensure the device is properly configured.

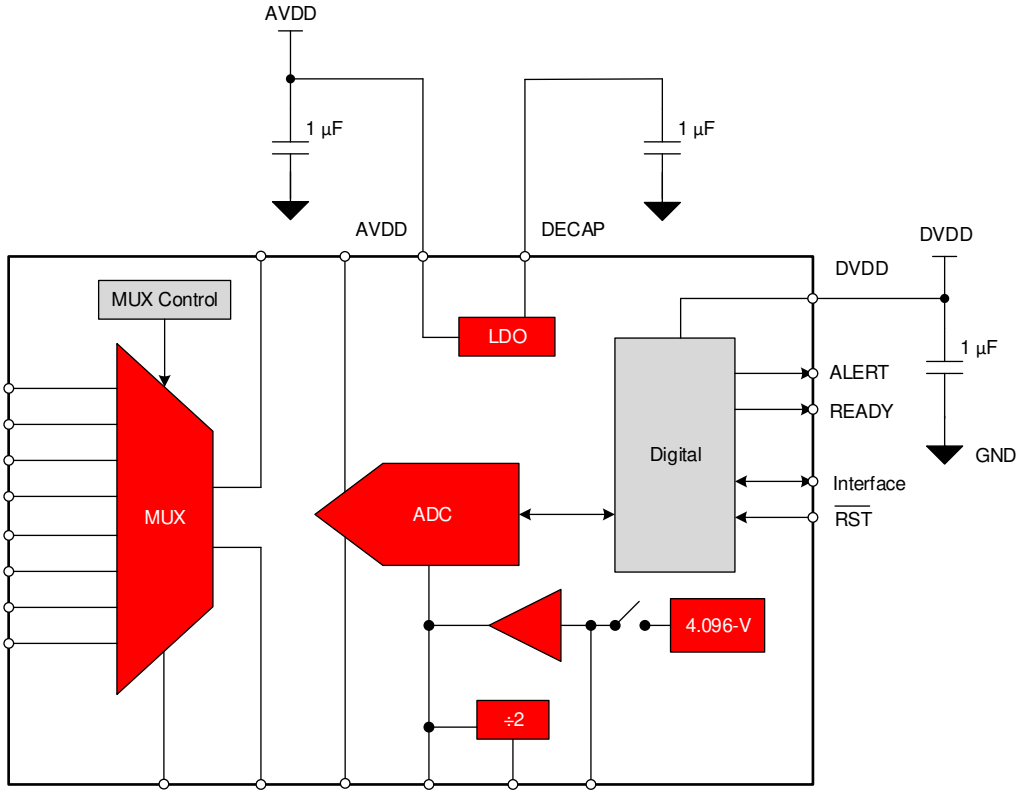


Figure 106. Power-Supply Decoupling

10 Layout

10.1 Layout Guidelines

This section provides some layout guidelines for achieving optimum performance with the ADS816x.

10.1.1 Analog Signal Path

As illustrated in Figure 108, the analog input signals are routed in opposite directions to the digital connections. The reference decoupling components are kept away from the switching digital signals. This arrangement prevents noise generated by digital switching activity from coupling to sensitive analog signals.

10.1.2 Grounding and PCB Stack-Up

Low inductance grounding is critical for achieving optimum performance. Place all critical components of the signal chain on the same PCB layer as the ADS816x.

For lowest inductance grounding, connect the GND pins of the ADS816x (pins 1, 21, and 31) and reference ground REFM (pin 4) directly to the device thermal pad. Connect the device thermal pad to the PCB ground using four vias; see Figure 108.

10.1.3 Decoupling of Power Supplies

Use wide traces or a dedicated power-supply plane to minimize trace inductance. Place 1-µF, X7R-grade, ceramic decoupling capacitors in close proximity on AVDD (pin 32), DECAP (pin 2), DVDD (pin 30), and REFby2 (pin 7). Avoid placing vias between any supply pin and the respective decoupling capacitor.

10.1.4 Reference Decoupling

When using the internal reference (see the *External Reference* section), REFIO (pin 3) must have a 1-µF, X7R-grade, ceramic capacitor with at least a 10-V rating. This capacitor must be placed close to the REFIO pin, as illustrated in Figure 108. In cases where an external reference is used, refer to the reference component data sheet for filtering capacitor requirements.

10.1.5 Reference Buffer Decoupling

Dynamic currents are present at the REFP and REFM pins during the conversion phase, and excellent decoupling is required to achieve optimum performance. Place a 22-µF, X7R-grade, ceramic capacitor with at least a 10-V rating between the REFP and the REFM pins, as illustrated in Figure 108. Select 0603- or 0805-size capacitors to keep the equivalent series inductance (ESL) low. Connect the REFM pin to the decoupling capacitor before connecting to a ground via.

10.1.6 Multiplexer Input Decoupling

Minimizing channel-to-channel parasitic capacitance reduces the crosstalk induced on the PCB. This lower capacitance can be achieved by increasing the spacing between the analog traces to the multiplexer input.

In Figure 108, each multiplexer input has an RC filter. Use C0G- or NPO-type capacitors in the RC filter to help reduce settling when switching between multiplexer channels. When not switching the multiplexer, as discussed in Figure 43 and Figure 44, the RC filter can be omitted.

10.1.7 ADC Input Decoupling

Dynamic currents are also present at the ADC analog inputs (pins 18 and 19) of the ADS816x. Use C0G- or NPO-type capacitors to decouple these inputs. With these type of capacitors, capacitance remains almost constant over the full input voltage range. Lower-quality capacitors (such as X5R and X7R) have large capacitance changes over the full input voltage range that may cause degradation in device performance.

In Figure 108, each multiplexer input has an RC filter that helps reduce settling when switching between multiplexer channels. When not switching the multiplexer, as discussed in Figure 43 and Figure 44, the RC filter can be omitted.

Layout Guidelines (continued)

10.1.8 Example Schematic

Figure 107 shows the schematic used for Figure 108.

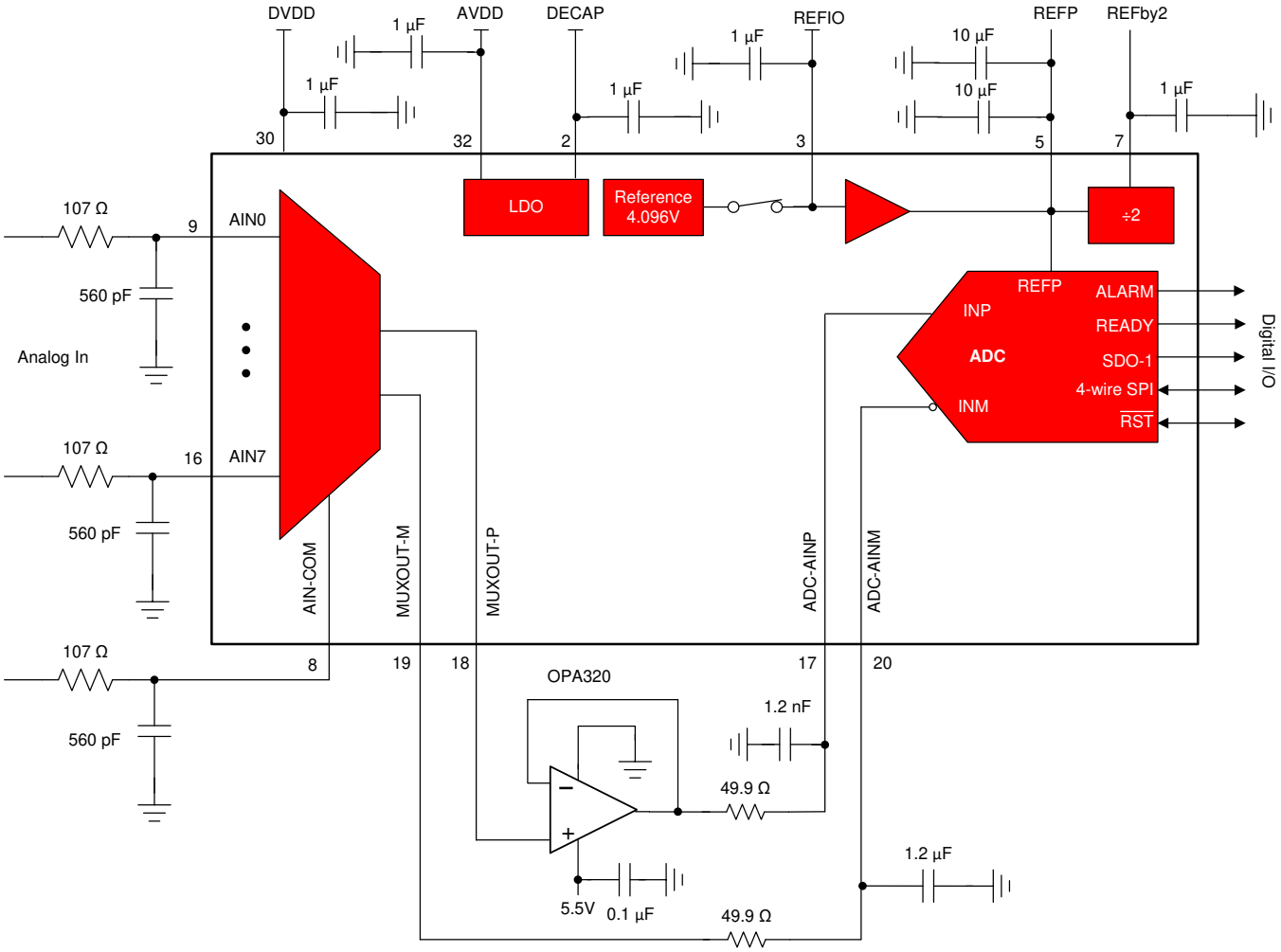


Figure 107. Example Schematic for Figure 108

10.2 Layout Example

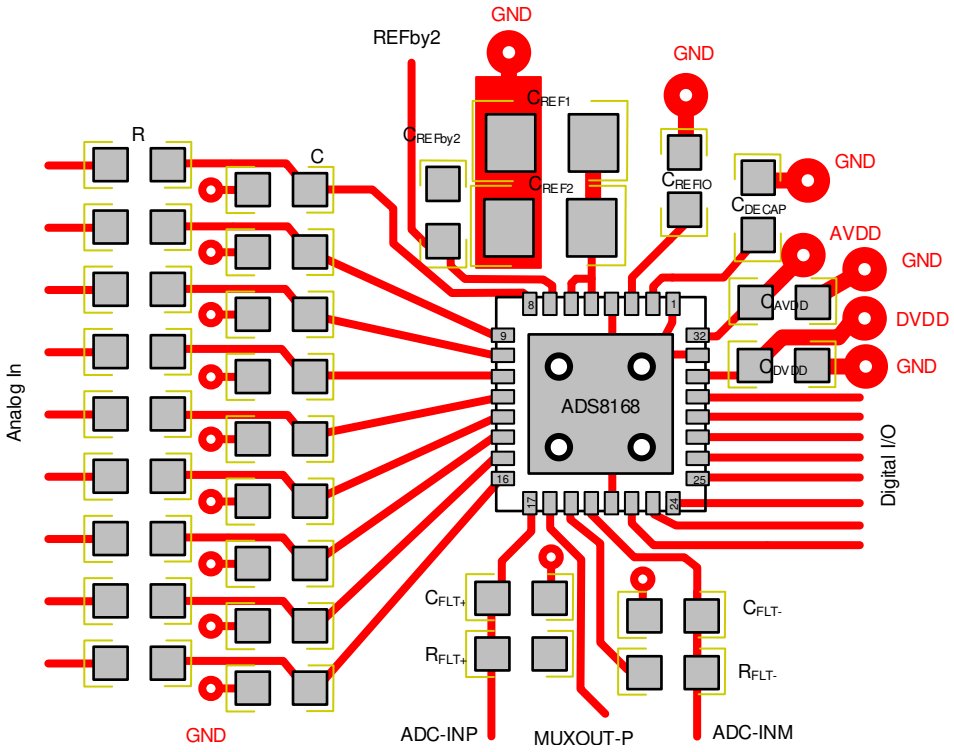


Figure 108. Recommended Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *16-Bit 1-MSPS Data Acquisition Reference Design for Single-Ended Multiplexed Applications* design guide
- Texas Instruments, *OPAx625 High-Bandwidth, High-Precision, Low THD+N, 16-Bit and 18-Bit Analog-to-Digital Converter (ADC) Drivers* data sheet
- Texas Instruments, *THS4551 Low Noise, Precision, 150MHz, Fully Differential Amplifier* data sheet
- Texas Instruments, *OPAx320x Precision, 20-MHz, 0.9-pA, Low-Noise, RRIO, CMOS Operational Amplifier With Shutdown* data sheet
- Texas Instruments, *1 MHz, Single-Supply, Photodiode Amplifier Reference Design* reference guide
- Texas Instruments, *Simplified System Design with Precision Multichannel ADC* application brief

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 60. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS8166	Click here	Click here	Click here	Click here	Click here
ADS8167	Click here	Click here	Click here	Click here	Click here
ADS8168	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

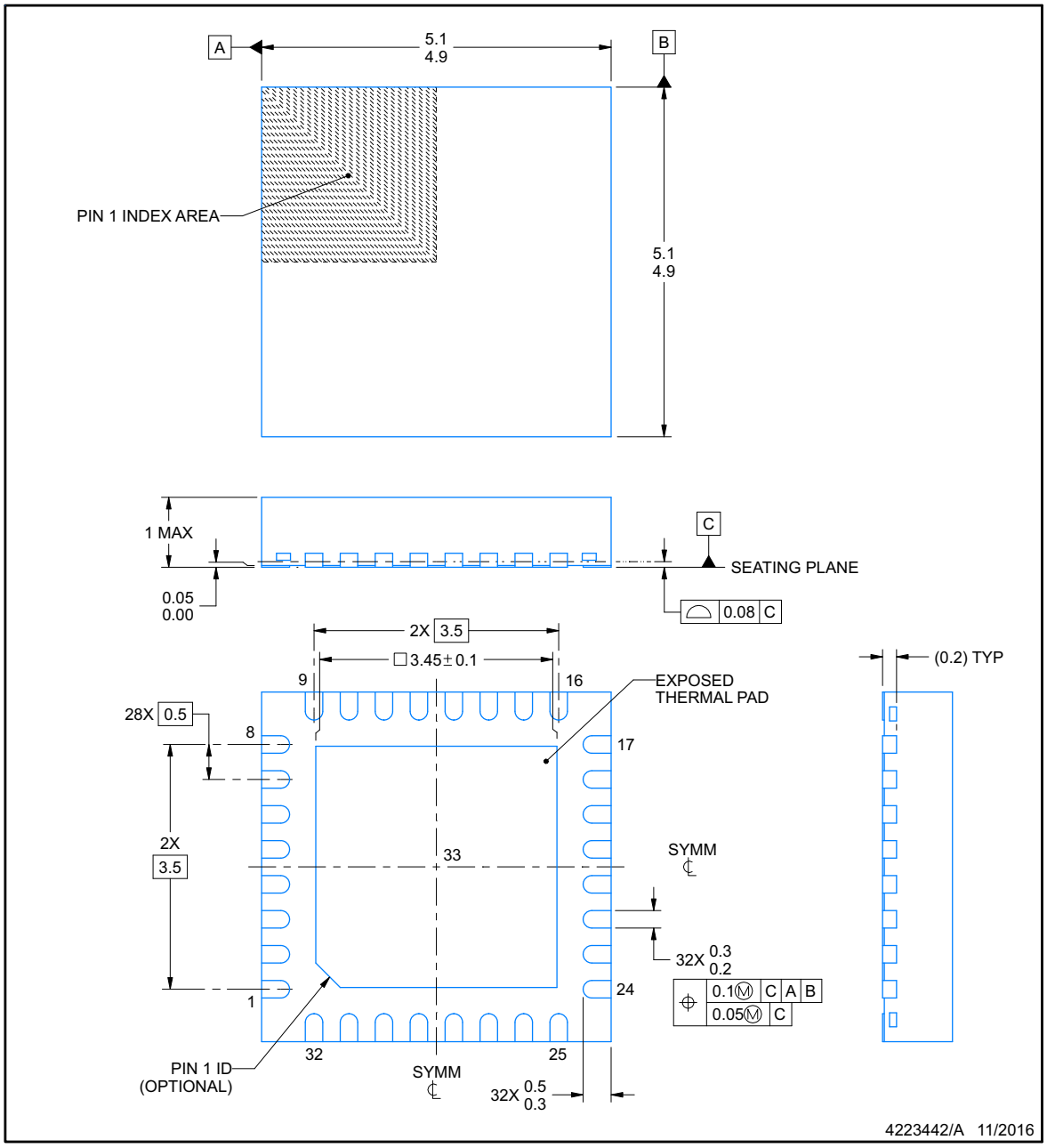
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

RHB0032E

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

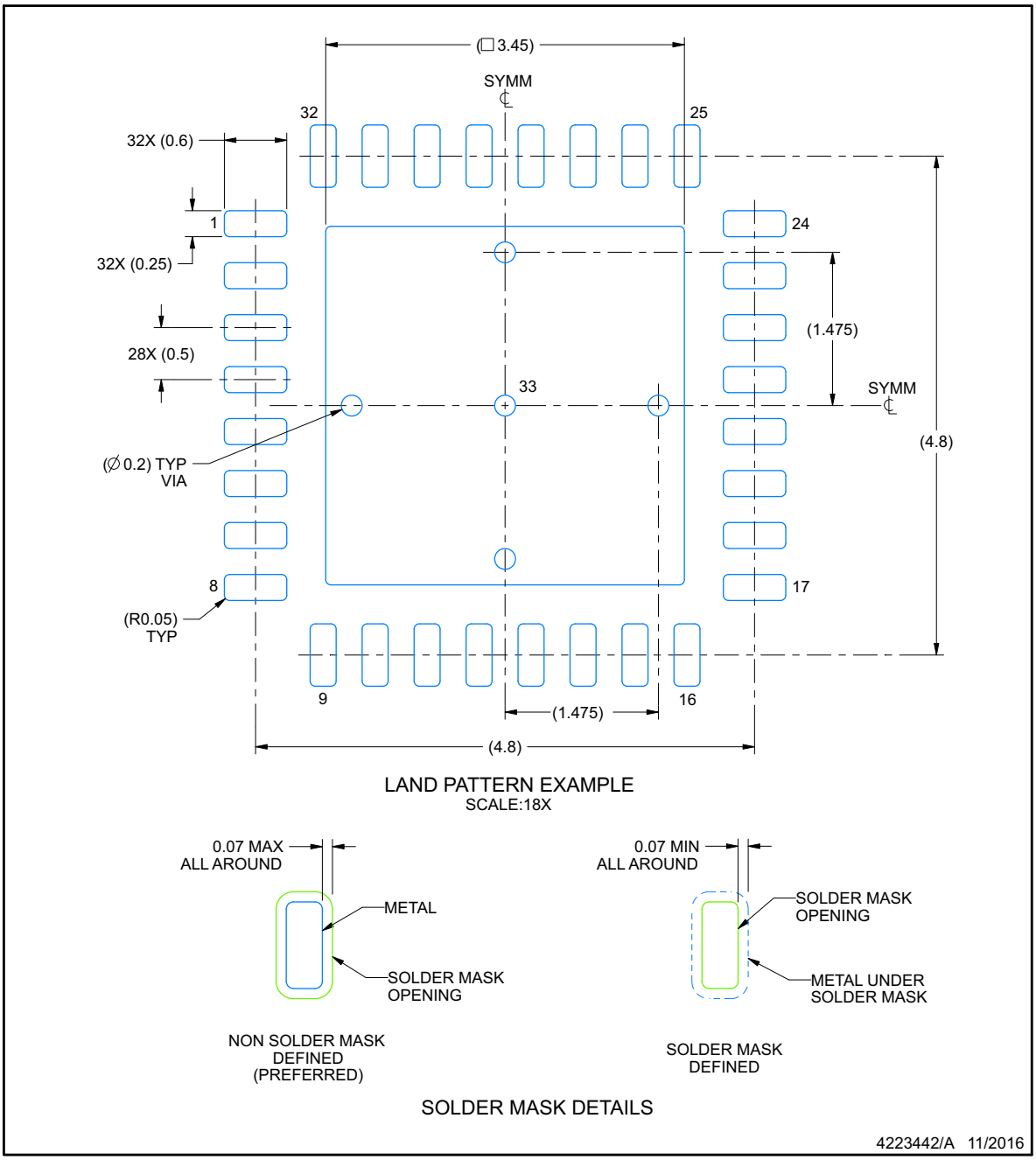
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



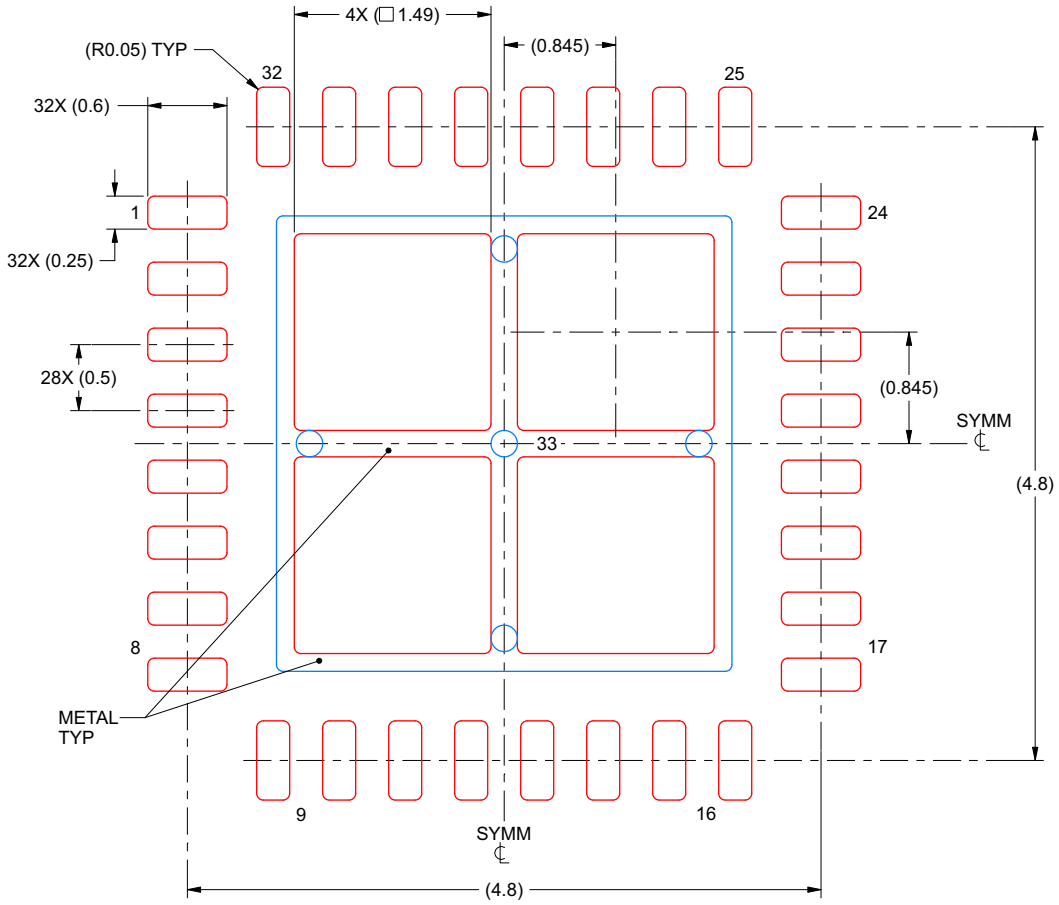
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8166IRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS 8166	Samples
ADS8166IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS 8166	Samples
ADS8167IRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS 8167	Samples
ADS8167IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS 8167	Samples
ADS8168IRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS 8168	Samples
ADS8168IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS 8168	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

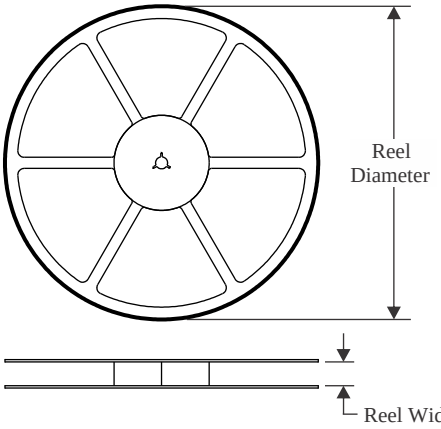
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

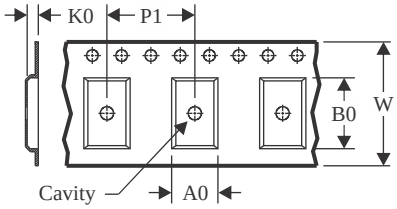
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

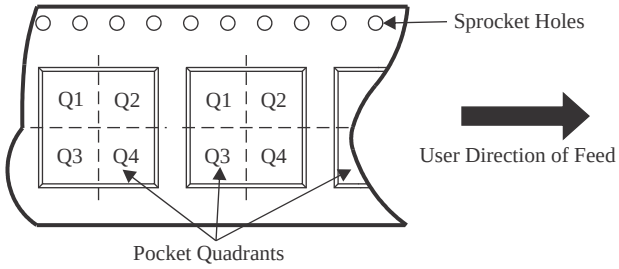


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

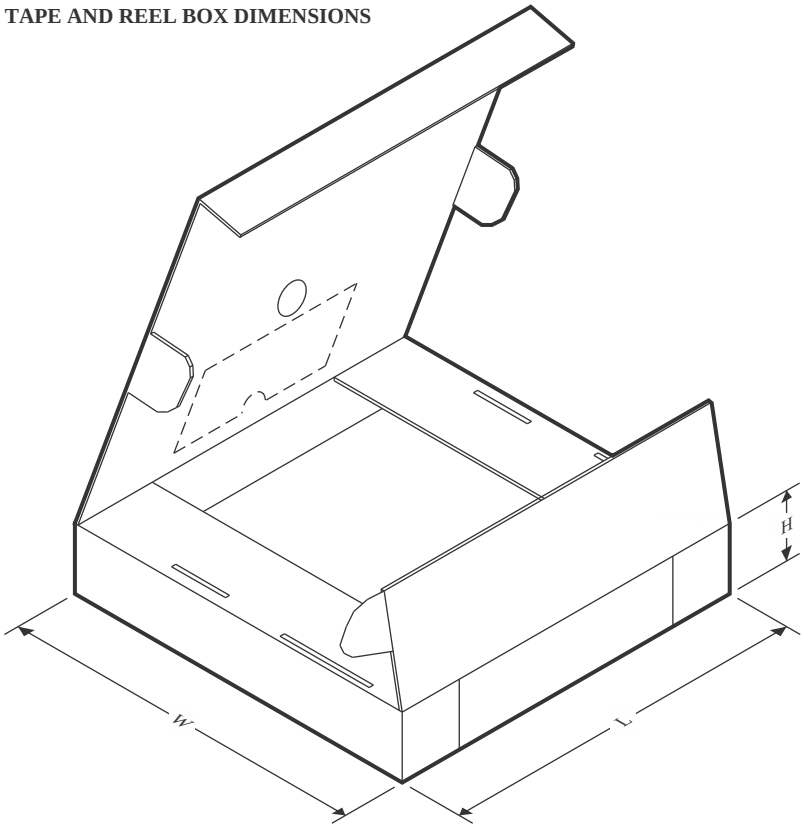
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8166IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS8166IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS8167IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS8167IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS8168IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS8168IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8166IRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS8166IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS8167IRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS8167IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS8168IRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
ADS8168IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

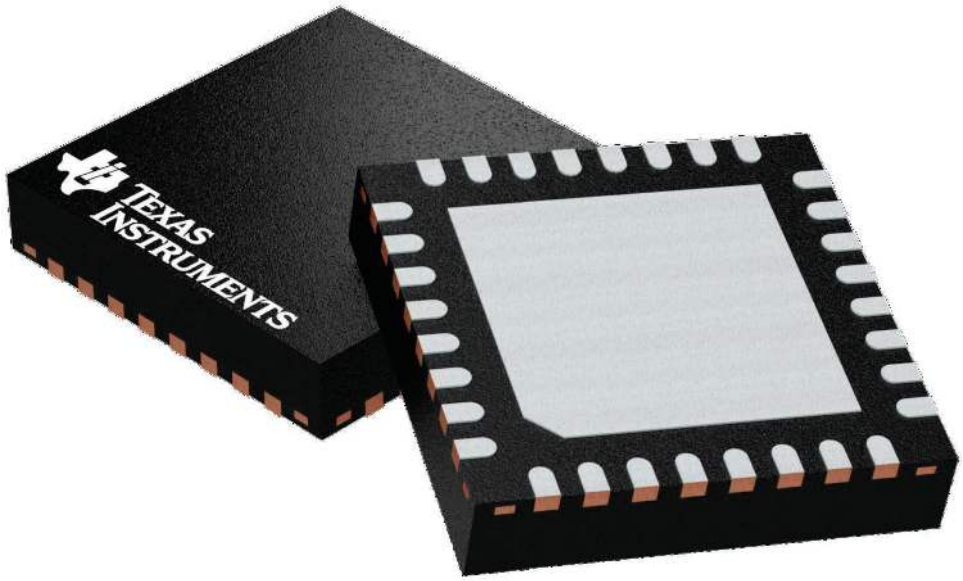
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

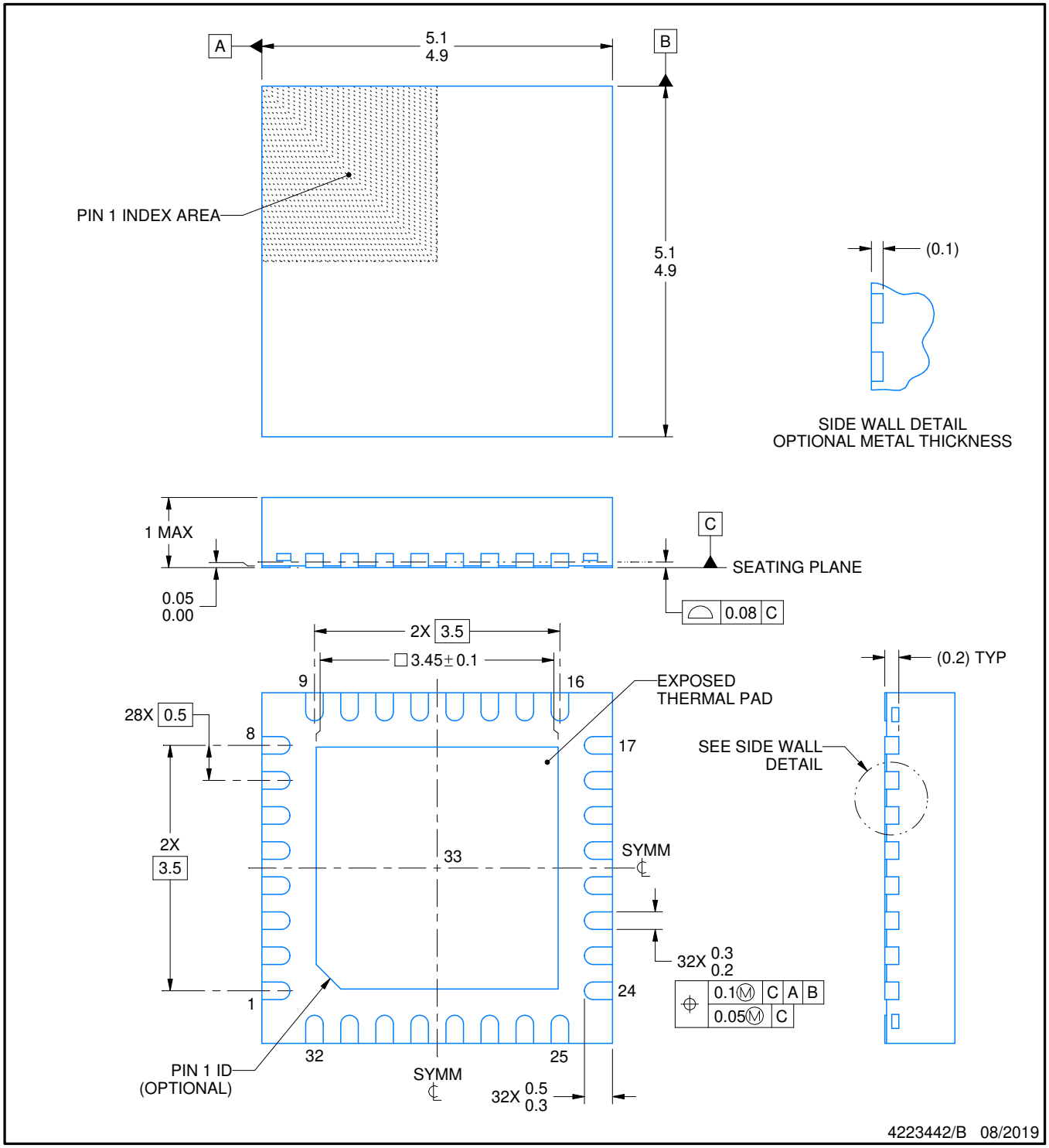
4224745/A

RHB0032E

PACKAGE OUTLINE

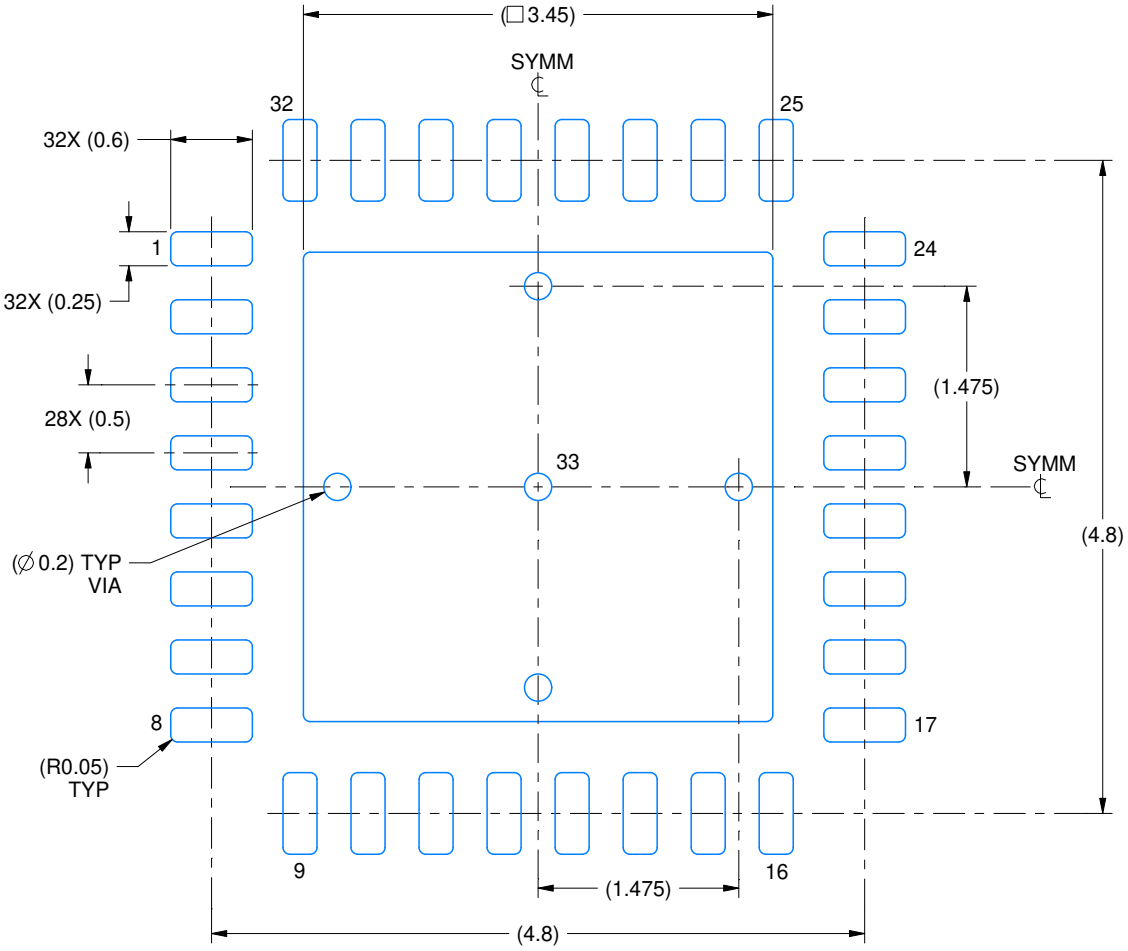
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

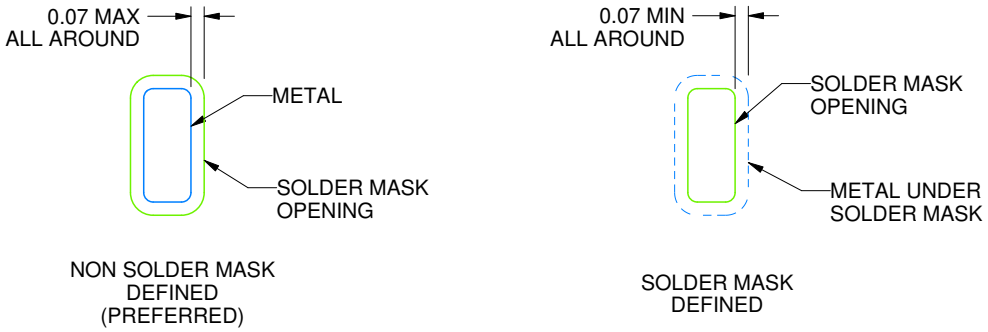


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

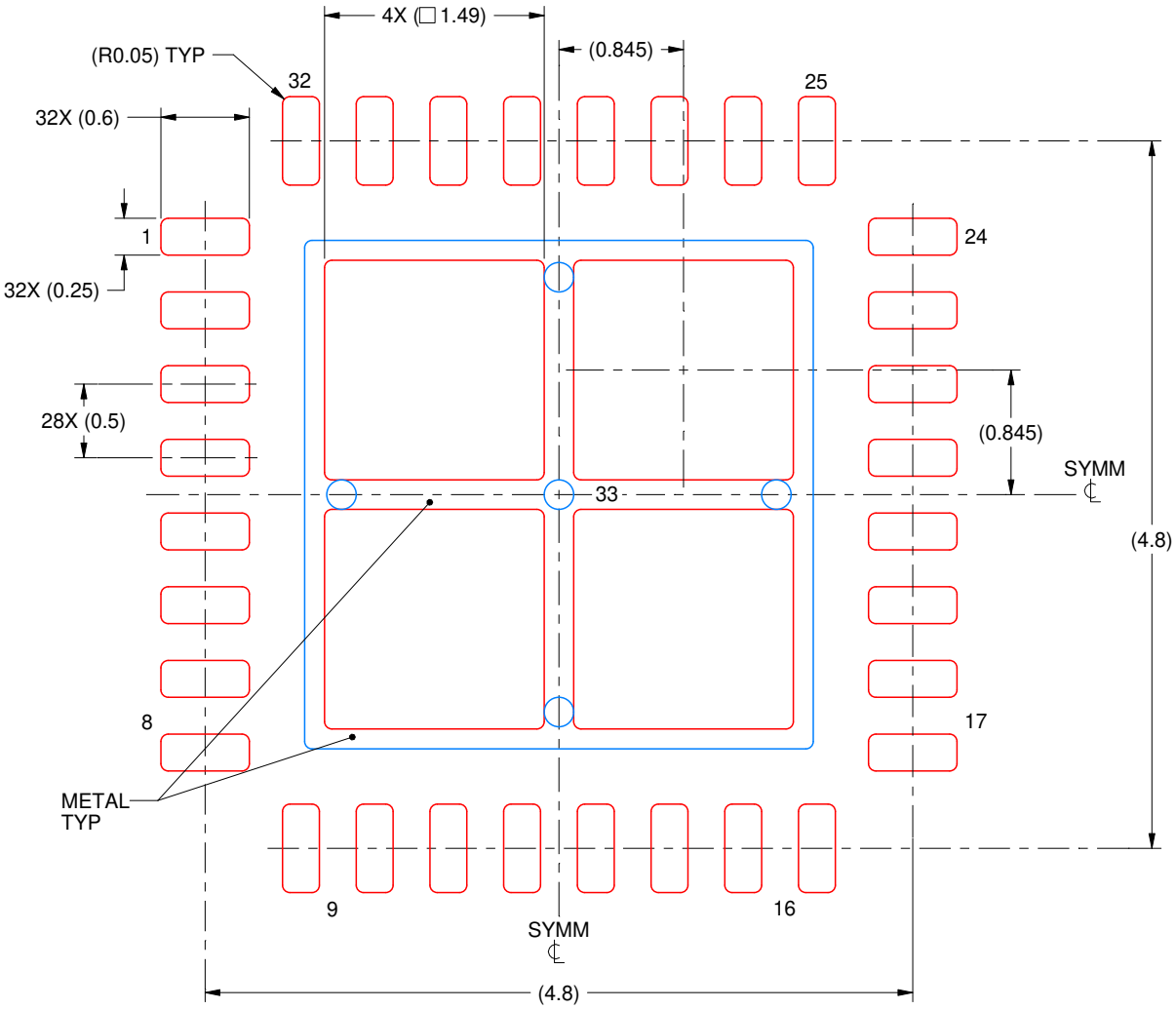


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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