ARM® Cortex®-M0
32-bit Microcontroller

NuMicro® Family
M051 DN/DE Series
Datasheet

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www.nuvoton.com

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1 GENERAL DESCRIPTION

The NuMicro® M051 DN/DE series 32-bit microcontroller is embedded with ARM® Cortex®-M0 core for industrial control and applications which need rich communication interfaces. The NuMicro® M051 DN/DE series includes the following part numbers: M052xDN/xDE, M054xDN/xDE, M058xDN/xDE and M0516xDN/xDE.

The NuMicro® M051 DN/DE series can run up to 50 MHz and operate at 2.5V ~ 5.5V, -40℃ ~ 85℃, while M05xxDE operates at -40℃ ~ 105℃, and thus can afford to support a variety of industrial control and applications which need high CPU performance. The NuMicro® M051 DN/DE series offers 8/16/32/64 KB flash, 4 KB Data Flash, 4 KB flash for the ISP, and 4 KB SRAM.

Many system level peripheral functions, such as I/O Port, EBI (External Bus Interface), Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, Window Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into The NuMicro® M051 DN/DE series in order to reduce component count, board space and system cost. These useful functions make The NuMicro® M051 DN/DE series powerful for a wide range of applications.

Additionally, the NuMicro® M051 DN/DE series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, and IAP (In-Application Programming), which allow the user to update the program memory without removing the chip from the actual end product.

Item	M05xxBN	M05xxDN	M05xxDE
Operating Temperature	-40℃ ~ 85℃	-40℃ ~ 85℃	-40℃ ~ 105℃
Hardware Divider	-	●	●
IAP Mode	-	●	●
Window WDT	-	●	●
Analog Comparators	2	4	4
Configurable I/O mode after POR	-	●	●
I^2C	1	2 (Supports Wake-up)	2 (Supports Wake-up)
SPI	- Only Supports HCLK as SPI clock source - No FIFO	- Supports HCLK and PLL as SPI clock source - 4-level FIFO	- Supports HCLK and PLL as SPI clock source - 4-level FIFO
PWM and ADC	PWM cannot trigger ADC	- PWM can trigger ADC conversion	- PWM can trigger ADC conversion

Table 1-1 M05xxBN, M05xxDN and M05xxDE Difference List

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 50 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
  - Provides hardware divider and supports signed 32-bit dividend, 16-bit divisor operation
- Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
  - 8KB/16KB/32KB/64KB Flash for program memory (APROM)
  - 4KB Flash for data memory (Data Flash)
  - 4KB Flash for loader (LDROM)
  - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
  - 22.1184 MHz internal oscillator
  - 4~24 MHz external crystal input
  - 10 kHz low-power oscillator for Watchdog Timer and wake-up in Sleep mode
  - PLL allows CPU operation up to the maximum 50 MHz
- I/O Port
  - Up to 40 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - Configurable I/O mode after POR
- Timer
  - Provides four channel 32-bit timers; one 8-bit pre-scale counter with 24-bit up-timer for each timer
  - Independent clock source for each timer
  - 24-bit timer value is readable through TDR (Timer Data Register)
  - Provides One-shot, Periodic and Toggle operation modes
  - Provides event counter function
  - Provides external capture/reset counter function
  - Two more timer clock sources from external trigger and internal 10 kHz
  - TIMER wake-up function
  - External capture input source selected from ACMP or TxEX
  - Toggle mode output pins selected from TxEX or TMx
  - Inter-Timer trigger mode
- WDT (Watchdog Timer)

- Multiple clock sources
- Supports wake-up from Power-down or Sleep mode
- Interrupt or reset selectable on watchdog time-out
- Time-out reset delay period time can be selected

- WWDT (Window Watchdog Timer)
  - 6-bit down counter with 11-bit pre-scale for wide range window selected
- PWM
  - Up to four built-in 16-bit PWM generators, providing eight PWM outputs or four complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - 16-bit digital Capture timers with rising/falling capture inputs
  - Supports capture interrupt
  - Internal 10 kHz to PWM clock source
  - Polar inverse function
  - Center-aligned type function
  - Timer duty interrupt enable function
  - Two kinds of PWM interrupt period/duty type selection
  - Period/duty trigger ADC function
  - PWM Timer synchronous start function
- UART
  - Up to two sets of UART devices
  - Programmable baud-rate generator
  - Buffered receiver and transmitter, each with 15 bytes FIFO
  - Optional flow control function (CTS and RTS)
  - Supports IrDA(SIR) function
  - Supports RS485 function
  - Supports LIN function
- SPI
  - Up to two sets of SPI devices
  - Supports Master/Slave mode
  - Full-duplex synchronous serial data transfer
  - Provides 3 wire function
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx latching data can be either at rising edge or at falling edge of serial clock
  - Tx sending data can be either at rising edge or at falling edge of serial clock
  - Supports Byte Suspend mode in 32-bit transmission
  - PLL clock source
  - 4-level depth FIFO buffer for better performance and flexibility in SPI Burst Transfer mode

- I^2C
  - Up to two sets of I^2C modules
  - Supports Master/Slave mode
  - Bidirectional data transfer between master and slave
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Supports multiple address recognition (four slave addresses with mask option)
- ADC
  - 12-bit SAR ADC
  - Up to 8-ch single-ended input or 4-ch differential input
  - Supports Single mode/Burst mode/Single-cycle Scan mode/Continuous Scan mode
  - Supports 2' complement/un-signed format in differential mode conversion results
  - Each channel with an individual result register
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Conversion started either by software trigger or external pin trigger
  - A/D conversion started by PWM center-aligned trigger or edge-aligned trigger
  - PWM trigger delay function
  - Supports conversion result with signed format in Differential input and Burst mode
- Analog Comparator
  - Up to four sets of Comparator analog modules
  - External input or internal band-gap voltage selectable at negative node
  - Interrupt when compared results change
  - Power-down wake-up
- EBI (External Bus Interface) for external memory-mapped device access
  - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
  - Supports 8-bit or 16-bit data width
  - Supports byte-write in 16-bit data width
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- IAP (In-Application Programming)
- One built-in temperature sensor with 1℃ resolution
- BOD (Brown-out Detector)
  - With 4 levels: 4.4V/3.7V/2.7V/2.2V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage level: 2.0V
- Operating Temperature:

- M05xxDN: -40℃~85℃
- M05xxDE: -40℃~105℃

- Packages:
  - Green package (RoHS)
  - 48-pin LQFP, 33-pin QFN

3 ABBREVIATIONS

3.1 List of Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output

SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION AND PIN CONFIGURATION

4.1 NuMicro® M051 Series M05xxDN Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity			COMP	PWM (16-Bit)	ADC (12-Bit)	WDT	WWDT	EBI	ISP/ICP/IAP	Package	Operating Temperature Range(℃)
							UART	SPI	I^2C									
M052LDN	8	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M052ZDN	8	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85
M054LDN	16	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M054ZDN	16	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85
M058LDN	32	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M058ZDN	32	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85
M0516LDN	64	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +85
M0516ZDN	64	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +85

Table 5-2 NuMicro® M051 Series M05xxDN Product Selection Guide

4.2 NuMicro® M051 Series M05xxDE Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity			COMP	PWM (16-Bit)	ADC (12-Bit)	WDT	WWDT	EBI	ISP/ICP/IAP	Package	Operating Temperature Range(℃)
							UART	SPI	I^2C									
M052LDE	8	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M052ZDE	8	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105
M054LDE	16	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M054ZDE	16	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105
M058LDE	32	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M058ZDE	32	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105
M0516LDE	64	4	4	4	40	4	2	2	2	4	8	8	√	√	√	√	LQFP48	-40 to +105
M0516ZDE	64	4	4	4	24	4	2	1	2	3	5	5	√	√		√	QFN33	-40 to +105

Table 5-2 NuMicro® M051 Series M05xxDE Product Selection Guide

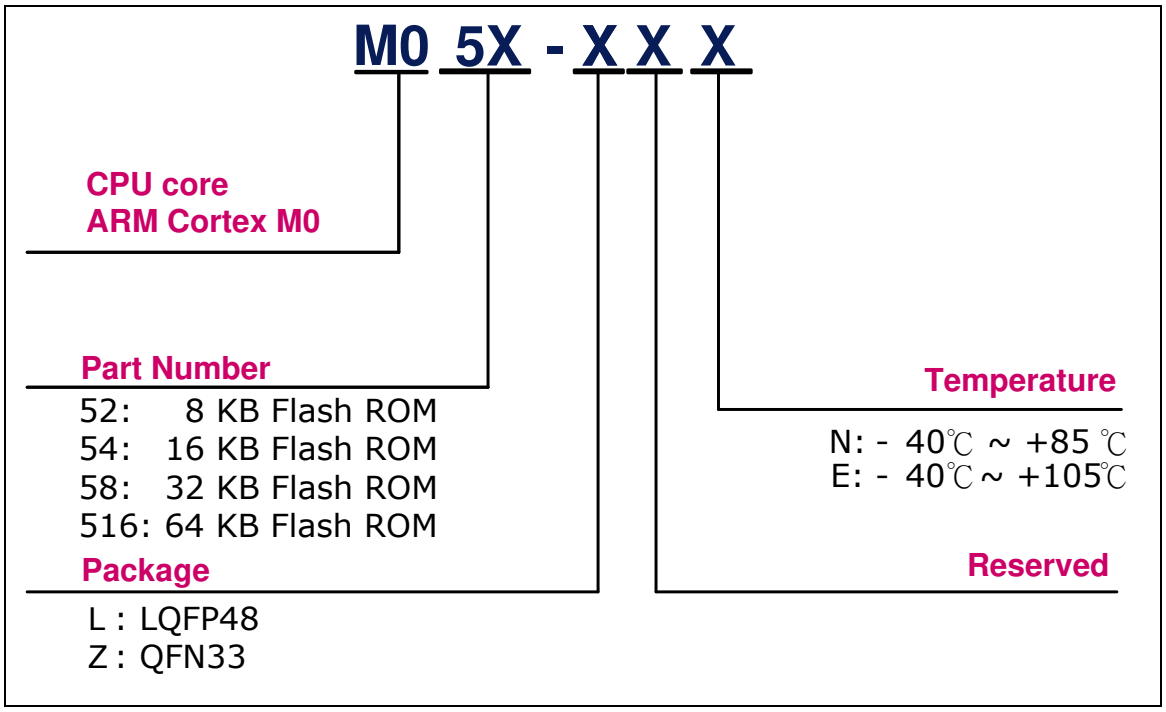


Figure 4-1 NuMicro® M051 DN/DE Series Naming Rule

4.3 Pin Diagrams

4.3.1 QFN 33-pin

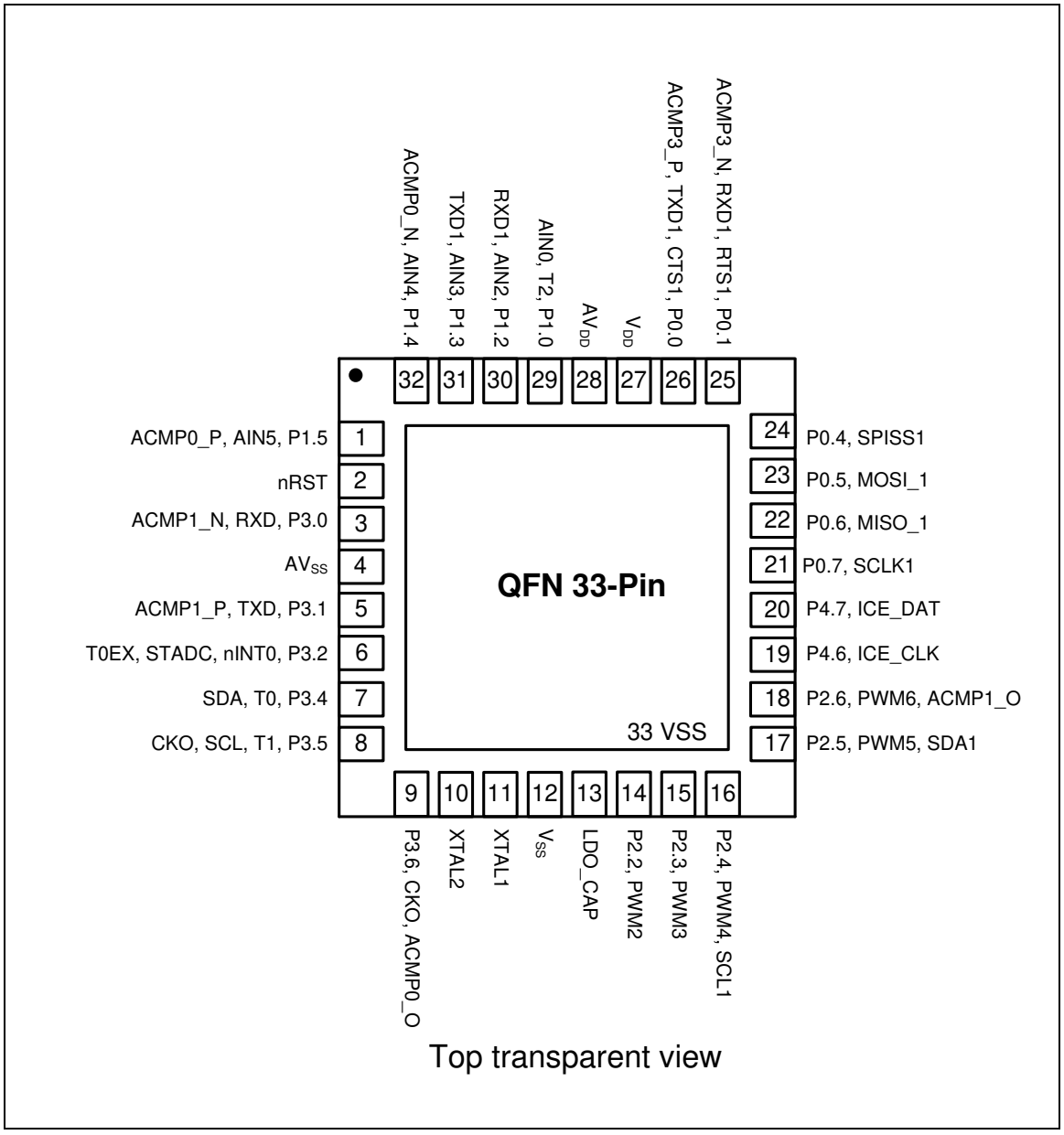


Figure 4-2 NuMicro® M051 DN/DE Series QFN-33 Pin Diagram

4.3.2 LQFP 48-pin

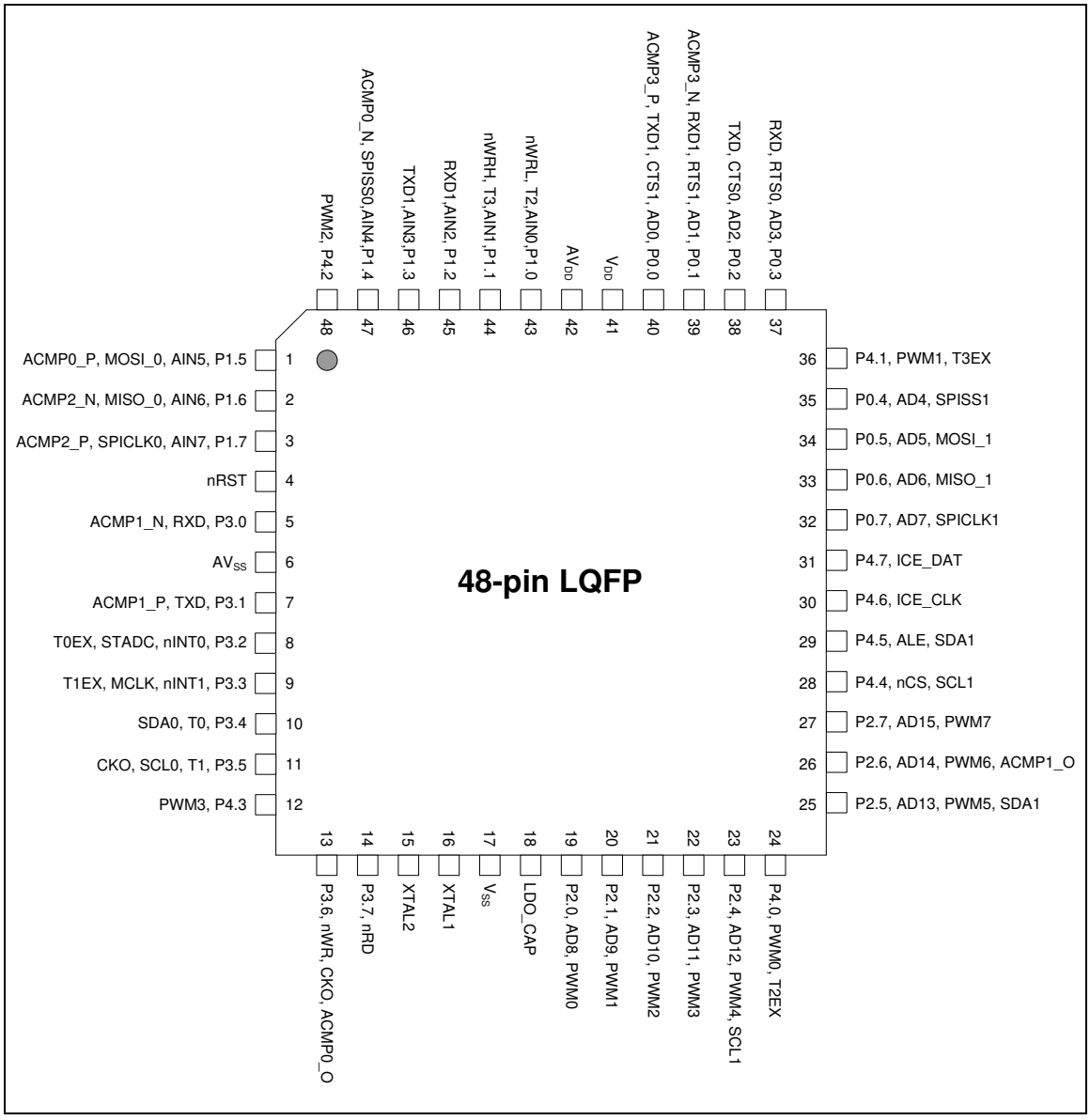


Figure 4-3 NuMicro® M051 DN/DE Series LQFP-48 Pin Diagram

4.4 Pin Description

Pin Number		Symbol	Alternate Function			Type[1]	Description
QFN33	LQFP48		1	2	3		
11	16	XTAL1				I (ST)	External 4~24 MHz (high speed) crystal input pin.
10	15	XTAL2				O	External 4~24 MHz (high speed) crystal output pin.
27	41	V_{DD}				P	Power supply to I/O ports and LDO source for internal PLL and digital circuit.
12	17	V_{SS}				P	Ground pin for digital circuit.
33							
28	42	AV_{DD}				P	Power supply to internal analog circuit.
4	6	AV_{SS}				P	Analog Ground pin for analog circuit.
13	18	LDO_CAP				P	LDO output pin. **Note:** This pin needs to be connected with a 1uF capacitor.
2	4	nRST				I (ST)	The nRST pin is a Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22M while the system clock is running will reset the device. The nRST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
26	40	P0.0	CTS1	AD0	TXD1[2], ACMP3_P	I/O	The P0.0 ~ P0.7 pins are called Port 0. Port 0 is a general purpose I/O port, which can be configured as Input, Output, Quasi Bi-direction and Open-drain mode. Port 0 supports multi-function pins, including CTS1, RTS1, CTS0, RTS0, SPISS1, MOSI_1, MISO_1, SPICLK1, AD0 ~ AD7, TXD1, RXD1, TXD, RXD, ACMP3_P, and ACMP3_N. AD0 ~ AD7 belong to EBI function for external memory accessing. The SPISS1, MOSI_1, MISO_1, and SPICLK1 pins are for SPI function. The CTS0 and CTS1 pins are clear to send input pin for UART0/1. The RTS0 and RTS1 pins are Request to Send output pin for UART0/1. The RXD and TXD pins are for UART0 function. The RXD1 and TXD1 pins are for UART1 function. The ACMP3_N and ACMP3_P pins are for ACMP3 negative/positive inputs.
25	39	P0.1	RTS1	AD1	RXD1[2], ACMP3_N	/O	
NC	38	P0.2	CTS0	AD2	TXD[2]	I/O	
NC	37	P0.3	RTS0	AD3	RXD[2]	I/O	
24	35	P0.4	SPISS1	AD4		I/O	
23	34	P0.5	MOSI_1	AD5		I/O	
22	33	P0.6	MISO_1	AD6		I/O	
21	32	P0.7	SPICLK1	AD7		I/O	
29	43	P1.0	T2	AIN0	nWRL	I/O	The P1.0 ~ P1.7 pins are called Port 1. Port 1 is a general purpose I/O port, which can be configured as Input, Output, Quasi-bidirectional and Open-drain mode.
NC	44	P1.1	T3	AIN1	nWRH	I/O	

30	45	P1.2	RXD1[2]	AIN2		I/O	Port 1 supports multi-function pins, including T2, T3, RXD1, TXD1, SPISS0, MOSI_0, MISO_0, SPICLK0, AIN0 ~ AIN7, nWRL, nWRH, ACMP0_N, ACMP0_P, ACMP2_N, and ACMP2_P. The SPISS0, MOSI_0, MISO_0, and SPICLK0 pins are for SPI function. The AIN0 ~ AIN7 pins are for 12 bits ADC function. The RXD1 and TXD1 pins are for UART1 function. The nWRL and nWRH pins are for low/high byte write enable output in 16-bit data width of EBI. The ACMP0_N and ACMP0_P pins are for ACMP0 negative/positive inputs. The ACMP2_N and ACMP2_P pins are for ACMP2 negative/positive inputs. The T2 and T3 pins are for Timer2/3 external even counter input and toggle mode output.
31	46	P1.3	TXD1[2]	AIN3		I/O	
32	47	P1.4	SPISS0	AIN4	ACMP0_N	I/O	
1	1	P1.5	MOSI_0	AIN5	ACMP0_P	I/O	
NC	2	P1.6	MISO_0	AIN6	ACMP2_N	I/O	
NC	3	P1.7	SPICLK0	AIN7	ACMP2_P	I/O	
NC	19	P2.0	PWM0[2]	AD8		I/O	The P2.0 ~ P2.7 pins are called Port 2. Port 2 is a general purpose I/O port, which can be configured as Input, Output, Quasi-bidirectional and Open-drain mode. Port 2 supports multi-function pins, including PWM0 ~ PWM7, AD8 ~ AD15, SCL1, SDA1 and ACMP1_O. The PWM0~PWM7 pins are for PWM function in the LQFP48 package. AD8 ~ AD15 belong to EBI function for external memory accessing. The SDA1 and SCL1 pins are for I^2C1 function and both of them are open-drain. The ACMP1_O pin is the output of ACMP1.
NC	20	P2.1	PWM1[2]	AD9		I/O	
14	21	P2.2	PWM2[2]	AD10		I/O	
15	22	P2.3	PWM3[2]	AD11		I/O	
16	23	P2.4	PWM4	AD12	SCL1[2]	I/O	
17	25	P2.5	PWM5	AD13	SDA1[2]	I/O	
18	26	P2.6	PWM6	AD14	ACMP1_O	I/O	
NC	27	P2.7	PWM7	AD15		I/O	
3	5	P3.0	RXD[2]		ACMP1_N	I/O	The P3.0 ~ P3.7 pins are called Port 3. Port 3 is a general purpose I/O port, which can be configured as Input, Output, Quasi-bidirectional and Open-drain mode. Port 3 supports multi-function pins, including RXD, TXD, nINT0, nINT1, T0, T1, nWR, nRD, STADC, MCLK, SDA, SCL, CKO, ACMP1_N, ACMP1_P, T0EX, T1EX, ACMP0_O. The RXD and TXD pins are for UART0 function. The nINT0 and nINT1 pins are for external interrupt input. The T0 and T1 pins are for Timer0/1 external even counter input and toggle mode output. The nWR, nRD and MCLK are for EBI function. The STADC pin is for ADC external trigger input. The SDA and SCL pins are for I^2C function and both of them are open-drain. The CKO is clock output pin for clock monitor. The ACMP1_N and ACMP1_P pins are for ACMP1 negative/positive inputs. The T0EX and T1EX pins are for external capture/reset trigger input of Timer0/1. The ACMP0_O pin is the output of Analog ACMP0.
5	7	P3.1	TXD[2]		ACMP1_P	I/O	
6	8	P3.2	nINT0	STADC	T0EX	I/O	
NC	9	P3.3	nINT1	MCLK	T1EX	I/O	
7	10	P3.4	T0	SDA		I/O	
8	11	P3.5	T1	SCL	CKO[2]	I/O	
9	13	P3.6	nWR	CKO	ACMP0_O	I/O	
NC	14	P3.7	nRD			I/O	
NC	24	P4.0	PWM0[2]		T2EX	I/O	The P4.0 ~ P4.7 pins are called Port 4. Port 4 is a general

NC	36	P4.1	PWM1[2]		T3EX	I/O	purpose I/O port, which can be configured as Input, Output, Quasi-bidirectional and Open-drain mode. Port 3 supports multi-function pins, including PWM0 ~ PWM3, nCS, ALE, ICE_CLK, ICE_DAT, SCL1, SDA1, T2EX and T3EX. The PWM0 ~ PWM3 pins are for PWM function. The nCS and ALE pins are for EBI function. The ICE_CLK and ICE_DAT pins are for Serial Wire Debug Interface. The SDA1 and SCL1 pins are for I^2C1 function and both of them are open-drain. The T2EX and T3EX pins are for external capture/reset trigger input of Timer2/3.
NC	48	P4.2	PWM2[2]			I/O	
NC	12	P4.3	PWM3[2]			I/O	
NC	28	P4.4	nCS	SCL1		I/O	
NC	29	P4.5	ALE	SDA1		I/O	
19	30	P4.6	ICE_CLK			I/O	
20	31	P4.7	ICE_DAT			I/O	

Note 1: I/O type description. I: Input, O: Output, I/O: Quasi-bidirectional, D: Open-drain, P: Power pins, ST: Schmitt trigger.

Note 2: The PWM0 ~ PWM3, RXD, TXD, RXD1, TXD1, SCL1, SDA1 and CKO can be assigned to different pins. However, a pin function can only be assigned to a pin at the same time, i.e. software cannot assign RXD to P0.3 and P3.0 at the same time.

5 BLOCK DIAGRAM

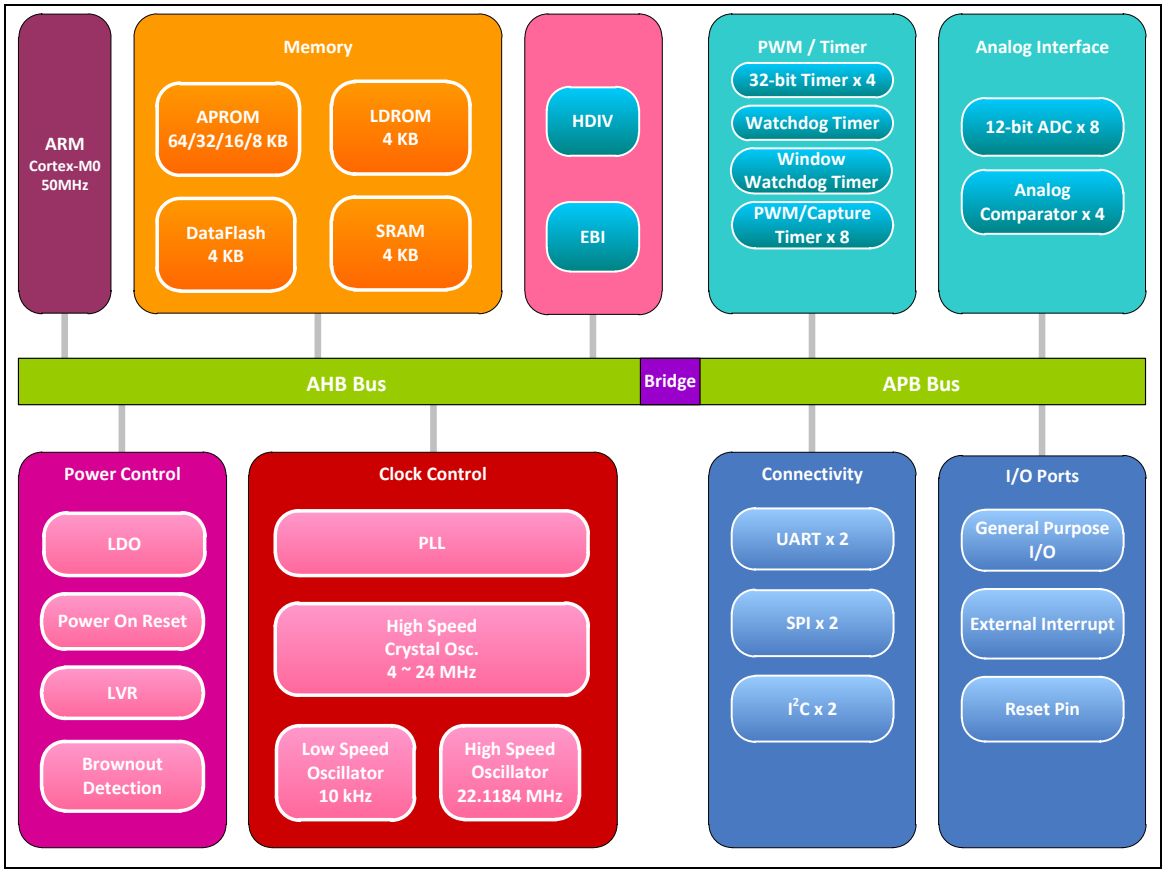


Figure 5-1 NuMicro® M051 DN/DE Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The following figure shows the functional controller of processor.

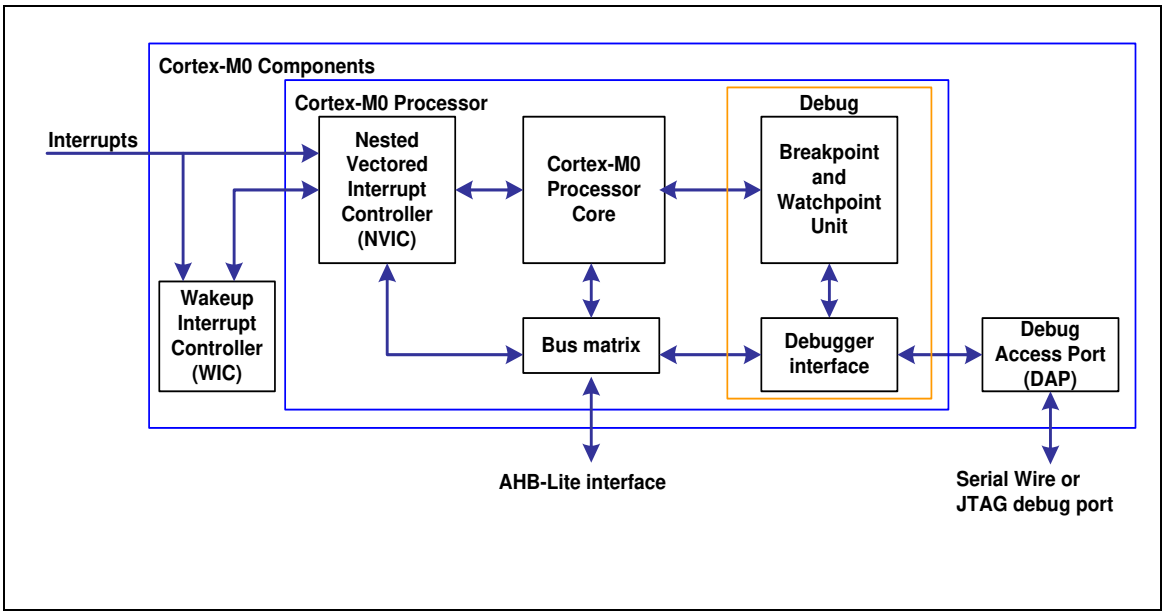


Figure 6-1 Functional Block Diagram

The implemented device provides:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and provides Ultra-low Power Sleep mode
- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Power Architecture
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, and multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the Reset Pin (nRST)
  - Watchdog Timer Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD)
- Software Reset
  - MCU Reset - SYSRESETREQ(AIRCR[2])
  - Cortex®-M0 Core One-shot Reset - CPU_RST(IPRSTC1[1])
  - Chip One-shot Reset - CHIP_RST(IPRSTC1[0])

Note: ISPCON.BS keeps the original value after MCU Reset and CPU Reset.

6.2.3 System Power Architecture

In this chip, the power distribution is divided into two segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation. AV_{DD} must be equal to V_{DD} to avoid leakage current.
- Digital power from V_{DD} and V_{SS} supplies the power to the I/O pins and internal regulator which provides a fixed 1.8 V power for digital operation.

The output of internal voltage regulator, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level as the digital power (V_{DD}). The following figure shows the power distribution of the NuMicro® M051 DN/DE series.

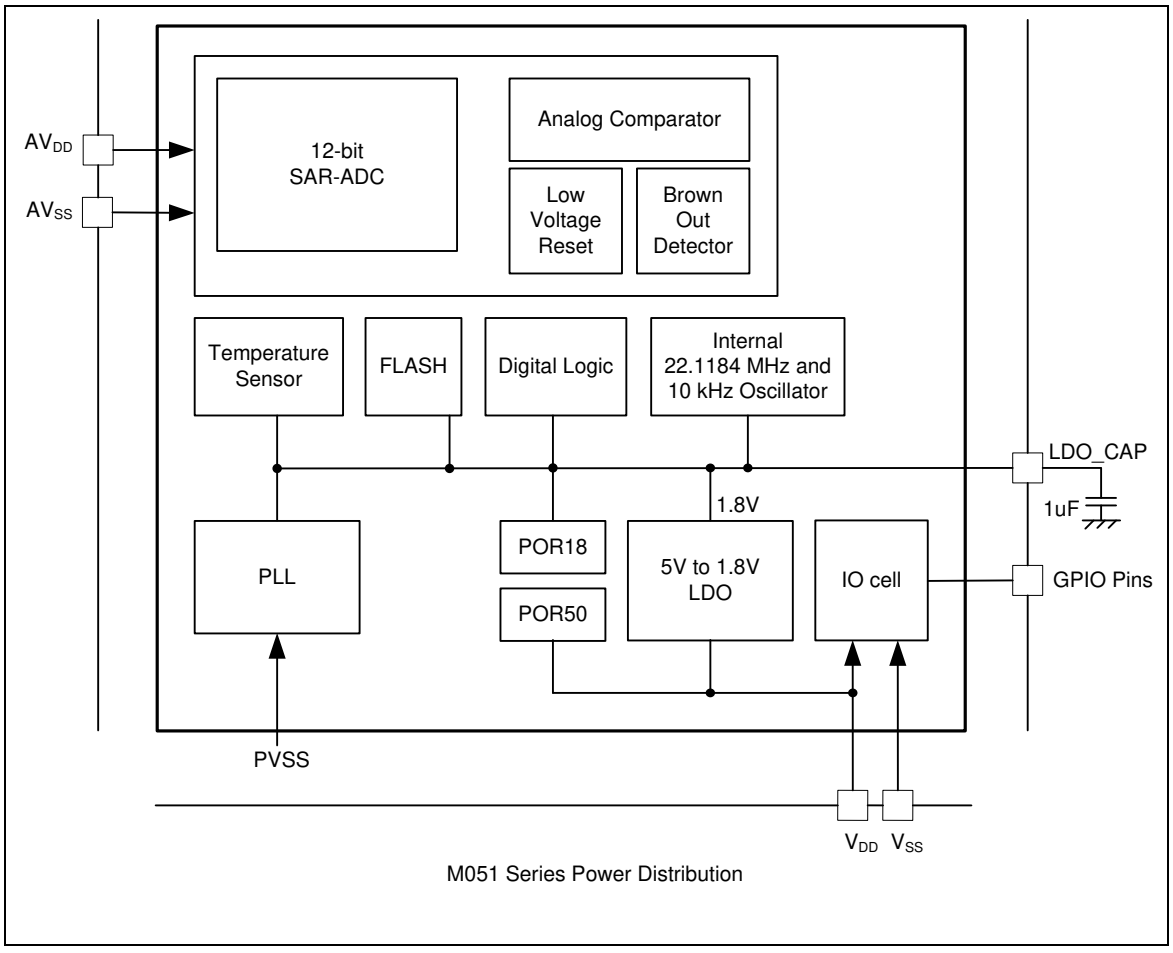


Figure 6-2 NuMicro® M051 DN/DE Series Power Architecture Diagram

6.2.4 System Memory Map

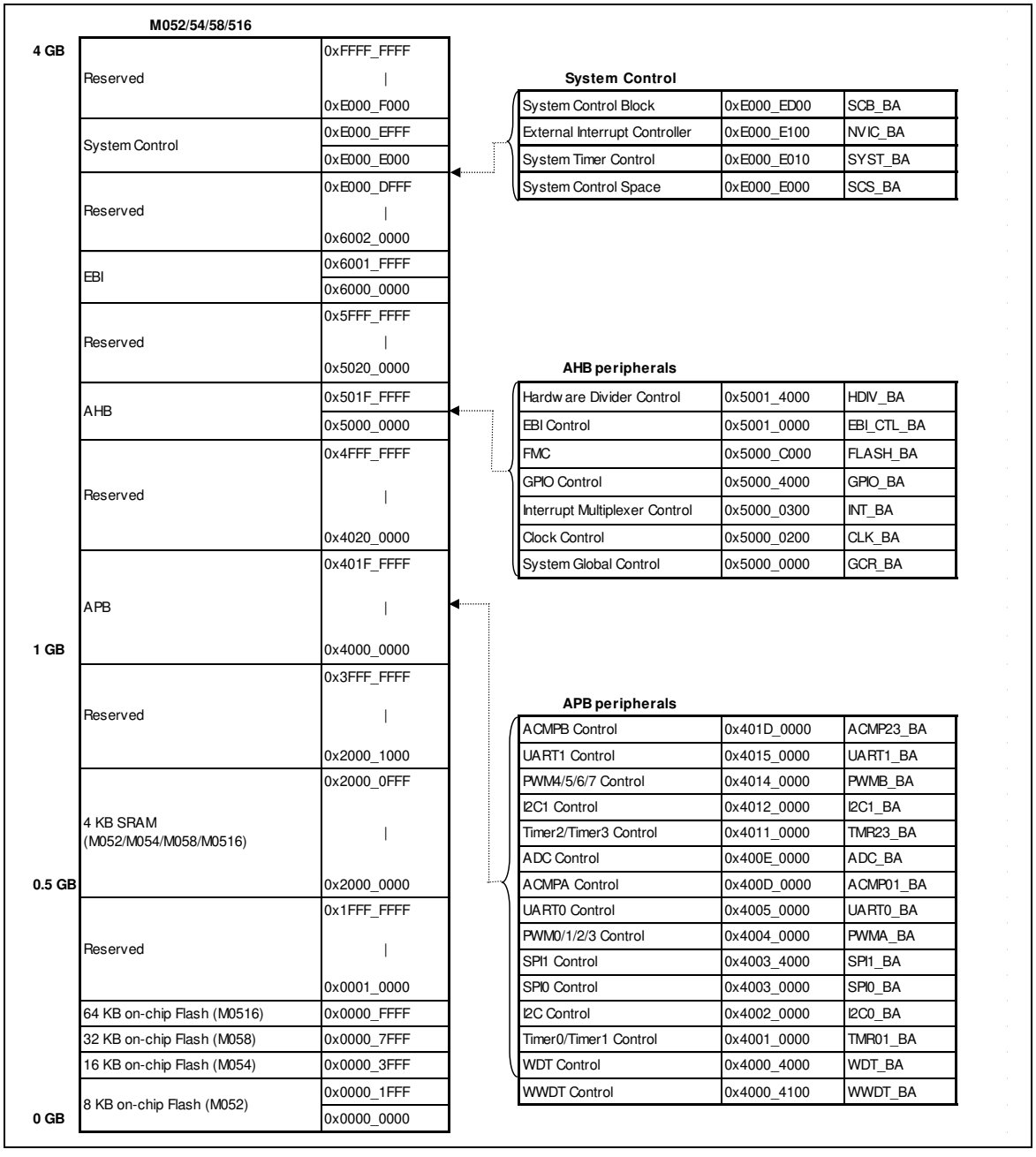
The NuMicro® M051 DN/DE series provides 4G-byte addressing space. The addressing space assigned to each on-chip controllers are shown in the following table. The detailed register definition, addressing space, and programming details will be described in the following sections for each on-chip peripheral. The NuMicro® M051 DN/DE series only supports little-endian data format.

Addressing Space	Token	Modules
Flash & SRAM Memory Space		
0x0000_0000 – 0x0000_FFFF	FLASH_BA	FLASH Memory Space (64 KB)
0x2000_0000 – 0x2000_0FFF	SRAM_BA	SRAM Memory Space (4 KB)
EBI Space (0x6000_0000 ~ 0x6001_FFFF)		
0x6000_0000 – 0x6001_FFFF	EBI_BA	External Memory Space (128 KB)
AHB Modules Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO (P0~P4) Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_CTL_BA	EBI Control Registers
0x5001_4000 – 0x5001_7FFF	HDIV_BA	Hardware Divider Register
APB Modules Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_00FF	WDT_BA	Watchdog Timer Control Registers
0x4000_4100 – 0x4000_7FFF	WWDT_BA	Window Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x400D_0000 – 0x400D_3FFF	ACMP01_BA	Analog Comparator 0/1 Control Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x401D_0000 – 0x401D_3FFF	ACMP23_BA	Analog Comparator 2/3 Control Registers
System Control Space (0xE000_E000 ~ 0xE000_EFFF)		

0xE000_E010 – 0xE000_E0FF	SYST_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	NVIC_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Block Registers

Table 6-1 Address Space Assignments for On-Chip Modules

6.2.5 Whole System Memory Mapping



6.2.6 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.7 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.7.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro® M051 DN/DE series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved

PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6-2 Exception Model

Exception Number	Vector Address	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description	Power-Down Wakeup
1-15					System exceptions	
16	0x40	0	BOD_INT	Brown-out	Brown-out low voltage detected interrupt	Yes
17	0x44	1	WDT_INT	WDT	Watchdog Timer interrupt	Yes
18	0x48	2	EINT0	GPIO	External signal interrupt from P3.2 pin	Yes
19	0x4C	3	EINT1	GPIO	External signal interrupt from P3.3 pin	Yes
20	0x50	4	GP01_INT	GPIO	External signal interrupt from P0[7:0] / P1[7:0]	Yes
21	0x54	5	GP234_INT	GPIO	External interrupt from P2[7:0]/P3[7:0]/P4[7:0], except P32 and P33	Yes
22	0x58	6	PWMA_INT	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt	No
23	0x5C	7	PWMB_INT	PWM4~7	PWM4, PWM5, PWM6 and PWM7 interrupt	No
24	0x60	8	TMR0_INT	TMR0	Timer 0 interrupt	No
25	0x64	9	TMR1_INT	TMR1	Timer 1 interrupt	No
26	0x68	10	TMR2_INT	TMR2	Timer 2 interrupt	No
27	0x6C	11	TMR3_INT	TMR3	Timer 3 interrupt	No
28	0x70	12	UART0_INT	UART0	UART0 interrupt	Yes
29	0x74	13	UART1_INT	UART1	UART1 interrupt	Yes
30	0x78	14	SPI0_INT	SPI0	SPI0 interrupt	No
31	0x7C	15	SPI1_INT	SPI1	SPI1 interrupt	No
32-33	0x80-0x84	16-17	Reserved	-	-	-
34	0x88	18	I2C0_INT	I^2C0	I^2C0 interrupt	Yes
35	0x8C	19	I2C1_INT	I^2C1	I^2C1 interrupt	Yes
36-40	0x90-0xA0	20-24	Reserved	-	-	-
41	0xA4	25	ACMP01_INT	ACMP0/1	Analog Comparator 0 or Comparator 1 interrupt	Yes

42	0xA8	26	ACMP23_INT	ACMP2/3	Analog Comparator 2 or Comparator 3 interrupt	Yes
43	0xAC	27	Reserved			
44	0xB0	28	PWRWU_INT	CLKC	Clock controller interrupt for chip wake-up from Power-down state	Yes
45	0xB4	29	ADC_INT	ADC	ADC interrupt	No
46-47	0xB8-0xBC	30-31	Reserved	-	-	

Table 6-3 System Interrupt Map Vector Table

6.2.7.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6-4 Vector Figure Format

6.2.7.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

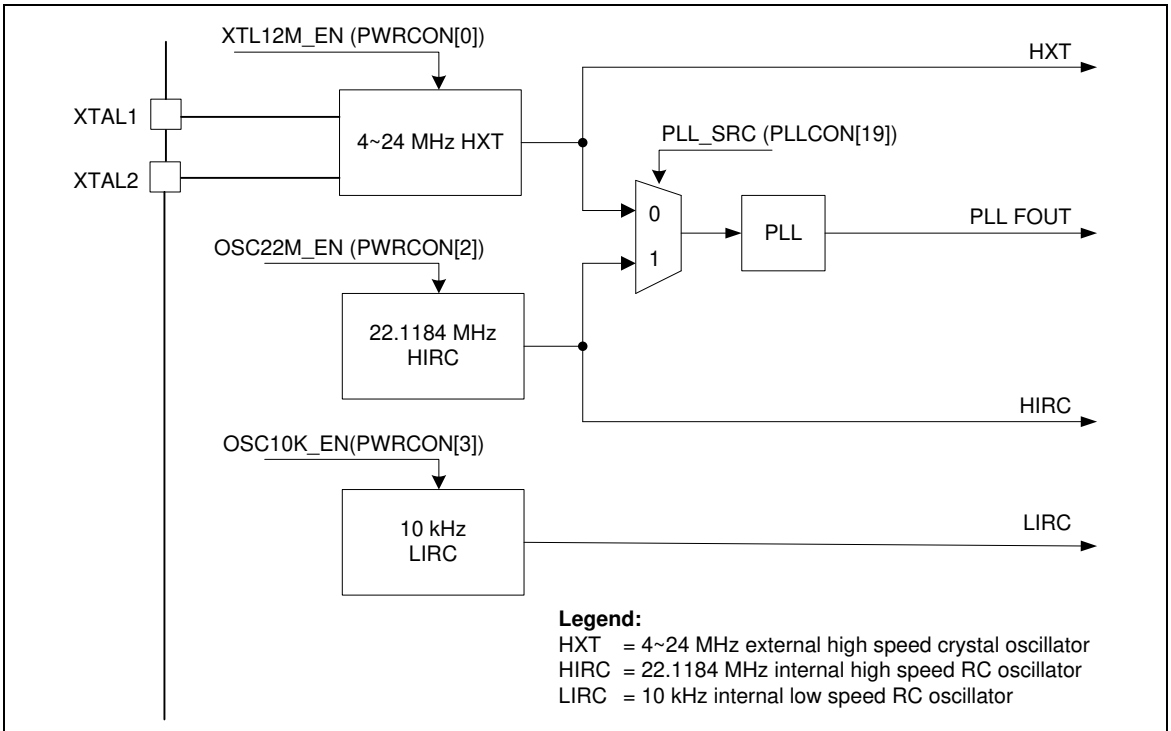
6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

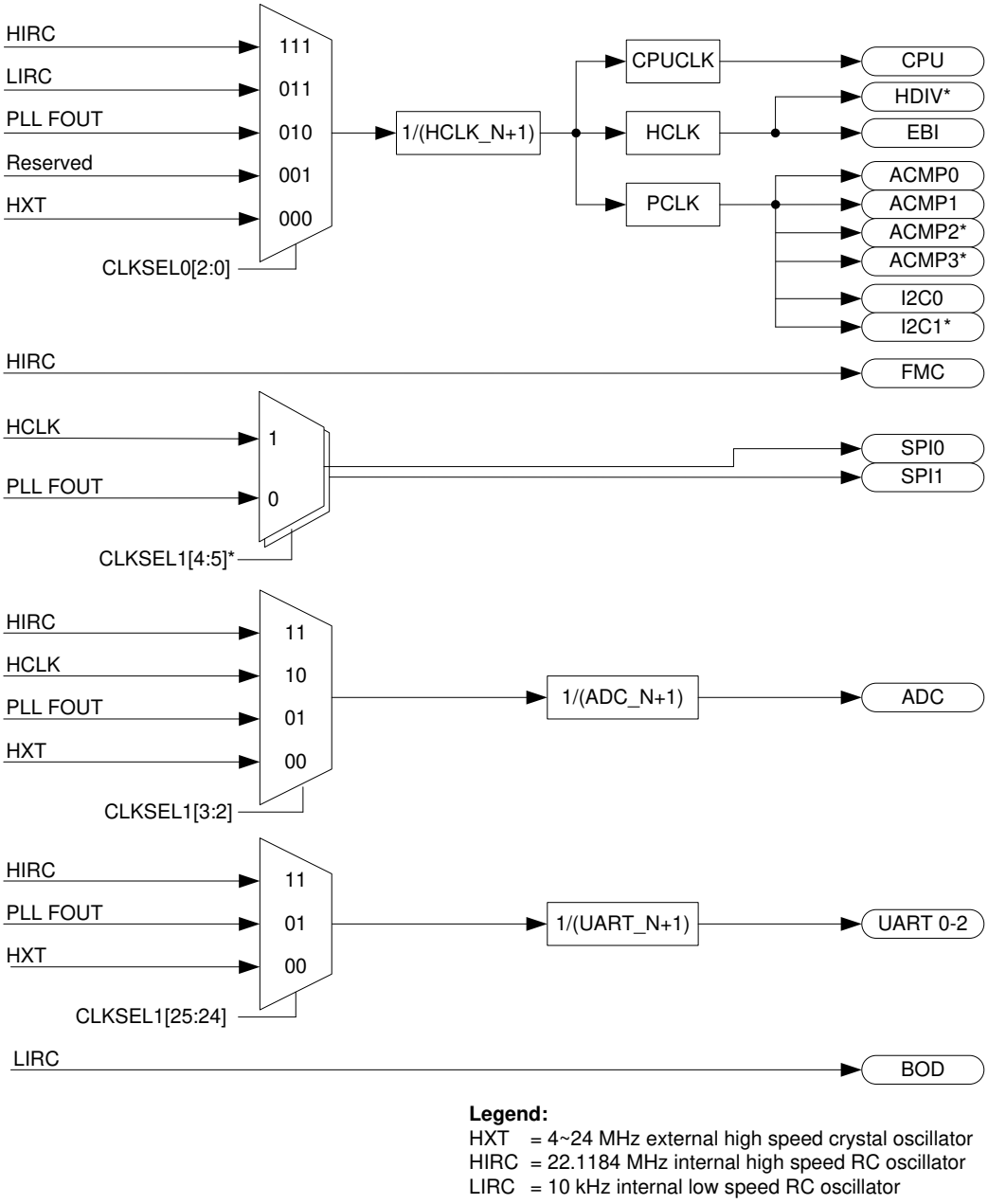
The clock generator consists of 4 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 22.1184 MHz internal high speed oscillator (HIRC)) (PLL FOUT)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)



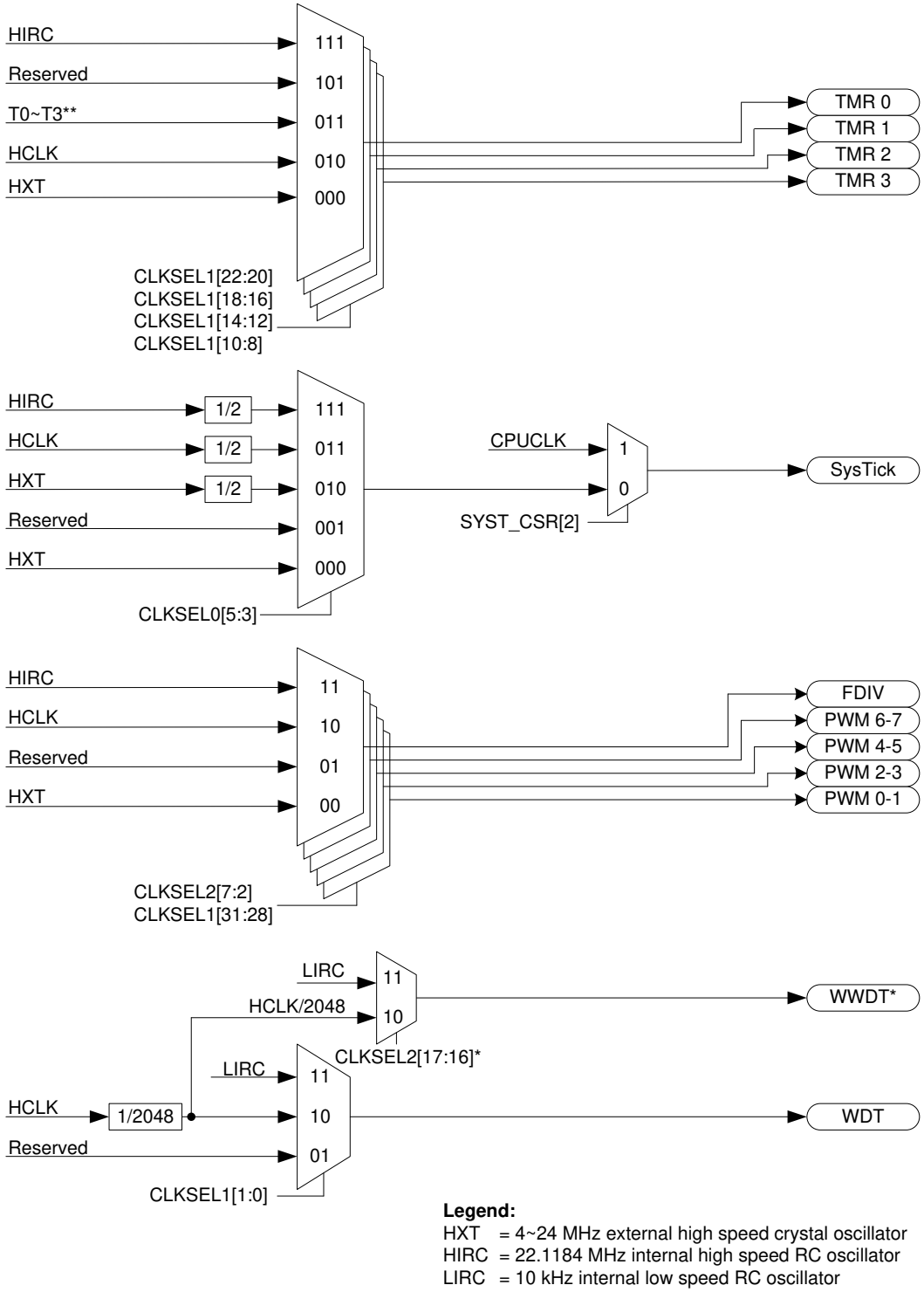
Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-3 Clock Generator Block Diagram



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-4 Clock Source Controller Overview (1/2)



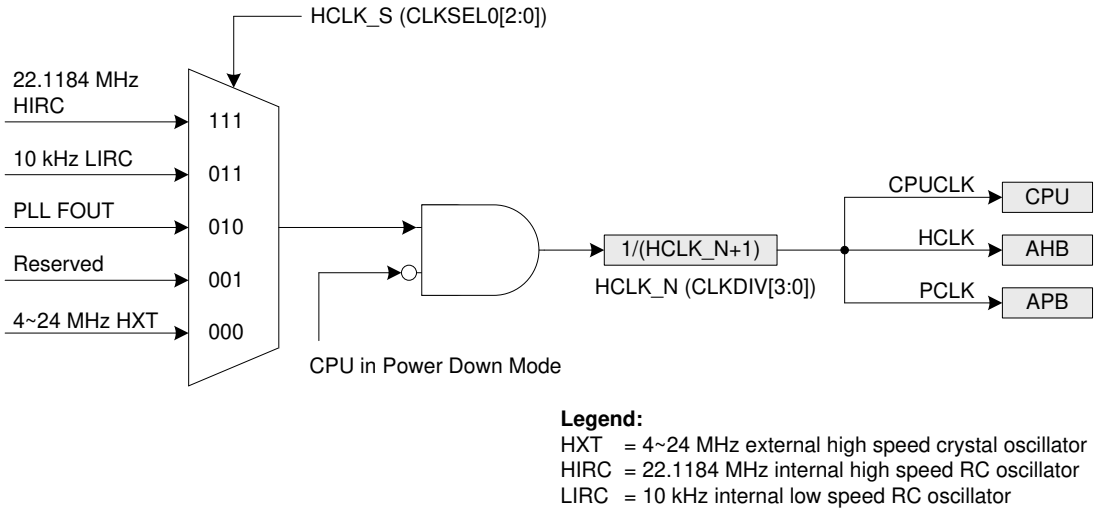
Note1: T0 is for TMR0, T1 is for TMR1, T2 is for TMR2 and T3 is for TMR3.

Note2: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-5 Clock Source Controller Overview (2/2)

6.3.2 System Clock and SysTick Clock

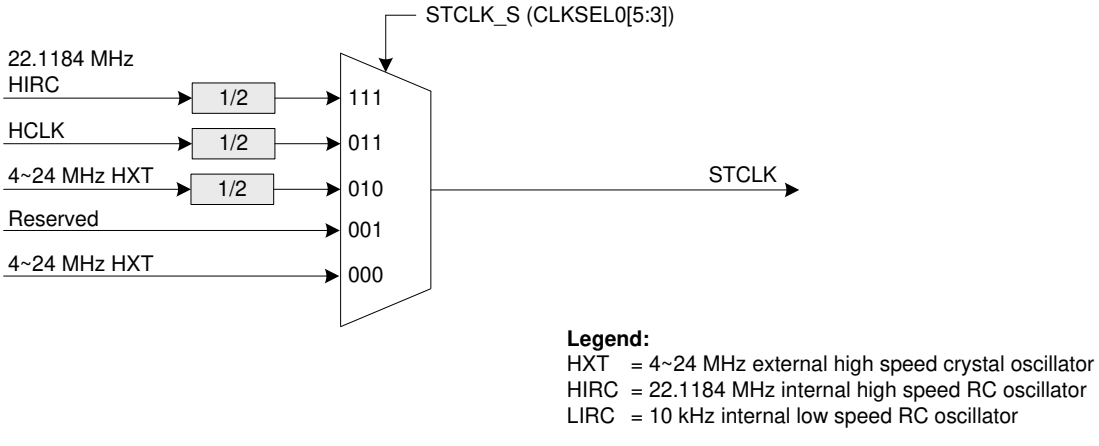
The system clock has 4 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown below.



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-6 System Clock Block Diagram

The clock source of SysTick in Cortex-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]. The block diagram is shown below.



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-7 SysTick clock Control Block Diagram

6.3.3 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator clock
- Peripherals Clock (when 10 kHz low speed oscillator is adopted as clock source)

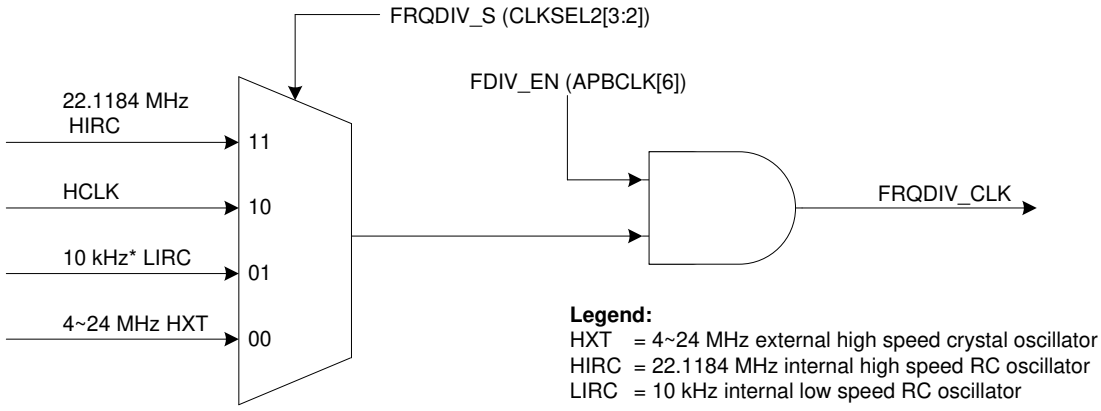
6.3.4 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\boldsymbol{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV [3:0]).

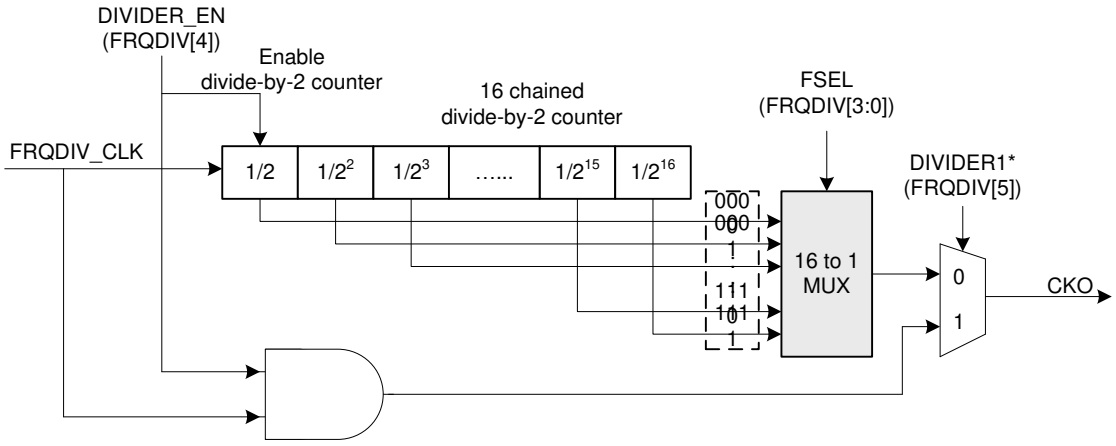
When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1(FRQDIV[5]) set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CKO pin directly.



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-8 Clock Source of Frequency Divider



Note1: DIVIDER1 = 1 is only available on M05xxDE.
Note2: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-9 Block Diagram of Frequency Divider

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The M05xxDN/DE are equipped with 64/32/16/8 Kbytes on chip embedded Flash memory for application program (APROM) that can be updated through ISP registers. In-System-Programming (ISP) and In-Application-Programming (IAP) enable user to update program memory when chip is soldered on PCB. After chip power on Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the M05xxDN/DE also provide additional 4 Kbytes DATA Flash for user to store some application depended data before chip power off in 64/32/16/8 Kbytes APROM model.

The M05xxDN/DE provides more settings in CONFIG0 to support more advanced functions, including power-on with tri-state I/O, default to enable WDT after booting, enable WDT in Power-down mode, and IAP functions.

6.4.2 Features

- Runs up to 50 MHz with zero wait state for continuous address read access
- 64/32/16/8 Kbytes application program memory (APROM)
- 4 Kbytes in system programming (ISP) loader program memory (LDROM)
- Fixed 4 Kbytes Data Flash
- All embedded flash memory supports 512 bytes page erase
- In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM

6.5 External Bus Interface (EBI)

6.5.1 Overview

The NuMicro® M05xxDN/DE LQFP-48 package has an external bus interface (EBI) for access external device.

To save the connections between external device and this chip, EBI supports address bus and data bus multiplex mode which is differentiated by address latch enable signal.

6.5.2 Features

The External Bus Interface has the following functions:

- Supports external devices with max. 64 KB size (8-bit data width) / 128 KB (16-bit data width)
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports 8-bit or 16-bit data width
- Supports variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD)
- Supports address bus and data bus multiplex mode to save the address pins
- Supports configurable idle cycle for different access condition: Write command finish (W2X), Read-to-Read (R2R)
- Supports zero address hold time with read/write operation and write buffer for write operation to enhance read/write performance

6.6 General Purpose I/O (GPIO)

6.6.1 Overview

The NuMicro® M05xxDN/DE has up to 40 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 40 pins are arranged in 5 ports named as P0, P1, P2, P3 and P4. Each port has the maximum of 8 pins. Each of the 40 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each pin can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins is stay in quasi-bidirectional mode and each port data register Px_DOUT[7:0] resets to 0x000_00FF. Each I/O pin has a very weakly individual pull-up resistor which is about 110 kΩ ~ 300 kΩ for V_{DD} which is from 5.0 V to 2.5 V.

6.6.2 Features

- Four I/O modes:
  - Input only with high impedance
  - Push-pull output
  - Open-drain output
- Quasi-bidirectional TTL/Schmitt trigger input mode selected by Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function
- Configurable default I/O mode of all pins after reset by CIOINI(CONFIG[10]) setting
  - CIOINI = 0, all GPIO pins in Input tri-state mode after chip reset
  - CIOINI = 1, all GPIO pins in Quasi-bidirectional mode after chip reset

6.7 Timer Controller (TMR)

6.7.1 Overview

The Timer Controller includes four 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.7.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides four timer counting modes: one-shot, periodic, toggle and continuous counting
- Time-out period = (Period time of timer clock input) * (8-bit prescale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period time of timer clock
- 24-bit up counter value is readable through TDR (Timer Data Register)
- Supports event counting function to count the input event from external counter pin (T0~T3)
- 24-bit capture value is readable through TCAP (Timer Capture Data Register)
- Supports external capture pin (T0EX~T3EX) for interval measurement
- Supports external capture pin (T0EX~T3EX) to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode

6.8 PWM Generator and Capture Timer (PWM)

6.8.1 Overview

The NuMicro® M051 DN/DE series has two sets of PWM groups supporting a total of four sets of PWM generators, which can be configured as eight independent PWM outputs, PWM0~PWM7, or as four complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable Dead-zone generators.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM counters for PWM period control, two 16-bit comparators for PWM duty control and one Dead-zone generator. The 4 sets of PWM generators provide eight independent PWM period interrupt flags set by hardware when the corresponding PWM period down counter reaches 0. Each PWM period interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When DZEN01 (PCR[4]) is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM period, duty and Dead-zone are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively. Refer to figures below for the architecture of PWM Timers.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers, the updated value will be loaded into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM-Timer is set as Auto-reload mode when the down counter reaches 0, it is reloaded with PWM Counter Register (CNRx) automatically and then starts decreasing repeatedly. If the PWM-Timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-Timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM0 and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must set the PWM-Timer before enabling the Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CRL_IE0 (CCR0[1]) (Rising latch Interrupt enable) and CFL_IE0 (CCR0[2]) (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CRL_IE1 (CCR0[17]) and CFL_IE1 (CCR0[18]). The capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, including: Read PIIR to get interrupt source, read CRLRx/CFLRx (x = 0~3) to get capture value and finally write 1 to clear PIIR to 0. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0.

6.8.2 Features

PWM function:

PWM group has two PWM generators. Each PWM generator supports one 8-bit prescaler, one clock divider, two PWM-Timers (down counter), one dead-zone generator and two PWM outputs.

- Up to 2 PWM groups (PWMA/PWMB) to support 8 PWM channels or 4 complementary PWM paired channels
- Each PWM group has two PWM generators with each PWM generator supporting one 8-bit prescaler, two clock dividers, two PWM-Timers, one Dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- One-shot or Auto-reload mode
- Edge-aligned type or Center-aligned type option
- PWM trigger ADC start-to-conversion

Capture function:

- Timing control logic shared with PWM generators
- Supports 8 Capture input channels shared with 8 PWM output channels
- Each channel supports one rising latch register (CRLRx), one falling latch register (CFLRx) and Capture interrupt flag (CAPIFx)

6.9 Watchdog Timer (WDT)

6.9.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.9.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable Watchdog Timer reset delay period 3/18/130/1026 * WDT_CLK
- Supports to force Watchdog Timer enabled after chip powered on or reset while CWDTEN (CONFIG[31] Watchdog Enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

6.10 Window Watchdog Timer (WWDT)

6.10.1 Overview

The Window Watchdog Timer is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.10.2 Features

- 6-bit down counter value (WWDTCVAL) and 6-bit compare window value (WINCMP) to make the WWDT time-out window period flexible
- Supports 4-bit value to programmable maximum 11-bit prescale counter period of WWDT counter

6.11 UART Controller (UART)

6.11.1 Overview

The NuMicro® M05xxDN/DE provides two channels of Universal Asynchronous Receiver/Transmitters (UART). UART Controller performs Normal Speed UART, and support flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, LIN master/slave function and RS-485 function mode. Each UART Controller channel supports seven types of interrupts.

6.11.2 Features

- Full-duplex, asynchronous communications
- Separate receive / transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control and flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UA_TOR [15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enable to program RTS pin to control RS-485 transmission direction directly

6.12 I²C Serial Interface Controller (I²C)

6.12.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. There are two sets of I²C which supports Power-down wake-up function.

6.12.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between master and slave
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clocks allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down Wake-up function

6.13 Serial Peripheral Interface (SPI)

6.13.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full-duplex transfer. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. The NuMicro® M051 DN/DE series contains up to two sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device.

6.13.2 Features

- Up to two sets of SPI controllers
- Supports Master or Slave mode operation
- Configurable transfer bit length
- Provides FIFO buffers
- Supports MSB or LSB first transfer
- Supports byte reorder function
- Supports byte or word suspend mode
- Supports Slave 3-wire mode
- SPI bus clock rate can be configured to equal the system clock rate

6.14 Analog-to-Digital Converter (ADC)

6.14.1 Overview

The NuMicro® M05xxDN/DE contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with eight input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (STADC/P3.2) or PWM trigger.

6.14.2 Features

- Analog input voltage range: 0 ~ AV_{DD}
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to eight single-end analog input channels or 4 differential analog input channels
- Maximum ADC peripheral clock frequency is 16 MHz
- Up to 760 kSPS sample rate
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - PWM trigger with optional start delay period
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- Channel 7 supports 3 input sources: external analog voltage, internal band-gap voltage and
- Internal temperature sensor output.

6.15 Analog Comparator (ACMP)

6.15.1 Overview

The NuMicro® M05xxDN/DE contains up to four comparators which can be used in a number of different configurations. The comparator output is logic 1 when positive input greater than negative input, otherwise the output is 0. Each comparator can be configured to generate interrupt request when the comparator output value changes.

6.15.2 Features

- Up to four sets of ACMP
- Analog input voltage range: 0 ~ AV_{DD}
- Supports Hysteresis function
- Supports ACMP output inverse Function (M05xxDE only)
- Optional internal reference voltage source for each comparator negative input
- Two interrupt vectors for the four analog comparators

6.16 Hardware Divider (HDIV) (M05xxDN/DE Only)

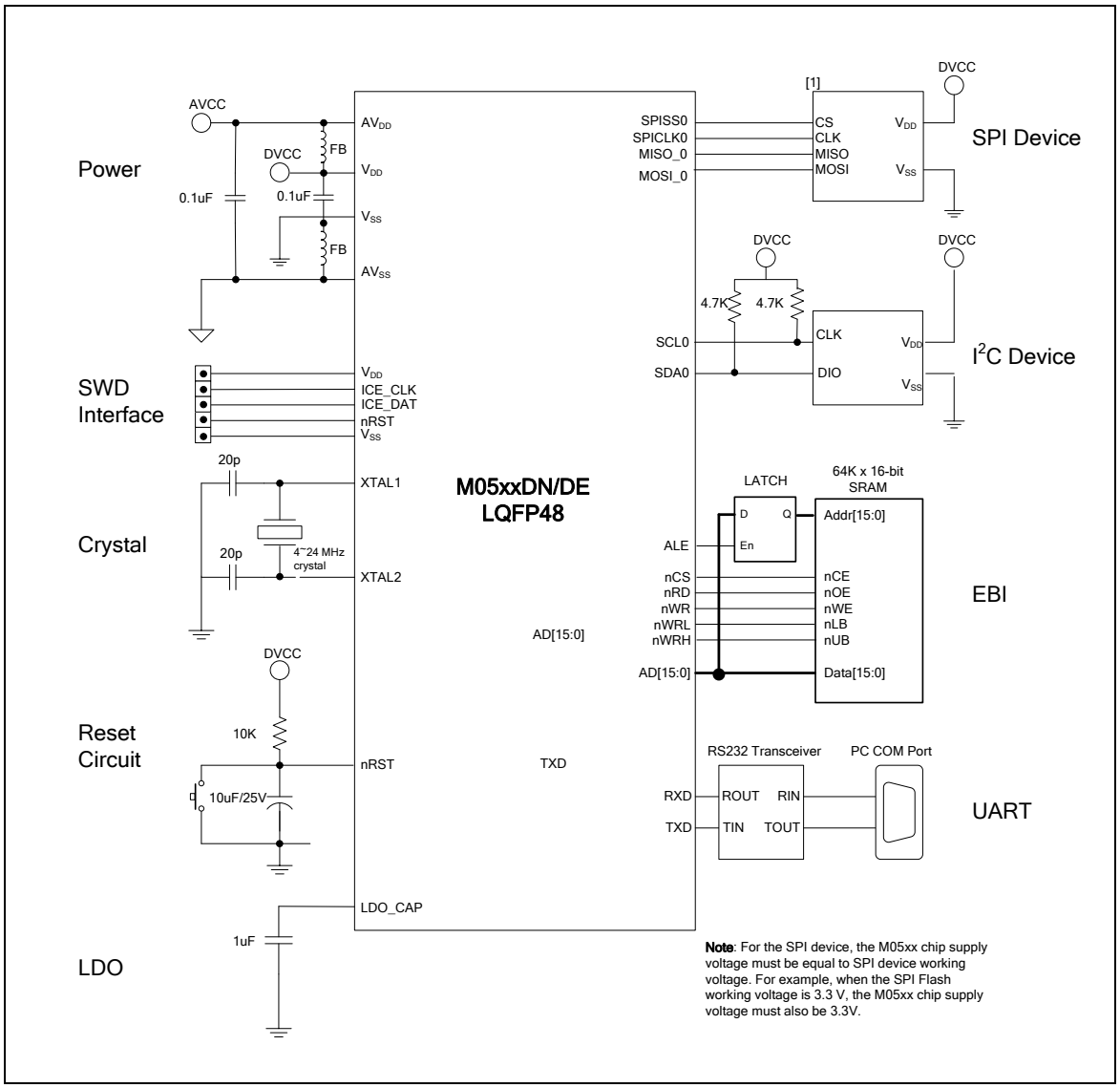
6.16.1 Overview

The hardware divider (HDIV) is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

6.16.2 Features

- Signed (two's complement) integer calculation
- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- 6 HCLK clocks taken for one cycle calculation
- Write divisor to trigger calculation
- Waiting for calculation ready automatically when reading quotient and remainder

7 APPLICATION CIRCUIT



8 M05XXDN ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD} - V_{SS}$	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+85	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

8.2 DC Electrical Characteristics

(V_{DD} - V_{SS} = 2.5 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions				
V_{DD}	Operation voltage	2.5	-	5.5	V	V_{DD} = 2.5 V ~ 5.5 V up to 50 MHz				
V_{SS} / AV_{SS}	Power Ground	-0.3	-	-	V					
V_{LDO}	LDO Output Voltage	1.62	1.8	1.98	V	V_{DD} ≥ 2.5 V				
V_{BG}	Band-gap Voltage	1.16	1.20	1.24	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = 25°C				
		1.14	1.20	1.26	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = -40°C~85°C				
V_{DD}-AV_{DD}	Allowed Voltage Difference for V_{DD} and AV_{DD}	-0.3	0	0.3	V	-				
I_{DD1}	Operating Current Normal Run Mode HCLK = 50 MHz while(1){} Executed from Flash	-	21	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	12 MHz	X	V	V
I_{DD2}		-	15	-	mA	5.5V	12 MHz	X	V	X
I_{DD3}		-	20	-	mA	3.3V	12 MHz	X	V	V
I_{DD4}		-	13	-	mA	3.3V	12 MHz	X	V	X
I_{DD5}	Operating Current Normal Run Mode HCLK =22.1184 MHz while(1){} Executed from Flash	-	6.6	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	X	V	X	V
I_{DD6}		-	3.7	-	mA	5.5V	X	V	X	X
I_{DD7}		-	6.4	-	mA	3.3V	X	V	X	V
I_{DD8}		-	3.6	-	mA	3.3V	X	V	X	X
I_{DD9}	Operating Current Normal Run Mode HCLK = 12 MHz while(1){} Executed from Flash	-	5.4	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	12 MHz	X	X	V
I_{DD10}		-	3.6	-	mA	5.5V	12 MHz	X	X	X
I_{DD11}		-	4.0	-	mA	3.3V	12 MHz	X	X	V
I_{DD12}		-	2.3	-	mA	3.3V	12 MHz	X	X	X
I_{DD13}	Operating Current Normal Run Mode HCLK =4 MHz while(1){} Executed from Flash	-	3.3	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	4 MHz	X	X	V
I_{DD14}		-	2.5	-	mA	5.5V	4 MHz	X	X	X
I_{DD15}		-	2.0	-	mA	3.3V	4 MHz	X	X	V
I_{DD16}		-	1.3	-	mA	3.3V	4 MHz	X	X	X

I_{DD17}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	110	-	µA	V_{DD}	HXT	HIRC	LIRC	PLL	All digital modules
						5.5V	X	X	V	X	V[4]
I_{DD18}		-	105	-	µA	5.5V	X	X	V	X	X
I_{DD19}		-	92	-	µA	3.3V	X	X	V	X	V[4]
I_{DD20}		-	90	-	µA	3.3V	X	X	V	X	X
I_{IDLE1}	Operating Current Idle Mode HCLK = 50 MHz	-	17	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	12 MHz	X	V	V	
I_{IDLE2}		-	10	-	mA	5.5V	12 MHz	X	V	X	
I_{IDLE3}		-	15	-	mA	3.3V	12 MHz	X	V	V	
I_{IDLE4}		-	8	-	mA	3.3V	12 MHz	X	V	X	
I_{IDLE5}	Operating Current Idle Mode HCLK =22.1184 MHz	-	4.5	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	X	V	X	V	
I_{IDLE6}		-	1.6	-	mA	5.5V	X	V	X	X	
I_{IDLE7}		-	4.4	-	mA	3.3V	X	V	X	V	
I_{IDLE8}		-	1.6	-	mA	3.3V	X	V	X	X	
I_{IDLE9}	Operating Current Idle Mode HCLK =12 MHz	-	4.1	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	12 MHz	X	X	V	
I_{IDLE10}		-	2.4	-	mA	5.5V	12 MHz	X	X	X	
I_{IDLE11}		-	2.8	-	mA	3.3V	12 MHz	X	X	V	
I_{IDLE12}		-	1.2	-	mA	3.3V	12 MHz	X	X	X	
I_{IDLE13}	Operating Current Idle Mode HCLK =4 MHz	-	2.9	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	4 MHz	X	X	V	
I_{IDLE14}		-	2.1	-	mA	5.5V	4 MHz	X	X	X	
I_{IDLE15}		-	1.6	-	mA	3.3V	4 MHz	X	X	V	
I_{IDLE16}		-	0.9	-	mA	3.3V	4 MHz	X	X	X	
I_{IDLE17}	Operating Current Idle Mode at 10 kHz	-	106	-	µA	V_{DD}	HXT	HIRC	LIRC	PLL	All digital modules
						5.5V	X	X	V	X	V[4]
I_{IDLE18}		-	104	-	µA	5.5V	X	X	V	X	X
I_{IDLE19}		-	90	-	µA	3.3V	X	X	V	X	V[4]
I_{IDLE20}		-	89	-	µA	3.3V	X	X	V	X	X
I_{PWD1}	Standby Current	-	10	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.					

I_{PWD2}	Power-down Mode (Deep Sleep Mode)	-	8	-	μA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off.
I_{IL}	Logic 0 Input Current P0/1/2/3/4 (Quasi-bidirectional Mode)	-	-65	-75	μA	V_{DD} = 5.5 V, V_{IN} = 0V
I_{TL}	Logic 1 to 0 Transition Current P0/1/2/3/4 (Quasi-bidirectional Mode) [*3]	-	-690	-750	μA	V_{DD} = 5.5 V, V_{IN} = 2.0V
I_{LK}	Input Leakage Current P0/1/2/3/4	-1	-	+1	μA	V_{DD} = 5.5 V, 0 < V_{IN} < V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage P0/1/2/3/4 (TTL Input)	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
V_{IH1}	Input High Voltage P0/1/2/3/4 (TTL Input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{IL3}	Input Low Voltage XTAL1[*2]	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 2.5 V
V_{IH3}	Input High Voltage XTAL1[*2]	3.5	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{ILS}	Negative-going Threshold (Schmitt Input), nRST	-0.3	-	0.2 V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), nRST	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
R_{RST}	Internal nRST Pin Pull-up Resistor	40		150	kΩ	-
V_{ILS}	Negative-going Threshold (Schmitt input), P0/1/2/3/4	-0.3	-	0.3 V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt input), P0/1/2/3/4	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
I_{SR11}	Source Current P0/1/2/3/4 (Quasi-bidirectional Mode)	-300	-420	-	μA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR12}		-50	-75	-	μA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR13}		-40	-67	-	μA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SR21}	Source Current P0/1/2/3/4 (Push-pull Mode)	-20	-26	-	mA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR22}		-3	-5	-	mA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR23}		-2.5	-4.2	-	mA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SK11}	Sink Current P0/1/2/3/4 (Quasi-bidirectional, Open-	10	16	-	mA	V_{DD} = 4.5 V, V_S = 0.45 V
I_{SK12}		6	9	-	mA	V_{DD} = 2.7 V, V_S = 0.45 V

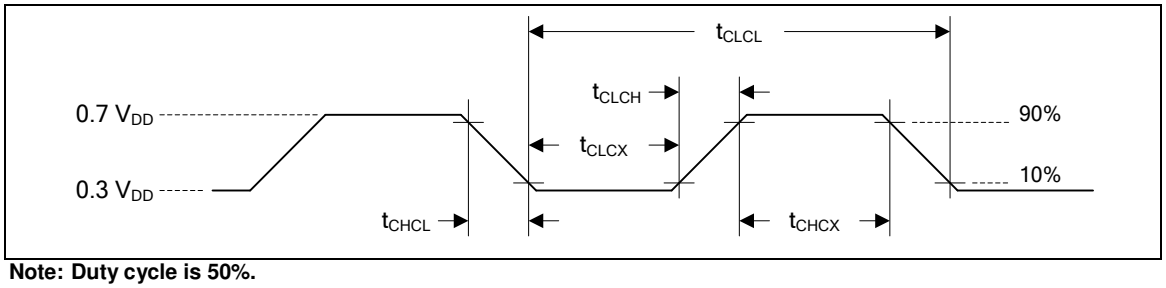
I_{SK13}	Drain and Push-pull Mode)	5	8	-	mA	V_{DD} = 2.5 V, V_S = 0.45 V

Notes:

1. nRST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when V_{IN} approximates to 2V.
4. Only enable modules which support 10 kHz LIRC clock source.

8.3 AC Electrical Characteristics

8.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

8.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Condition
V_{HXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	85	℃	-
I_{HXT}	Operating Current	-	2	-	mA	12 MHz, V_{DD} = 5.5V
		-	0.8	-	mA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

8.3.3 Typical Crystal Application Circuits

Crystal	C1	C2
4 MHz ~ 24 MHz	10~20 pF	10~20 pF

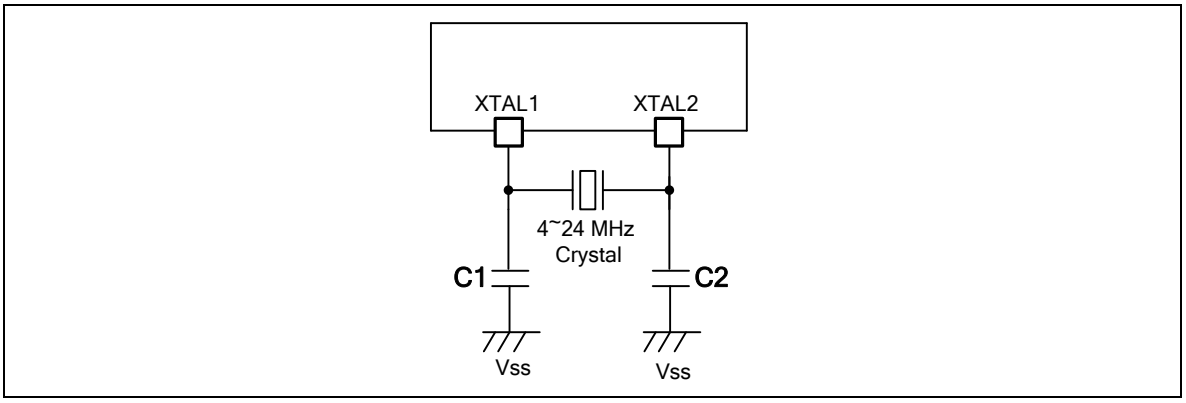


Figure 8-1 M05xxDN Typical Crystal Application Circuit

8.3.4 22.1184 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	22.1184	-	MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5 V
		-3	-	+3	%	T_A = -40 ℃ ~ 85 ℃ V_{DD} = 2.5 V ~ 5.5 V
I_{HRC}	Operating Current	-	800	-	μA	T_A = 25 ℃,V_{DD} = 5 V

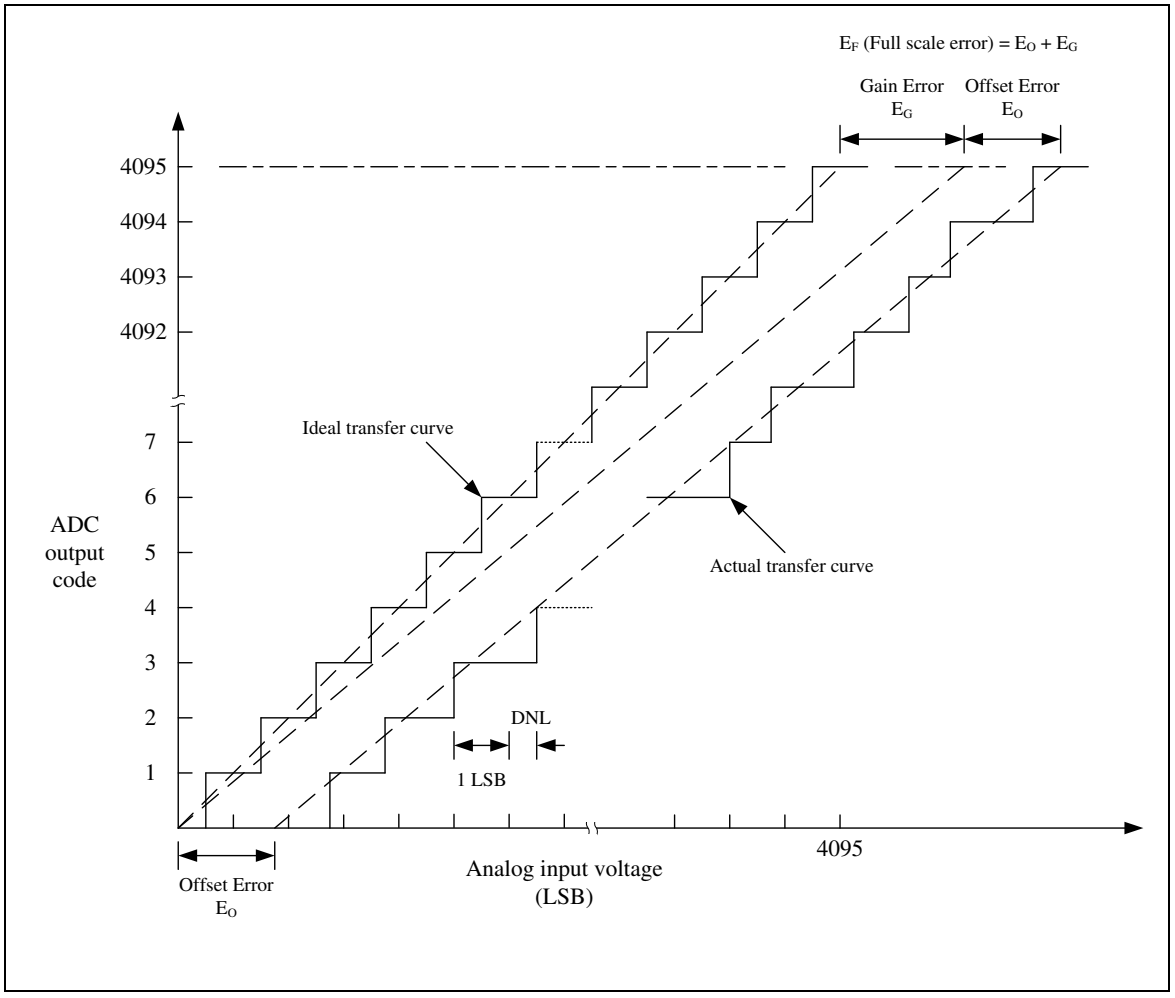
8.3.5 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{LRC}	Supply Voltage	2.5	-	5.5	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-10	-	+10	%	V_{DD} = 2.5 V ~ 5.5 V T_A = 25℃
		-40	-	+40	%	V_{DD} = 2.5 V ~ 5.5 V T_A = -40℃ ~ +85℃

8.4 Analog Characteristics

8.4.1 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	±1	-1~+4	LSB	-
INL	Integral Nonlinearity Error	-	±2	±4	LSB	-
E_O	Offset Error	-	2	4	LSB	-
E_G	Gain Error (Transfer Gain)	-	-2	-4	LSB	-
E_A	Absolute Error	-	3	4	LSB	-
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency	-	-	16	MHz	AV_{DD} = 4.5~5.5 V
		-	-	8		AV_{DD} = 2.5~5.5 V
F_S	Sample Rate (F_{ADC}/T_{CONV})	-	-	800	kSPS	AV_{DD} = 4.5~5.5 V
		-	-	400	kSPS	AV_{DD} = 2.5~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	7			$1/F_{ADC}$	-
T_{CONV}	Total Conversion Time	20			$1/F_{ADC}$	-
AV_{DD}	Supply Voltage	2.5	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	2.9	-	mA	AV_{DD} = 5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	3.2	-	pF	-
R_{IN}	Input Load	-	6	-	kΩ	-



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.5	-	5.5	V	-
V_{LDO}	Output Voltage	1.62	1.8	1.98	V	-
T_A	Temperature	-40	25	85	℃	-
C_{LDO}	Capacitor	-	1	-	μF	R_{ESR} = 1Ω

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1μF or higher capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

8.4.3 Low Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	85	℃	-
I_{LVR}	Quiescent Current	-	1	5	μA	AV_{DD} = 5.5 V
V_{LVR}	Threshold Voltage	1.90	2.00	2.20	V	T_A = 25 ℃
		2.00	2.10	2.40	V	T_A = -40 ℃
		1.70	1.90	2.10	V	T_A = 85 ℃

8.4.4 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	85	℃	-
I_{BOD}	Quiescent Current	-	-	140	μA	AV_{DD} = 5.5 V
V_{BOD}	Brown-out Voltage (Falling edge)	4.2	4.38	4.55	V	BOV_VL [1:0] = 11
		3.5	3.68	3.85	V	BOV_VL [1:0] = 10
		2.5	2.68	2.85	V	BOV_VL [1:0] = 01
		2.0	2.18	2.35	V	BOV_VL [1:0] = 00
V_{BOD}	Brown-out Voltage (Rising edge)	4.3	4.52	4.75	V	BOV_VL [1:0] = 11
		3.5	3.8	4.05	V	BOV_VL [1:0] = 10
		2.5	2.77	3.05	V	BOV_VL [1:0] = 01
		2.0	2.25	2.55	V	BOV_VL [1:0] = 00

8.4.5 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	-
V_{POR}	Reset Voltage	-	2	-	V	V+
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	-	-	100	mV	-
RR_{VDD}	V_{DD} Raising Rate to Ensure Power-on Reset	0.025	-	-	V/ms	-
t_{POR}	Minimum Time for V_{DD} Stays at VPOR to Ensure Power-on Reset	0.5	-	-	ms	-

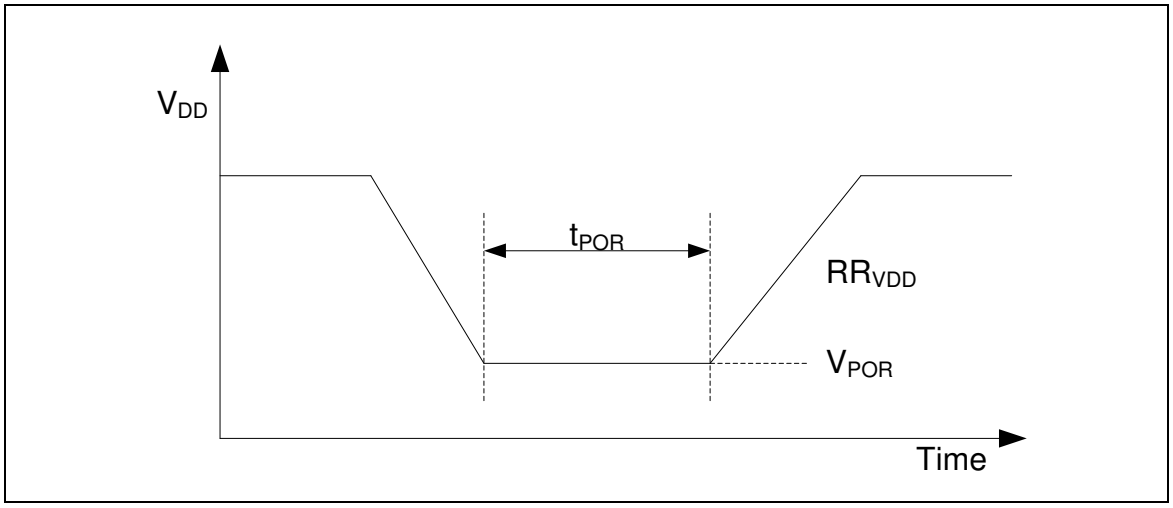


Figure 8-2 Power-up Ramp Condition

8.4.6 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{TEMP}	Supply Voltage	1.62	1.8	1.98	V	
T_A	Temperature	-40	-	85	℃	
I_{TEMP}	Current Consumption	-	16	-	μA	
-	Gain	-1.65	-1.75	-1.85	mV/℃	
-	Offset	714	724	734	mV	T_A = 0 ℃

Note:

The temperature sensor formula for the output voltage (Vtemp) is as below equation.

Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)

8.4.7 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.5		5.5	V	
T_A	Temperature	-40	25	85	℃	-
I_{CMP}	Operation Current	-	50	100	μA	AV_{DD} = 5 V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	AV_{DD} - 0.1	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD} – 0.1	V	-
-	DC Gain	40	70	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{CM} = 1.2 V, V_{DIFF} = 0.1 V
V_{HYS}	Hysteresis	-	±20	±30	mV	
T_{STB}	Stable time	-	-	1	μs	

8.5 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply Voltage	1.62	1.8	1.98	V	
T_{RET}	Data Retention	10	-	-	year	T_A = 85℃
T_{ERASE}	Page Erase Time	-	3	-	ms	
T_{PROG}	Program Time	-	40	-	us	
I_{DD1}	Read Current	-	0.25	-	mA	
I_{DD2}	Program Current	-	7	-	mA	
I_{DD3}	Erase Current	-	20	-	mA	

Notes:

1. V_{FLA} is source from chip LDO output voltage.
2. Guaranteed by design, and not tested in production.

8.6 SPI Dynamic Characteristics

8.6.1 Dynamic Characteristics of Data Input and Output Pin

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI MASTER MODE (V_{DD} = 4.5 V ~ 5.5 V, 30 PF LOADING CAPACITOR)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4	-	-	ns
t_V	Data output valid time	-	9	11	ns
SPI MASTER MODE (V_{DD} = 3.0 V ~ 3.6 V, 30 PF LOADING CAPACITOR)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4	-	-	ns
t_V	Data output valid time	-	19.5	20.5	ns
SPI SLAVE MODE (V_{DD} = 4.5 V ~ 5.5 V, 30 PF LOADING CAPACITOR)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4	-	-	ns
t_V	Data output valid time	-	26	34	ns
SPI SLAVE MODE (V_{DD} = 3.0 V ~ 3.6 V, 30 PF LOADING CAPACITOR)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4	-	-	ns
t_V	Data output valid time	-	44	48	ns

9 M05XXDE ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD} - V_{SS}$	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}	-	120	mA
I_{IO}	Maximum Current sunk by an I/O pin	-	35	mA
	Maximum Current sourced by an I/O pin	-	35	mA
	Maximum Current sunk by total I/O pins	-	100	mA
	Maximum Current sourced by total I/O pins	-	100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

9.2 DC Electrical Characteristics

(V_{DD} - V_{SS} = 2.5 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions				
V_{DD}	Operation voltage	2.5	-	5.5	V	V_{DD} = 2.5 V ~ 5.5 V up to 50 MHz				
V_{SS} / AV_{SS}	Power Ground	-0.3	0	0.3	V					
V_{LDO}	LDO Output Voltage	1.62	1.8	1.98	V	V_{DD} ≥ 2.5 V				
V_{BG}	Band-gap Voltage	1.22	1.25	1.28	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = 25°C				
		1.18	1.25	1.32	V	V_{DD} = 2.5 V ~ 5.5 V, T_A = -40°C~105°C				
V_{DD}-AV_{DD}	Allowed voltage difference for V_{DD} and AV_{DD}	-0.3	0	0.3	V					
I_{DD1}	Operating Current Normal Run Mode HCLK = 50 MHz while(1){} executed from flash	-	21	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	12 MHz	X	V	V
I_{DD2}		-	15	-	mA	5.5V	12 MHz	X	V	X
I_{DD3}		-	20	-	mA	3.3V	12 MHz	X	V	V
I_{DD4}		-	13	-	mA	3.3V	12 MHz	X	V	X
I_{DD5}	Operating Current Normal Run Mode HCLK =22.1184 MHz while(1){} executed from flash	-	6.6	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	X	V	X	V
I_{DD6}		-	3.7	-	mA	5.5V	X	V	X	X
I_{DD7}		-	6.4	-	mA	3.3V	X	V	X	V
I_{DD8}		-	3.6	-	mA	3.3V	X	V	X	X
I_{DD9}	Operating Current Normal Run Mode HCLK = 12 MHz while(1){} executed from flash	-	5.4	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	12 MHz	X	X	V
I_{DD10}		-	3.6	-	mA	5.5V	12 MHz	X	X	X
I_{DD11}		-	4	-	mA	3.3V	12 MHz	X	X	V
I_{DD12}		-	2.3	-	mA	3.3V	12 MHz	X	X	X
I_{DD13}	Operating Current Normal Run Mode HCLK =4 MHz while(1){} executed from flash	-	3.3	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules
						5.5V	4 MHz	X	X	V
I_{DD14}		-	2.5	-	mA	5.5V	4 MHz	X	X	X
I_{DD15}		-	2.0	-	mA	3.3V	4 MHz	X	X	V
I_{DD16}		-	1.3	-	mA	3.3V	4 MHz	X	X	X

I_{DD17}	Operating Current Normal Run Mode HCLK = 10 kHz while(1){} Executed from Flash	-	110	-	µA	V_{DD}	HXT	HIRC	LIRC	PLL	All digital modules
						5.5V	X	X	V	X	V[4]
I_{DD18}		-	105	-	µA	5.5V	X	X	V	X	X
I_{DD19}		-	92	-	µA	3.3V	X	X	V	X	V[4]
I_{DD20}		-	90	-	µA	3.3V	X	X	V	X	X
I_{IDLE1}	Operating Current Idle Mode HCLK = 50 MHz	-	17	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	12 MHz	X	V	V	
I_{IDLE2}		-	10	-	mA	5.5V	12 MHz	X	V	X	
I_{IDLE3}		-	14	-	mA	3.3V	12 MHz	X	V	V	
I_{IDLE4}		-	6	-	mA	3.3V	12 MHz	X	V	X	
I_{IDLE5}	Operating Current Idle Mode HCLK =22.1184 MHz	-	5.2	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	X	V	X	V	
I_{IDLE6}		-	2	-	mA	5.5V	X	V	X	X	
I_{IDLE7}		-	5	-	mA	3.3V	X	V	X	V	
I_{IDLE8}		-	1.8	-	mA	3.3V	X	V	X	X	
I_{IDLE9}	Operating Current Idle Mode HCLK =12 MHz	-	4.3	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	12 MHz	X	X	V	
I_{IDLE10}			2.4		mA	5.5V	12 MHz	X	X	X	
I_{IDLE11}		-	3.2	-	mA	3.3V	12 MHz	X	X	V	
I_{IDLE12}		-	1.3	-	mA	3.3V	12 MHz	X	X	X	
I_{IDLE13}	Operating Current Idle Mode HCLK =4 MHz	-	2.9	-	mA	V_{DD}	HXT	HIRC	PLL	All digital modules	
						5.5V	4 MHz	X	X	V	
I_{IDLE14}		-	2.1	-	mA	5.5V	4 MHz	X	X	X	
I_{IDLE15}		-	1.8	-	mA	3.3V	4 MHz	X	X	V	
I_{IDLE16}		-	1	-	mA	3.3V	4 MHz	X	X	X	
I_{IDLE17}	Operating Current Idle Mode at 10 kHz	-	106	-	µA	V_{DD}	HXT	HIRC	LIRC	PLL	All digital modules
						5.5V	X	X	V	X	V[4]
I_{IDLE18}		-	104	-	µA	5.5V	X	X	V	X	X
I_{IDLE19}		-	90	-	µA	3.3V	X	X	V	X	V[4]
I_{IDLE20}		-	89	-	µA	3.3V	X	X	V	X	X
I_{PWD1}	Standby Current	-	10	-	µA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.					

I_{PWD2}	Power-down Mode (Deep Sleep Mode)	-	8	-	µA	V_{DD} = 3.3 V, All oscillators and analog blocks turned off.
I_{IL}	Logic 0 Input Current P0/1/2/3/4 (Quasi-bidirectional mode)	-	-65	-75	µA	V_{DD} = 5.5 V, V_{IN} = 0V
I_{TL}	Logic 1 to 0 Transition Current P0/1/2/3/4 (Quasi-bidirectional mode) [*3]	-	-510	-650	µA	V_{DD} = 5.5 V, V_{IN} = 2.0V
I_{LK}	Input Leakage Current P0/1/2/3/4	-1	-	+1	µA	V_{DD} = 5.5 V, 0 < V_{IN} < V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage P0/1/2/3/4 (TTL input)	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
V_{IH1}	Input High Voltage P0/1/2/3/4 (TTL input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{IL3}	Input Low Voltage XT1[*2]	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 2.5 V
V_{IH3}	Input High Voltage XT1[*2]	3.5	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{ILS}	Negative going threshold (Schmitt input), nRST	-0.3	-	0.2 V_{DD}	V	
V_{IHS}	Positive going threshold (Schmitt input), nRST	0.7 V_{DD}	-	V_{DD} + 0.3	V	
R_{RST}	Internal nRST pin pull up resistor	40		150	kΩ	
V_{ILS}	Negative going threshold (Schmitt input), P0/1/2/3/4	-0.3	-	0.3 V_{DD}	V	
V_{IHS}	Positive going threshold (Schmitt input), P0/1/2/3/4	0.7 V_{DD}	-	V_{DD} + 0.3	V	
I_{SR11}	Source Current P0/1/2/3/4 (Quasi-bidirectional Mode)	-300	-370	-	µA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR12}		-50	-70	-	µA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR13}		-40	-60	-	µA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SR21}	Source Current P0/1/2/3/4 (Push-pull Mode)	-20	-25	-	mA	V_{DD} = 4.5 V, V_S = 2.4 V
I_{SR22}		-3	-5	-	mA	V_{DD} = 2.7 V, V_S = 2.2 V
I_{SR23}		-2.5	-4.5	-	mA	V_{DD} = 2.5 V, V_S = 2.0 V
I_{SK11}	Sink Current P0/1/2/3/4 (Quasi-bidirectional, Open-	10	15	-	mA	V_{DD} = 4.5 V, V_S = 0.45 V
I_{SK12}		6	9	-	mA	V_{DD} = 2.7 V, V_S = 0.45 V

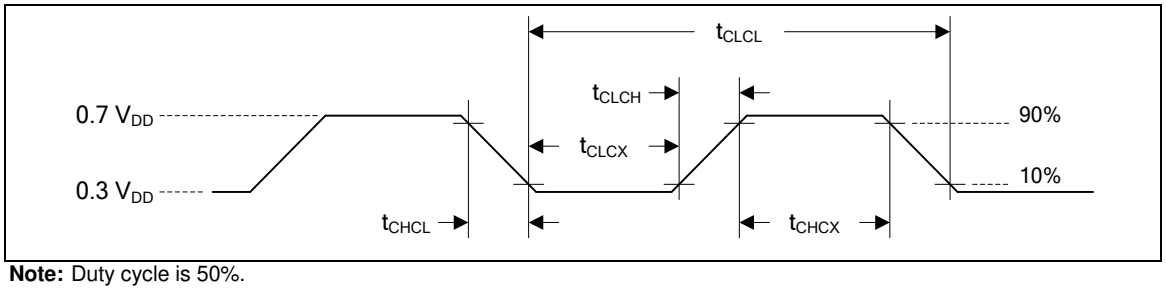
I_{SK13}	Drain and Push-pull Mode)	5	8	-	mA	V_{DD} = 2.5 V, V_S = 0.45 V

Notes:

1. nRST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when V_{IN} approximates to 2V.
4. Only enable modules which support 10 kHz LIRC clock source.

9.3 AC Electrical Characteristics

9.3.1 External Input Clock



Note: Duty cycle is 50%.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_{CHCX}	Clock High Time	10	-	-	ns	-
t_{CLCX}	Clock Low Time	10	-	-	ns	-
t_{CLCH}	Clock Rise Time	2	-	15	ns	-
t_{CHCL}	Clock Fall Time	2	-	15	ns	-

9.3.2 External 4~24 MHz High Speed Crystal (HXT)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.5	-	5.5	V	-
T_A	Temperature	-40	-	105	℃	-
I_{HXT}	Operating Current	-	2	-	mA	12 MHz, V_{DD} = 5.5V
		-	0.8	-	mA	12 MHz, V_{DD} = 3.3V
f_{HXT}	Clock Frequency	4	-	24	MHz	-

9.3.3 Typical Crystal Application Circuits

Crystal	C1	C2
4 MHz ~ 24 MHz	10~20 pF	10~20 pF

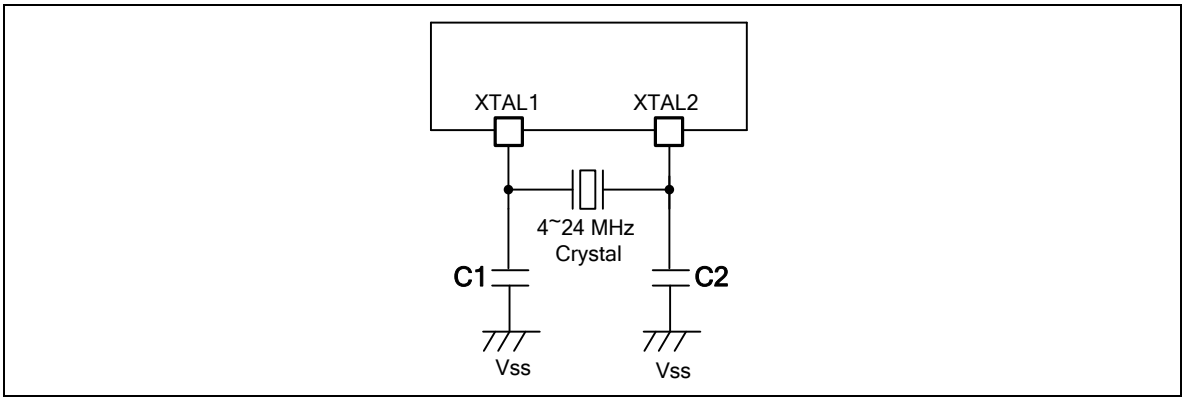


Figure 9-1 M05xDE Typical Crystal Application Circuit

9.3.4 22.1184 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	22.1184		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5 V
		-2	-	+2	%	T_A = -40 ℃ ~ 105 ℃ V_{DD} = 2.5 V ~ 5.5 V
I_{HRC}	Operating Current	-	800	-	μA	T_A = 25 ℃, V_{DD} = 5 V

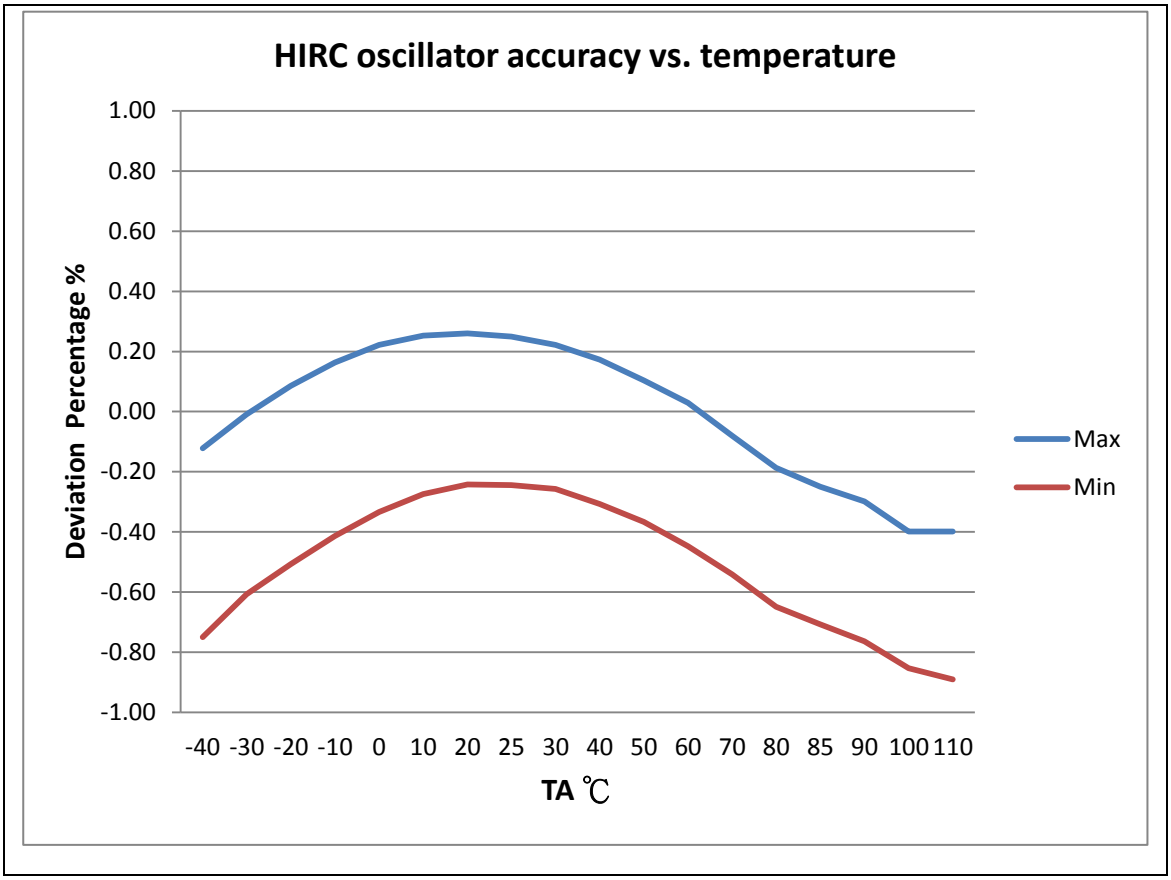


Figure 9-2 HIRC Accuracy vs. Temperature

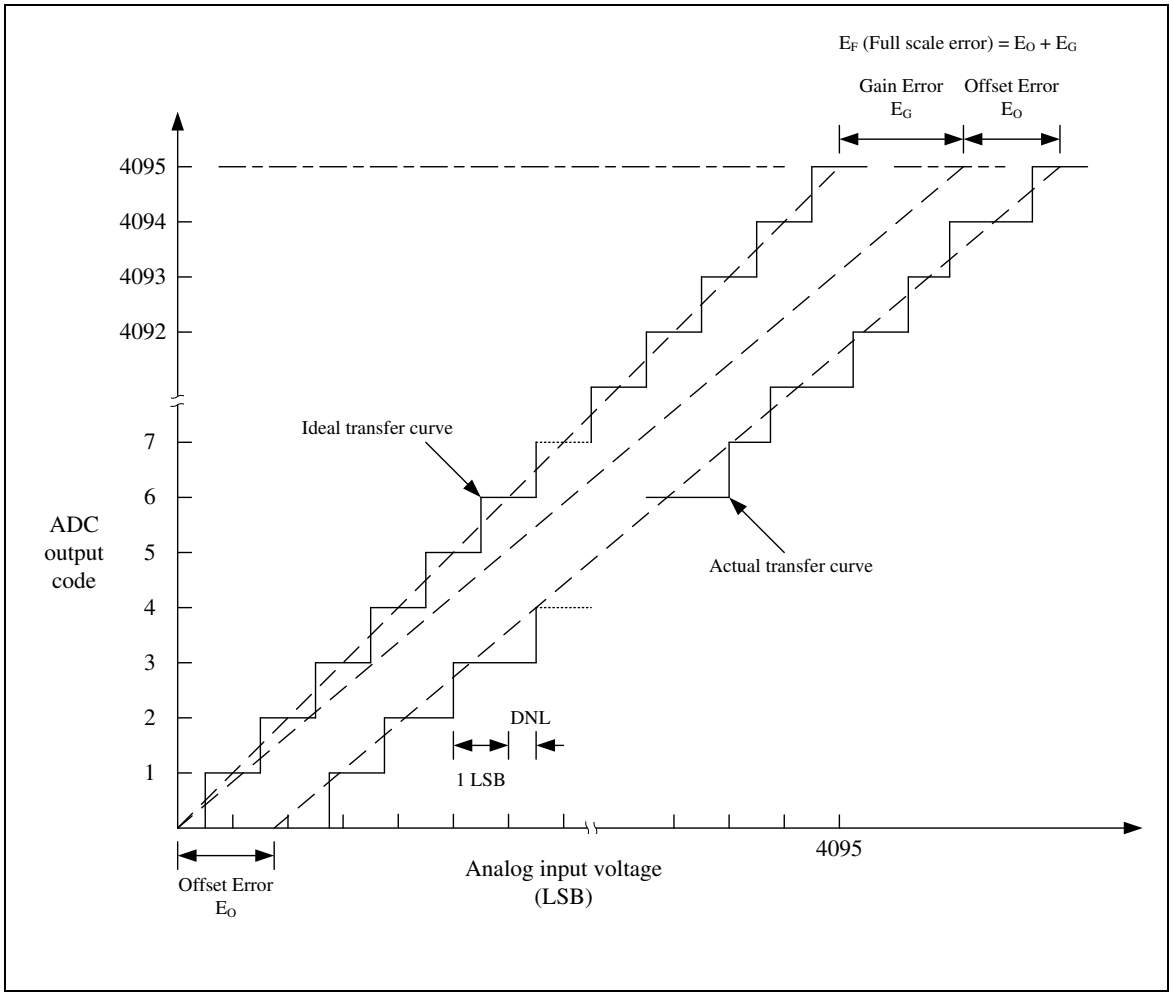
9.3.5 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	2.5	-	5.5	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	-
	Oscillator Frequency	-10	-	+10	%	V_{DD} = 2.5 V ~ 5.5 V T_A = 25℃
		-40	-	+40	%	V_{DD} = 2.5 V ~ 5.5 V T_A = -40℃ ~ +105℃

9.4 Analog Characteristics

9.4.1 12-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	12	Bit	-
DNL	Differential Nonlinearity Error	-	±1	-1~+4	LSB	-
INL	Integral Nonlinearity Error	-	±2	±4	LSB	-
E_O	Offset Error	-	2	4	LSB	-
E_G	Gain Error (Transfer Gain)	-	-2	-4	LSB	-
E_A	Absolute Error	-	3	4	LSB	-
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency	-	-	20	MHz	AV_{DD} = 4.5~5.5 V
		-	-	8		AV_{DD} = 2.5~5.5 V
F_S	Sample Rate (F_{ADC}/T_{CONV})	-	-	1000	kSPS	AV_{DD} = 4.5~5.5 V
		-	-	400	kSPS	AV_{DD} = 2.5~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	7			$1/F_{ADC}$	-
T_{CONV}	Total Conversion Time	20			$1/F_{ADC}$	-
AV_{DD}	Supply Voltage	2.5	-	5.5	V	-
I_{DDA}	Supply Current (Avg.)	-	2.5	-	mA	AV_{DD} = 5 V
V_{IN}	Analog Input Voltage	0	-	AV_{DD}	V	-
C_{IN}	Input Capacitance	-	3.2	-	pF	-
R_{IN}	Input Load	-	6	-	kΩ	-



9.4.2 LDO & Power Management

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	2.5	-	5.5	V	-
V_{LDO}	Output Voltage	1.62	1.8	1.98	V	-
T_A	Temperature	-40	25	105	℃	
C_{LDO}	Capacitor	-	1	-	μF	R_{ESR} = 1Ω

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1μF or higher capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

9.4.3 Low Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition

AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{LVR}	Quiescent Current	-	1	5	μA	AV_{DD} = 5.5 V
V_{LVR}	Threshold Voltage	1.90	2.00	2.10	V	T_A = 25 ℃
		1.70	1.90	2.05	V	T_A = -40 ℃
		2.00	2.20	2.45	V	T_A = 105 ℃

9.4.4 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	5.5	V	-
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current	-	-	140	μA	AV_{DD} = 5.5 V
V_{BOD}	Brown-out Voltage (Falling edge)	4.2	4.38	4.55	V	BOV_VL [1:0] = 11
		3.5	3.68	3.85	V	BOV_VL [1:0] = 10
		2.5	2.68	2.85	V	BOV_VL [1:0] = 01
		2.0	2.18	2.35	V	BOV_VL [1:0] = 00
V_{BOD}	Brown-out Voltage (Rising edge)	4.3	4.52	4.75	V	BOV_VL [1:0] = 11
		3.5	3.8	4.05	V	BOV_VL [1:0] = 10
		2.5	2.77	3.05	V	BOV_VL [1:0] = 01
		2.0	2.25	2.55	V	BOV_VL [1:0] = 00

9.4.5 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Reset Voltage	1.6	2	2.4	V	-
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	-	-	100	mV	
RR_{VDD}	V_{DD} Raising Rate to Ensure Power-on Reset	0.025	-	-	V/ms	
t_{POR}	Minimum Time for V_{DD} Stays at VPOR to Ensure Power-on Reset	0.5	-	-	ms	

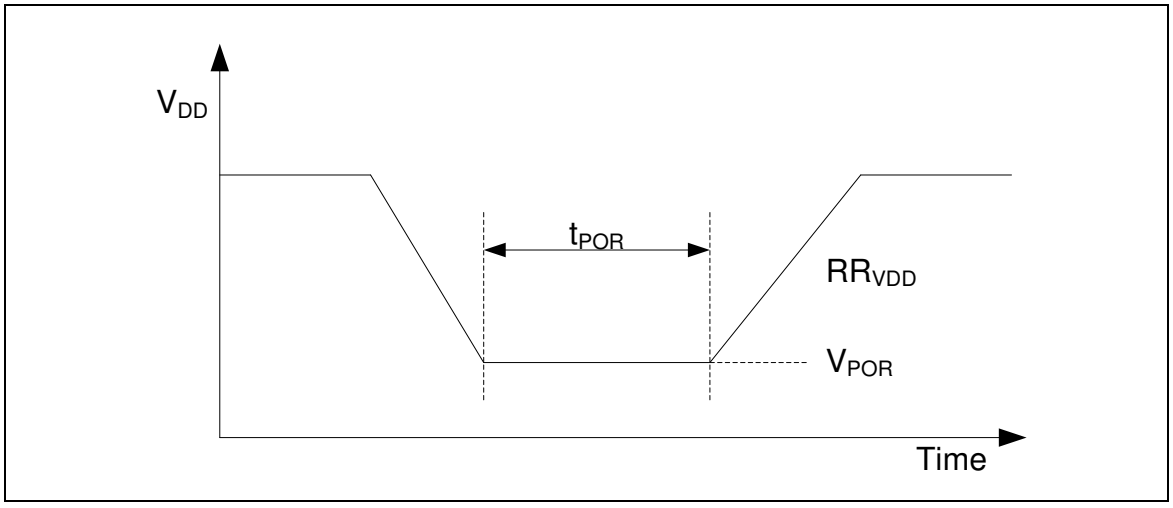


Figure 9-3 Power-up Ramp Condition

9.4.6 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	-	105	℃	
I_{TEMP}	Current Consumption	-	16	-	μA	
-	Gain	-1.55	-1.65	-1.75	mV/℃	
-	Offset	735	745	755	mV	T_A = 0 ℃

Note:

The temperature sensor formula for the output voltage (Vtemp) is as below equation.

Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)

9.4.7 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.5	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	35	70	μA	AV_{DD} = 5 V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	AV_{DD} - 0.1	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD} – 0.1	V	-
-	DC Gain	40	70	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{CM} = 1.2 V, V_{DIFF} = 0.1 V
V_{HYS}	Hysteresis	-	±40	±60	mV	
T_{STB}	Stable time	-	-	1	μs	

9.5 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.62	1.8	1.98	V	
N_{ENDUR}	Endurance	20,000	-	-	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A = 85℃
T_{ERASE}	Page Erase Time	-	20	-	ms	
T_{PROG}	Program Time	-	40	-	us	
I_{DD1}	Read Current	-	6	-	mA	
I_{DD2}	Program Current	-	8	-	mA	
I_{DD3}	Erase Current	-	12	-	mA	

Notes:

1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
3. Guaranteed by design, not test in production.

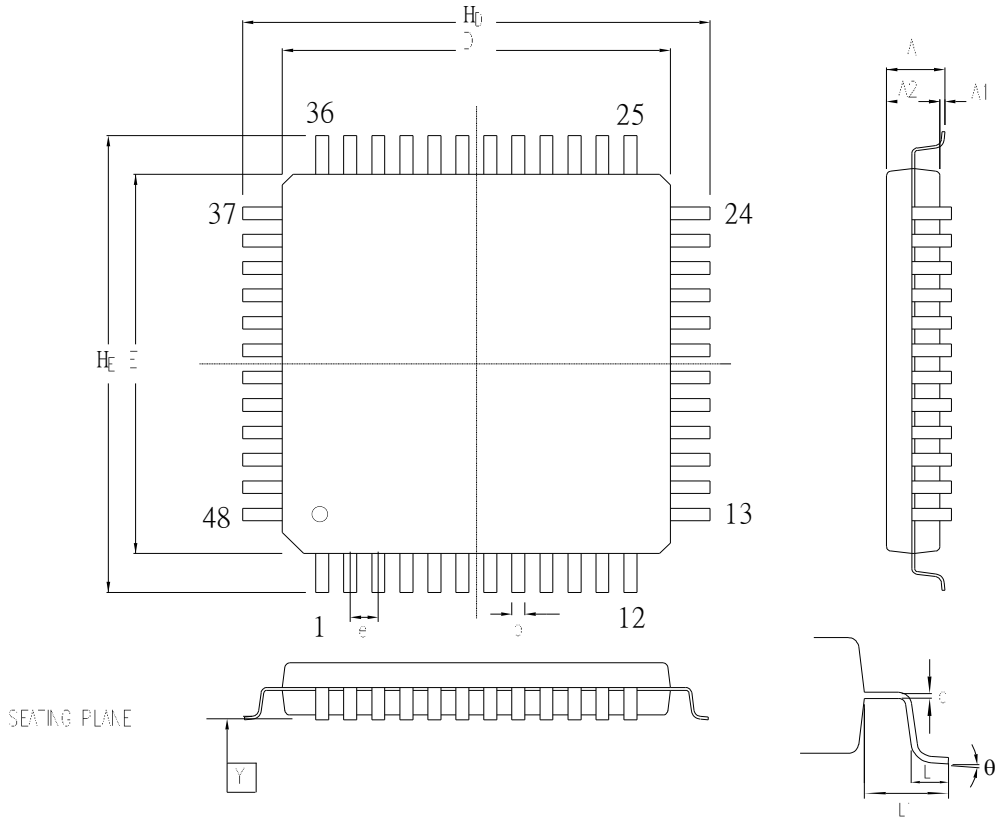
9.6 SPI Dynamic Characteristics

9.6.1 Dynamic Characteristics of Data Input and Output Pin

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
SPI MASTER MODE (V_{DD} = 4.5 V~5.5V, 30 PF LOADING CAPACITOR)					
$t_{W(SCKH)}$ $t_{W(SCKL)}$	SPI high and low time, peripheral clock = 20MHz	22.5	-	27.5	ns
t_{DS}	Data input setup time	0	-	-	ns
$t_{H(MI)}$	Data input hold time	5	-	-	ns
t_V	Data output valid time	-	1	2	ns
$t_{H(MO)}$	Data output hold time	1	-	-	ns
SPI MASTER MODE (V_{DD} = 3.0~3.6 V, 30 PF LOADING CAPACITOR)					
$t_{W(SCKH)}$ $t_{W(SCKL)}$	SPI high and low time, peripheral clock = 20MHz	22.5	-	27.5	ns
t_{DS}	Data input setup time	0	-	-	ns
$t_{H(MI)}$	Data input hold time	4	-	-	ns
t_V	Data output valid time		0	1	ns
$t_{H(MO)}$	Data output hold time	1	-	-	ns

10 PACKAGE DIMENSIONS

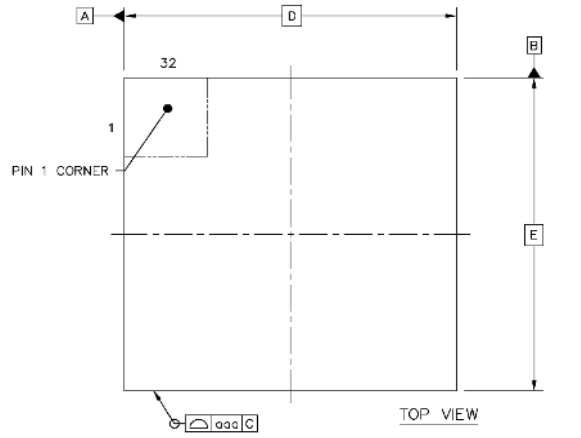
10.1 LQFP-48 (7x7x1.4mm^2 Footprint 2.0mm)

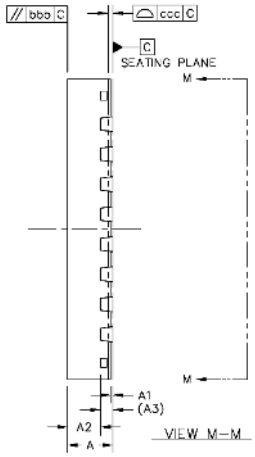


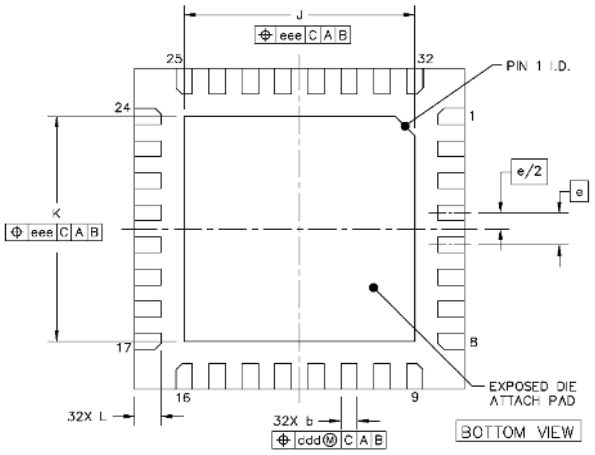
Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

10.2 QFN-33 (5X5 mm^2, Thickness 0.8mm, Pitch 0.5 mm)







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

11 REVISION HISTORY

Date	Revision	Description
2013.09.15	1.00	1. Initially issued.
2014.06.03	1.01	1. Modified M05xDN LVR specification
2015.05.12	1.02	1. Changed the order of Chapter 5 BLOCK DIAGRAM and Chapter 6 FUNCTIONAL DESCRIPTION. 2. Fixed typos and obscure description. 3. Fixed the number of COMP. sets in 4.1 NuMicro® M051 Series M05xxDN Selection Guide and 4.2 NuMicro® M051 Series M05xxDE Selection Guide 4. Added clock switching note in Chapter 6.3 Clock Controller. 5. Removed description about ACMP output inverse function available on M05xxDN.
2015.10.05	1.03	1. Changed NuMicro™ to NuMicro®. 2. Updated Figure 5-1 NuMicro® M051 DN/DE Series Block Diagram.

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