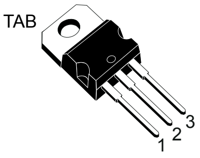
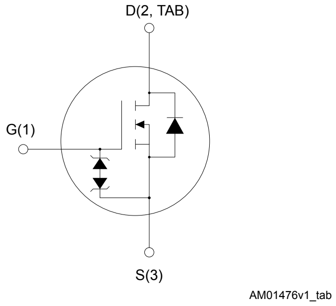
STP65N150M9

Datasheet

N-channel 650 V, 128 mΩ typ., 20 A MDmesh M9 Power MOSFET in a TO-220 package



TO-220



Product status link
STP65N150M9

Product summary	
Order code	STP65N150M9
Marking	65N150M9
Package	TO-220
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP65N150M9	650 V	150 mΩ	20 A

- Worldwide best FOM $R_{DS(on)}$*Qg among silicon-based devices
- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested
- Zener-protected

Applications

- High efficiency switching applications

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	20	A
	Drain current (continuous) at T_C = 100 °C	12.5	
I_{DM}(1)	Drain current (pulsed)	60	A
P_{TOT}	Total power dissipation at T_C = 25 °C	140	W
dv/dt(2)	Peak diode recovery voltage slope	50	V/ns
di/dt(2)	Peak diode recovery current slope	900	A/µs
dv/dt(3)	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. $I_{SD} \leq 10$ A, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.
3. V_{DS} (peak) < $V_{(BR)DSS}$, $V_{DD} \leq 400$ V.

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.89	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. **Avalanche characteristics**

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	200	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. **On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)			200	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.2	3.7	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10 A		128	150	mΩ

1. *Specified by design, not tested in production.*

Table 5. **Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 400 V, f = 1 MHz, V_{GS} = 0 V	-	1240	-	pF
C_{oss}	Output capacitance		-	25	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	290	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 10 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	32	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.*

Table 6. **Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 17. Turn-off switching time waveform on inductive load)	-	8	-	ns
$t_{r(v)}$	Voltage rise time		-	5	-	ns
$t_{f(i)}$	Current fall time		-	7	-	ns
$t_{c(off)}$	Crossing time off		-	40	-	ns
$t_{d(i)}$	Current delay time	V_{DD} = 400 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 18. Turn-on switching time waveform on inductive load)	-	14	-	ns
$t_{r(i)}$	Current rise time		-	4	-	ns
$t_{f(v)}$	Voltage fall time		-	10	-	ns
$t_{c(on)}$	Crossing time on		-	12	-	ns

Table 7. **Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
I_{SDM}(1)	Source-drain current (pulsed)		-		60	A
V_{SD}(2)	Forward on voltage	I_{SD} = 20 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs, V_{DD} = 100 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	192		ns
Q_{rr}	Reverse recovery charge		-	1.8		µC
I_{RRM}	Reverse recovery current		-	17.5		A
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_J = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	280		ns
Q_{rr}	Reverse recovery charge		-	3.6		µC
I_{RRM}	Reverse recovery current		-	20.5		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

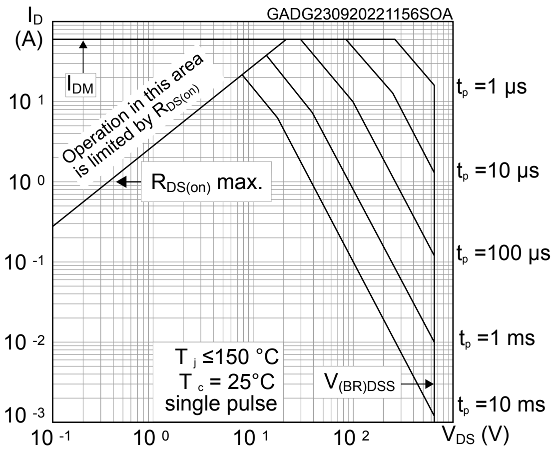


Figure 2. Maximum transient thermal impedance

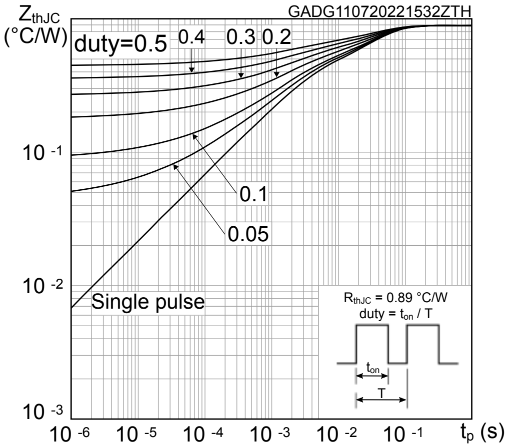


Figure 3. Typical output characteristics

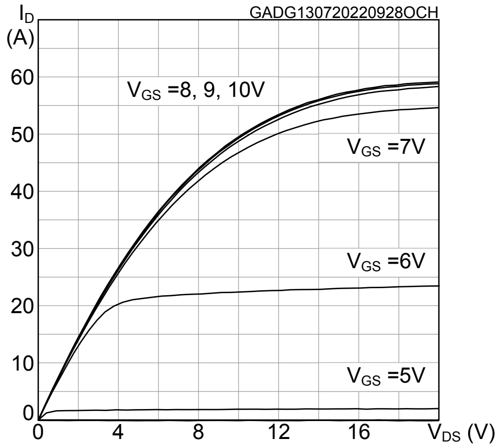


Figure 4. Typical transfer characteristics

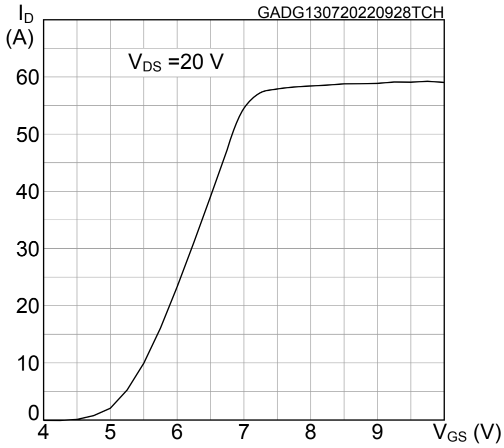


Figure 5. Typical gate charge characteristics

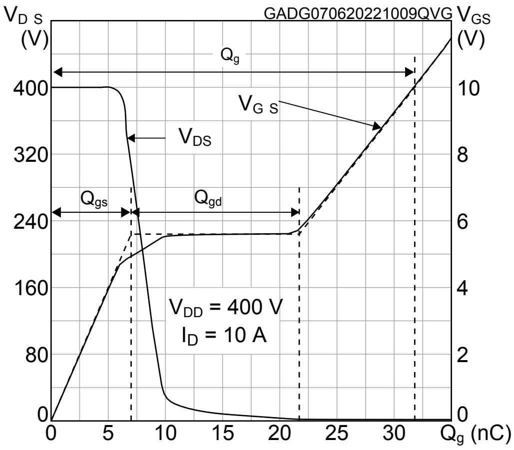


Figure 6. Typical capacitance characteristics

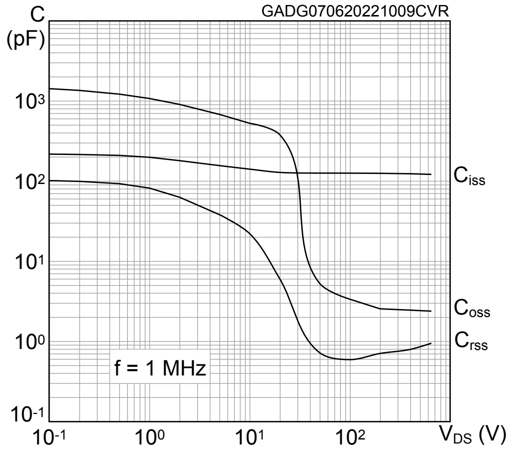


Figure 7. Typical drain-source on-resistance

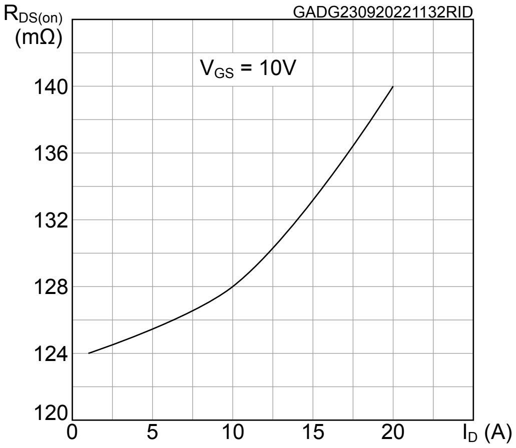


Figure 8. Normalized on-resistance vs temperature

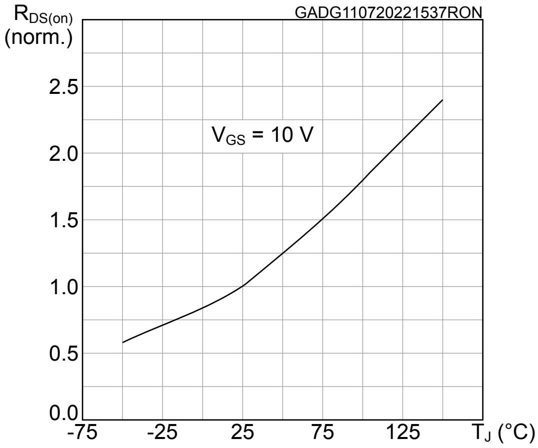


Figure 9. Normalized gate threshold vs temperature

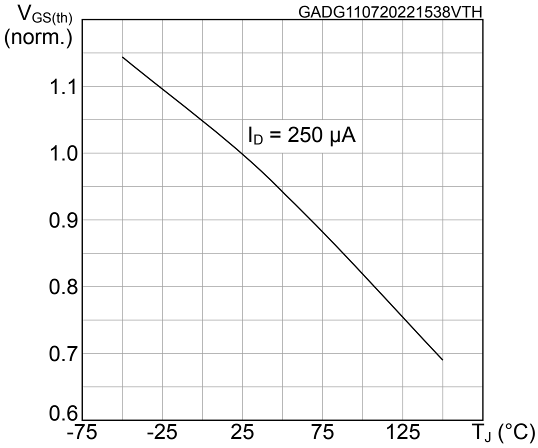


Figure 10. Normalized breakdown voltage vs temperature

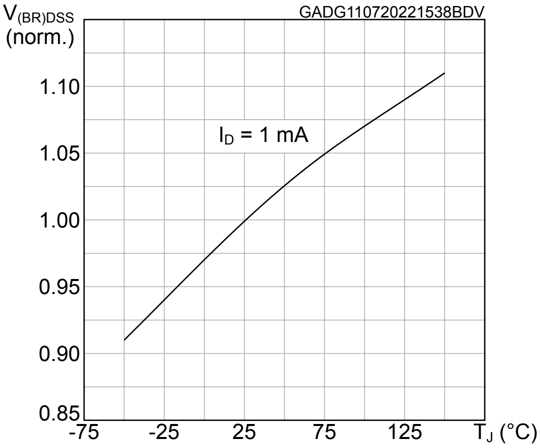


Figure 11. Typical reverse diode forward characteristics

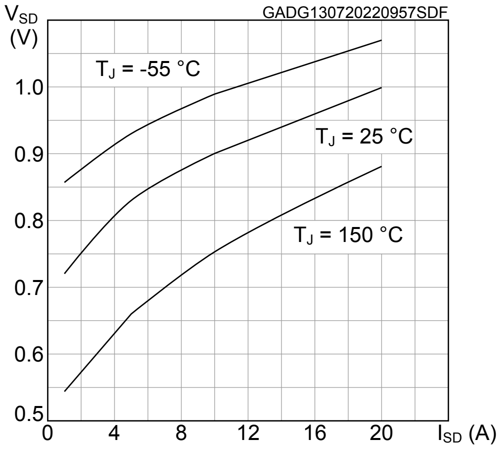
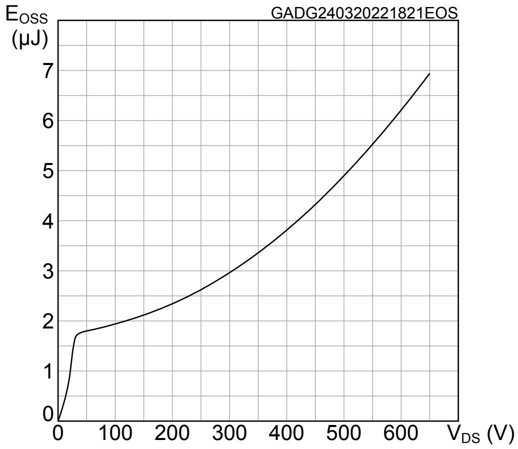


Figure 12. Typical output capacitance stored energy



3 Test circuits

Figure 13. Unclamped inductive load test circuit

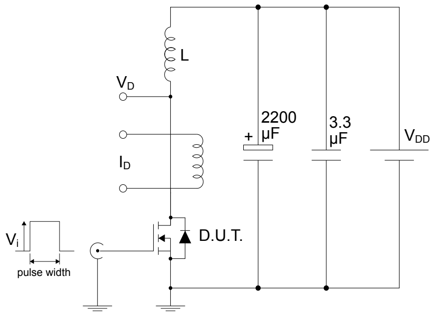


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Figure 14. Unclamped inductive waveform

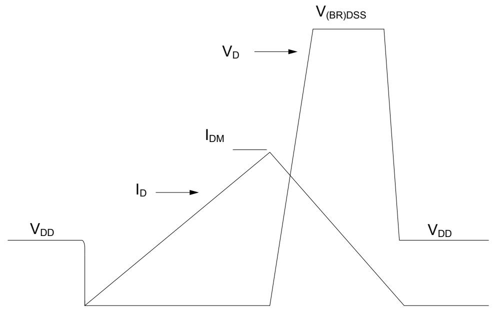

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Figure 15. Test circuit for gate charge behavior

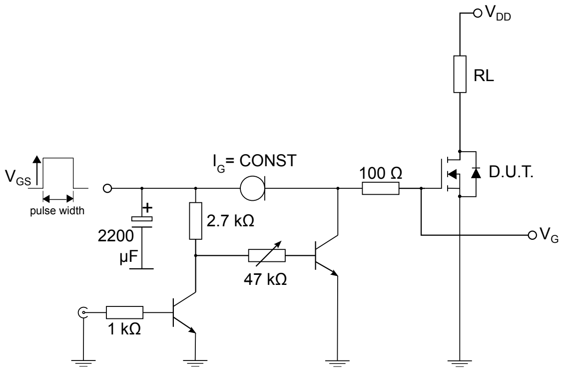

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Figure 16. Test circuit for inductive load switching and diode recovery times

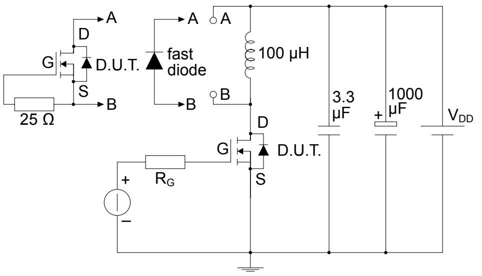

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Figure 17. Turn-off switching time waveform on inductive load

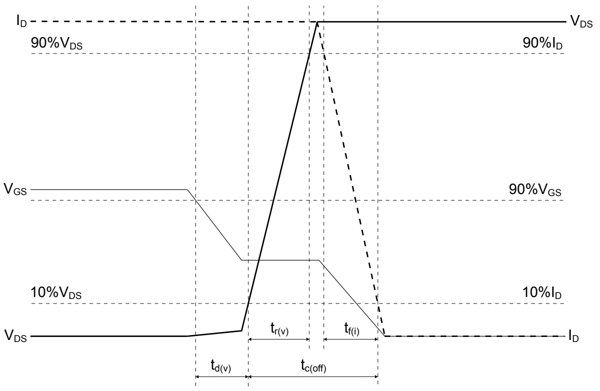

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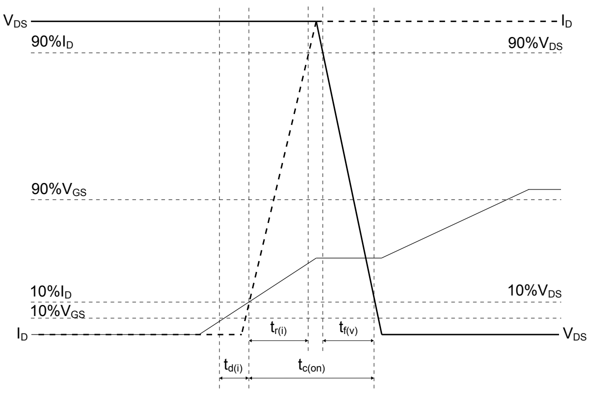
Figure 18. Turn-on switching time waveform on inductive load



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 19. TO-220 type A package outline

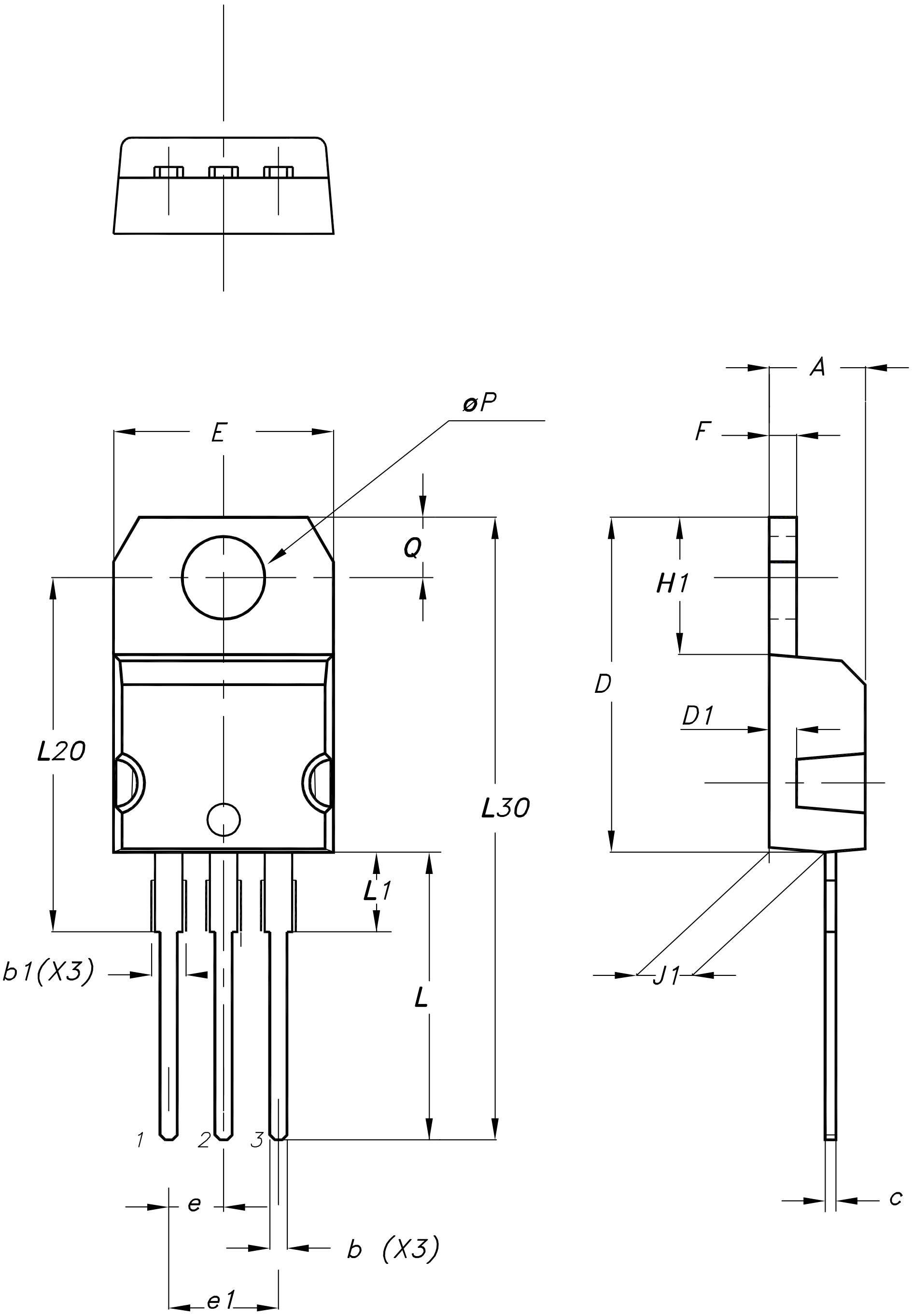

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Table 8. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Jul-2022	1	First release.
01-Dec-2022	2	Updated *Table 1. Absolute maximum ratings.* Updated *Table 5. Dynamic.* Updated *Table 7. Source-drain diode.* Updated *Figure 1. Safe operating area.* Updated *Figure 3. Typical output characteristics.* Updated *Figure 4. Typical transfer characteristics.* Updated *Figure 5. Typical gate charge characteristics.* Updated *Figure 6. Typical capacitance characteristics.* Updated *Figure 7. Typical drain-source on-resistance.* Updated *Figure 11. Typical reverse diode forward characteristics.*
22-Feb-2023	3	Updated Table 1. Absolute maximum ratings. Updated Table 4. On/off states.

Contents

IMPORTANT NOTICE – READ CAREFULLY