

# CBTL08GP053

## USB Type-C High performance Crossbar Switch IC

Rev. 2 — 1 August 2016

Product data sheet

## 1. General description

---

CBTL08GP053 is a USB Type-C High Performance Crossbar Switch IC meant to be used for Type-C connector interface high speed passive switching applications. It provides switching of high speed differential signals that correspond to various interface standards: USB3.1 (10 Gbps), DP1.3 (8.1 Gbps), PCI Express 3.0 (8 Gbps), etc. It supports switching of single ended signals over Type-C interface. In addition, side band switching of AUX and other dedicated signals for transport over SBU1 and SBU2.

It provides the I<sup>2</sup>C-bus interface for switch control, configuration and status update. It operates from a single platform power supply V<sub>DD</sub>.

This IC is targeted for a wide range of platforms (PCs, tablets, convertibles, smart phones) and PC accessories (e.g. docks, monitors, etc.) applications.

CBTL08GP053 is available in a small footprint package option: VFPGA40 4.75 mm × 3.25 mm, 0.5 mm pitch.

## 2. Features and benefits

---

### 2.1 High speed switch features

- Supports the following interface standards: USB3.1, DP1.3, DP++, PCIe 3.0
- Supports signaling rates up to 10 Gbps
- Performs multiplexing or switching of high speed differential signals or single ended signals
- All switches are direction agnostic
- Design based on both patented and patent pending high performance switch technology
- Target performance specification
  - ◆ Differential signaling (peak to peak) of 1.4 V and common mode level over 0 V to 2.2 V
  - ◆ 1.8 V single ended rail to rail signaling
  - ◆ R<sub>on</sub>: 7 Ω (typ)
  - ◆ Insertion loss: 1.2 dB at 2.7 GHz, 1.8 dB at 5.4 GHz, 3dB at 8.5 GHz (typ)
  - ◆ Isolation: 23 dB at 2.7 GHz, 16.5 dB at 5.4 GHz (typ)
  - ◆ Cross talk: 32 dB at 2.7 GHz, 24 dB at 5.4 GHz (typ)
  - ◆ Return loss: 20 dB at 2.7 GHz, 16 dB at 5.4 GHz (typ)
- Very low intra pair skew
- Very low propagation delay (80 ps typical) and inter pair skew (35 ps typical)



- Switch paths selectable through the I<sup>2</sup>C-bus interface (registers for atomic and sequential switch selection)

## 2.2 Sideband auxiliary crossbar switch features

- Single ended 2:1 multiplexing/switching with single ended cross bar switching of both differential AUX or single ended UART or I2C or miscellaneous signals
- Switches are direction agnostic
- Switches are 5.5 V tolerant
- Target performance specification (typical values)
  - ◆ R<sub>on</sub> 8 Ω (typ) at V<sub>cm</sub> = 0.5 V to 2.65 V
- Very low intra pair skew
- Very low propagation delay (80 ps typical)
- Switch paths selectable through the I<sup>2</sup>C-bus interface (registers for atomic and sequential switch selection)

## 2.3 General

- Supports I2C slave interface Standard mode (100 kbit/s) and Fast mode (400 kbit/s)
- I2C slave address programmable up to 4 values
- Back current protection on control pins and exposed connector side I/O pins
- Single 3.3V power supply
- Current consumption
  - ◆ Active mode (all switches are functional): 300 μA (typ)
  - ◆ Standby mode (all switches in Hi-Z): 15 μA (max)
- Operating temperature: -40 to 105 °C
- ESD 2 kV HBM, 500 V CDM
- Package: VFBGA40 4.75 mm × 3.25 mm, 0.5 mm pitch

## 3. Applications

- PC platforms: notebook PCs, desktop PCs, ultrabooks
- Tablets, 2:1 convertibles, smartphones and portable devices
- PC accessories/peripherals: multi-function monitors, etc.

## 4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
CBTL08GP053EV <sup>[1]</sup>	GP053	VFBGA	plastic, very fine-pitch ball grid array package; body 4.75 mm × 3.25 mm × 0.92 mm; 0.5 mm pitch	SOT1439-1

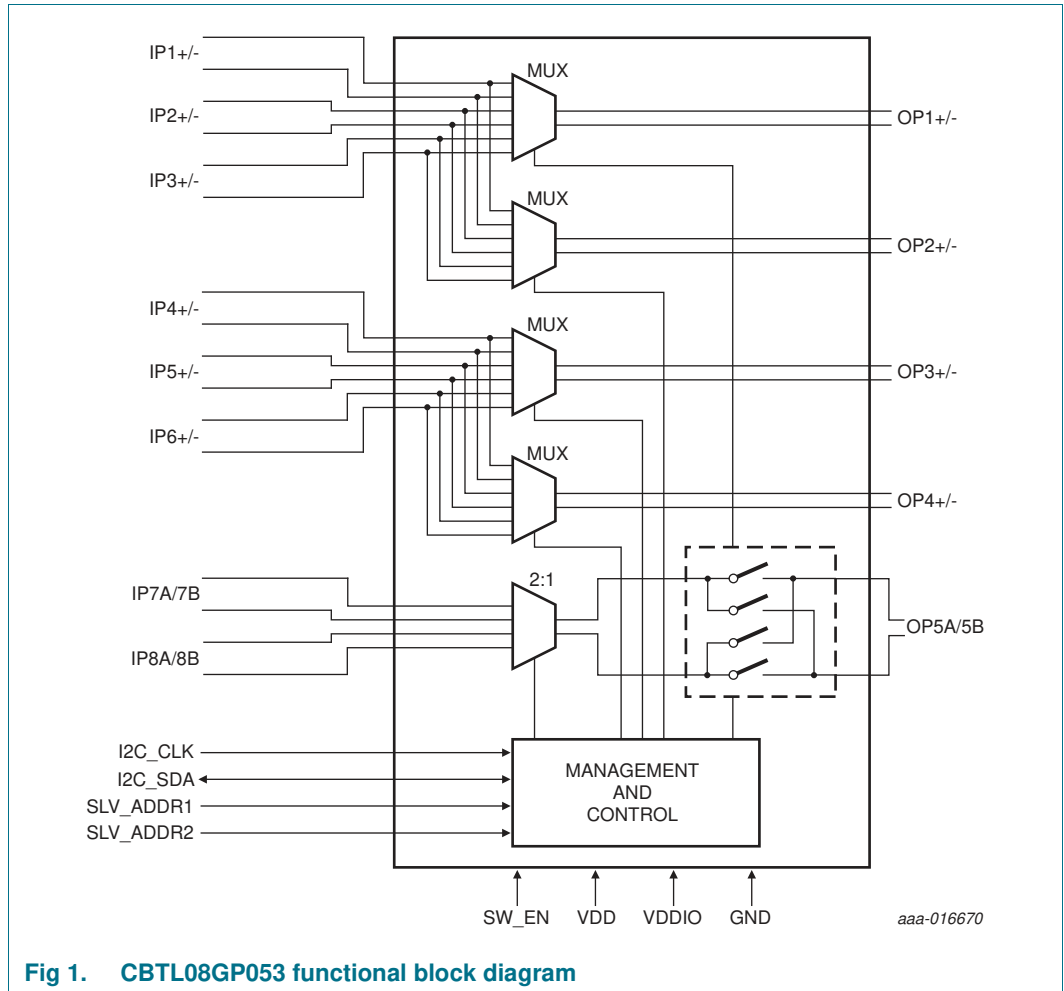
[1] Total height after printed-circuit board mounting ≤1 mm (maximum)

### 4.1 Ordering options

Table 2. Ordering options

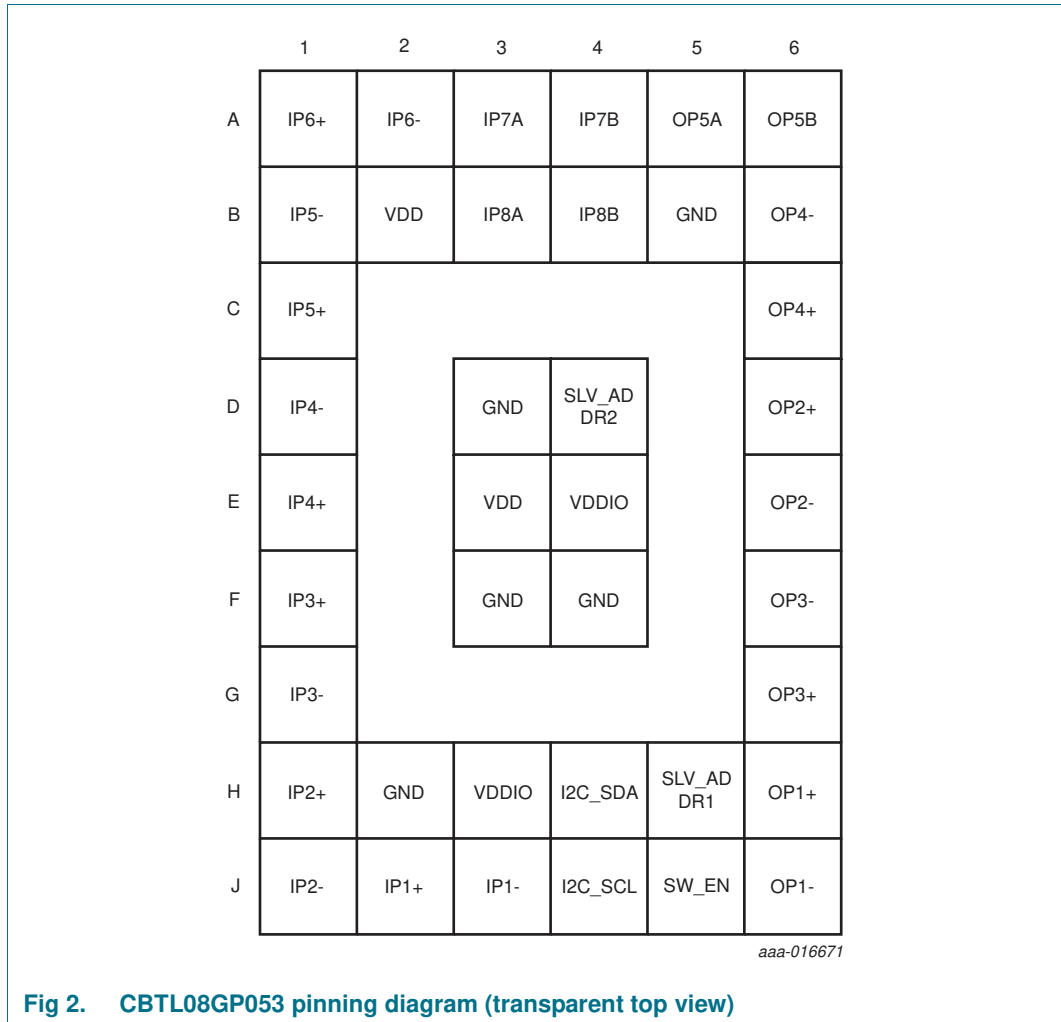
Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
CBTL08GP053EV	CBTL08GP053EVY	VFBGA	Reel 13" Q1/T1 *standard mark SMD DP	5000	T <sub>amb</sub> = -40 °C to +85 °C

**5. Block diagram**



## 6. Pinning information

### 6.1 Pinning



**Fig 2. CBTL08GP053 pinning diagram (transparent top view)**

## 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
IP1+	J2	Differential I/O	Six high-speed differential pairs for DisplayPort, PCI Express, USB3 on system side
IP1-	J3	Differential I/O	
IP2+	H1	Differential I/O	
IP2-	J1	Differential I/O	
IP3+	F1	Differential I/O	
IP3-	G1	Differential I/O	
IP4+	E1	Differential I/O	
IP4-	D1	Differential I/O	
IP5+	C1	Differential I/O	
IP5-	B1	Differential I/O	
IP6+	A1	Differential I/O	
IP6-	A2	Differential I/O	
OP1+	H6	Differential I/O	Four high-speed differential pairs for DisplayPort, PCI Express, USB3 on connector side
OP1-	J6	Differential I/O	
OP2+	D6	Differential I/O	
OP2-	E6	Differential I/O	
OP3+	G6	Differential I/O	
OP3-	F6	Differential I/O	
OP4+	C6	Differential I/O	
OP4-	B6	Differential I/O	
IP7A	A3	I/O	Differential or Single ended signals on system side
IP7B	A4	I/O	
IP8A	B3	I/O	
IP8B	B4	I/O	
OP5A	A5	I/O	
OP5B	A6	I/O	
I2C_SCL	J4	Control IN	I2C slave address signal
I2C_SDA	H4	Control I/O	I2C slave data signal
SLV_ADDR1	H5	Control IN	Binary valued address selection pin for I2C slave address
SW_EN	J5	Control IN	Switch enable control input
VDD	B2, E3	Power	Supply pin

**Table 3. Pin description ...continued**

Symbol	Pin	Type	Description
VDDIO	H3, E4	I/O power	I/O supply pin
GND	B5, D3, F3, F4, H2		Ground
SLV_ADDR2	D4	Control I/O	Binary valued address selection pin for I2C slave address

## 7. Functional description

CBTL08GP053 is a highly integrated Type-C switch targeting Type-C applications. All high speed signal paths are implemented using high-bandwidth pass-gate technology and are non-directional. The side band switches are designed to support 5.5 V tolerance. No clock or reset signal is needed for the multiplexer to function. The switching paths for all the switches can be selected using the I<sup>2</sup>C-bus interface.

CBTL08GP053 functionality can be categorized under three portions:

- High speed switch
  - This has four sub networks of switches corresponding to four I/Os (OPx) connected to Type-C connector interface
  - Each sub network consist of a multiplexer of three high speed I/Os (IPx) on the system side interface
  - All switch paths handles differential signaling or 1.8 V rail to rail single ended signals
  - All switch paths support up to 10 Gbps signaling
  - All multiplexers I/Os are selectable through the I<sup>2</sup>C-bus interface
  - The connector side I/Os can be put in Hi-Z through the I<sup>2</sup>C-bus interface. Default for the I/O is Hi-Z
- Sideband Auxiliary crossbar switch
  - This has a 2:1 multiplexer followed by single ended selectable crossbar function
  - Switch handles both 3.3 V single ended and differential signals
  - Switch I/Os are 5.5 V tolerant
  - Switch handles 5 V rail to rail signaling
  - Crossbar function (normal or reversible) is selectable through the I<sup>2</sup>C-bus interface
  - The connector side I/Os can be put in Hi-Z through the I<sup>2</sup>C-bus interface. Default for the I/O is Hi-Z

At power on, all switches are in Hi-Z condition. After the host platform identifies Type-C interface (including Alternate mode support), it configures the switches. Each individual switch output can be selectively activated and specific switch paths can be selected. Each switch output can also remain in Hi-Z individually.

The SW\_EN pin is used to enable or disable the switch paths only but the I2C register contents are not reset when SW\_EN toggles LOW. When SW\_EN is HIGH, the switches can be enabled and if it is LOW, the switches remain in Hi-Z condition irrespective of the register contents. This pin can toggle dynamically in real time in the application.

Table 4. Truth table for SW\_EN and I2C register contents

SW_EN	SWITCH_EN SYS_CTRL[7]	I2C register settings	Switch output	Power consumption condition
LOW	0	Remain unchanged	Hi-Z	Standby
LOW	1	Remain unchanged	Hi-Z	Standby
HIGH	0	Remain unchanged	Hi-Z	Standby
HIGH	1	Remain unchanged	Output (based on register settings)	Active

### 7.1 CBTL08GP053 - Use case view

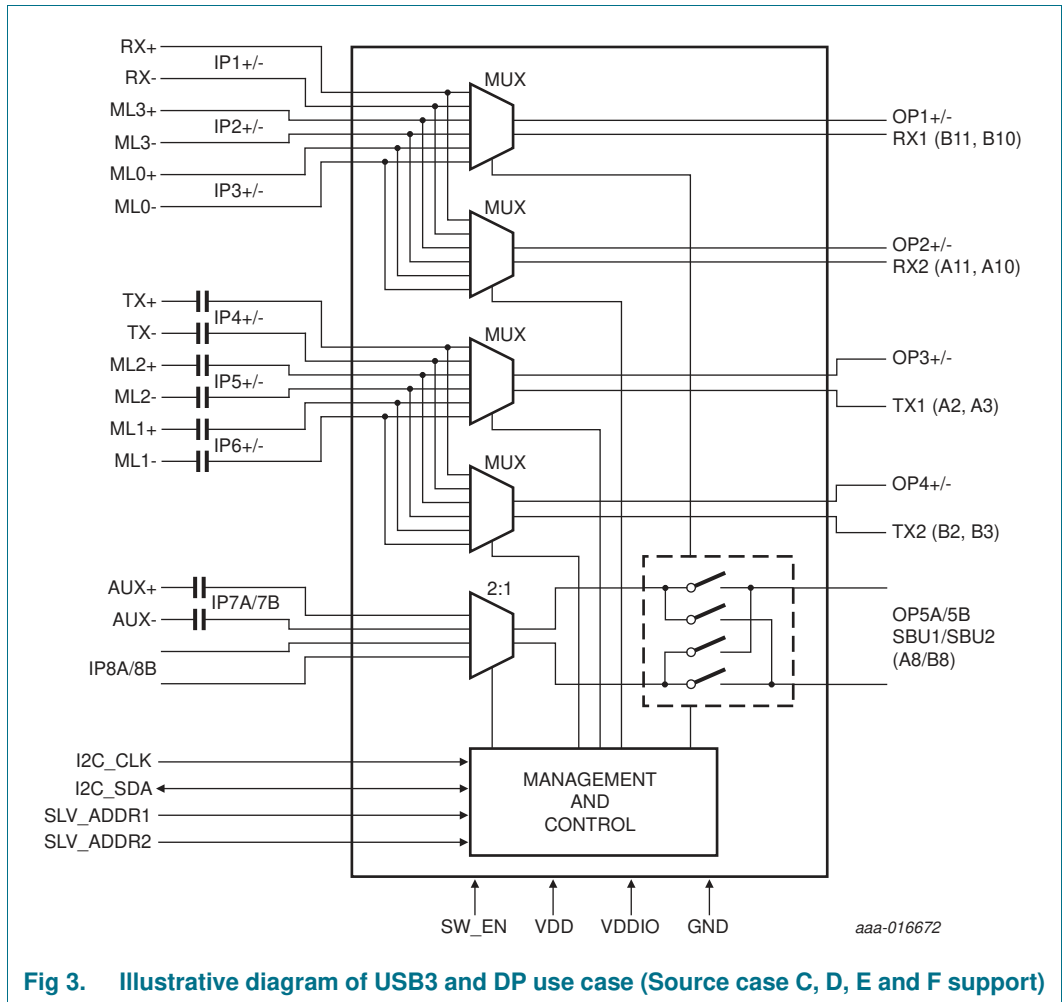
CBTL08GP053 is a versatile high performance switch with flexibility and programmability to route various signals on to Type-C connector interface. It is designed to work over a range of product categories, platform applications, use cases and usage modes. With its configurability, it can serve the needs of both general and custom applications.

The following subsections cover the use case illustrations of CBTL08GP053.



**7.1.1 System application examples**

**7.1.1.1 CBTL08GP053 in Notebook/Ultrabook PC or Tablet - USB3, DP use**



**Fig 3. Illustrative diagram of USB3 and DP use case (Source case C, D, E and F support)**

7.1.1.2 CBTL08GP053 in display monitor use case

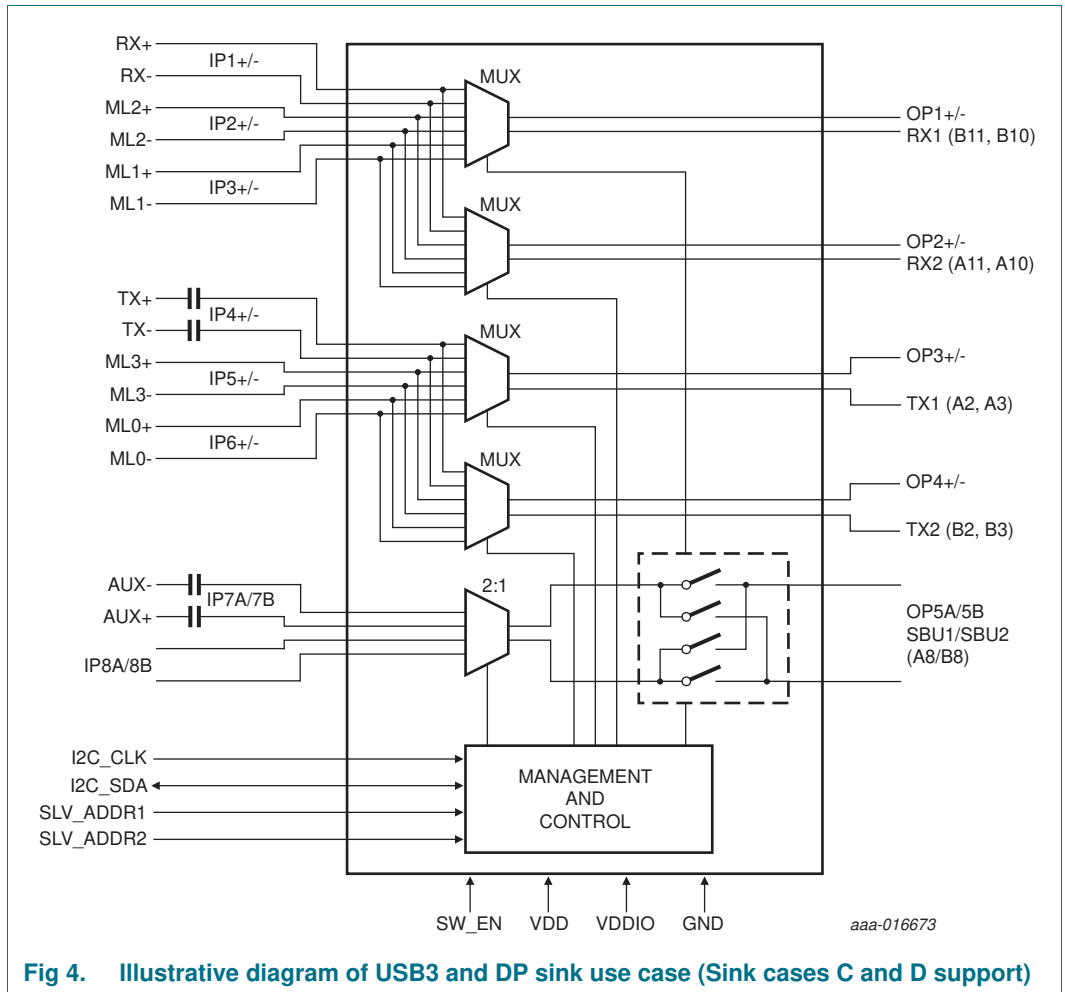


Fig 4. Illustrative diagram of USB3 and DP sink use case (Sink cases C and D support)

Other similar use cases can be constructed as well.

**7.2 Host interface**

The host interface of CBTL08GP053 consists of following data/control signals:

- SLV\_ADDR1, SLV\_ADDR2
- I2C\_SCL
- I2C\_SDA

CBTL08GP053 implements I<sup>2</sup>C-bus slave interface and the host processor can issue commands, monitor status and receive response through this bus. A detailed description of the I<sup>2</sup>C-bus specification, with applications, is given in UM10204, “I<sup>2</sup>C-bus specification and user manual” [3]. It supports I<sup>2</sup>C-bus data transfers in both Standard-mode (100kbit/s) and Fast-mode (400 kbit/s).

As an exception to the I<sup>2</sup>C-bus specification, CBTL08GP053 does not support the I<sup>2</sup>C-bus “General Call” address (and therefore does not issue an Acknowledge), clock stretching, Software Reset command, nor 10-bit address.

The various registers, address offsets and bit definition, as defined in this section and subsections later.

Referring to I<sup>2</sup>C-bus protocol, CBTL08GP053 positively acknowledges all 256 register offset addresses. CBTL08GP053 I<sup>2</sup>C-bus interface implements a special “Auto-Increment” feature that facilitates higher throughput realization by the host system. With this feature, the address wraps back to 0x00 from 0xFF on continuous reads and writes.

CBTL08GP053 supports up to a maximum of four I<sup>2</sup>C-bus slave address options. The address is selected through SLV\_ADDR1 and SLV\_ADDR2 pins. Table 5 shows the different I<sup>2</sup>C-bus device address options selectable based on pin values.

Please refer to the *CBTL08GP053 Programming Guide* (AN11663) for more details.

**Table 5. Device slave address**

SLV_ADDR2	SLV_ADDR1	I <sup>2</sup> C-bus device address
LOW	LOW	0x60/0x61
LOW	HIGH	0x64/0x65
HIGH	LOW	0x68/0x69
HIGH	HIGH	0x6C/0x6D

Table 6. Register bit map overview

Address	Register name	Access <sup>[1]</sup>	Default POR value	Bit								
				7	6	5	4	3	2	1	0	
0x01	SYS_CTRL	RW	b'00000000	SWITCH_EN								
0x02	OP1_CTRL	RW	b'00000000						IP3	IP2	IP1	
0x03	OP2_CTRL	RW	b'00000000						IP3	IP2	IP1	
0x04	OP3_CTRL	RW	b'00000000			IP6	IP5	IP4				
0x05	OP4_CTRL	RW	b'00000000			IP6	IP5	IP4				
0x06	OP5_CTRL	RW	b'00000000	IP8	IP7							
0x07	CROSS5_CTRL	RW	b'00000001							CROSS	PASS	
0x08	SW_CTRL	W	b'00000000			X5_SET	OP5_SET	OP4_SET	OP3_SET	OP2_SET	OP1_SET	
0x09	REVISION	R	b'10100000	REVISION ID								
0x0A to 0xFF	Reserved	-	b'XXXXXXXX	RESERVED								

[1] 'R' Read only register, 'W' Write only register, 'RW' Read/Write register

### 7.2.1 SYS\_CTRL register

**Table 7.** SYS\_CTRL register (address 0x01) bit description

Default: b'00000000

Bit	Symbol	Access	Value	Description
7	SWITCH_EN	R/W	1	CBTL08GP053 is in functional mode. The host shall write a '1' into this bit to put the device into functional mode.
			0	CBTL08GP053 is in Shutdown mode. After POR, the device enters and remains in shutdown mode. To put the device into shutdown mode, this host shall write a '0' into this register bit.
6:0	RESERVED	R/W	XXXXXXX	Reserved bit fields. Reads will be zeros and writes do not have any effect.

### 7.2.2 OP1\_CTRL register

**Table 8.** OP1\_CTRL register (address 0x02) bit description

Default: b'00000000

Bit	Symbol	Access	Value	Description
7:3	RESERVED	R/W	XXXXX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
2	IP3	R/W	0	Switch inputs IP3+/- are not selected
			1	Switch inputs IP3+/- are selected for connection to OP1+/-
1	IP2	R/W	0	Switch inputs IP2+/- are not selected
			1	Switch inputs IP2+/- are selected for connection to OP1+/-
0	IP1	R/W	0	Switch inputs IP1+/- are not selected
			1	Switch inputs IP1+/- are selected for connection to OP1+/-

- [1] The only valid bit values are b'XXXXX001, b'XXXXX010 and b'XXXXX100. Any other bit combination of LS 3 bits will result in Hi-Z at the outputs OP1+/-.

### 7.2.3 OP2\_CTRL register

**Table 9.** OP2\_CTRL register (address 0x03) bit description

Default: b'00000000

Bit	Symbol	Access	Value	Description
7:3	RESERVED	R/W	XX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
2	IP3	R/W	0	Switch inputs IP3+/- are not selected
			1	Switch inputs IP3+/- are selected for connection to OP2+/-
1	IP2	R/W	0	Switch inputs IP2+/- are not selected
			1	Switch inputs IP2+/- are selected for connection to OP2+/-
0	IP1	R/W	0	Switch inputs IP1+/- are not selected
			1	Switch inputs IP1+/- are selected for connection to OP2+/-

- [1] The only valid bit values are b'XXXXX001, b'XXXXX010 and b'XXXXX100. Any other bit combination of LS 3 bits will result in Hi-Z at the outputs OP2+/-.

### 7.2.4 OP3\_CTRL register

**Table 10. OP3\_CTRL register (address 0x04) bit description**

Default: b'00000000

Bit	Symbol	Access	Value	Description
7:6	RESERVED	R/W	XX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
5	IP6	R/W	0	Switch inputs IP6+/- are not selected
			1	Switch inputs IP6+/- are selected for connection to OP3+/-
4	IP5	R/W	0	Switch inputs IP5+/- are not selected
			1	Switch inputs IP5+/- are selected for connection to OP3+/-
3	IP4	R/W	0	Switch inputs IP4+/- are not selected
			1	Switch inputs IP4+/- are selected for connection to OP3+/-
2:0	RESERVED	R/W	XX	Reserved bit fields. Reads will be zeros and writes do not have any effect.

[1] The only valid bit values are b'XX100XXX, b'XX010XXX and b'XX001XXX. Any other bit combination of 3 bits (5:3) will result in Hi-Z at the outputs OP3+/-.

### 7.2.5 OP4\_CTRL register

**Table 11. OP4\_CTRL register (address 0x05) bit description**

Default: b'00000000

Bit	Symbol	Access	Value	Description
7:6	RESERVED	R/W	XX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
5	IP6	R/W	0	Switch inputs IP6+/- are not selected
			1	Switch inputs IP6+/- are selected for connection to OP4+/-
4	IP5	R/W	0	Switch inputs IP5+/- are not selected
			1	Switch inputs IP5+/- are selected for connection to OP4+/-
3	IP4	R/W	0	Switch inputs IP4+/- are not selected
			1	Switch inputs IP4+/- are selected for connection to OP4+/-
2:0	RESERVED	R/W	XXXX	Reserved bit fields. Reads will be zeros and writes do not have any effect.

[1] The only valid bit values are b'XX100XXX, b'XX010XXX and b'XX001XXX. Any other bit combination of 3 bits (5:3) will result in Hi-Z at the outputs OP4+/-.

### 7.2.6 OP5\_CTRL register

**Table 12. OP5\_CTRL register (address 0x06) bit description**

Default: b'00000000

Bit	Symbol	Access	Value	Description
7	IP8	R/W	0	Switch inputs IP8A/B are not selected
			1	Switch inputs IP8A/B are selected for connection to OP5A/B
6	IP7	R/W	0	Switch inputs IP7A/B are not selected
			1	Switch inputs IP7A/B are selected for connection to OP5A/B
5:0	RESERVED	R/W	XXXXX	Reserved bit fields. Reads will be zeros and writes do not have any effect.

[1] The only valid bit values are b'01XXXXXX and b'10XXXXXX. Any other bit combination of 2 bits (7:6) will result in Hi-Z at the outputs OP5A/B.

### 7.2.7 CROSS5\_CTRL register

**Table 13. CROSS5\_CTRL register (address 0x07) bit description**

Default: b'00000001

Bit	Symbol	Access	Value	Description
7:2	RESERVED	R/W	XXXXXX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
1	CROSS	R/W	0	OP5A/B will be Hi-Z
			1	OP5B is connected to either IP7A or IP8A depending on OP5_CTRL register value OP5A is connected to either IP7B or IP8B depending on OP5_CTRL register value
0	PASS	R/W	0	OP5A/B will be Hi-Z
			1	OP5B is connected to either IP7B or IP8B depending on OP5_CTRL register value OP5A is connected to either IP7A or IP8A depending on OP5_CTRL register value

[1] The only valid bit field values are b'XXXXXX10 and b'XXXXXX01. The bit fields b'XXXXXX00 and b'XXXXXX11 will result in Hi-Z at the outputs OP5A/B.

### 7.2.8 SW\_CTRL register

**Table 14. SW\_CTRL register (address 0x08) bit description**

Default: b'00000000

Bit	Symbol	Access	Value	Description
7:6	RESERVED	R/W	XX	Reserved bit fields. Reads will be zeros and writes do not have any effect.
5	X5_SET	R/W	0	Prior output setting is unchanged
			1	CROSS5_CTRL register value is used to select passing through or crossing the inputs
4	OP5_SET	R/W	0	Prior output setting is unchanged
			1	OP5A/B is connected to one of the inputs based on OP5_CTRL register

**Table 14. SW\_CTRL register (address 0x08) bit description ...continued**

Default: b'00000000

Bit	Symbol	Access	Value	Description
3	OP4_SET	R/W	0	Prior output setting is unchanged
			1	OP4+/- is connected to one of the inputs based on OP4_CTRL register
2	OP3_SET	R/W	0	Prior output setting is unchanged
			1	OP3+/- is connected to one of the inputs based on OP3_CTRL register
1	OP2_SET	R/W	0	Prior output setting is unchanged
			1	OP2+/- is connected to one of the inputs based on OP2_CTRL register
0	OP1_SET	R/W	0	Prior output setting is unchanged
			1	OP1+/- is connected to one of the inputs based on OP1_CTRL register

### 7.2.9 REVISION register

**Table 15. REVISION register (address 0x09) bit description**

Default: b'10100000

Bit	Symbol	Access	Value	Description
7:0	REVISION ID	R	b'10100000	Revision ID A0 = First silicon version

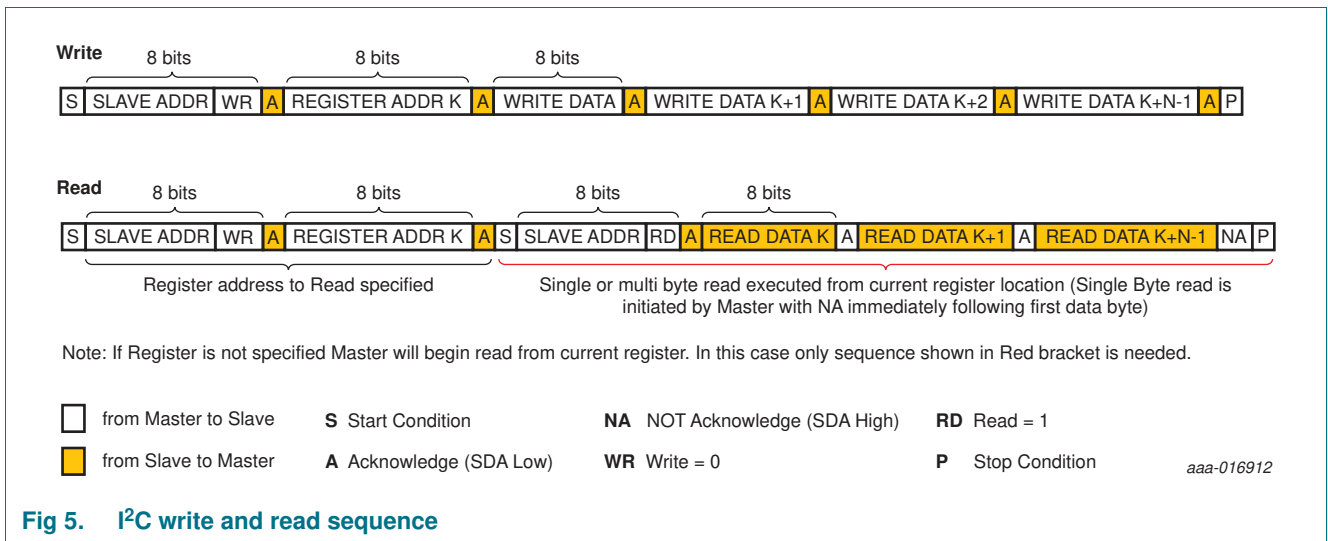


### 7.3 I<sup>2</sup>C read and write sequence

An example of an I<sup>2</sup>C write and read sequence is shown in [Figure 5](#).

Table 16. I<sup>2</sup>C slave address

Name	Size (bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave address	8	0	1	1	0	SLV_ADDR2	SLV_ADDR1	0	Write = 0 Read = 1



## 8. Limiting values

**Table 17. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Max <sup>[2]</sup>	Unit
V <sub>DD</sub>	supply voltage	on pin VDD	-0.5	+4.6	V
V <sub>DD(I/O)</sub>	input/output supply voltage	on pin VDDIO	-0.5	+4.6	V
V <sub>I</sub>	input voltage	IP1+/-, IP2+/-, IP3+/-, IP4+/-, IP5+/-, IP6+/-	-0.5	+2.6	V
		OP1+/-, OP2+/-, OP3+/-, OP4+/-	-0.5	+2.6	V
		IP7A/7B, IP8A/8B	-0.5	+6.0	V
		OP5A/5B	-0.5	+6.0	V
		SLV_ADDR1, SLV_ADDR2, SW_EN	-0.5	+4.6	V
		I2C_SCL, I2C_SDA (external pull-up needed on the I <sup>2</sup> C-bus interface)	-0.5	+4.6	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+125	°C
V <sub>ESD</sub>	electrostatic discharge voltage	HBM <sup>[3]</sup>	2000	-	V
		CDM <sup>[4]</sup>	500	-	V

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

[2] Stresses above the absolute maximum ratings may damage the device. The device may not function or be operating above the Recommended Operating Conditions and it is strongly recommended not to exceed these levels. Also, the device reliability may get affected if it is subjected to stress levels above the Recommended Operating Conditions.

[3] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA; JEDEC Solid State Technology Association, Arlington, VA, USA.

[4] Charged Device Model: JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

## 9. Recommended operating conditions

**Table 18. Operating conditions**

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	supply voltage	on pin VDD	2.9	-	3.6	V
V <sub>DD(IO)</sub>	input/output supply voltage	on pin VDDIO	1.7	-	3.6	V
T <sub>amb</sub>	ambient temperature		-40	-	+105	°C

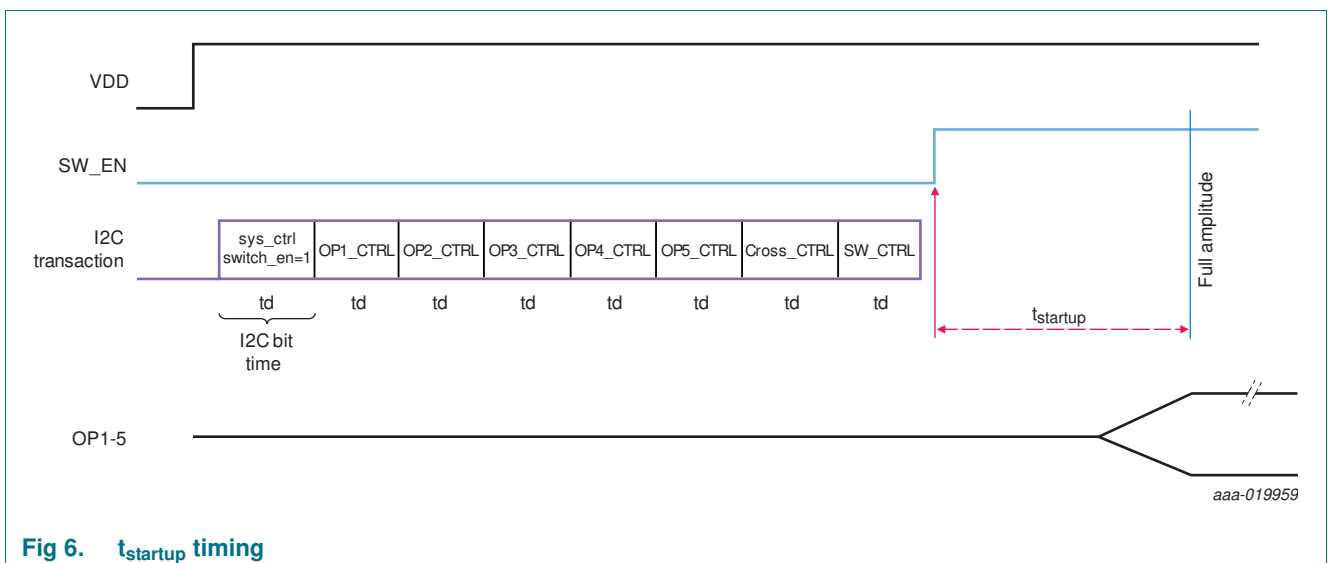
## 10. Characteristics

### 10.1 Device characteristics

**Table 19. Device characteristics**

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>act</sub>	active current	switches are enabled	-	300	-	μA
I <sub>stdby</sub>	standby current	all switches in Hi-Z	-	-	15	μA
t <sub>startup</sub>	start-up time	SW_EN going LOW → HIGH to switches functioning as per specified operating characteristics; with a non-zero and valid switch selection (refer to <a href="#">Figure 6</a> )	-	60	300	μs
t <sub>rcfg</sub>	reconfiguration time	Time interval between end of I2C ACK response last bit and switches functioning as per specified operating characteristics	-	-	20	μs



**Fig 6. t<sub>startup</sub> timing**

## 10.2 High speed switch characteristics

**Table 20. High speed switch characteristics**

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_I$	input voltage		-0.3	-	+2.55	V
$V_{se, LO}$	Single ended voltage LOW level	Applicable for single ended signal switching use cases	-	-	$0.3 \times V_{DD(IO)}$	V
$V_{se, HI}$	Single ended voltage HIGH level	Applicable for single ended signal switching use cases	$0.7 \times V_{DD(IO)}$	-	2.55	V
$V_{se,pp swing}$	Single ended peak to peak voltage swing	Applicable for differential signal switching use cases	-	-	0.7	V
$V_{cm}$	Common mode voltage	Applicable for differential signal switching use cases	0	-	2.2	V
$R_{on}$	ON-state resistance	$V_{cm} = 0\text{ V to }2.2\text{ V}, I = 15\text{ mA}$	-	7	10	$\Omega$
$I_{max}$	Maximum sustained DC current flow		-	-	15	mA
$t_{pd}$	Propagation delay	At mid-point of differential voltage transition	-	80	120	ps
$t_{SK,diff}$	Intra pair skew	Between mid points of positive and negative terminals of an IO	-	-	6	ps
$t_{SK}$	Inter pair skew	Skew between different lanes	-	35	-	ps
BW	-3 dB Bandwidth		-	8.5	-	GHz
DDIL	Differential Insertion Loss on both IPx (x = 1 to 6) and OPy+/- (y = 1 to 4)	Switch path is disabled				
		f = 5.4 GHz	-	16.5	-	dB
		f = 2.7 GHz	-	23	-	dB
		Switch path is enabled				
		f = 5.4 GHz	-	1.8	-	dB
		f = 2.7 GHz	-	1.2	-	dB
		f = 1.35 GHz	-	0.9	-	dB
DDRL	Differential return loss on IPx (x = 1 to 6)	f = 5.4 GHz	-	16	-	dB
		f = 2.7 GHz	-	20	-	dB
		f = 1.35 GHz	-	23	-	dB
		DDRL	Differential return loss on OPx (x = 1 to 4)	f = 5.4 GHz	-	16
f = 2.7 GHz	-			20	-	dB
f = 1.35 GHz	-			23	-	dB
DDXTLK	Differential Crosstalk on IPx+/- (x = 1 to 6)	f = 5.4 GHz	-	24	-	dB
		f = 2.7 GHz	-	32	-	dB
		f = 1.35 GHz	-	37	-	dB
DDXTLK	Differential crosstalk on OPx+/- (x = 1 to 4)	f = 5.4 GHz	-	24	-	dB
		f = 2.7 GHz	-	32	-	dB
		f = 1.35 GHz	-	37	-	dB

All S-parameter measurements are with respect to 100  $\Omega$  differential impedance reference and 50  $\Omega$  single-ended impedance reference.

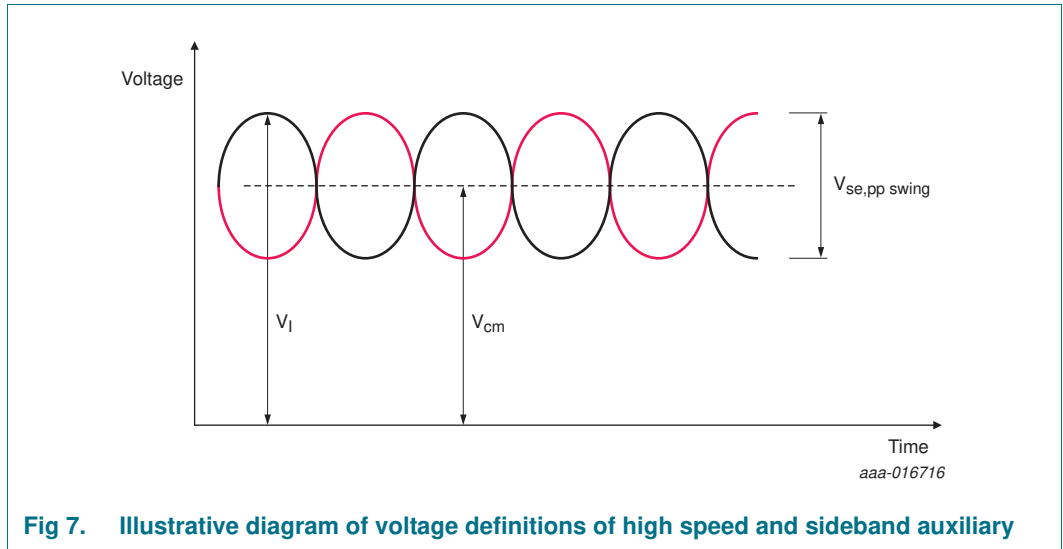
### 10.3 Sideband Auxiliary Crossbar switch characteristics

**Table 21. Sideband Auxiliary Crossbar switch characteristics**

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_I$	input voltage		-0.3	-	+5.3	V
$V_{se, LO}$	Single ended voltage LOW level	Applicable for single ended signal switching use cases	-	-	$0.3 \times V_{DD(IO)}$	V
$V_{se, HI}$	Single ended voltage HIGH level	Applicable for single ended signal switching use cases	$0.7 \times V_{DD(IO)}$	-	5.3	V
$V_{se,pp\ swing}$	Single ended peak to peak voltage swing (diff. signal switching use cases)	Up to 75 MHz	-	-	5.3	V
		75 MHz to 500 MHz	0.075	-	0.575	V
$V_{cm}$	Common mode voltage (diff. signal switching use cases)	Up to 75 MHz	0.8	-	2.65	V
		75 MHz to 500 MHz	-0.05	-	+0.5	V
$R_{on}$	ON-state resistance	$V_{cm} = -0.05\text{ V to }2.65\text{ V}, I = 20\text{ mA}$	-	7.1	10	$\Omega$
$I_{max}$	Maximum sustained DC current flow		-	-	20	mA
$t_{pd}$	Propagation delay	At mid-point of differential voltage transition	-	80	100	ps
$t_{sk}$	Intra pair skew		-	-	5	ps
BW	-3 dB bandwidth		-	750	-	MHz
DDDIL	Differential Insertion Loss	Switch path is not enabled				
		f = 500 MHz	-	20	-	dB
		f = 250 MHz	-	26	-	dB
		Switch path is enabled				
		f = 750 MHz	-	3.0	-	dB
		f = 500 MHz	-	1.5	-	dB
		f = 375 MHz	-	1.2	-	dB
DDRL	Differential return loss	f = 500 MHz	-	11	-	dB
		f = 375 MHz	-	13	-	dB
		f = 250 MHz	-	16	-	dB

All S-parameter measurements are with respect to 100  $\Omega$  differential impedance reference and 50  $\Omega$  single-ended impedance reference.



### 10.4 Control I/O characteristics

**Table 22. Control I/O characteristics**

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>System side CMOS interface pins (SW_EN, SLV_ADDR1, SLV_ADDR2)</b>						
V <sub>IH</sub>	HIGH-level input voltage		0.7 × V <sub>DD(IO)</sub>	-	V <sub>DD(IO)</sub> + 0.3	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.3 × V <sub>DD(IO)</sub>	V
I <sub>IL</sub>	Input leakage current	For input levels (LOW, HIGH)	-10	-	+10	μA
C <sub>I</sub>	Capacitance of pin		-	-	10	pF
<b>System side open drain interface pins (I2C_SCL, I2C_SDA); pulled up externally to V<sub>DD(IO)</sub><sup>[1]</sup> through resistor</b>						
V <sub>IH</sub>	HIGH-level input voltage		0.7 × V <sub>DD(IO)</sub>	-	V <sub>DD(IO)</sub> + 0.3	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.3 × V <sub>DD(IO)</sub>	V
V <sub>OL</sub>	LOW-level output voltage at 3 mA sink current	V <sub>DD(IO)</sub> > 2 V	0	-	0.4	V
		V <sub>DD(IO)</sub> < 2 V	0	-	0.2 × V <sub>DD(IO)</sub>	V
I <sub>IL</sub>	LOW-level input current	Pin voltage: 0.1 × V <sub>DD(IO)</sub> to 0.9 × V <sub>IO,max</sub>	-10	-	+10	μA
C <sub>I</sub>	capacitance of I/O pin		-	-	10	pF

[1] V<sub>DD(IO)</sub> is pull-up voltage on I<sup>2</sup>C-bus interface and the pull-up resistors are sized for 3 mA. It can be different from V<sub>DD</sub>. Note this is not a chip level power supply.

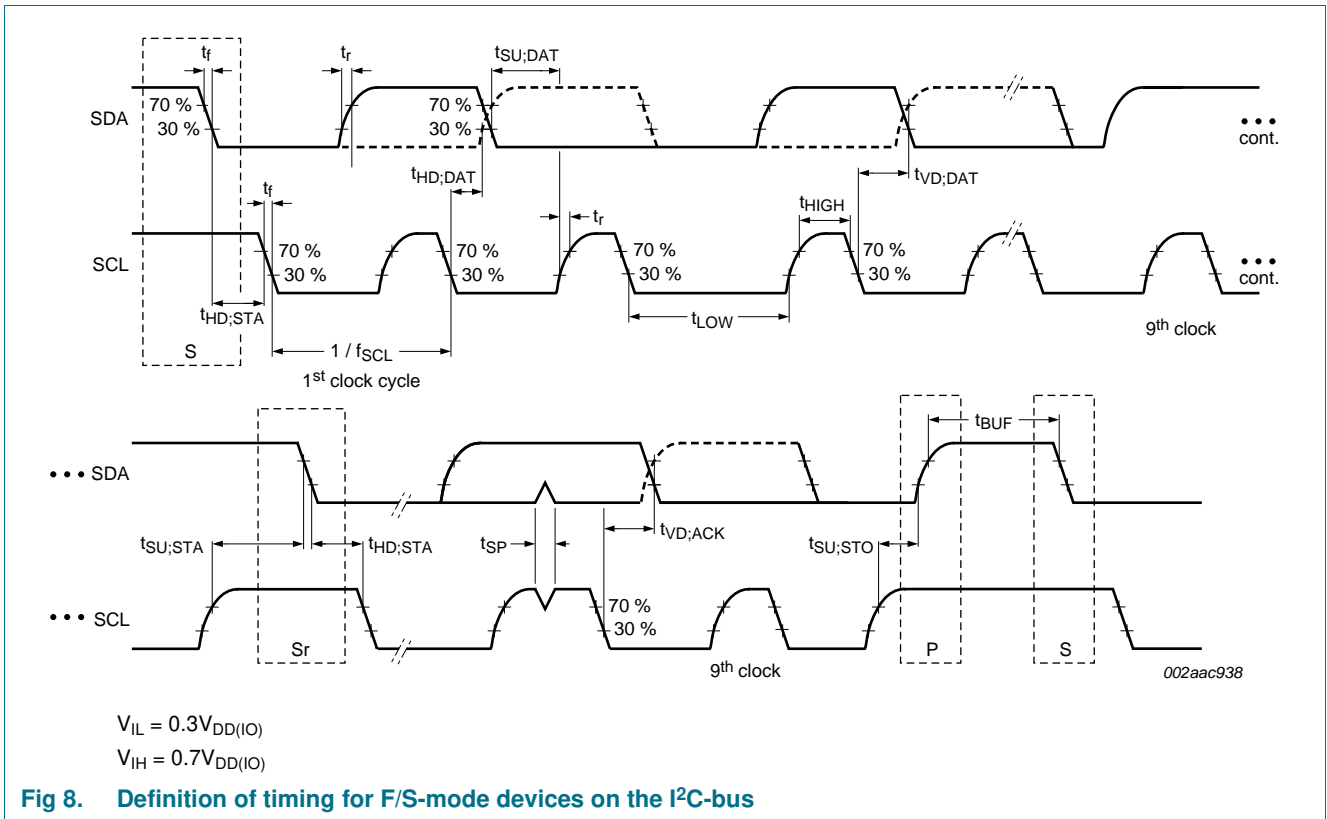
## 10.5 I<sup>2</sup>C-bus dynamic characteristics

**Table 23. I<sup>2</sup>C-bus dynamic characteristics**

Over ambient temperature and power supply ranges (unless otherwise noted). Typical values are specified at 27 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f <sub>SCL</sub>	SCL clock frequency		-	-	400	kHz
t <sub>HD;STA</sub>	hold time (repeated) START condition	Fast mode; after this period, the first clock pulse is generated	0.6	-	-	μs
t <sub>LOW</sub>	LOW period of the SCL clock	Fast mode	1.3	-	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock	Fast mode	0.6	-	-	μs
t <sub>SU;STA</sub>	set-up time for a repeated START condition	Fast mode	0.6	-	-	μs
t <sub>HD;DAT</sub>	data hold time	Fast mode	0	-	-	μs
t <sub>SU;DAT</sub>	data set-up time	Fast mode	100	-	-	ns
t <sub>r</sub>	rise time of both SDA and SCL signals		20 + 0.1 × C <sub>B</sub> <sup>[1]</sup>	-	300	ns
t <sub>f</sub>	fall time of both SDA and SCL signals		20 + 0.1 × C <sub>B</sub> <sup>[1]</sup>	-	300	ns
t <sub>SU;STO</sub>	set-up time for STOP condition		0.6	-	-	μs
t <sub>BUF</sub>	bus free time between a STOP and START condition		1.3	-	-	μs
t <sub>VD;DAT</sub>	data valid time		-	-	0.9	μs
t <sub>VD;ACK</sub>	data valid acknowledge time		-	-	0.9	μs
t <sub>SP</sub>	pulse width of spikes that must be suppressed by input filter		0	-	50	μs

[1] C<sub>B</sub> = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times according to Table 6 of [3] are allowed





11. Package outline

VFBGA40: plastic very thin fine-pitch ball grid array package; 40 balls

SOT1439-1

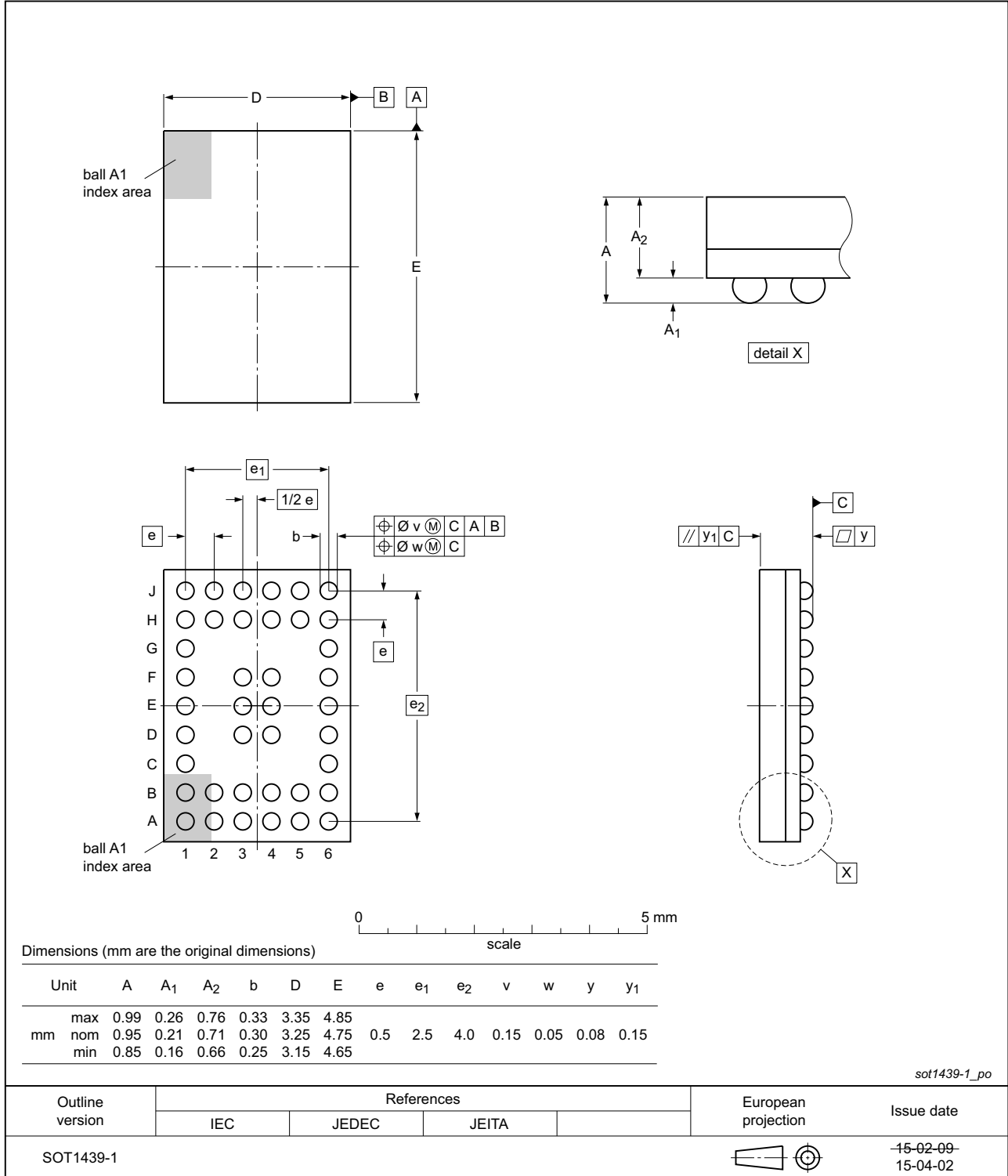
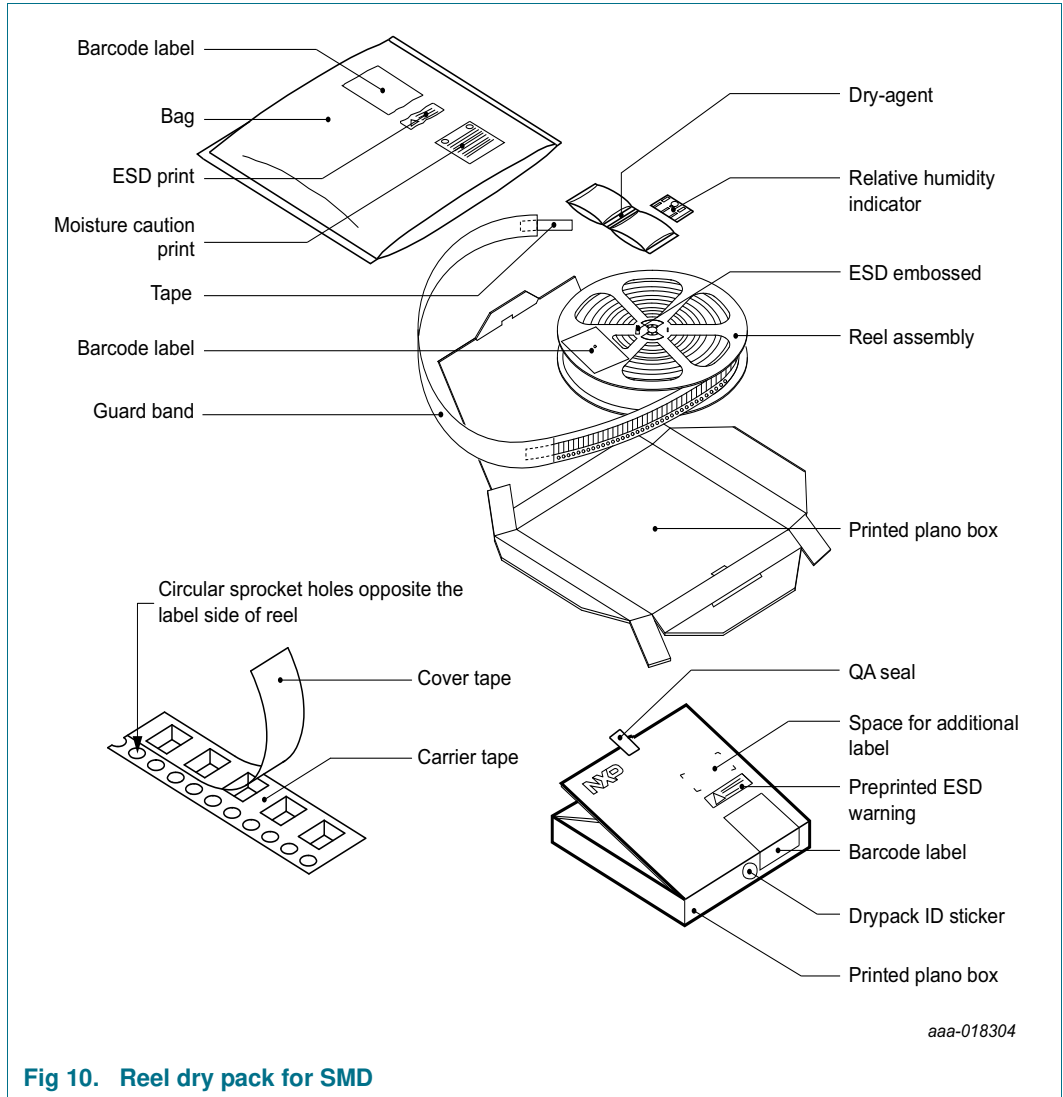


Fig 9. Package outline SOT1439-1 (VFBGA40)

## 12. Packing information

### 12.1 Packing method VFBGA40; Reel dry pack, SMD, 13"; Q1/T1 standard product orientation; Orderable part number ending ,518 or Y; Ordering code (12NC) ending 518



**Table 24. Dimensions and quantities**

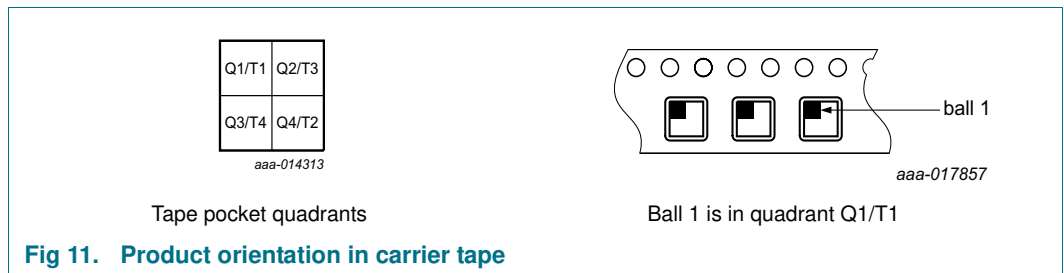
Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box	Outer box dimensions l × w × h (mm)
330 × 12	5000	1	342 × 338 × 39

[1] d = reel diameter; w = tape width.

[2] Packing quantity dependent on specific product type.

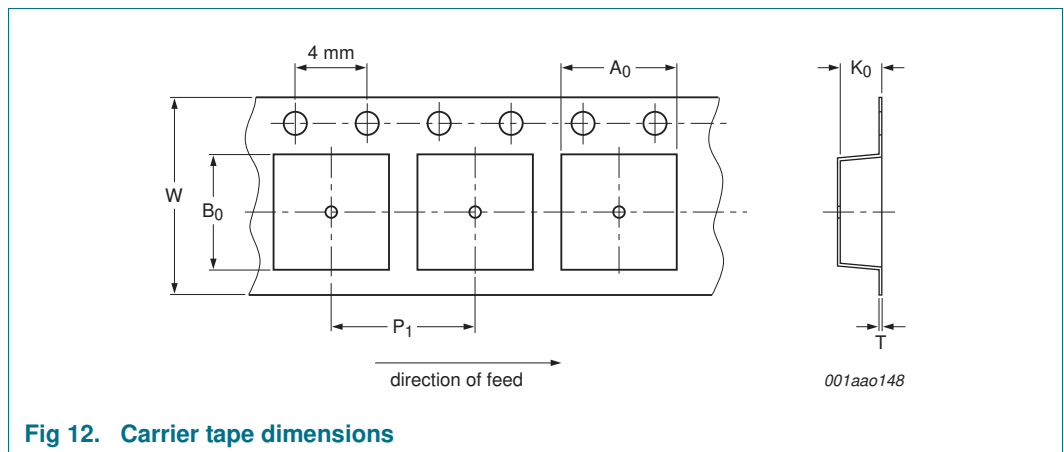
View ordering and availability details at [NXP order portal](#), or contact your local NXP representative.

**12.1.1 Product orientation**



**Fig 11. Product orientation in carrier tape**

**12.1.2 Carrier tape dimensions**



**Fig 12. Carrier tape dimensions**

**Table 25. Carrier tape dimensions**

In accordance with IEC 60286-3.

A <sub>0</sub> (mm)	B <sub>0</sub> (mm)	K <sub>0</sub> (mm)	T (mm)	P <sub>1</sub> (mm)	W (mm)
3.55 ± 0.10	5.05 ± 0.10	1.20 ± 0.10	0.3 ± 0.05	8.0 ± 0.10	12 ± 0.30

12.1.3 Reel dimensions

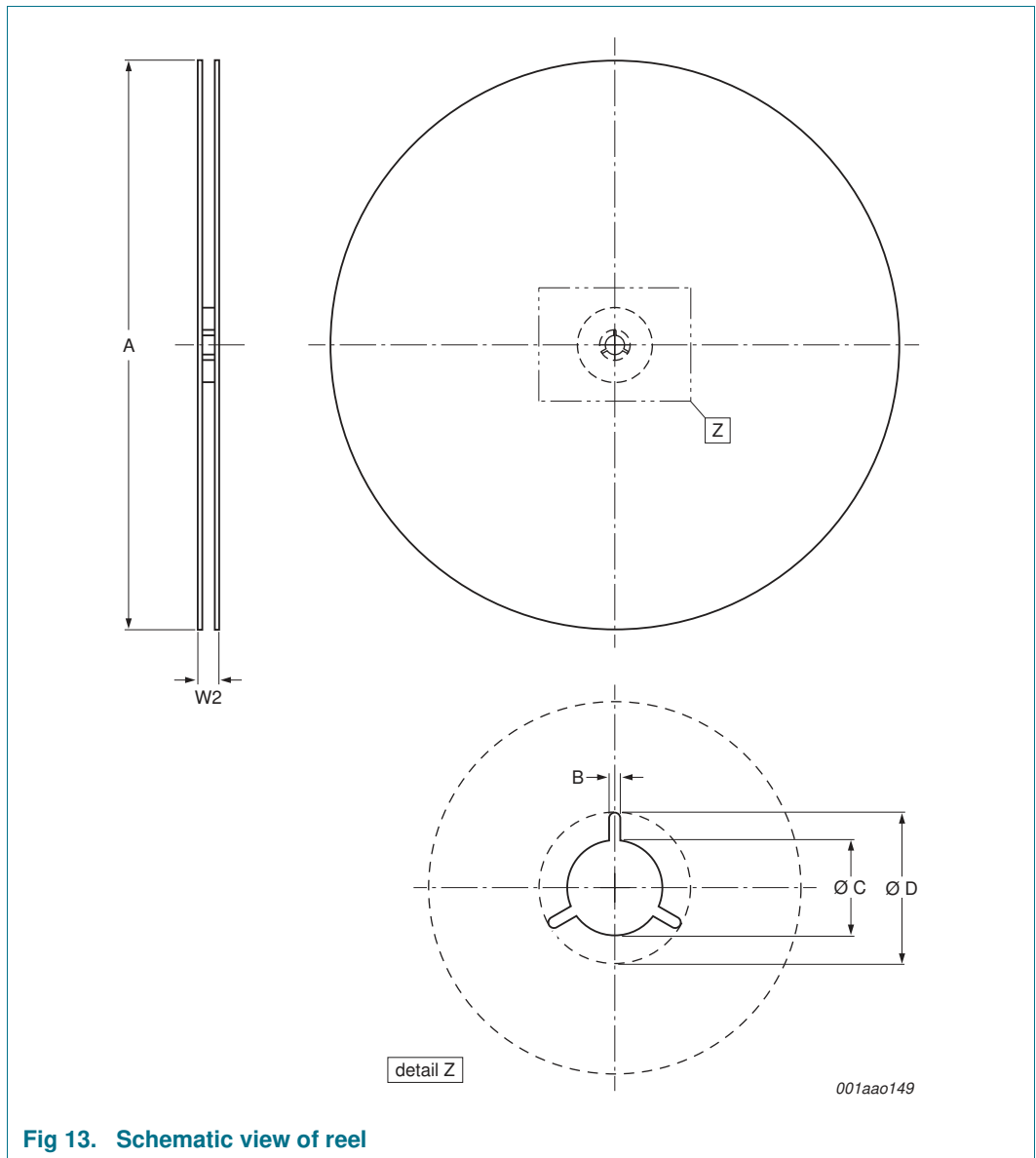


Fig 13. Schematic view of reel

**Table 26. Reel dimensions**  
In accordance with IEC 60286-3.

A [nom] (mm)	W2 [max] (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
330	18.4	1.5	12.8	20.2

12.1.4 Barcode label

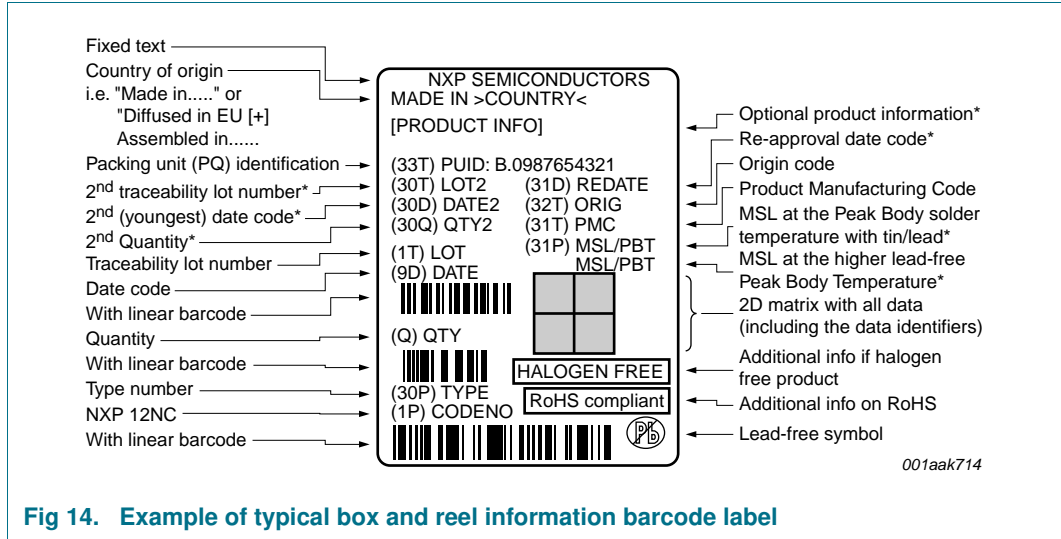


Fig 14. Example of typical box and reel information barcode label

Table 27. Barcode label dimensions

Box barcode label l × w (mm)	Reel barcode label l × w (mm)
100 × 75	100 × 75

## 13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 15](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 28](#) and [29](#)

**Table 28. SnPb eutectic process (from J-STD-020D)**

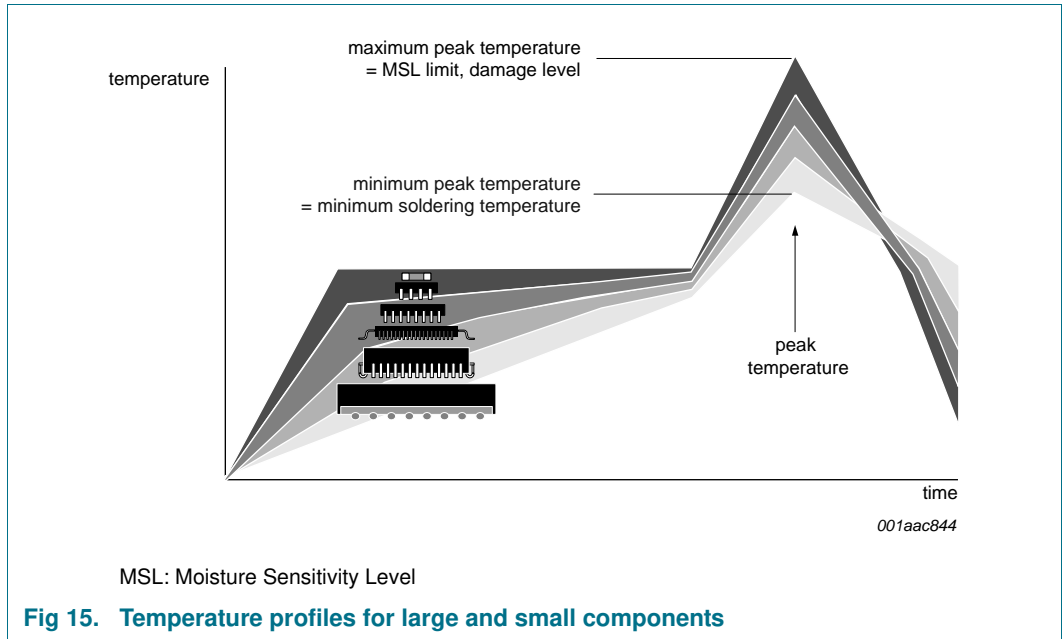
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 29. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

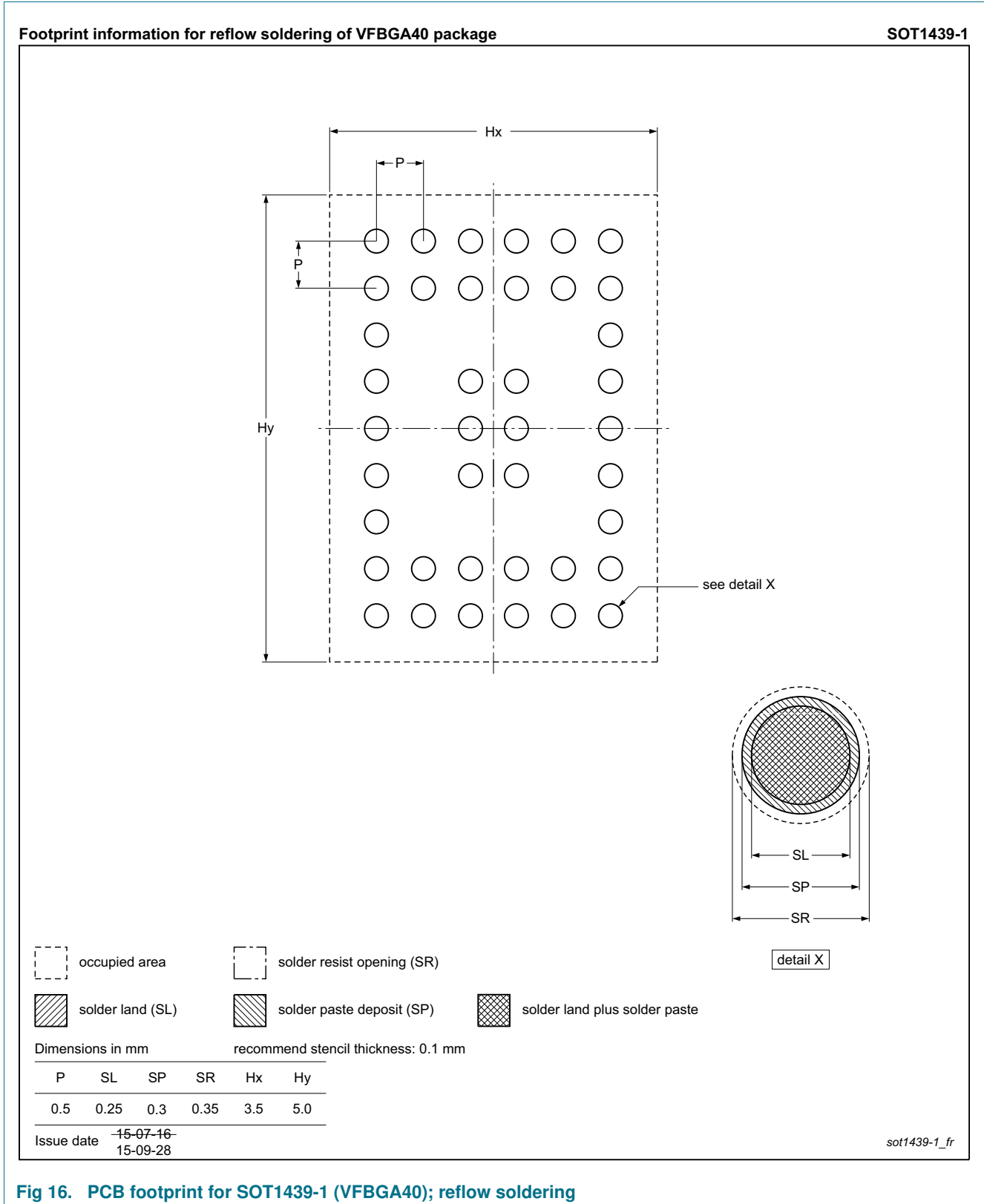
Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 15](#).



For further information on temperature profiles, refer to Application Note *AN10365* "Surface mount reflow soldering description".



**14. Soldering: PCB footprints**



**Fig 16. PCB footprint for SOT1439-1 (VFPGA40); reflow soldering**

## 15. Abbreviations

Table 30. Abbreviations

Acronym	Description
AP	Application Processor
ASIC	Application Specific Integrated Circuit
AUX	Auxiliary channel of DisplayPort specification
CDM	Charged Device Model, an ESD standard
DFP	Downstream Facing Port
DP	VESA DisplayPort specification
DRP	Dual Role Port
EC	Embedded Controller
FS	USB Full Speed signaling
HBM	Human Body Model, an ESD standard
HDI	High Density Interconnect
HPD	Hot Plug Detect channel of DisplayPort or HDMI
HS	USB High Speed signaling
LS	USB Low Speed signaling
MM	Machine Model, an ESD standard
PCH	Platform Controller Hub
PCIe	PCIe specification
PD	Power Delivery specification
POR	Power ON Reset
SS	USB3.0 Super Speed Signaling
UFP	Upstream Facing Port
USB	Universal Serial Bus

## 16. References

- [1] USB Type-C specification v1.0, Aug 2014
- [2] USB Type-C DisplayPort Alternate Mode specification, v1.0, Sep, 2014
- [3] UM10204, "I<sup>2</sup>C-bus specification and user manual"; NXP Semiconductors, Revision 03 June 19, 2007

## 17. Revision history

Table 31. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTL08GP053 v.2	20160801	Product data sheet	-	CBTL08GP053 v.1
Modifications:	<ul style="list-style-type: none"><li>• <a href="#">Table 2 "Ordering options"</a>: Removed CBTL08GP053EVAZ</li><li>• <a href="#">Table 3 "Pin description"</a>: Corrected description for IP1 to IP6; there are only six high-speed differential pairs, not eight</li></ul>			
CBTL08GP053 v.1	20151207	Product data sheet	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 18.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 18.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 19. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 20. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>	12.1.2	Carrier tape dimensions . . . . .	27
<b>2</b>	<b>Features and benefits</b> . . . . .	<b>1</b>	12.1.3	Reel dimensions . . . . .	28
2.1	High speed switch features . . . . .	1	12.1.4	Barcode label . . . . .	29
2.2	Sideband auxiliary crossbar switch features . . . . .	2	<b>13</b>	<b>Soldering of SMD packages</b> . . . . .	<b>30</b>
2.3	General . . . . .	2	13.1	Introduction to soldering . . . . .	30
<b>3</b>	<b>Applications</b> . . . . .	<b>2</b>	13.2	Wave and reflow soldering . . . . .	30
<b>4</b>	<b>Ordering information</b> . . . . .	<b>3</b>	13.3	Wave soldering . . . . .	30
4.1	Ordering options . . . . .	3	13.4	Reflow soldering . . . . .	31
<b>5</b>	<b>Block diagram</b> . . . . .	<b>4</b>	<b>14</b>	<b>Soldering: PCB footprints</b> . . . . .	<b>33</b>
<b>6</b>	<b>Pinning information</b> . . . . .	<b>5</b>	<b>15</b>	<b>Abbreviations</b> . . . . .	<b>34</b>
6.1	Pinning . . . . .	5	<b>16</b>	<b>References</b> . . . . .	<b>34</b>
6.2	Pin description . . . . .	6	<b>17</b>	<b>Revision history</b> . . . . .	<b>35</b>
<b>7</b>	<b>Functional description</b> . . . . .	<b>7</b>	<b>18</b>	<b>Legal information</b> . . . . .	<b>36</b>
7.1	CBTL08GP053 - Use case view . . . . .	8	18.1	Data sheet status . . . . .	36
7.1.1	System application examples . . . . .	9	18.2	Definitions . . . . .	36
7.1.1.1	CBTL08GP053 in Notebook/Ultrabook PC or Tablet - USB3, DP use . . . . .	9	18.3	Disclaimers . . . . .	36
7.1.1.2	CBTL08GP053 in display monitor use case . . . . .	10	18.4	Trademarks . . . . .	37
7.2	Host interface . . . . .	11	<b>19</b>	<b>Contact information</b> . . . . .	<b>37</b>
7.2.1	SYS_CTRL register . . . . .	13	<b>20</b>	<b>Contents</b> . . . . .	<b>38</b>
7.2.2	OP1_CTRL register . . . . .	13			
7.2.3	OP2_CTRL register . . . . .	13			
7.2.4	OP3_CTRL register . . . . .	14			
7.2.5	OP4_CTRL register . . . . .	14			
7.2.6	OP5_CTRL register . . . . .	15			
7.2.7	CROSS5_CTRL register . . . . .	15			
7.2.8	SW_CTRL register . . . . .	15			
7.2.9	REVISION register . . . . .	16			
7.3	I <sup>2</sup> C read and write sequence . . . . .	17			
<b>8</b>	<b>Limiting values</b> . . . . .	<b>18</b>			
<b>9</b>	<b>Recommended operating conditions</b> . . . . .	<b>19</b>			
<b>10</b>	<b>Characteristics</b> . . . . .	<b>19</b>			
10.1	Device characteristics . . . . .	19			
10.2	High speed switch characteristics . . . . .	20			
10.3	Sideband Auxiliary Crossbar switch characteristics . . . . .	21			
10.4	Control I/O characteristics . . . . .	22			
10.5	I <sup>2</sup> C-bus dynamic characteristics . . . . .	23			
<b>11</b>	<b>Package outline</b> . . . . .	<b>25</b>			
<b>12</b>	<b>Packing information</b> . . . . .	<b>26</b>			
12.1	Packing method VFBGA40; Reel dry pack, SMD, 13"; Q1/T1 standard product orientation; Orderable part number ending ,518 or Y; Ordering code (12NC) ending 518 . . . . .	26			
12.1.1	Product orientation . . . . .	27			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2016.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 1 August 2016

Document identifier: CBTL08GP053