LOW-CAPACITANCE 2-CHANNEL ±15-kV ESD-PROTECTION ARRAY FOR HIGH-SPEED DATA INTERFACES

Check for Samples: TPD2E001-Q1

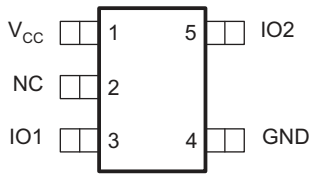
FEATURES

- **Qualified for Automotive Applications**
- **ESD Protection Exceeds**
  - **±15-kV Human-Body Model (HBM)**
  - **±8-kV IEC 61000-4-2 Contact Discharge**
  - **±15-kV IEC 61000-4-2 Air-Gap Discharge**
- **Low 1.5-pF Input Capacitance**
- **Low 1-nA (Max) Leakage Current**
- **0.9-V to 5.5-V Supply-Voltage Range**
- **Two-Channel Device**
- **Space-Saving DRL Package**
- **Alternate 3-, 4-, 6-Channel Options Available: TPD3E001, TPD4E001, and TPD6E001**

APPLICATIONS

- **USB 2.0**
- **Ethernet**
- **FireWire™**
- **Video**
- **Cell Phones**
- **SVGA Video Connections**
- **Glucose Meters**

DRL PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The TPD2E001 is a low-capacitance ±15-kV ESD-protection diode array designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steer ESD current pulses to V_{CC} or GND. The TPD2E001 protects against ESD pulses up to ±15-kV Human-Body Model (HBM), ±8-kV Contact Discharge, and ±15-kV Air-Gap Discharge, as specified in IEC 61000-4-2. This device has a 1.5-pF capacitance per channel, making it ideal for use in high-speed data IO interfaces.

The TPD2E001 is a two-channel device intended for USB and USB 2.0 applications.

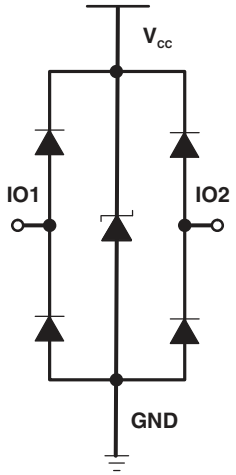
The TPD2E001 is available in the DRL package and is specified for –40°C to 85°C operation.

ORDERING INFORMATION(1)

T_A	PACKAGE (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOT-533 – DRL	Reel of 4000	TPD2E001IDRLRQ1	OEQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

LOGIC BLOCK DIAGRAM



PIN DESCRIPTION

NO.	NAME	FUNCTION
3, 5	IOx	ESD-protected channel
4	GND	Ground
1	V_{CC}	Power-supply input. Bypass V_{CC} to GND with a 0.1-µF ceramic capacitor.
2	N.C.	No connection. Not internally connected.
	EP	Exposed pad. Connect to GND.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}			–0.3	7	V
V_{IO}			–0.3	V_{CC} + 0.3	V
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction temperature			150	°C
	Bump temperature (soldering)	Infrared (15 s)		220	°C
		Vapor phase (60 s)		215	
	Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V ± 10%, T_A = -40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP (1)	MAX	UNIT
V_{CC}	Supply voltage			0.9		5.5	V
I_{CC}	Supply current				1	120	nA
V_F	Diode forward voltage	I_F = 10 mA		0.65		0.95	V
V_{BR}	Breakdown Voltage	I_{BR} = 10mA		11			V
V_C	Channel clamp voltage(2)	T_A = 25°C, ±15-kV HBM, I_F = 10 A	Positive transients			V_{CC} + 25	V
			Negative transients			–25	
		T_A = 25°C, ±8-kV Contact Discharge (IEC 61000-4-2), I_F = 24 A	Positive transients			V_{CC} + 60	
			Negative transients			–60	
		T_A = 25°C, ±15-kV Air-Gap Discharge (IEC 61000-4-2), I_F = 45 A	Positive transients			V_{CC} + 100	
			Negative transients			–100	
$I_{i/o}$	Channel leakage current(2)	$V_{i/o}$ = GND to V_{CC}				±1	nA
$C_{i/o}$	Channel input capacitance	V_{CC} = 5 V, Bias of V_{CC}/2			1.5		pF

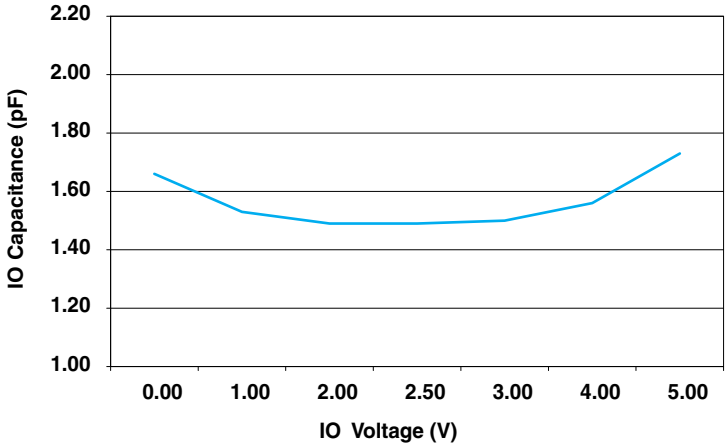
(1) Typical values are at V_{CC} = 5 V and T_A = 25°C
(2) Not production tested

ESD PROTECTION

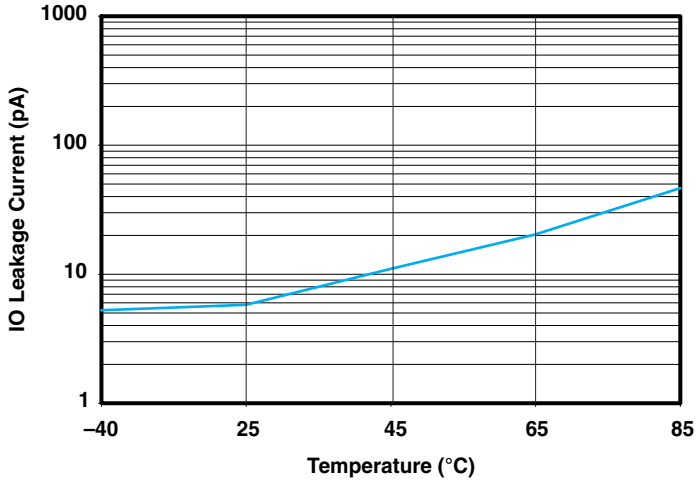
PARAMETER	TYP	UNIT
HBM	±15	kV
IEC 61000-4-2 Contact Discharge	±8	kV
IEC 61000-4-2 Air-Gap Discharge	±15	kV

TYPICAL OPERATING CHARACTERISTICS

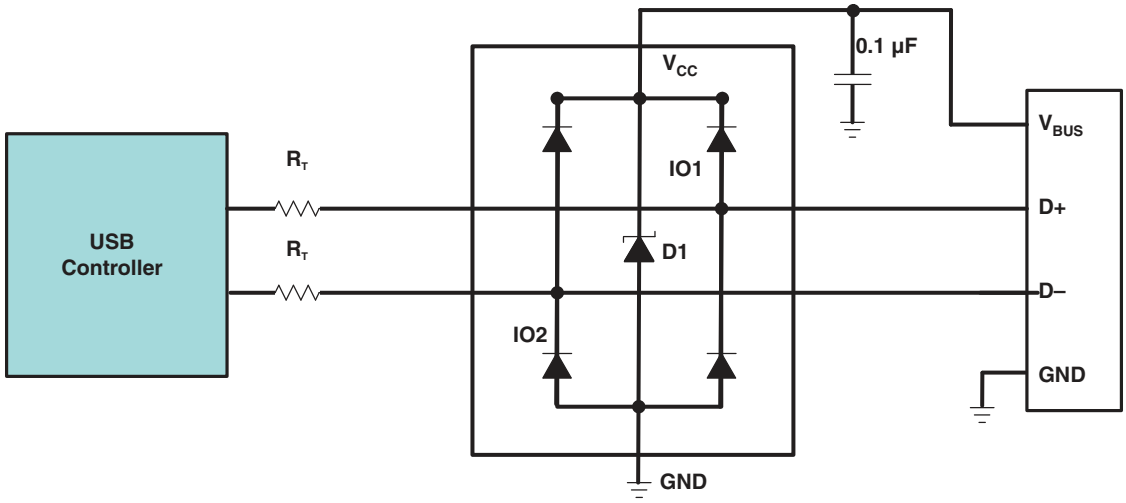
IO CAPACITANCE vs IO VOLTAGE (V_{CC} = 5.0 V)



IO LEAKAGE CURRENT vs TEMPERATURE (V_{CC} = 5.5 V)



APPLICATION INFORMATION



Detailed Description

When placed near the connector, the TPD2E001 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD2E001 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, the following layout/ design guidelines should be followed:

1. Place the TPD2E001 solution close to the connector. This allows the TPD2E001 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1-µF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
3. Make sure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD2E001 consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating.
5. The V_{CC} pin can be connected in two different ways:
   (a) If the V_{CC} pin is connected to the system power supply, the TPD2E001 works as a transient suppressor for any signal swing above V_{CC} + V_F. A 0.1-µF capacitor on the device V_{CC} pin is recommended for ESD bypass.
   (b) If the V_{CC} pin is not connected to the system power supply, the TPD2E001 can tolerate higher signal swing in the range up to 10 V. Please note that a 0.1-µF capacitor is still recommended at the V_{CC} pin for ESD bypass.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E001IDRLRQ1	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OEQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

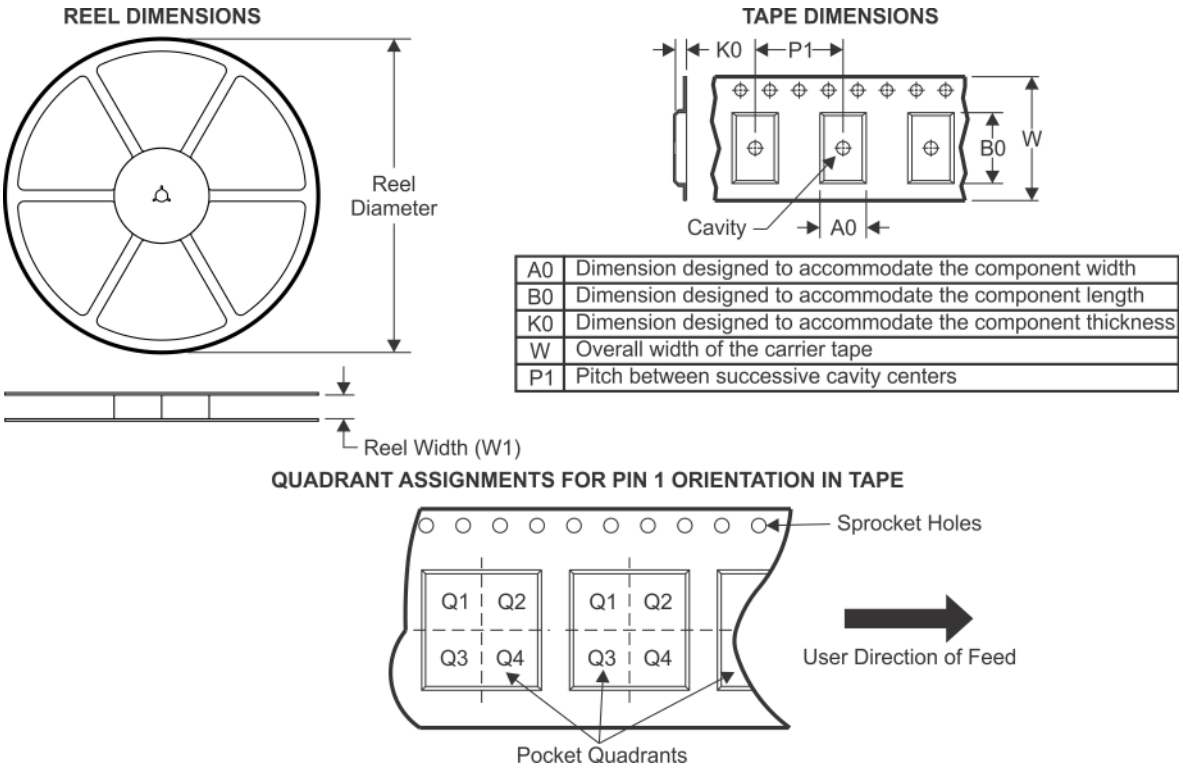
OTHER QUALIFIED VERSIONS OF TPD2E001-Q1 :

- Catalog: TPD2E001

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

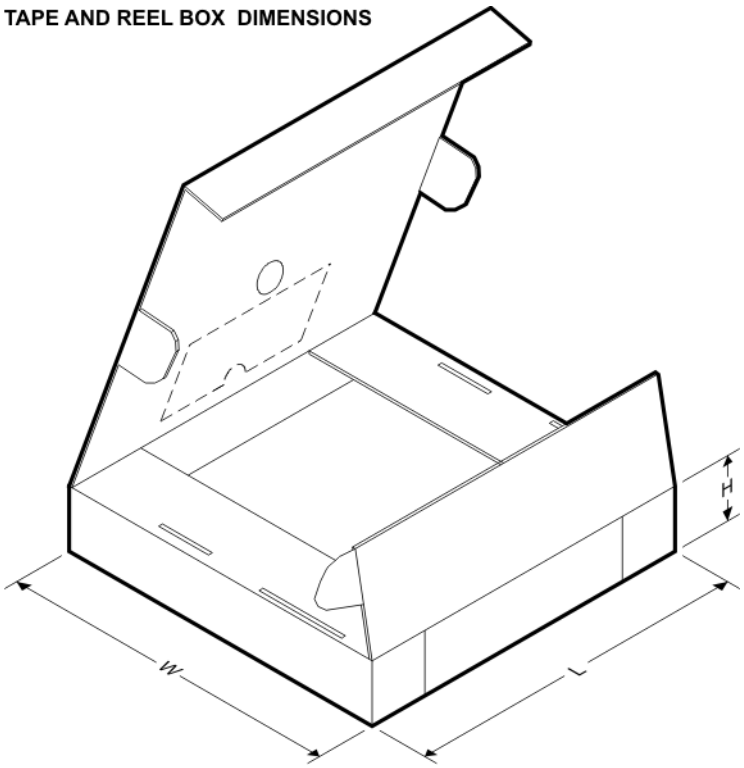


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E001IDRLRQ1	SOT-5X3	DRL	5	4000	180.0	8.4	1.78	1.78	0.69	4.0	8.0	Q3

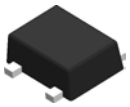
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E001IDRLRQ1	SOT-5X3	DRL	5	4000	183.0	183.0	20.0

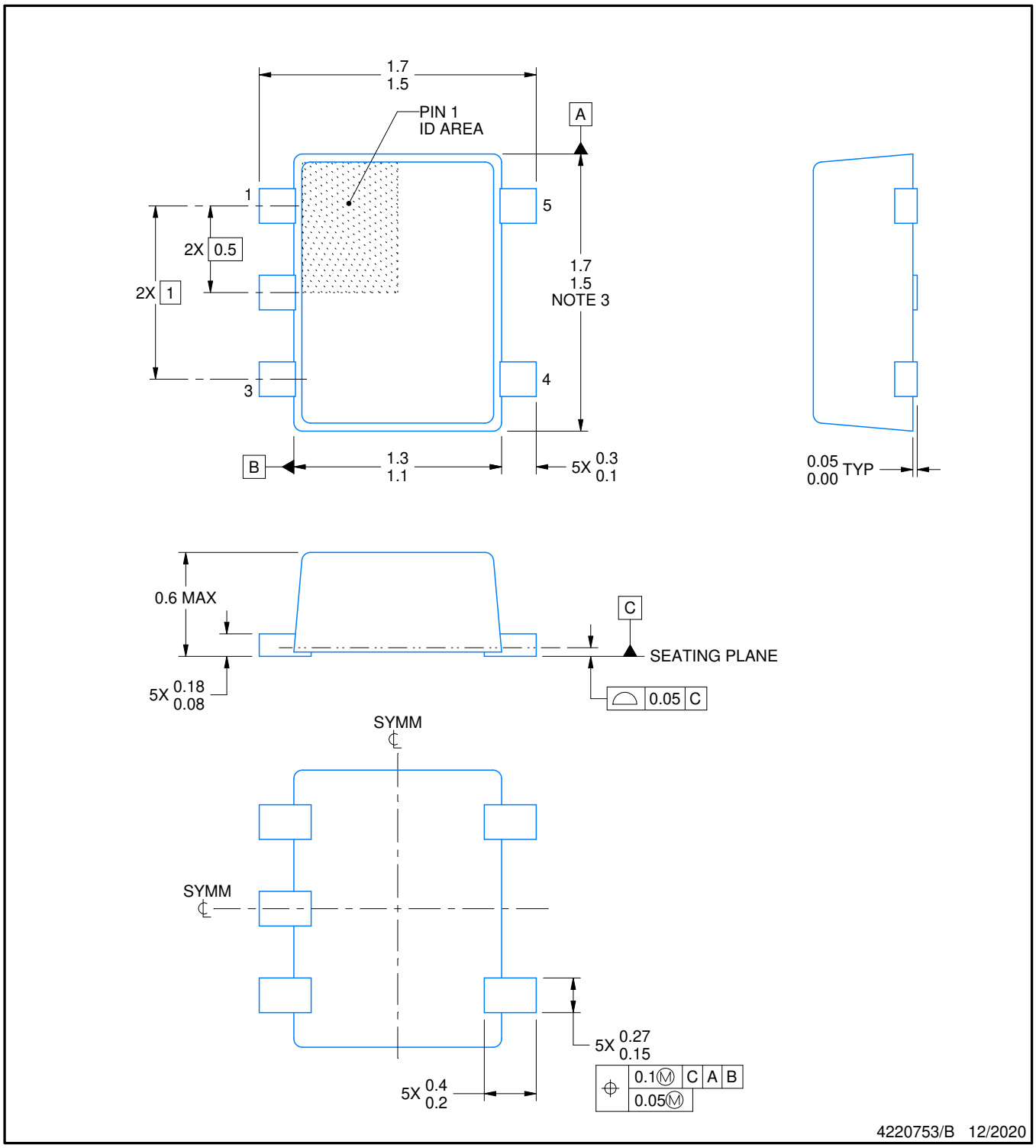
DRL0005A



PACKAGE OUTLINE

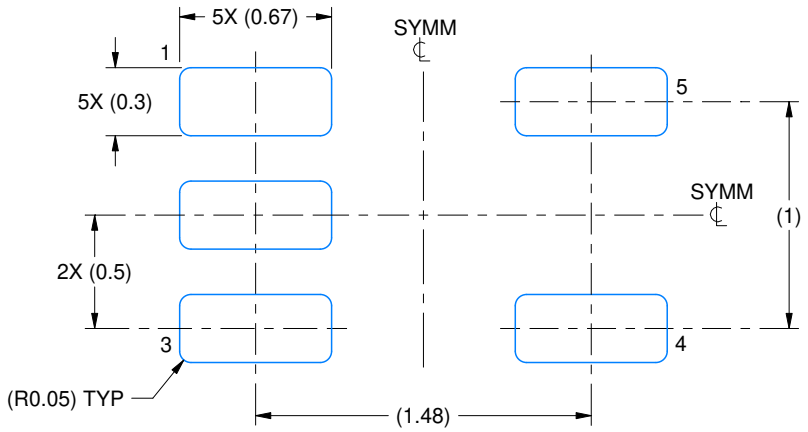
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

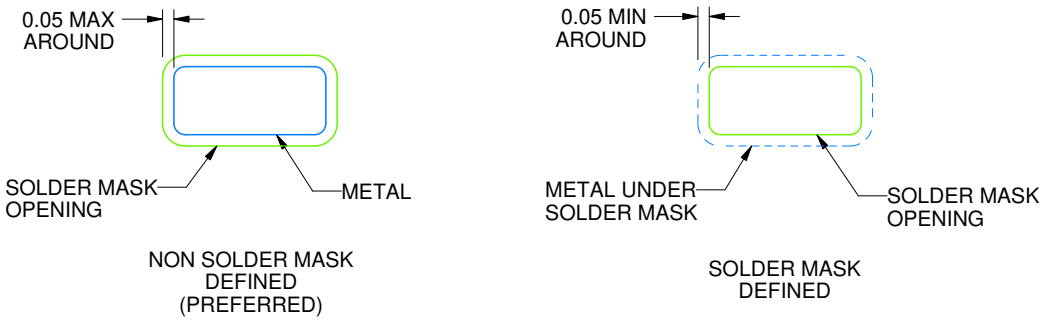


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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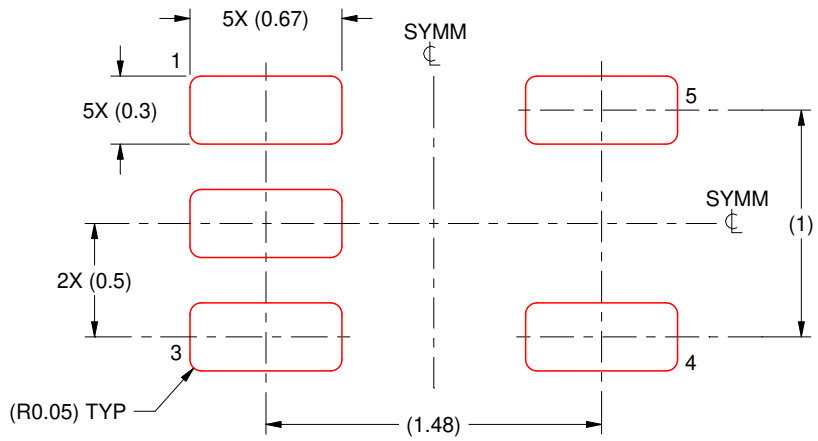
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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