CY29350

2.5V or 3.3V, 200-MHz, 9-Output Clock Driver

Features

- **Output frequency range: 25 MHz to 200 MHz**
- **Input frequency range: 6.25 MHz to 31.25 MHz**
- **2.5V or 3.3V operation**
- **Split 2.5V/3.3V outputs**
- **±2.5% max Output duty cycle variation**
- **Nine Clock outputs: Drive up to 18 clock lines**
- **Two reference clock inputs: Xtal or LVCMOS**
- **150-ps max output-output skew**
- **Phase-locked loop (PLL) bypass mode**
- **Spread Aware™**
- **Output enable/disable**
- **Pin-compatible with MPC9350**
- **Industrial temperature range: –40°C to +85°C**
- **32-pin 1.0mm TQFP package**

Functional Description

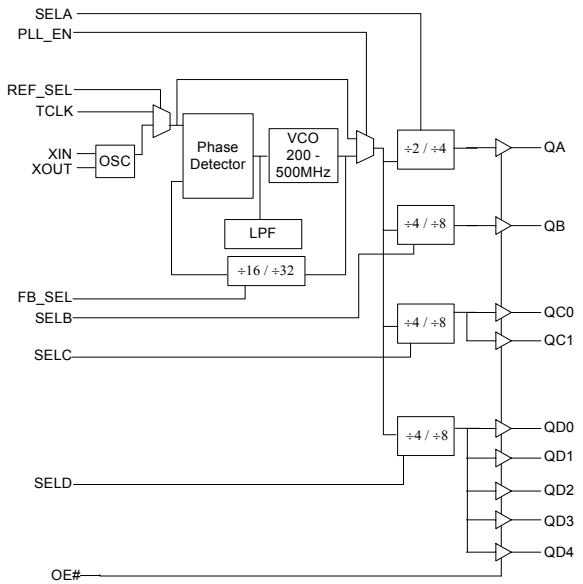
The CY29350 is a low-voltage high-performance 200-MHz PLL-based clock driver designed for high speed clock distribution applications.

The CY29350 features Xtal and LVCMOS reference clock inputs and provides nine outputs partitioned in four banks of 1, 1, 2, and 5 outputs. Bank A divides the VCO output by 2 or 4 while the other banks divide by 4 or 8 per SEL(A:D) settings, see . These dividers allow output to input ratios of 16:1, 8:1, 4:1, and 2:1. Each LVCMOS compatible output can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:18.

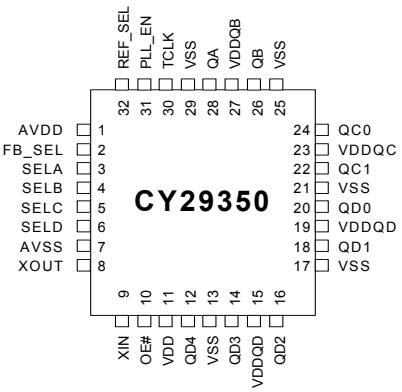
The PLL is ensured stable given that the VCO is configured to run between 200 MHz to 500 MHz. This allows a wide range of output frequencies from 25 MHz to 200 MHz. The internal VCO is running at multiples of the input reference clock set by the feedback divider, see *Table 1.*

When PLL_EN is LOW, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

Block Diagram



Pin Configuration



Pin Definitions[1]

Pin	Name	I/O	Type	Description
8	XOUT	O	Analog	**Oscillator Output**. Connect to a crystal.
9	XIN	I	Analog	**Oscillator Input**. Connect to a crystal.
30	TCLK	I, PD	LVCMOS	**LVCMOS/LVTTL reference clock input**
28	QA	O	LVCMOS	**Clock output bank A**
26	QB	O	LVCMOS	**Clock output bank B**
22, 24	QC(1:0)	O	LVCMOS	**Clock output bank C**
12, 14, 16, 18, 20	QD(4:0)	O	LVCMOS	**Clock output bank D**
2	FB_SEL	I, PD	LVCMOS	**Internal Feedback Select Input**. See *Table 1*.
10	OE#	I, PD	LVCMOS	**Output enable/disable input**. See *Table 2*.
31	PLL_EN	I, PU	LVCMOS	**PLL enable/disable input**. See *Table 2*.
32	REF_SEL	I, PD	LVCMOS	**Reference select input**. See *Table 2*.
3, 4, 5, 6	SEL(A:D)	I, PD	LVCMOS	**Frequency select input, Bank (A:D)**. See *Table 2*.
27	VDDQB	Supply	VDD	**2.5V or 3.3V Power supply for bank B output clock**[2,3]
23	VDDQC	Supply	VDD	**2.5V or 3.3V Power supply for bank C output clocks**[2,3]
15, 19	VDDQD	Supply	VDD	**2.5V or 3.3V Power supply for bank D output clocks**[2,3]
1	AVDD	Supply	VDD	**2.5V or 3.3V Power supply for PLL**[2,3]
11	VDD	Supply	VDD	**2.5V or 3.3V Power supply for core, inputs, and bank A output clock**[2,3]
7	AVSS	Supply	Ground	**Analog ground**
13, 17, 21, 25, 29	VSS	Supply	Ground	**Common ground**

Table 1. Frequency Table

FB_SEL	Feedback Divider	VCO	Input Frequency Range (AVDD = 3.3V)	Input Frequency Range (AVDD = 2.5V)
0	÷32	Input Clock * 32	6.25 MHz to 15.625 MHz	6.25 MHz to 11.875 MHz
1	÷16	Input Clock * 16	12.5 MHz to 31.25 MHz	12.5 MHz to 23.75 MHz

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	Xtal	TCLK
PLL_EN	1	Bypass mode, PLL disabled. The input clock connects to the output dividers	PLL enabled. The VCO output connects to the output dividers
OE#	0	Outputs enabled	Outputs disabled (three-state)
FB_SEL	0	Feedback divider ÷ 32	Feedback divider ÷ 16
SELA	0	÷ 2 (Bank A)	÷ 4 (Bank A)
SELB	0	÷ 4 (Bank B)	÷ 8 (Bank B)
SELC	0	÷ 4 (Bank C)	÷ 8 (Bank C)
SELD	0	÷ 4 (Bank D)	÷ 8 (Bank D)

Notes:
1. PU = Internal pull-up, PD = Internal pull-down.
2. A 0.1μF bypass capacitor should be placed as close as possible to each positive power pin (<0.2”). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the traces.
3. AVDD and VDD pins must be connected to a power supply level that is at least equal or higher than that of VDDQB, VDDQC, and VDDQD output power supply pins.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		–0.3	5.5	V
V_{DD}	DC Operating Voltage	Functional	2.375	3.465	V
V_{IN}	DC Input Voltage	Relative to V_{SS}	–0.3	V_{DD} + 0.3	V
V_{OUT}	DC Output Voltage	Relative to V_{SS}	–0.3	V_{DD} + 0.3	V
V_{TT}	Output termination Voltage			$V_{DD} \div 2$	V
LU	Latch Up Immunity	Functional	200		mA
R_{PS}	Power Supply Ripple	Ripple Frequency < 100 kHz		150	mVp-p
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
T_J	Temperature, Junction	Functional		+150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Functional		42	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	Functional		105	°C/W
ESD_H	ESD Protection (Human Body Model)		2000		Volts
FIT	Failure in Time	Manufacturing test	10		ppm

DC Electrical Specifications (V_{DD} = 2.5V ± 5%, T_A = –40°C to +85°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Voltage, Low	LVCMOS	–	–	0.7	V
V_{IH}	Input Voltage, High	LVCMOS	1.7	–	V_{DD}+0.3	V
V_{OL}	Output Voltage, Low[4]	I_{OL} = 15mA	–	–	0.6	V
V_{OH}	Output Voltage, High[4]	I_{OH} = –15mA	1.8	–	–	V
I_{IL}	Input Current, Low[5]	V_{IL} = V_{SS}	–	–	–100	µA
I_{IH}	Input Current, High[5]	V_{IL} = V_{DD}	–	–	100	µA
I_{DDA}	PLL Supply Current	AVDD only	–	5	10	mA
I_{DDQ}	Quiescent Supply Current	All VDD pins except AVDD	–	–	7	mA
I_{DD}	Dynamic Supply Current	Outputs loaded @ 100 MHz	–	180	–	mA
		Outputs loaded @ 200 MHz	–	210	–	
C_{IN}	Input Pin Capacitance		–	4	–	pF
Z_{OUT}	Output Impedance		14	18	22	Ω

DC Electrical Specifications (V_{DD}= 3.3V ± 5%, T_A = –40°C to +85°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Voltage, Low	LVCMOS	–	–	0.8	V
V_{IH}	Input Voltage, High	LVCMOS	2.0	–	V_{DD}+0.3	V
V_{OL}	Output Voltage, Low[4]	I_{OL} = 24 mA	–	–	0.55	V
		I_{OL} = 12 mA	–	–	0.30	
V_{OH}	Output Voltage, High[4]	I_{OH} = –24 mA	2.4	–	–	V
I_{IL}	Input Current, Low[5]	V_{IL} = V_{SS}	—	–	–100	µA
I_{IH}	Input Current, High[5]	V_{IL} = V_{DD}	–	–	100	µA
I_{DDA}	PLL Supply Current	AVDD only	–	5	10	mA
I_{DDQ}	Quiescent Supply Current	All VDD pins except AVDD	–	–	7	mA
I_{DD}	Dynamic Supply Current	Outputs loaded @ 100 MHz	–	270	–	mA
		Outputs loaded @ 200 MHz	–	300	–	
C_{IN}	Input Pin Capacitance		–	4	–	pF
Z_{OUT}	Output Impedance		12	15	18	Ω

Notes:

4. Driving one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, each output drives up to two 50Ω series terminated transmission lines.
5. Inputs have pull-up or pull-down resistors that affect the input current.

AC Electrical Specifications (V_{DD} = 2.5V ± 5%, T_A = –40°C to +85°C) [6]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f_{VCO}	VCO Frequency		200	–	380	MHz
f_{in}	Input Frequency	÷16 Feedback	12.5	–	23.75	MHz
		÷32 Feedback	6.25	–	11.87	
		Bypass mode (PLL_EN = 0)	0	–	200	
f_{XTAL}	Crystal Oscillator Frequency		10	–	23.75	MHz
f_{refDC}	Input Duty Cycle		25	–	75	%
t_r , t_f	TCLK Input Rise/FallTime	0.7V to 1.7V	–	–	1.0	ns
f_{MAX}	Maximum Output Frequency	÷2 Output	100	–	190	MHz
		÷4 Output	50	–	95	
		÷8 Output	25	–	47.5	
DC	Output Duty Cycle	f_{MAX} < 100 MHz	47.5	–	52.5	%
		f_{MAX} > 100 MHz	45	–	55	
t_r , t_f	Output Rise/Fall times	0.6V to 1.8V	0.1	–	1.0	ns
$t_{sk(O)}$	Output-to-Output Skew		–	–	150	ps
$t_{PLZ, HZ}$	Output Disable Time		–	–	10	ns
$t_{PZL, ZH}$	Output Enable Time		–	–	10	ns
BW	PLL Closed Loop Bandwidth (-3dB)	÷16 Feedback	–	0.7 - 0.9	–	MHz
		÷32 Feedback	–	0.6 - 0.8	–	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency	–	–	150	ps
		Multiple frequencies	–	–	250	
$t_{JIT(PER)}$	Period Jitter	Same frequency	–	–	100	ps
		Multiple frequencies	–	–	175	
t_{LOCK}	Maximum PLL Lock Time		–	–	1	ms

AC Electrical Specifications (V_{DD} = 3.3V ± 5%, T_A = –40°C to +85°C) [6]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f_{VCO}	VCO Frequency		200	–	500	MHz
f_{in}	Input Frequency	÷16 Feedback	12.5	–	31.25	MHz
		÷32 Feedback	6.25	–	15.625	
		Bypass mode (PLL_EN = 0)	0	–	200	
f_{XTAL}	Crystal Oscillator Frequency		10	–	25	MHz
f_{refDC}	Input Duty Cycle		25	–	75	%
t_r , t_f	TCLK Input Rise/FallTime	0.8V to 2.0V	–	–	1.0	ns
f_{MAX}	Maximum Output Frequency	÷2 Output	100	–	200	MHz
		÷4 Output	50	–	125	
		÷8 Output	25	–	62.5	
DC	Output Duty Cycle	f_{MAX} < 100 MHz	47.5	–	52.5	%
		f_{MAX} > 100 MHz	45	–	55	
t_r , t_f	Output Rise/Fall times	0.8V to 2.4V	0.1	–	1.0	ns
$t_{sk(O)}$	Output-to-Output Skew	Banks at same voltage	–	–	150	ps
tsk(B)	Bank-to-Bank Skew	Banks at different voltages	–	–	350	ps
$t_{PLZ, HZ}$	Output Disable Time		–	–	10	ns
$t_{PZL, ZH}$	Output Enable Time		–	–	10	ns

Note:
6. AC characteristics apply for parallel output termination of 50Ω to V_{TT}. Parameters are guaranteed by characterization and are not 100% tested.

AC Electrical Specifications (V_{DD} = 3.3V ± 5%, T_A = –40°C to +85°C)(continued)[6]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
BW	PLL Closed Loop Bandwidth (–3dB)	÷16 Feedback	–	0.7 – 0.9	–	MHz
		÷32 Feedback	–	0.6 – 0.8	–	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	Same frequency	–	–	150	ps
		Multiple frequencies	–	–	250	
$t_{JIT(PER)}$	Period Jitter	Same frequency	–	–	100	ps
		Multiple frequencies	–	–	150	
t_{LOCK}	Maximum PLL Lock Time		–	–	1	ms

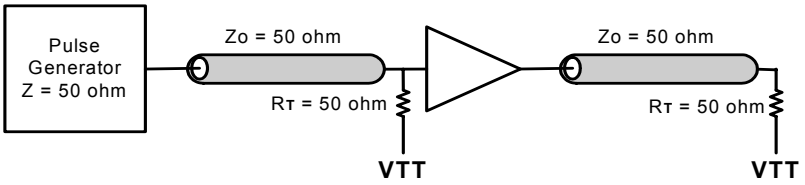


Figure 1. AC Test Reference for V_{DD} = 3.3V / 2.5V

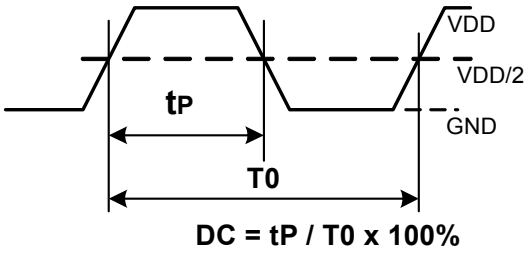


Figure 2. Output Duty Cycle (DC)

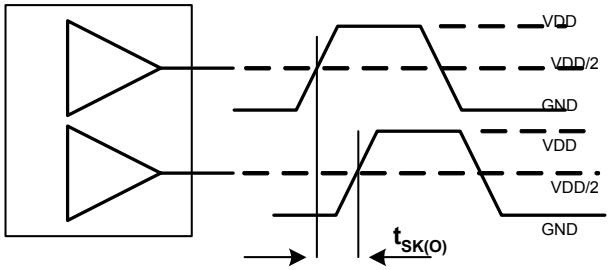


Figure 3. Output-to-Output Skew , $t_{sk(O)}$

Table 3. Suggested Oscillator Crystal Parameters

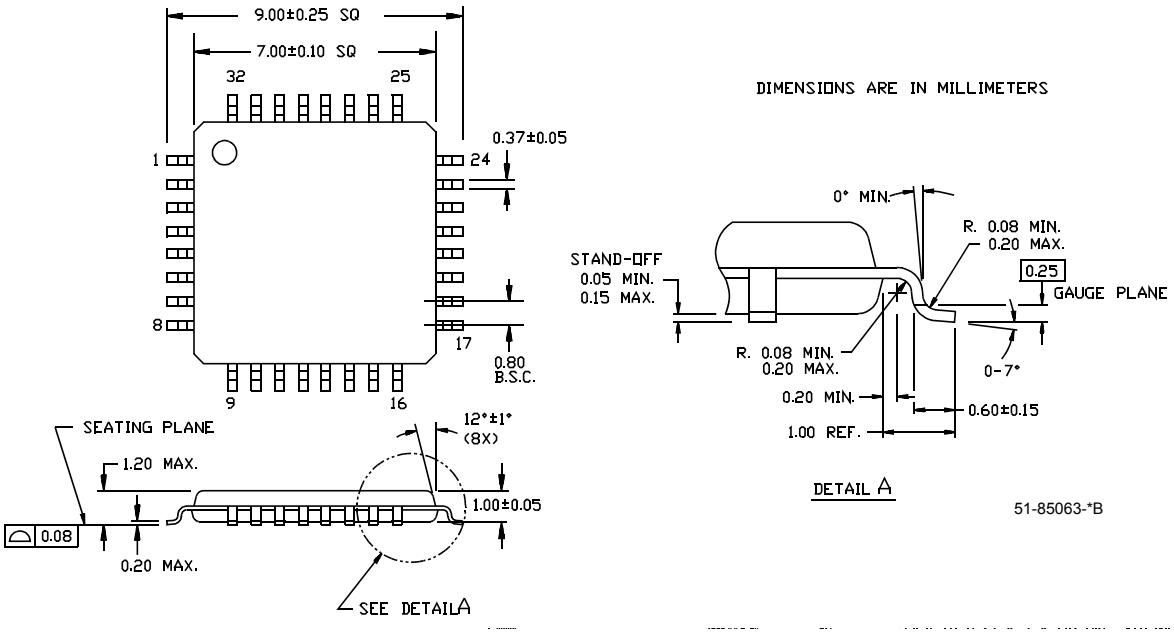
Characteristic	Symbol	Conditions	Min	Typ	Max	Units
Frequency Tolerance	T_C		–	–	±100	PPM
Frequency Temperature Stability	T_S	(T_A –10 +60C)	–	–	±00	PPM
Aging	T_A	First three years @ 25C	–	–	5	PPM/yr
Load Capacitance	C_L	Crystal's rated load	–	20	–	pF
Effective Series Resistance	R_{ESR}		–	40	80	Ω

Ordering Information

Part Number	Package Type	Product Flow
CY29350AI	32-pin TQFP	Industrial, –40°C to +85°C
CY29350AIT	32-pin TQFP – Tape and Reel	Industrial, –40°C to 85°C

Package Drawing and Dimension

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.0 mm A32



Document History Page

Document Title:CY29350 2.5V or 3.3V, 200-MHz, 9-Output Clock Driver Document Number: 38-07474				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	128104	07/07/03	RGL	New Data Sheet
*A	245393	See ECN	RGL	Re-worded Select Function Descriptions in table 2.